AN1234

Understanding Cypress's Zero Delay Buffers

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AN1234 describes the Cypress's zero delay buffers and its multiple applications in detail. Zero Delay Buffers are ideal for a variety of clock distribution applications, which require tight input-output and output-output skews.

Contents

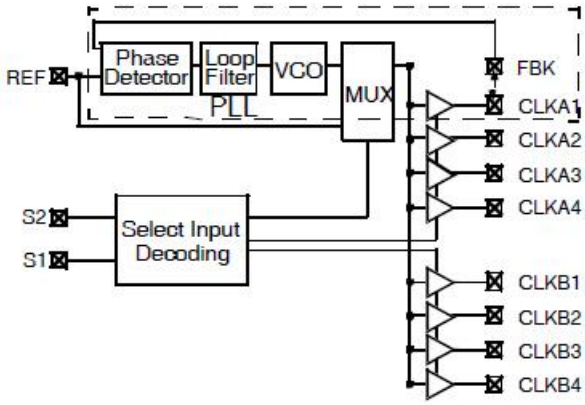
Introduction to Cypress's Zero Delay Buffers

A zero delay buffer is a device that can fan out one clock signal into multiple clock signals with no delay and low skew between the outputs. A simplified diagram of a zero delay buffer is shown in Figure 1. A zero delay buffer is built with a PLL (phase locked loop) that uses a reference input (REF) and a feedback input (FBK). The feedback input is driven by one of the outputs. The phase detector inside the PLL adjusts the output frequency of the VCO (voltage controlled oscillator) in a way such that its two inputs have no phase or frequency difference. Since, the PLL control loop includes one of the outputs and its load, it dynamically compensates the load placed on that output. That is, the PLL has zero delay from the input to the output that drives feedback, irrespective of the loading on that output.

Note This is only the case for the output being monitored by the Feedback input; all other outputs have an input to output delay that is affected by the differences in the output loads. See the section "Lead or Lag Adjustments" for details.

Cypress has a broad portfolio of zero delay buffers (ZDBs). For Example: CY2304, CY2305, CY2308, CY2309 and so on. These ZDBs support frequencies ranging from 10 MHz to 200 MHz and differ from each other in features. For example, architectural differences that include internal vs. external feedback, number of outputs, frequency multiplication, multiple output frequencies, and output enable functionality. CY2308 has eight outputs and provides the flexibility to externally close the feedback path, whereas, CY2305/CY2309 has five and nine outputs respectively and have an integrated feedback path connection for simpler system design. Other devices have 2, 4, 5, 9, 10, 11, or 12 outputs. For more information, see the product section of our web site: www.cypress.com. We are using CY2308, CY2305, and CY2309 as an example in this application note to understand ZDBs and their multiple applications.

Figure 1. Simplified Block Diagram of CY2308



CY2308

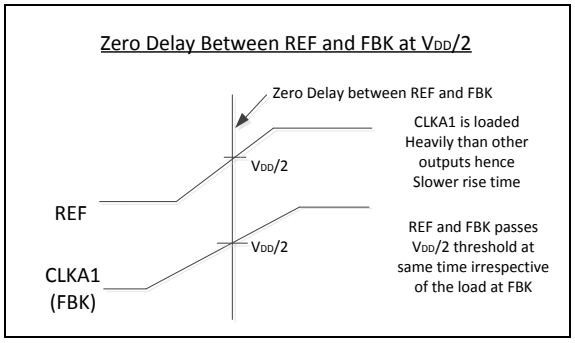
The Cypress CY2308 is a dual bank general-purpose ZDB providing eight copies of a single input clock with zero delay from input to output and low skew between outputs. The CY2308 is an open feedback device. To function as a ZDB, the feedback loop must be closed. Any of the eight outputs can be fed back into the feedback (FBK) pin to close the loop and form a simple ZDB. The capability to externally close the feedback path on the CY2308 provides skew-control, and options to use them for various clock distribution applications. The key feature of loading on the output (which is fed back) differently compared to the other outputs can be used for simple lead or lag adjustments, which is explained in the following section.

Lead or Lag Adjustments

By properly loading the output (which is fed back), the other outputs can be made to lead or lag the Reference clock. Here, the property of PLL is used to make the outputs lead or lag compared to other outputs. Note that we have two pins named REF and FBK in CY2308 (See Figure 1) that are input to PLL. Reference signal (clock) is given as input to the REF pin, whereas FBK pin is used to externally close the feedback path. Read the following list of properties of PLL to understand the feature of connecting any output to the FBK pin.

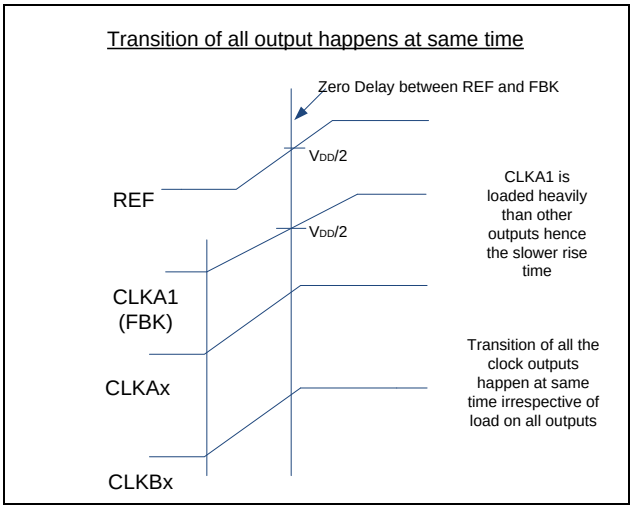
1. The PLL senses the phase (and frequency) of the FBK pin at a threshold of $V_{DD}/2$ and compares it to the REF pin at the same $V_{DD}/2$ threshold. Therefore, the ZDBs always adjust themselves to keep the $V_{DD}/2$ point of the FBK input at zero delay from the $V_{DD}/2$ point of the REF input due to the property of a PLL.

Figure 2. Zero Delay between REF and FBK at $V_{DD}/2$



2. All of the outputs start their transition at the same time, including the output driving FBK.

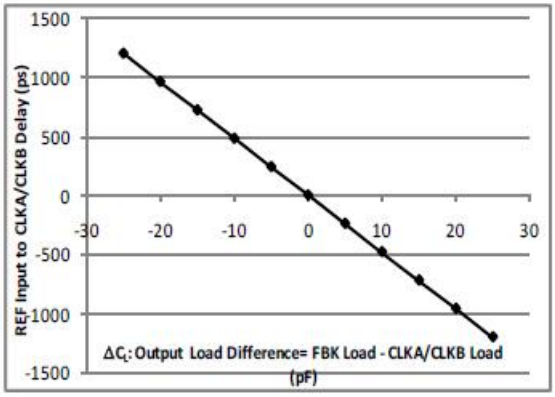
Figure 3. Transition of all Outputs



Hence, changing the load on an output changes its rise time and therefore how long it takes the output to reach the $V_{DD}/2$ threshold. According to these properties, the outputs can be advanced by loading the feedback output heavier than the other outputs, or they can be delayed (lagged) by loading the feedback output lighter than the other outputs. This is explained in Figure 3.

The chart in Figure 4 shows delta delay vs. the difference in the loading between the feedback output and the other outputs. Delta delay is the measurement which shows how many picoseconds the output is moved. As a first order approximation, the adjustment is 50 ps/pF of loading difference.

Figure 4. Lead Lag Adjustments

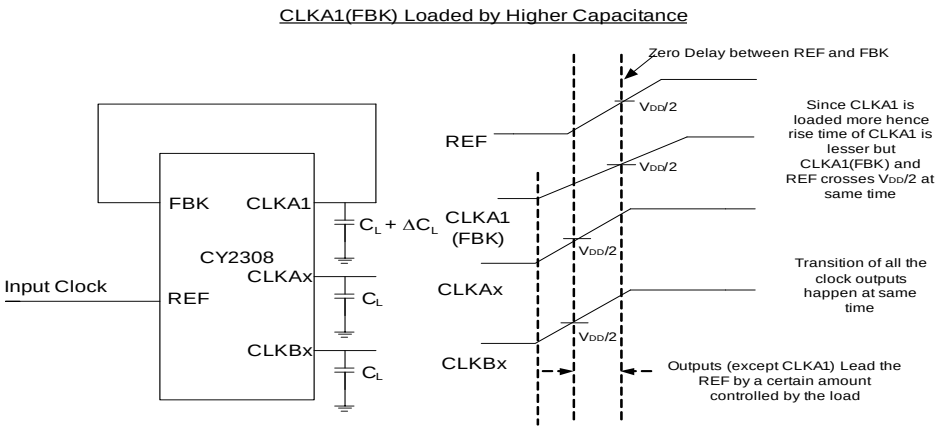


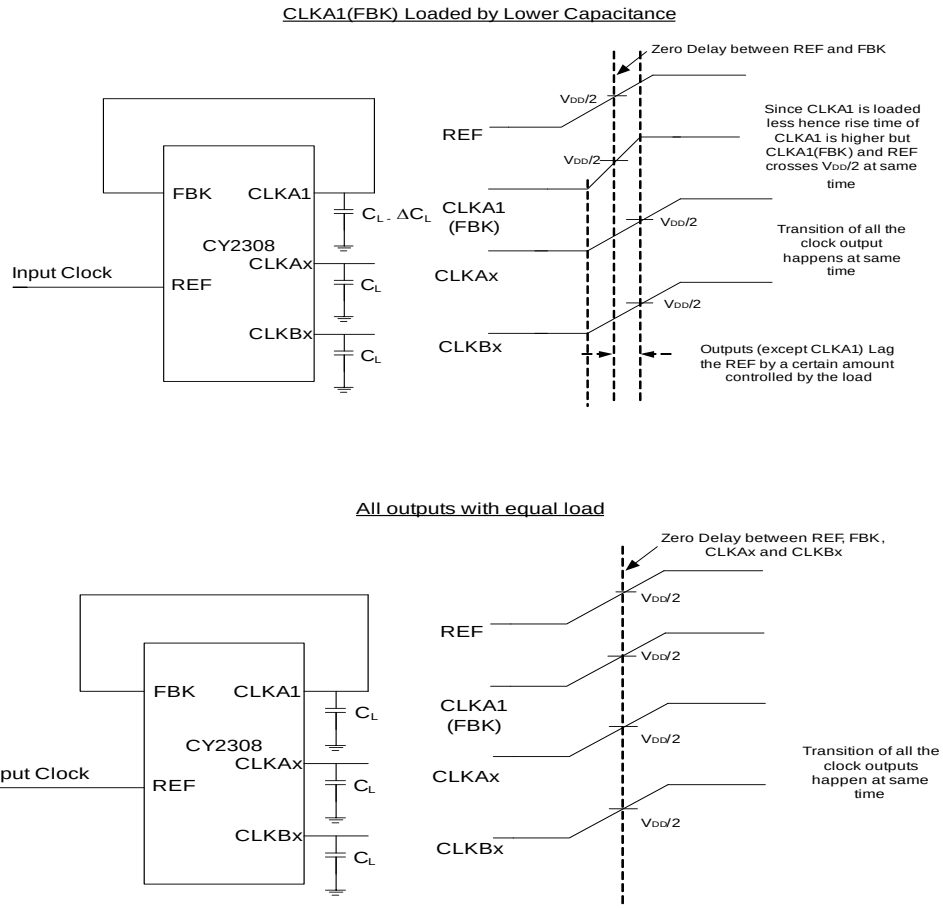
Zero Delay and Slew Control

All outputs must have the same load on them to achieve zero output-to-output skew. The feedback loop does not dynamically adjust the skew between FBK and the other outputs. Figure 5 shows how output loading affects output-to-output skew. Here, FBK is assumed to be driven by CLKA1, though any of the outputs can be used to drive FBK. If the other outputs are lightly loaded than CLKA1, they will lead CLKA1; and if the other outputs are heavily loaded, they will lag CLKA1 as explained in earlier section. In this case, because CLKA1 is the only output that is monitored, it will be the output that has zero delay from the reference (REF). The timing of the other clocks will be relative to CLKA1 as determined by their loading differences.

Note that the unused outputs should be left floating, without any additional capacitance or trace.

Figure 5. CY2308 Timing Diagram with Different Loading Configurations, and CLKA1 Driving FBK



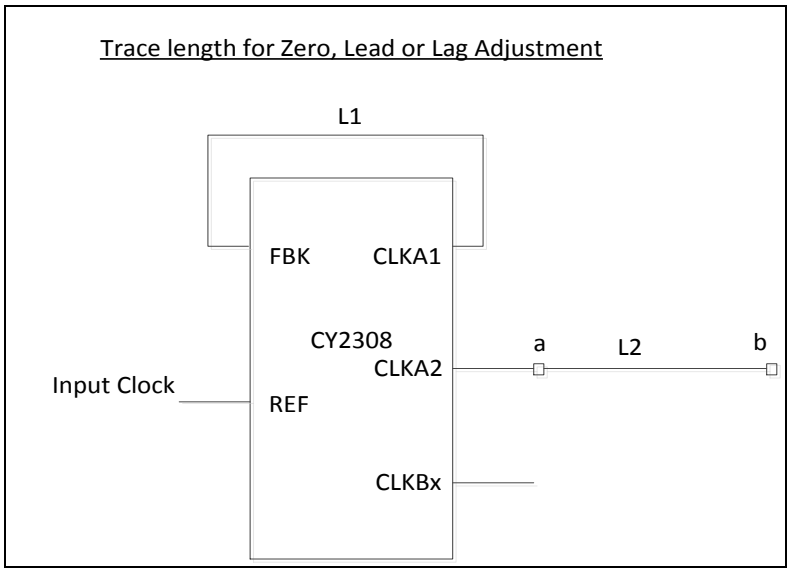


Trace Length for Zero, Lead or Lag Adjustment

So far, we have discussed only the effect of capacitive loading on lead and lag timing and output skew. A similar concept applies to trace length. To achieve zero delay between the REF input and the CLK signals arriving at their destinations, the general rule is that the feedback trace length (from CLK pin to FBK pin) should be equal to the traces from the other CLK outputs to their respective destinations. Figure 7 shows how we can make zero lead or lag adjustment in the output clocks by altering the trace length. Here, FBK is assumed to be driven by CLKA1, trace length from CLKA1 to FBK is L1 and from CLKA2 to its destination is L2 as shown in Figure 6.

Figure 6

Figure 6. Trace Length for Zero, Lead or Lag Adjustments



Note that there will be a delay (t) between CLKA1 and FBK due to trace length L1. According to the property of PLL, the CLKA1 will be advanced from REF by the same amount of delay (t) to keep crossing point of $V_{DD}/2$ threshold at same time for FBK and REF as shown in figure 7. All the outputs (CLKA2 in figure 7) will start making transition at the same time (as explained earlier in "Lead and Lag Adjustments Section") with CLKA1, so CLKA2 (point a) will also be advanced with respect to REF. but CLKA2 at destination (point b) will be delayed by a time t' compared to CLKA2 (point a) due to trace length L2.

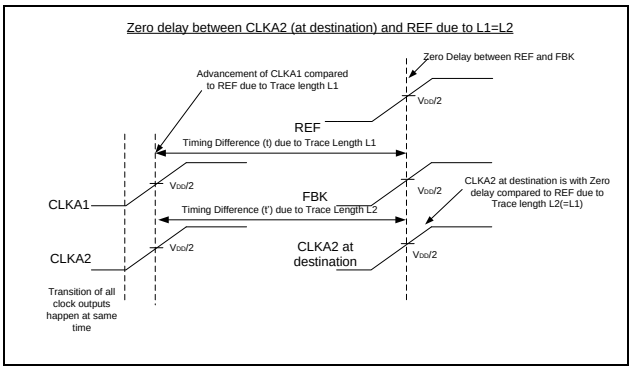
In Summary,

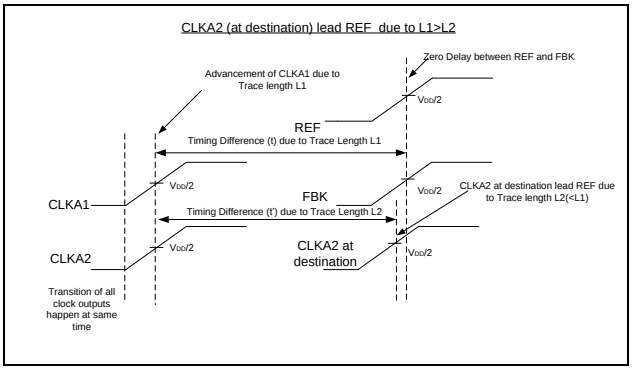
If L1 = L2, then t = t', hence there is a zero delay between REF and CLKA2 at destination as shown in Figure 7.

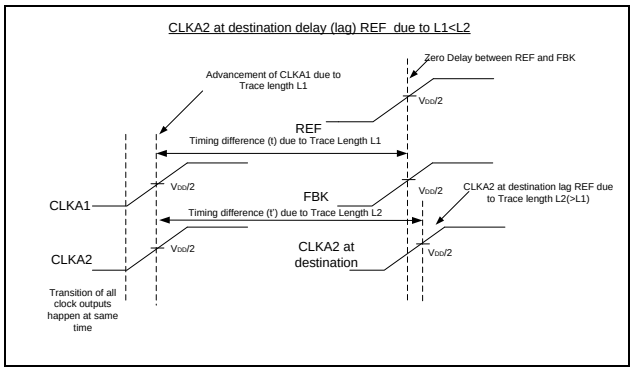
If L1 > L2, then t > t', hence CLKA2 at destination (point b) gets advanced relative to REF as shown in Figure 7.

If L1 < L2, then t < t', hence CLKA2 at destination gets delayed (lagged) relative to REF as explained in Figure 7.

Figure 7. Zero Delay, Lead or Lag Adjustment with Trace Length







As with any buffer, individual clocks may be advanced by shortening that particular trace, or delayed by lengthening it. When lengthening traces, beware that a tight serpentine routing adds less delay than an equal length trace that does not bend back on itself. This is because the closely routed trace couples to itself, which helps to speed the propagation of the signal.

Drive Capability

The CY2308 has high drive outputs designed to drive 30 pF capacitance each. If we assume a typical CMOS input as 7 pF, it means that up to four CMOS inputs can be driven from a single output of a CY2308. However, the output loading on the CY2308 must be equal on all used outputs to maintain zero delay from the input.

Special Power-Down Feature

The CY2308 has a unique power-down mode: if the input reference is stopped, the part automatically enters a shutdown state by making the PLL off and tri-stating the outputs. When the part is in shutdown mode, it draws less than 50 µA, and can come out of shutdown mode with the PLL locked in less than 1 ms.

The outputs are treated as two banks of four outputs each and two select lines are provided to individually tri-state the two banks of four outputs, and even power-down the PLL for low power operation.

A mode is also available in which the outputs are driven from the reference, and the PLL is bypassed. Refer Table 1 for various operating configurations using select lines.

Table 1. Select Input Decoding

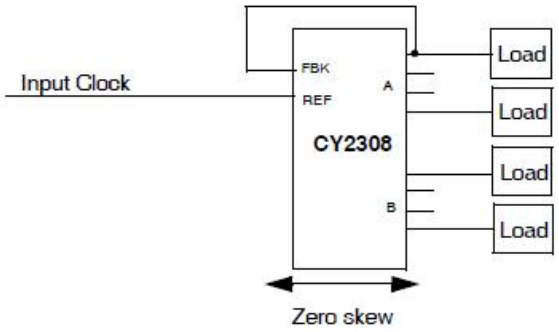
S2	S1	CLK A1-A4	CLK B1-B4	Output Source	PLL
0	0	OFF	OFF	-	OFF
0	1	Driven	OFF	PLL	ON
1	0	Driven	Driven	Ref	OFF
1	1	Driven	Driven	PLL	ON

Applications

Increasing Fanout (Buffering) of a Clock Signal without Skew Penalty

Increasing fanout, increasing drive strength or simply re-establishing a weak clock signal on a long trace requires the use of clock buffers. Traditional high-speed buffers have a propagation delay, which designers have to make note of while performing timing analyses on the design. As shown in Figure 8, PLL based zero delay buffers like the CY2308 provide required buffering without the associated penalty of propagation delay if trace length are kept properly.

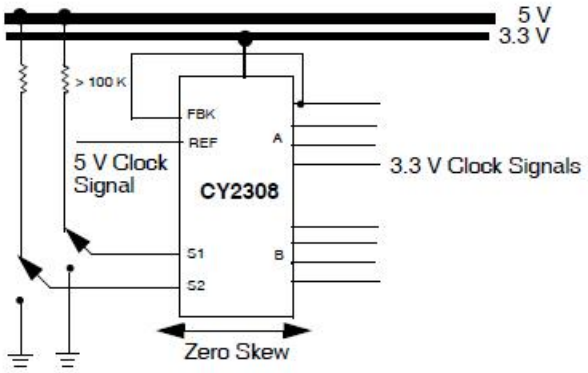
Figure 8. Clock Buffering



5 V to 3.3 V Level Shifting

The CY2308 can act as a 5 V to 3.3 V level shifter. The reference input pad is 5 V signal-compatible. Because many system components still operate at 5 V, this feature provides the capability to generate multiple 3.3 V clocks from a single 5 V reference clock without any propagation delay introduced in the level shifting. Note that this 5 V signal-compatibility is only available on the reference pad; the select inputs on the CY2308 are not 5 V compatible. However, a large resistor (>100 KOhms) can be used to connect the select pins to a 5 V supply. Also, the select lines have weak internal pull-ups and can be left floating. See Figure 9.

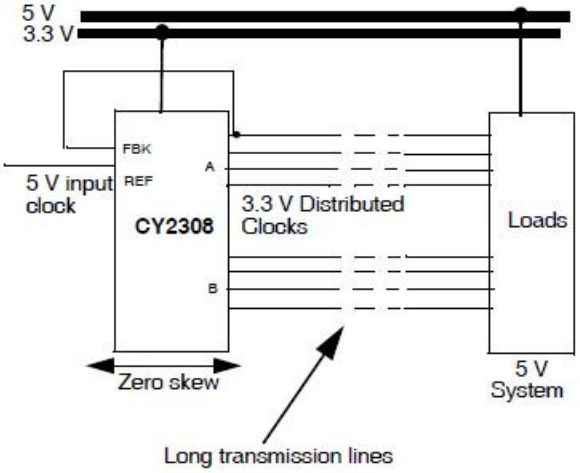
Figure 9. Voltage Level Shifting



Reducing EMI/EMC in Clock Distribution by Level Shifting

Electromagnetic interference (EMI) and Electromagnetic coupling (EMC) are caused by high energy Electromagnetic fields (EMF) travelling around the system. This is caused by high frequency switching signals on a system. Long transmission lines distributing these high frequency signals are the main cause of EMC and EMI. Using proper termination and impedance matching on these lines helps reduce this problem by properly dissipating the transmitted energy (For more information, refer to the application note "Layout and Termination Techniques for Cypress Clock Generators"). Another technique to control EMI and EMC is to reduce the actual energy of the high frequency signal. The CY2308 can be used for this purpose. As shown in the previous example, the CY2308 can be used to convert 5 V clock signals into 3.3 V clock signals on the output. In Figure 10 below, these 3.3 V signals are distributed over long transmission lines instead of 5 V signals, and the energy in the generated EMF is substantially reduced. The output of the CY2308 is 3.3 V, swinging rail to rail, making it 5 V TTL compliant. Hence at the load, it can be driven into a 5 V device. The only requirement here is the presence of a 3.3 V supply.

Figure 10. Reducing EMI



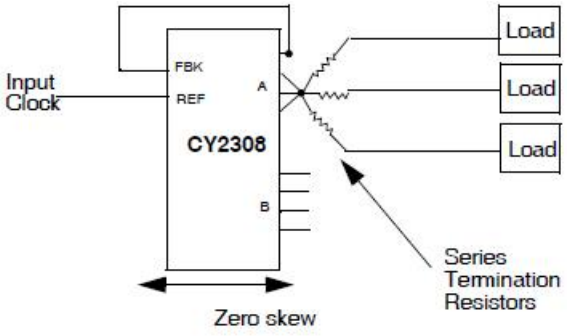
Reducing Output-to-Output Skew by Ganging Outputs

Output-to-Output skew is one of the important factors in today's system design.

An innovative approach to reduce output-to-output skew is to gang multiple outputs together. This method has been used to both increase drive to a particular input and eliminate the output-to-output skews associated with multiple outputs.

In Figure 11, three outputs of CY2308 are shown ganged together, and then distributed to three different loads. This reduces the skew between the clocks delivered to those loads. Note that three separate series termination resistors are shown for the three loads.

Figure 11. Ganged Outputs



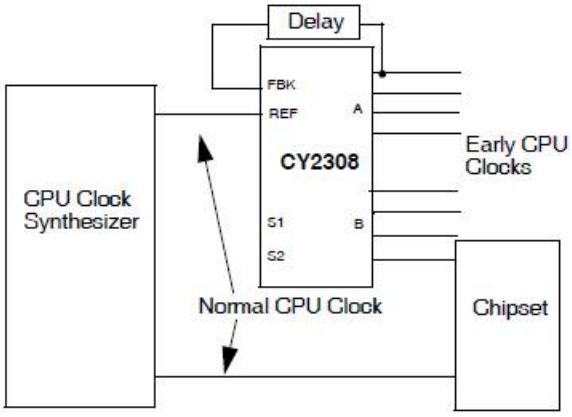
Using External Feedback

CY2308 has an open feedback path which is closed (by driving any output into the FBK pin) for zero delay buffer operation. However, the feedback path can be used for other applications and few of them discussed here.

Generation of 'Early' Clocks

Certain chipsets require some copies of the host clock that arrive early compared to the rest of the copies of the host clock. This is achieved by using a discrete delay element in the feedback path. As we know, the phase detector inside PLL adjusts the output frequency of the VCO so its two inputs (REF and FBK in CY2308) have no phase or frequency difference. Because we have added a discrete delay element in the feedback path, the phase detector will adjust the output of VCO inside the PLL to generate early clocks such that there is no phase difference between REF and FBK as shown in Figure 12. Using CY2308 in this method generates eight outputs, which leads the input signal. These eight outputs are 'Early' as compared to the input clock. See Figure 12 that suggests a circuit implementation to generate such early clocks.

Figure 12. Early Clock



Using Variable Loading to Create Leading or Lagging Clocks

A simple approach can be incorporated in the CY2308 to create leading or lagging clock edges with respect to the REF clock. This can be done by adjusting the load on the clock being fed back to the FBK pin, which is discussed earlier in section "Lead or Lag Adjustments".

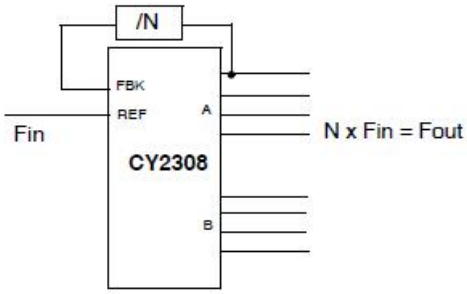
Using Variable Trace length to Create Leading or Lagging Clocks

The leading or lagging can also be achieved by altering the length of the feedback trace, which is discussed earlier in section "Trace Length for Zero, Lead or Lag Adjustment". Typical propagation delay times are 150 ps/inch for microstrip and 180 ps/inch for stripline.

Frequency Multiplier

Using an external divider in the feedback path can create a frequency multiplier out of the CY2308. As shown in Figure 13, a /N divider in the feedback path causes all outputs to run at a frequency which is x N times the input frequency. Whatever the multiplication factor, the input and output frequencies must be within the range of 10–130 MHz, which means the divider cannot be larger than 13.

Figure 13. Frequency Multiplier



Zero Delay Frequency Multiplier/Divider Using Internal Feedback

The Extended Family of Zero Delay Buffers

There are many situations when you need to have simple multiply/divide functions from a single chip without any delay. To serve in these situations, the family of zero delay buffers is expanded to include dividers internal to the CY2308. The block diagram of the CY2308-2, -3, -4 is shown in Figure 14. Driving FBK from a specific output bank can generate the required functions on the outputs.

Table 2 defines the outputs to be used for feedback and can be used as a reference while deriving functions.

Figure 14. Simplified Block Diagram of CY2308-2, -3, -4

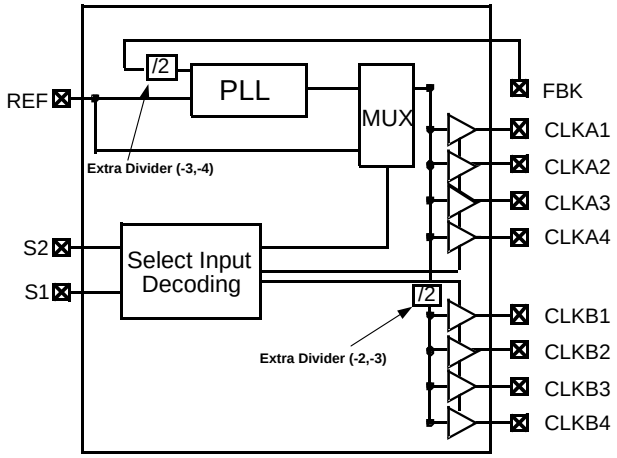


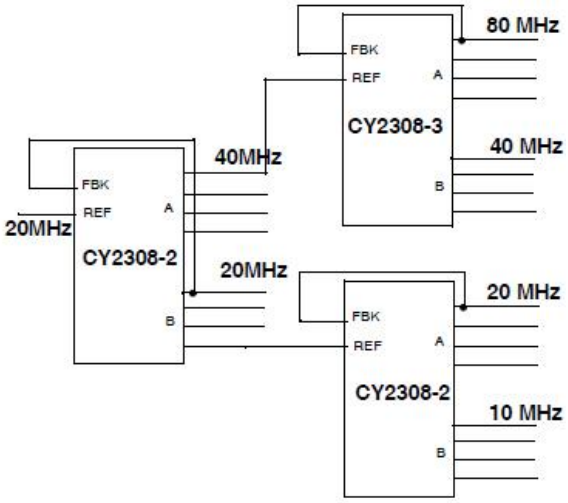
Table 2. CY2308-2,-3,-4 configurations

P/N	FBK	Output Frequency	
	Output	Bank A	Bank B
CY2308-1	A or B	×1	×1
CY2308-2	A	×1	×0.5
CY2308-2	B	×2	×1
CY2308-3	A	×2	×1[11]
CY2308-3	B	×4	×2
CY2308-4	A or B	×2	×2

Multiple Frequency Clock Distribution Network Using Cascaded CY2308

Cascading CY2308-2, 3, 4's can create some interesting clock distribution networks with multiple frequencies having low skew between them. An example is shown in Figure 15. Here a 20 MHz input signal is used to generate multiple copies of 10, 20, 40 and 80 MHz signals, all phase aligned with each other and with zero skew between them. Cascading PLLs in this method may increase jitter on a system. However, good V_{DD} filtering as described in the section "Suggested Layout Recommendations for Cypress's Zero Delay Buffers" reduces this issue.

Figure 15. CY2308-x Clock Tree



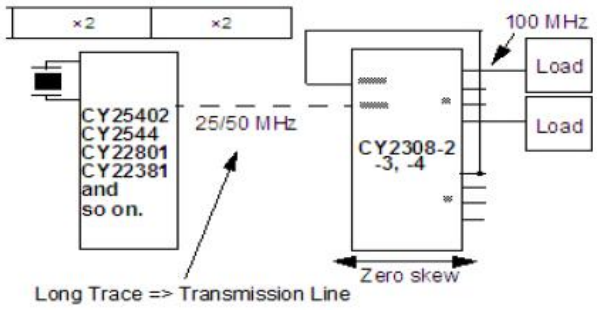
[1] Output phase is in determinant - either 0 ° or 180 ° from input clock. If predictable phase is required, use CY2308-2.

Reducing EMI/EMC Using CY2308-2,-3,-4

In an earlier application we discussed reducing EMI/EMC by reducing the swing from 5 V (rail-to-rail) to 3.3 V (rail-to-rail) with a CY2308. The CY2308-2,-3,-4 provide an additional way to reduce EMI/EMC from long transmission lines, by reducing the frequency of distributed signals.

For example, a certain load requires a high frequency such as 100 MHz and the load is physically located far from the clock source. Normally, to provide the clock, a 100 MHz signal would need to be generated at the source and delivered to the load over a long transmission line (switching at 100 MHz and generating substantial EMI/EMC). An alternative solution shown in Figure 16 is to generate a 25 or 50 MHz clock at the source, transmit this lower frequency over the transmission line and multiply the frequency up to 100 MHz at the load using the CY2308-2, -3, and -4. If this lower frequency clock has reduced edge rates, then the EMI/EMC would be reduced on the long traces as the EMI/EMC depends on the edge rates.

Figure 16. Reducing EMI with CY2308-2, 3, and 4



CY2305/CY2309

In the earlier section, CY2308 was used for understanding few applications of ZDB. Here, the CY2305/CY2309 is used to explain few more applications like PCI and SDRAM buffer solution by ZDB. The CY2305 and CY2309 is a general-purpose ZDB providing five and nine outputs respectively of a single input clock. For simpler system design, CY2305/CY2309 is designed with integrated feedback path. CLKOUT (pin 8 in CY2305 and pin 16 in CY2309) and REF (pin 1 in CY2305/CY2309) are connected internally for simpler system designs.

PCI Buffer Solution

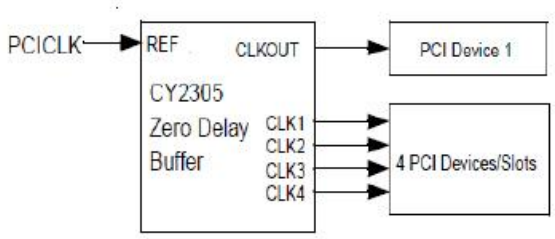
The CY2305/CY2309 ZDBs serve the need in a system that requires more PCI clocks. CY2305 is intended for buffering one clock into five clocks for PCI buffering whereas, CY2309 is intended for buffering one clock into nine clocks for PCI buffering. Five and nine PCI device/slot ZDB solution using these two devices are discussed in the following sections.

The Five Device/Slot Solution

The system requiring five PCI clocks can be served by use of CY2305 ZDB as shown in Figure 17. The guidelines for implementing five-PCI buffer solution are as follows:

- PCI/Slot 1 (CLKOUT) must always be loaded.
- If PCI Slots represent different loads, they will have earlier or later clocks (See "Lead or Lag Adjustments" section)

Figure 17. CY2305 as a Five PCI Device/Slot Zero Delay Buffer Solution

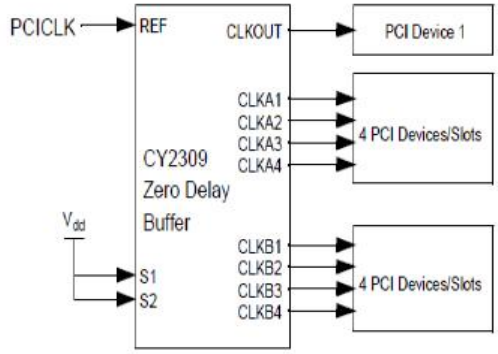


The Nine Device/Slot Solution

The system requiring nine PCI clocks can be served by use of CY2309 ZDB as shown in Figure 18. The guidelines for implementing Nine-PCI buffer solution are as follows:

- PCI/Slot 1 (CLKOUT) must always be loaded.
- Select lines can be used to shut down output banks, for more information, look into the CY2305/CY2309 data sheet.

Figure 18. CY2309 as a 9 PCI Device/slot Zero Delay Buffer Solution



SDRAM Buffer Solution

SDRAM (Synchronous DRAM) is dynamic random access memory (DRAM) that is synchronized with the computer's system bus. SDRAM has a synchronous interface, meaning that it responds to the control inputs only when the clock signal is present.

For systems having one or more than one SDRAM DIMM module, they need to be operated with similar clock with zero delay. The CY2305/CY2309 is best clocking solution for this kind of system as they have integrated feedback path. Examples explained below assume that one SDRAM module accepts total of four clock signals. CY2305 is intended for buffering four clocks for use with one SDRAM module whereas, CY2309 is intended for buffering eight clocks for use with two SDRAM modules. However, for more than two SDRAM modules, cascading of CY2305 and CY2309 is done.

The ZDB solution explained here is for system having three SDRAM DIMM module by cascading CY2305 and CY2309.

Three SDRAM DIMM Zero Delay Buffer Solution

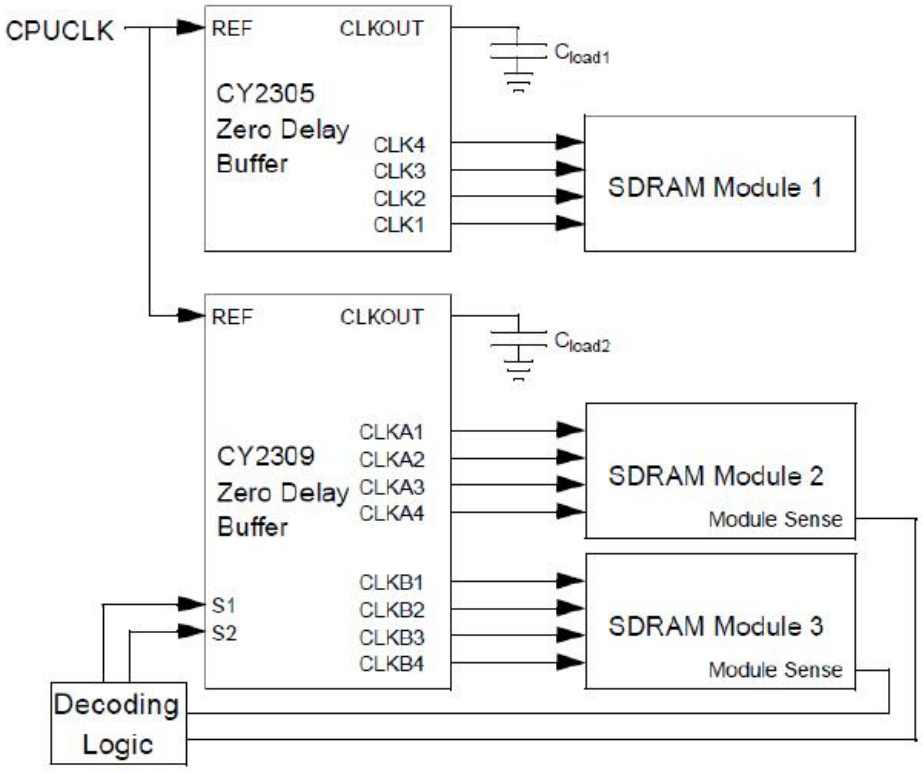
There are two solutions for implementing three SDRAM DIMMs support with the CY2305 and CY2309. The first is the adjustable delay solution and the second is the self adjusting delay solution.

The Adjustable Delay Solution

In Adjustable Delay solution, CLKOUT is loaded with capacitive loads as shown in Figure 19. Hence the delay between SDRAM inputs and reference (CPUCLK) can be adjusted. There are few guidelines/recommendations for implementing three SDRAM DIMM adjustable delay solution:

- For Zero Delay between CPUCLK and SDRAM input, Cload1 and Cload2 must be equal to SDRAM module loading.
- To make the SDRAM inputs lead or lag with respect to the reference input; see the "Lead or Lag Adjustments" section of this Application Note.
- SDRAM modules must be installed in order (module 1 first and module 3 last).
- Module 2 and 3 clocks are tri-stated when those SDRAM modules are not present, but CLKOUT will continue to run.
- Module 1 clocks can only be tri-stated by tri-stating CPUCLK which will also tri-state modules 2 and 3.

Figure 19. Adjustable Delay Solution for three SDRAM DIMM using CY2305 and CY2309



The Self Adjusting Solution

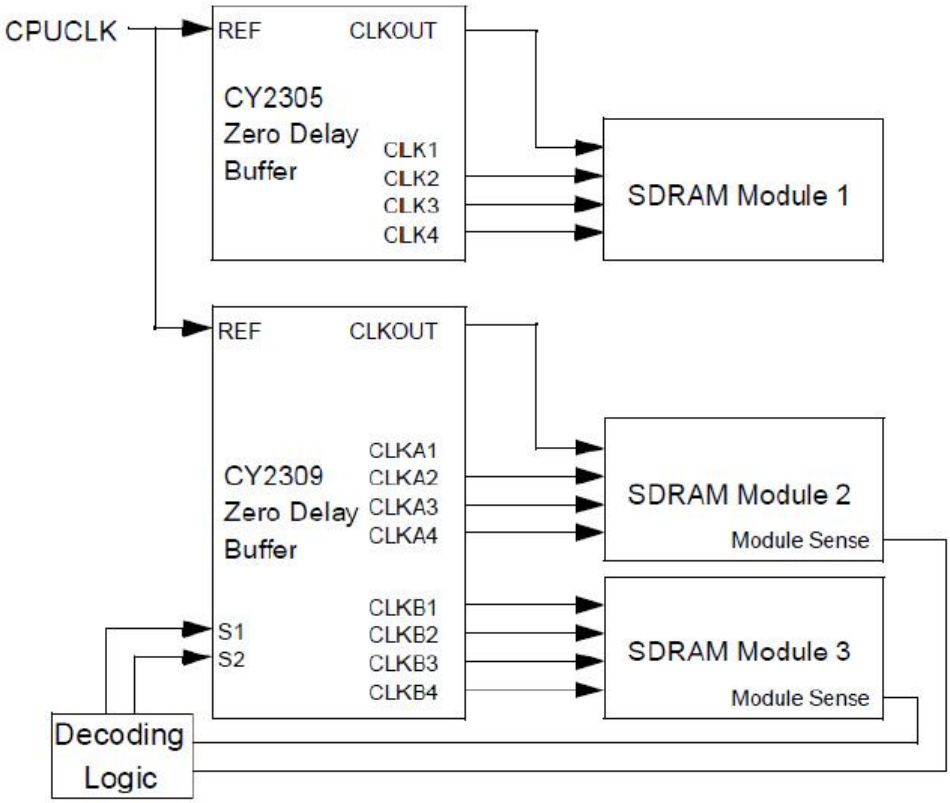
In Self Adjusting Solution, CLKOUT is connected to the SDRAM module directly as shown in Figure 20. Hence, there will always be a zero delay between CPUCLK and SDRAM module inputs (Module 1 and Module 2). There are few guidelines/recommendations for three SDRAM DIMM self adjusting solution as explained below:

- This solution will automatically compensate for different SDRAM input loads (only on Module 1 and Module 2) because CLKOUT is directly connected to SDRAM module.
- CLKOUT must drive CK0 [22] on the SDRAM module 1 and module 2 so that CLKOUT is always fully loaded.
- SDRAM modules must be installed in order (module 1 first and module 3 last).
- Module 2 and 3 clocks are tri-stated when those SDRAM modules are not present, but CLKOUT will continue to run.
- Module 1 clocks can only be tri-stated by tri-stating CPUCLK which will also tri-state modules 2 and 3.

Note that the example explained is for three SDRAM DIMM buffer Solution. Similarly, these ZDB can also be used for 1, 2 or 4 SDRAM DIMM buffer solution. For example, we can use one CY2305 for one SDRAM DIMM solution or one CY2309 for two SDRAM DIMM solutions or two CY2309 for four SDRAM DIMM solutions.

[2] CK0 is one of the Clock input in SDRAM DIMM module. For Ex: in 168-Pin SDRAM DIMM module, Pin 42-CK0

Figure 20. Self Adjusting Solution for three SDRAM DIMM using CY2305 and CY2309

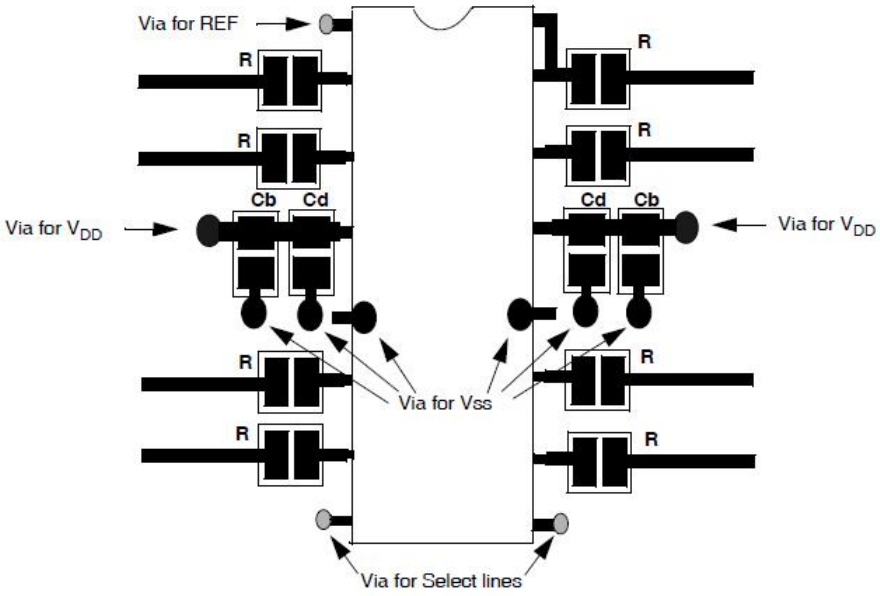


Suggested Layout Recommendations for Cypress's Zero Delay Buffers

1. It is suggested that both a 100-pF and a 0.01-mF capacitor be placed between V_{DD} and V_{SS} on pins 4 and 12. The 0.01-mF capacitor will be used as a bypass capacitor (Cb) to prevent power supply droop when the clock buffer is switching all outputs simultaneously with maximum capacitive load. The 100-pF cap (Cd) is used for decoupling noise from the power supply. Decoupling and bypass capacitors should be placed between the V_{DD} pin and the V_{DD} Via.
2. Use as many vias as possible to ensure solid V_{DD} and V_{SS} layers on the component level. It is recommended that larger vias be used on V_{DD} and V_{SS} pins. It is also suggested to use individual vias to V_{SS} on all decoupling capacitors, bypass capacitors and V_{SS} pins, as shown in Figure 21. Use of good quality surface mount capacitors is recommended.
3. A series damping resistor used to prevent wave reflection is suggested for each of the clocks being driven by the CY2308. This value can be between 10 and 75 ohms depending on the impedance of the circuit board traces. Series termination resistors should be placed as close to the output pins as possible.

Note For any additional assistance with Schematic and Layout verification, contact Cypress customer support at www.cypress.com/support.

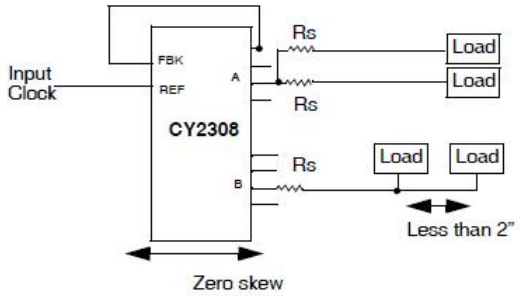
Figure 21. Layout Recommendations for the CY2308



Suggested Routing of Clock Signals for Cypress's Zero Delay Buffers

1. When driving multiple loads on a single output, either daisy chain the outputs (when distance < 2" at 50 MHz) or route individual traces to each load from as close to the source as possible. When individual traces are used from a single output, each trace should have a separate series termination resistance. See Figure 22.
2. Ensure that a minimum number of vias are used on clock signals. Try to route clocks on a single layer.
3. Do not use 90 degree angles when routing clocks. Use smooth curving traces as much as possible.
4. Ensure that a solid ground plane is on the layer adjacent to the clock trace routing layer.

Figure 22. Driving Multiple Outputs



Summary

Cypress's ZDB is a device that can fan out one clock signal into multiple clock signals with no delay and low skew between the outputs. Increasing fan out, increasing drive strength or simply re-establishing a weak clock signal on a long trace requires the use of clock buffers. Cypress' ZDB is an ideal choice in such applications. The CY2305/CY2309 ZDBs serve the need in a system that requires more PCI clocks. CY2305 is intended for buffering one clock into five clocks for PCI buffering whereas, CY2309 is intended for buffering one clock into nine clocks for PCI buffering. It is recommended to follow the aforementioned usage examples and layout guidelines while using the Cypress ZDB device in your application.

Document History

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Document Number: 001-35239

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1509343	RGL	10/16/2007	New spec. # for note to be added to spec. system.
*A	3020452	KVM	09/01/2010	General revision. Removed dated material.
*B	3180416	BASH	02/23/2011	Removed all references of obsolete part (CY2308-5). Added note on page 11 to contact Cypress for assistance on Schematic and Layout verification.
*C	3242252	CXQ	04/27/2011	Minor Template updates
*D	3358221	BASH	08/30/2011	Change Title to "Understanding Zero Delay Buffer". Changed Abstract section.
*E	3537194	PURU	02/28/2012	Rewrote Whole Application note Added Contents Section Added CY2305 and CY2309 Zero delay Buffer information in whole document for explaining PCI Buffer solution and SDRAM Buffer solution. Updated in new template.
*F	4404356	MEMJ	06/10/2014	Updated in new template. Completing Sunset Review.

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