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Spec No: 001-16957

Spec Title: CYPRESS USB-HOST, OTG, HUB, AND PERIPHERAL SELECTION GUIDE - AN1222

Sunset Owner: Prajith Cheerakkoda (PRJI)

Replaced by: None

Cypress USB-Host, OTG, Hub, and Peripheral Selection Guide

AN1222

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Associated Project: None
Software Version: None
Associated Application Notes: None

Abstract

The USB designers are guided through the process of determining the most suitable Cypress USB chip for their product in this Application Note. It covers only the generic USB devices and does not cover the USB mass-storage solutions offered by Cypress.

Introduction

With the widest portfolio of USB chips, Cypress Semiconductor has a device for every application. AN1222 takes you through the process of determining whether you need a device with host, hub, or peripheral functionality. It helps also you decide whether your application requires low, full, high, or super-speed signaling.

Step 1 - Host, OTG, Hub, or Peripheral?

Every USB system must have only one host; that is, a bus master. USB does not support a peer-peer topology. A host has a downstream port to which peripherals (slaves) can be connected either directly or via one or more hubs. The host initiates all USB traffic either by transmitting data itself, or requesting data from a device on the bus. USB host controllers are typically PCI bus devices, controlled via the PCI bus by a powerful microprocessor. Most PC chipsets now include an integrated USB host controller. When the PC is removed from the system, and the application requires a USB host in a set-top box or PDA/cell - phone or a USB OTG in a PDA/cell - phone, Cypress recognizes the paradigm shift towards an embedded host/OTG market and offers the EZ-Host/EZ-OTG, SL811HST as solutions. To learn more about these products, see the “Cypress USB Embedded Host/OTG Selection Guide” section of this application note.

A USB hub is a repeating device that allows multiple downstream peripherals to be connected to a single upstream host or hub port. The USB specification permits up to five tiers of hubs between a peripheral and a host. A hub cannot originate downstream traffic on its own downstream ports. All downstream data traffic is simply retransmission of data that the hub has received on its upstream port. In addition, a hub must behave in a similar manner to a peripheral on its upstream port, because the hub controller function can itself be regarded as a peripheral. It is possible to have a hub function and an independent peripheral function implemented in the same device; for example, a monitor or keyboard hub. To select the USB hub device that is right for your application, see the “Cypress USB Hub Device Selection Guide” section of this application note.

A peripheral has only one upstream port. Through this port, the device is connected to the downstream port of a host, either directly or through one or more hubs. A peripheral never transmits data without receiving a request from the host to do so.

Step 2 - Low-Speed, Full-Speed, High-Speed, or Super-Speed Peripheral?

USB has four data rates: low-speed, full-speed, high-speed, and super-speed .The signaling rates are 1.5 Mbps, 12 Mbps, 480 Mbps, and 5 Gbps respectively, but these rates do not accurately reflect the data throughput available to a single device using that signaling rate.

For low-speed signaling, the best guaranteed throughput is 8 bytes of payload data every 10 ms, per endpoint which is 6400 bps. If you compare this to RS-232 with one start, one stop, and one parity bit with continuous transmission (without handshake), it is equivalent to 8800 baud on a

traditional serial link. Using two endpoints on a single low-speed USB device may achieve an RS-232 equivalent data throughput of 17600 baud.

If this data throughput is adequate for your application, see the "Cypress Low-Speed Peripheral Device Selection Guide" section of this application note.

For full-speed signaling, the payload data throughput is limited only by the 12 Mbps signaling rate and the protocol overhead. The maximum data throughput shared between all devices connected to a single USB host is 1.216 MBps, which is equivalent to 9.728 Mbps. A single device to reserve up can only reserve up to 90% of this bandwidth using interrupt or Isochronous transfers. Sustained data throughputs of 8.7 Mbps have been demonstrated, even using Cypress's lowest specification AN21xx full-speed device. However, when bandwidth requirements approach the full-speed limit, it is recommended that high-speed signaling be selected. If this data throughput is adequate for your application, see the "Cypress Full-Speed USB Peripheral Device Selection Guide" section of this application note.

For high-speed signaling, the payload data throughput is limited by 480 Mbps signaling and the protocol overhead. The maximum data throughput shared between all devices connected to a single USB host is 53.248 MBps, which is equivalent to 425.984 Mbps. FX2 is capable of operating at the maximum throughput that high-speed signaling can offer. If this data throughput is adequate for your application, see the "Cypress High-Speed USB Peripheral Selection Guide" section of this application note; otherwise, see the "Cypress Super-Speed USB Peripheral Selection Guide" section of this application note

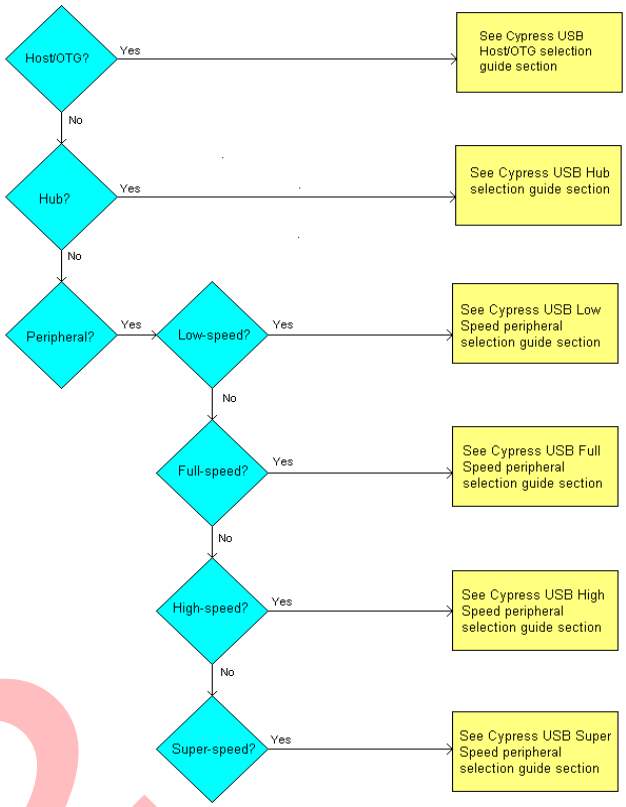

Figure 1 Device Selection Decision Tree

Cypress USB Embedded Host/OTG Selection Guide

For host applications, Cypress offers the SL811HST and EZ-Host/EZ-OTG for use in a variety of embedded applications such as PDAs, set-top boxes, MP3 players, printers, KVM switches, and so on.

The host/slave functionality provides support for both full-speed and low-speed devices in host mode. When a connection to a USB host is detected, the SL811HST automatically switches to slave mode. The SL811HST interfaces to any CPU or bus, which allows you to choose any microprocessor that best suits your application. It also supports a variety of microprocessors and operating systems, including VxWorks, Linux, and Windows CE.

The EZ-Host/EZ-OTG is a single chip programmable USB dual-role (host/peripheral) controller with two configurable serial interface engines (SIEs). These engines support a large number of interface protocols, which makes them a good choice for any embedded USB host/EZ-OTG design.

For embedded host designs that need a mass storage stack, use the EZ-Host mass storage reference design kit (CY4640). Use the CY4640 reference design kit to take your products to market in the shortest possible time.

Table 1. Cypress USB Embedded Host Selection Guide

	SL811HST	EZ-Host/EZ-OTG
RAM (Bytes)	256	16 k
ROM (Bytes)	N/A	8 k
Number of I/Os	8	32 (EZ-Host) 25 (EZ-OTG)
Package type	48-pin TQFP	100-pin TQFP (EZ-Host) 48-pin FBGA (EZ-OTG)
Interface	Memory-mapped or Programmed I/O	HPI, HSS, SPI, UART, GPIO
Development kit (DVK)/reference design kit (RDK)	CY3662 (DVK)	CY3663 (DVK) CY4640 (EZ-Host mass storage RDK)

Cypress USB Hub Device Selection Guide

Cypress offers a broad family of USB devices for USB hub applications ideally suited for docking stations, integrated keyboard, motherboard, monitor hubs, and so on. Also included in the Cypress USB hub device family are the stand alone USB hubs.

Cypress has announced HX2VL™ (CY7C65642), a high-performance standalone USB hub controller that is compliant with the USB 2.0 Specification. The Cypress innovative 'Tetra' architecture includes four downstream USB ports and four "transaction translators" (TT), making it the highest performance hub available. This self-contained device features an integrated SIE, hub controller, hub repeater, four transaction translators, and USB data transceivers. HX2VL can improve time-to-market in many USB 2.0 designs, including standalone hubs, motherboard hubs, and monitor hubs.

HX2VL can support four downstream ports as a bus-powered USB 2.0 hub device. Power management for all downstream ports supports power switching and over current detection with individual or ganged control. The four downstream ports support high-speed, full-speed, and low-speed devices. Four individual transaction translators are implemented, providing full 12 Mbps performance to each full-speed downstream port, whereas single transaction translator designs must split the full-speed bandwidth between all USB 1.1 peripherals attached to the hub. HX2VL has support for SPI and I^2C EEPROM that allows user customization of vendor and product IDs, removable ports, and so on, Cypress has also integrated the 1.5 kΩ pull-up resistor on the D+ line that is required for connect/disconnect detection on the upstream USB port.

Table 2. Cypress USB Hub Device Selection Guide

	CY7C65640A	CY7C65630/31	CY7C65620	CY7C65642	CY7C65632
Typical Applications	4-port USB 2.0 Hub	4-port USB 2.0 Hub	2-port USB 2.0 Hub	4-port USB 2.0 Hub	4-port USB 2.0 Hub
EEPROM	SPI	SPI	SPI	SPI, I^2C (only in 28-pin QFN)	SPI, I^2C (only in 28-pin QFN)
Number of transaction translators (TT)	4	1	1	4	1
Power	≤460 mA	≤260 mA	≤190 mA	≤100 mA	≤100 mA

consumption					
Package types	56-pin QFN	56-pin QFN	56-pin QFN	48-pin TQFP 28-pin QFN	48-pin TQFP 28-pin QFN
Development Kit/Reference Design kit	CY4602	CY4606	CY4605	CY4607/08	CY4607/08

Cypress Low-Speed Peripheral Device Selection Guide

The Cypress low-speed USB device family offers powerful, flexible, integrated solutions for a wide range of USB applications. The devices feature the industry's smallest 8-bit M8C core with RAM, flash, USB logic, and a USB transceiver integrated into a single device.

The latest line of Cypress low-speed devices is the enCore II™ (enhanced component reduction) family, featuring a range of USB chips with an internal oscillator that removes the requirement for any external resonator or crystal. Other components commonly found in low-speed USB applications such as pull-up resistors, wake-up circuitry, and a 3.3 V regulator are integrated into the chip to give an overall reduction in system cost.

Table 3. Cypress Low-Speed Peripheral Device Selection Guide

	CY7C63310	CY7C63801	CY7C638X3
Typical applications	Mice, joysticks, barcode scanners, security dongles, and so on.	Mice, joysticks, barcode scanners, security dongles, and so on.	Mice, joysticks, barcode scanners, security dongles, and so on.
RAM (Bytes)	128	256	256
Flash (Bytes)	3	4	8
Number of I/Os	14	14	16 (CY7C63813) 20 (CY7C63823)
Number of endpoints	3	3	3
Package types	16-pin SOIC	16-pin SOIC	16-pin SOIC, 24-pin QFN (CY7C63803), 18-pin PDIP, 18-pin SOIC (CY7C63813), 24-pin QSOP, 24-pin SOIC, die form, Wafer form (CY7C63823), 32-pin QFN (CY7C63833)
Development Kit	CY3655	CY3655	CY3655

Cypress Full-Speed USB Peripheral Device Selection Guide

Cypress offers a broad range of solutions for full-speed applications such as printers, scanners, xDSL modems, and digital cameras.

The CY64013C range of full-speed USB devices is based on the same architecture as the full-speed hub devices, and offers a simple and straightforward firmware migration path from these products.

The EZ-USB® range of full-speed USB devices is a richly featured family of devices with a patented RAM-based code storage architecture that allows the easiest possible in-field upgrading of product firmware. The firmware can be easily upgraded via download through USB. EZ-USB provides significant improvements over other USB architectures including an enhanced 8051 core, 16 Kbytes of RAM, an intelligent USB core, and high-performance I/O ports.

The EZ-USB FX1™ family showcases the highest performance full-speed USB device available on the market, and offers a simple and straightforward upgrade path to high-speed applications. The EZ-USB FX1 builds on the EZ-USB feature set, including an intelligent USB core, enhanced 8051, 16 KB of RAM, and high-performance I/O. The CY7C64713 enhances the EZ-USB family by providing faster operation and more ways to transfer data in and out of the chip at very high data rates. The new faster, extended EZ-USB FX1 family maintains code compatibility with EZ-USB and many of the original family's characteristics. EZ-USB FX1 expands the feature set that makes EZ-USB a popular choice for high-performance, highly integrated USB applications, adding super fast I/O, slave FIFOs, and a general programmable interface (GPIF) engine.

The internal FIFOs can be configured for 8 bit or 16-bit data paths, and can be mastered by the EZ-USB FX1 or external logic. The GPIF can be configured to provide a glueless to ASICs, DSPs, or standard interfaces such as ATAPI, UTOPIA, EPP (enhanced parallel port), wireless LAN chip sets, home PNA chip sets, and so on. The interface possibilities are endless.

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in many consumer and communication applications.

The enCoRe V family of devices is designed to replace multiple traditional full-speed USB microcontroller system components with one, low-cost single-chip programmable component. Communication peripherals (I^2C/SPI), a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts. Both enCoRe III and enCoRe V have the advantage of bootloading through USB or I^2C. Similar to other devices of enCoRe family, it features an internal oscillator that removes the requirement for an external oscillator. This product is an enhanced version of the Cypress successful full-speed USB peripheral controllers. Enhancements include faster CPU at lower voltage operation, lower current consumption, twice the RAM and Flash, hot-swappable I/Os, I^2C hardware address recognition, new very low current sleep mode, and new package options.

Table 4. Cypress Full-Speed Peripheral USB Device Selection Guide

	EZ-USB FX1 (CY7C64713)	CY7C64013C	CY7C64215	CY7C6431x/4x/5x
Typical applications	DSL Modems, memory card readers, ATAPI interface, networking	Analog modems, fingerprint, scanners, bar code reader	Mouse (optomechanical, optical, trackball), gamepads, barcode scanners, POS terminal	Mid-tier/Feature-rich USB dongle, remote control host module, USB keyboard
Microcontroller	Enhanced 8051	8-bit USB optimized	M8C	M8C
CPU Speed (MHz)	12, 24, 48 (firmware selectable)	12	24	24
Number of I/Os	24 (56-pin package) 40 (100 and 128-pin package)	19	22 (28-pin SSOP) 50 (56-pin QFN)	11 (CY7C6431x), 25 (CY7C6434x), 36 (CY7C6435x)
Firmware memory	16 k of RAM	8 k OTP PROM	16 k flash and 1 k SRAM	16 k flash and 1 k SRAM (CY7C64315/45/55), 8 k flash and 1 k SRAM (CY7C64343), 32 k flash and 2 k SRAM (CY7C64316/56)
Data path	8- or 16-bit	8-bit	N/A	N/A
Data transfer mode	Manual, Auto	Micro instructions	N/A	N/A
Parallel interface	Programmable (GPIF), slave FIFOs	HAPI	N/A	N/A
Serial interface	I^2C, 2 UARTs	I^2C	I^2C, SPI, 8-bit UART	I^2C, SPI, software TX
Number of endpoints	7 (3 fixed, 4 large configurable endpoints)	5 configurable endpoints	5 configurable endpoints	9 configurable endpoints
Max. bulk endpoint size	512	32	N/A	N/A
Max. Isochronous endpoint size	1024	32	N/A	N/A
Package	56-pin SSOP, 56-pin QFN, 100-pin TQFP, 128-pin TQFP	28-pin SOIC	28-pin SSOP, 56-pin QFN	16-pin QFN (CY7C6431x), 32-pin QFN (CY7C6434x), 48-pin QFN (CY7C6435x)
Development kit	CY3674	N/A	CY3664	CY3660

Cypress High-Speed USB Peripheral Selection Guide

The CY7C68013A is the Cypress flagship high-speed USB peripheral device. It is an integrated USB 2.0 solution that fully uses the bandwidth capabilities of USB 2.0. The FX2LP™ family offers higher performance and a higher level of integration than the previous EZ-USB products, including a 40x jump to a 480 Mbits/sec signaling rate. The FX2LP builds on the EZ-USB FX device by providing USB 2.0 support with an integrated transceiver, smart SIE, enhanced 8051 microcontroller, and a memory and programmable I/O interface. EZ-USB FX2LP can operate at either high-speed or full-speed.

Table 5. Cypress High-Speed USB Peripheral Selection Guide

	CY7C68013A
Microcontroller	Enhanced 8051
CPU Speed (MHz)	12/24/48 (Firmware Selectable)
Number of I/Os	24-40
Max I/O rate	96 MB/s
Firmware memory	16 KB
Data path	8- or 16-bit
Data transfer mode	Auto transfer (max USB 2.0 bandwidth)
Parallel interface	Programmable (GPIF), slave FIFOs
Serial interface	I^2C, 2 UARTs
Number of endpoints	7 (3 fixed, 4 large configurable endpoints)
Max. bulk endpoint size	512 Bytes
Max. isochronous endpoint size	1024 Bytes
Package	56-pin SSOP, 100-pin TQFP, 128-pin TQFP
Development Kit	CY3684

Cypress Super-Speed USB Peripheral Selection Guide

Cypress EZ-USB FX3 is the next generation USB 3.0 peripheral controller that provides highly integrated and flexible features that enable developers to add USB 3.0 functionality to any system. EZ-USB FX3 has a fully configurable, parallel, general programmable interface called GPIF II that can connect to any processor, ASIC, or FPGA. The general programmable interface GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB2.0 product. It provides easy and glueless connectivity to popular interfaces such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interface, parallel ATA, and so on.

Table 6. Cypress Super-Speed USB Peripheral Selection Guide

	CY7USB3014
Microcontroller	ARM926EJ
CPU Speed (MHz)	200
Number of I/Os	60
Max I/O rate	320 MBps
Firmware memory	512 kB Embedded SRAM and 16 kB TCM
Data path	8, 16, 24, or 32-bit
Interfaces	GPIF II, DMA, I^2C, UART, I^2S, SPI, GPIO
Number of endpoints	32
Package	121-ball FBGA

Summary

Cypress offers the industry's broadest line of USB devices and the development tools to support them. Cypress USB devices facilitate the design of low-speed, full-speed, high-speed, and super-speed peripherals, USB hubs in addition to USB hosts, USB OTG, and other systems that communicate via the USB standard.

Document History

Document Title: Cypress USB-Host, OTG, Hub, and Peripheral Selection Guide – AN1222

Document Number: 001-16957

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1345183	AASI	08/03/2007	New spec.
*A	3324612	AASI	08/01/2011	Updated template. Major rewrite.
*B	4108854	RSKV	08/30/2013	Obsolete application note

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.

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