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Spec No: 001-14537

Spec Title: AUTO CLOCK SWITCHING USING CYPRESS FAILSAFE(TM) DEVICES (CY23FS04/08) - AN1209

Sunset Owner: Hiromu Takehara (XHT)

Replaced by: None

Auto Clock Switching Using Cypress Failsafe™ Devices (CY23FS04/08)

Associated Project: No
Associated Part Family: CY23FS08/04
Related Application Notes: None

AN1209 describes the use of the Cypress Failsafe CY23FS08/04 as a clock redundancy device. Smooth transition between the two frequencies has been demonstrated. These input clocks can be of the same frequency or of different frequency (a fixed multiple of each other). A sample circuit to accomplish input clock redundancy is provided

Introduction

A clock-redundancy device provides an output clock that is automatically switched between two input reference clocks if one of them fails. This failsafe device is especially suitable for the following applications:

- Auto clock detection during power-up.
- Auto clock switching upon failure of one of the clock sources.
- Providing a stable clock even when both input reference clocks are missing.

Figure 1. Test Circuit Showing CY23FS08 as Auto Clock Switching Device

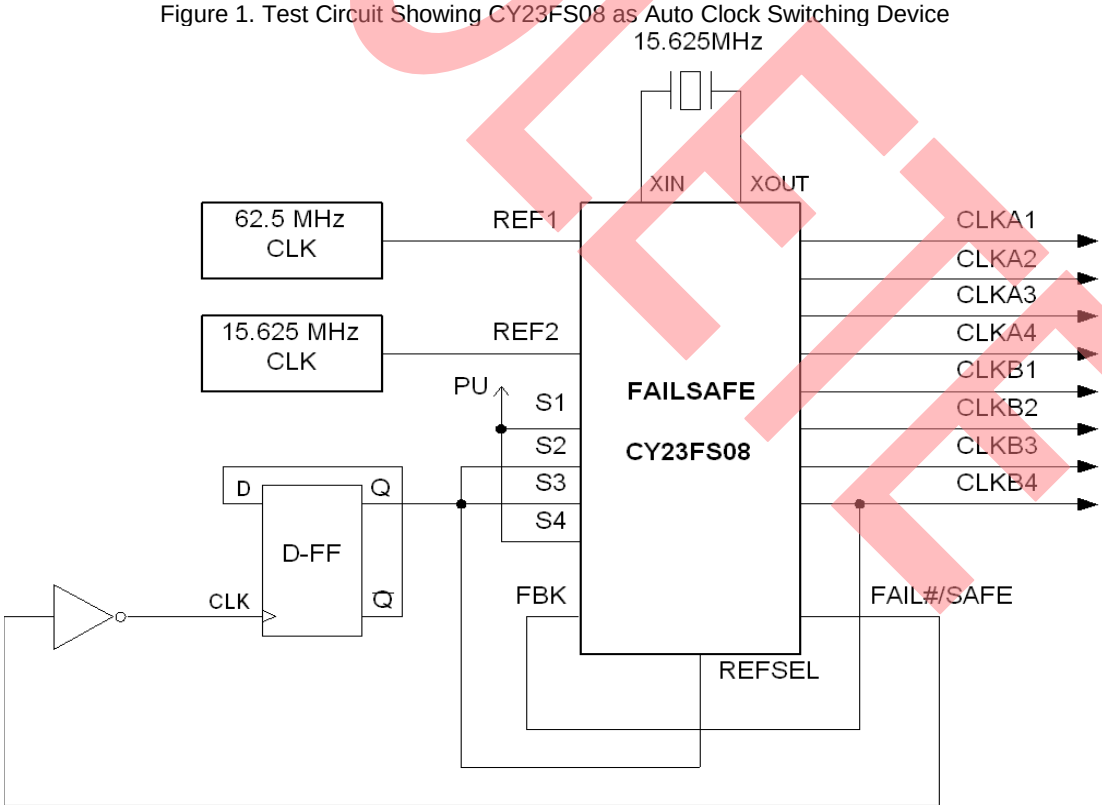


Figure 1 shows a simplified circuit diagram that includes these features. More complex external programmed logic can be used to access the full features of this device.

There are several other features that are advantageous in system design when using this failsafe device, including:

- High-frequency clock jitter cleanup due to the low bandwidth of the DCXO
- Smooth clock switching
- Multiple outputs with zero delay buffer (ZDB) functionality.

Functional Description

Figure 1 shows simple circuitry that may be used to switch input clocks between REF1 and REF2. 62.500 MHz and 15.625 MHz clocks from two different signal generators are used as the inputs REF1 and REF2, respectively. A 15.625 MHz XTAL is used in the DCXO circuit of the Failsafe device. The FAIL#/SAFE output is the valid reference indicator that goes low when the selected input reference clock is either missing or its frequency drifts out of lock range. This FAIL#/SAFE output is inverted and used to toggle the D flip-flop output, which in turn drives the select lines S[1:4] and the REFSEL input of the Failsafe device. The signal at the inputs, outputs, and the control lines (REFSEL and S[1:4]) are shown in the following table.

REF INPUT	REFSEL	S[1:4]	CLK OUTPUT
REF1 (62.5MHz)	High	[1111]	62.5MHz
REF2 (15.625MHz)	Low	[1001]	15.625MHz

Upon detection of a missing clock at the REF1 input, the FAIL#/SAFE output goes LOW, which in turn changes the REFSEL and select lines S[1:4] to a division ration that is appropriate for REF2 input clock. The DCXO then locks to the REF2 clock input.

This example shows a real application of using the FAIL#/SAFE line provided by the device to change the device modes using REFSEL and select lines S[1:4]. The Failsafe device also provides a clock in the event that both input reference clocks fail; this is done by maintaining the last phase and frequency information of the last valid reference clock.

The switching characteristics of the output clock of the failsafe device are shown in Figure 2 and Figure 3. These are modulation domain analyzer screen captures showing the frequency switch when one of the reference clocks is turned off. Smooth frequency switching with a maximum transition time of 200 ms has been measured.

Figure 2. Modulation Domain Analyzer Screen Capture Showing Output Clock Switching from 15.625 MHz to 62.5 MHz

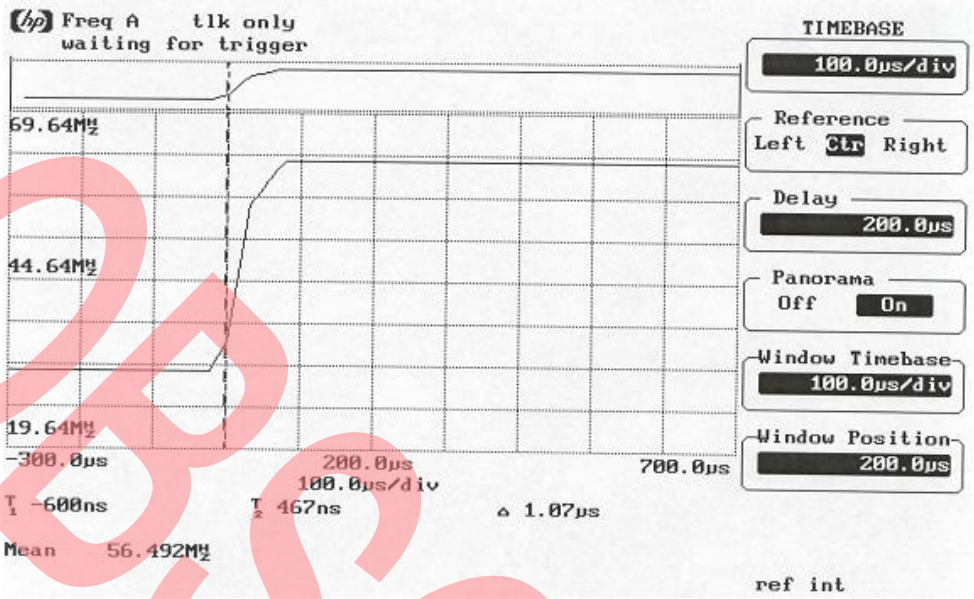
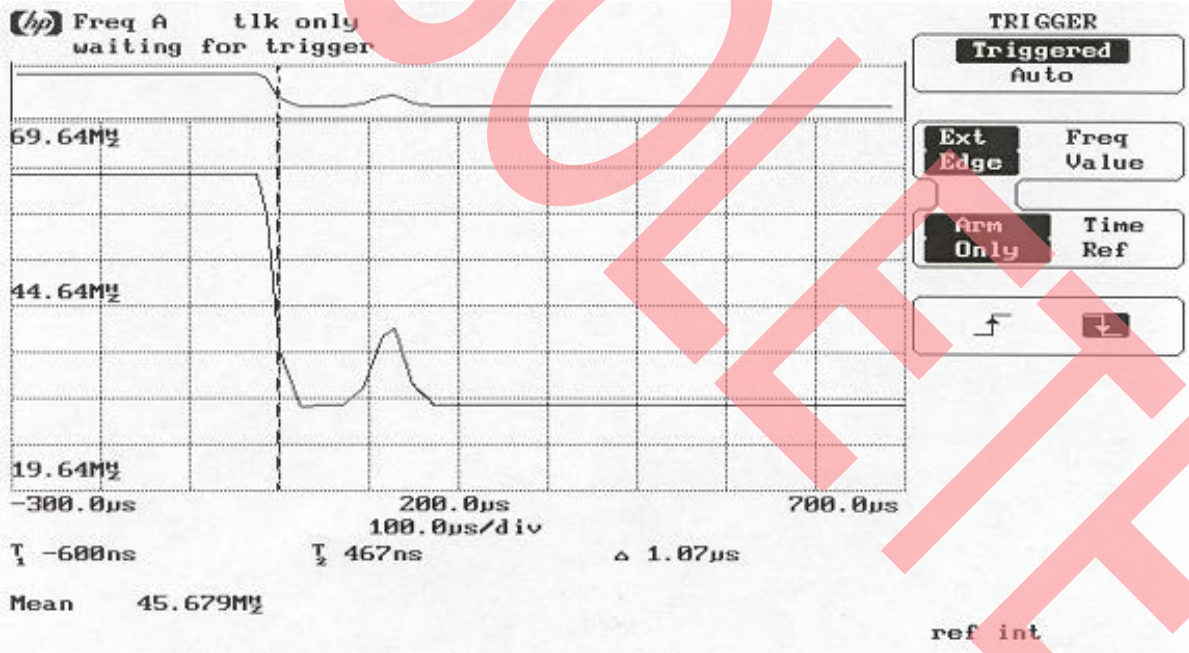


Figure 3. Modulation Domain Analyzer Screen Capture Showing Output Clock Switching from 62.5 MHz to 15.625 MHz



Document History

Document Title: Auto Clock Switching Using Cypress Failsafe™ Devices (CY23FS04/08) – AN1209

Document Number: 001-14537

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	956503	RGL	04/12/2007	Recataloged spec
*A	3244640	CXQ	05/04/2011	Updated Template
*B	4393300	XHT	05/29/2014	Sunset review. Updated template
*C	4468126	XHT	08/15/2014	Obsolete document

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