AN1125

Interfacing the CYS25G0101DX to Differential LVPECL

Author: Cypress
Associated Project: No
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Associated Application Notes: AN1162

AN1125 demonstrates how to connect the single-ended interface of CYS25G0101DX to a differential LVPECL device and provides simple formulas to help users calculate the values of the termination circuitry.

Introduction

The CYS25G0101DX is a SONET OC-48 Transceiver. It provides complete parallel-to-serial and serial-to-parallel conversions, clock and data recovery, and clock synthesis functions in a single chip. The synchronous parallel input and output interface of the CYS25G0101DX are HSTL and LVCMOS compliant, and support differential and single ended LVPECL standards devices. The following sections will discuss how to interface a differential LVPECL device to the CYS25G0101DX.

Parallel Transmit Data Inputs

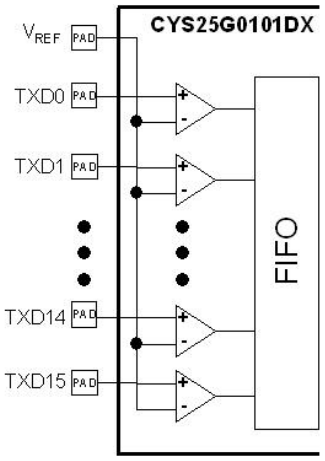
The CYS25G0101DX equips a 16 x 155.52 Mbps parallel transmit data bus. The inputs are a single-ended interface with a common reference voltage at V_{REF}. Figure 1 shows the block diagram of the parallel transmit data input port, and Table 1 shows the specification of the inputs. The receiver threshold voltage requirement in the LVPECL specification is ±270 mV and the input threshold of the CYS25G0101DX is +130 mV, –100 mV. Therefore, the receiver meets the LVPECL requirement.

An LVPECL device has a differential output and an LVPECL driver requires an external load defined as 50 ohms at V_{CC} – 2 V. Figure 2 illustrate how to interface a differential LVPECL driver to a single-ended input. Detailed information about the ECL output configuration, as well as the matched loading, can be found from the "HOTLink® Design Considerations" - AN1162.

Transmission Line Termination

The objective of a transmission line termination is to prevent the reflection of power from the destination back to the source. The PECL output is designed to drive a 50-ohm loading at V_{CC} – 2.0 V. In a Thévenin equivalent termination (Figure 3), R1, R2, R3, and R4 are used to form a Thévinin equivalent circuit consisting of a 50-ohm termination resistor (R_T) connected to V_{CC} – 2.0V (V_{TT}). R1, R2, R3, and R4 can be calculated as follows:

Figure 1. The Parallel Transmit Data Inputs of the CYS25G0101DX



$R1 = R3 = (V_{CC} * R_T)/V_{TT}$ Equation 1

$R2 = R4 = (V_{CC} * R_T)/(V_{CC} – V_{TT})$ Equation 2

Where V_{CC} = 3.3 V, R_T is termination resistance = 50 Ω, $V_{TT} = V_{CC} – 2.0$ V

From the Equation 1 and 2, R1 = R3 = 127 Ω and R2 = R4 = 82.5 Ω.

R5 and R6 form a voltage divider to provide a reference voltage for the V_{REF} pin for incoming signals. From Table 2, we can calculate the voltage range to be between 1.88 V and 2.05 V. The recommended resistors in this example are R5 = 820 Ω and R6 = 1.3 kΩ.

Table 1. The DC Specification of the Parallel Transmit Data of the CYS25G0101DX

Parameter	Description	Min	Max	Unit
V_{IHH}	Input HIGH Voltage	V_{REF} +0.13	V_{cc} +0.13	V
V_{ILH}	Input LOW Voltage	-0.3	V_{REF} - 0.1	V

Figure 2. Connecting the Parallel Transmit data Input of the CYS25G0101DX to an LVPECL Device

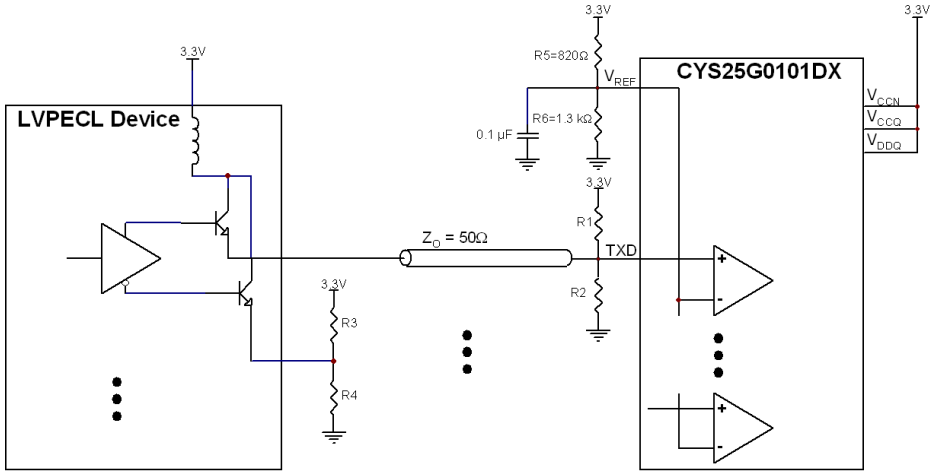
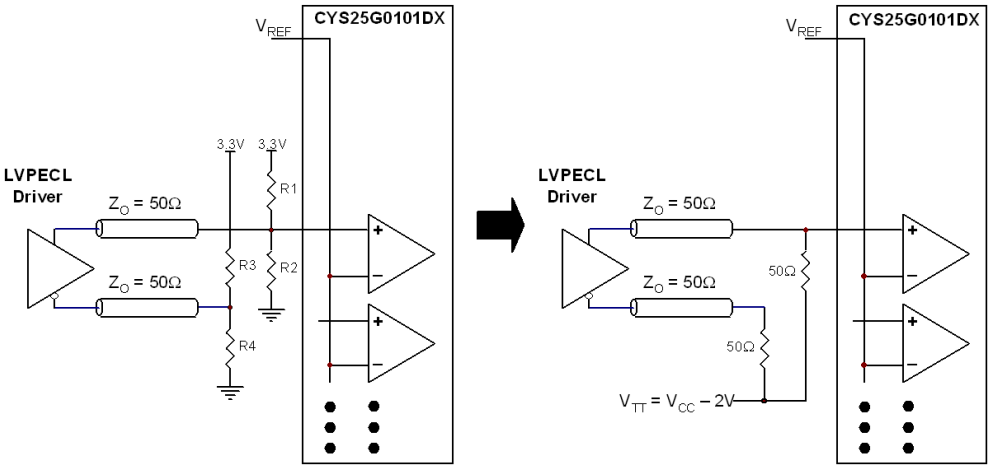


Figure 3. Thévenin Equivalent Termination



Parallel Receive Data Outputs

The parallel receive data output of the CYS25G0101DX is a 16-bit single ended output port which can support HSTL, LVCMOS, and LVPECL devices. Figure 4 illustrates how to connect the parallel receive data output of the CYS25G0101DX to an LVPECL device. Resistors R7 and R8 form a 50-ohm termination for the CYS25G0101DX. The output level of the CYS25G0101DX is LVCMOS, and thus it is necessary to convert this to an LVPECL-level signal by using a damping resistor, R_D. To calculate R7, R8, and R_D in Figure 4, it is necessary to understand the LVPECL output specification. Figure 5 illustrates the JEDEC LVPECL input and output signal levels and these values are summarized in Table 2.

Figure 4. Connecting the Parallel Receive Data Output of the CYS25G0101DX to an LVPECL Device

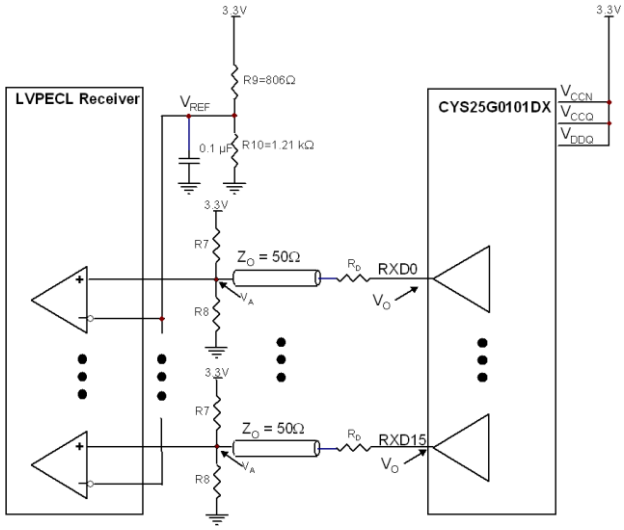


Figure 5. The LVPECL Input and Output Signal Level

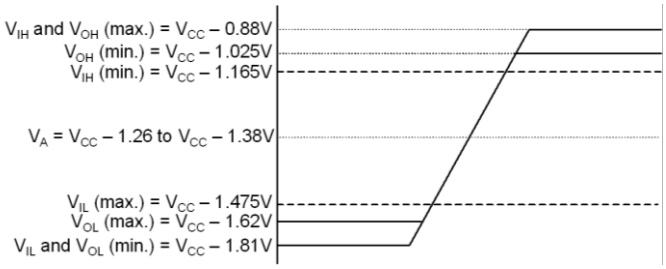


Table 2. The JEDEC LVPECL Output and Input Specification

Parameter	Description	Min	Max	Units
VOH	Output High	VCC –1.025	VCC –0.88	V
VOL	Output Low	VCC –1.81	VCC –1.62	V
VIH	Input High	VCC –1.165	VCC –0.88	V
VIL	Input Low	VCC –1.81	VCC –1.475	V

Calculation of the Termination Resistances (R7, R8)

All calculations in the following sections are used assuming V_{CC} = 3.3 V. In Figure 5, the V_A can be calculated by taking the middle value of V_{OH} and V_{OL}. R7 and R8 can be calculated by using equations similar to Equation 1 and Equation 2.

$V_A = V_{CC}*R8/(R7+R8)$ Equation 3

$Z_O = R7*R8/(R7+R8)$ Equation 4

Substituting V_{CC} = 3.3 V, V_A = 1.98 V, and Z_O = 50 ohms into Equations V and Z yields R7 = 83.3 W and R8 = 125 W.

Calculation of the Damping Resistance (R_D)

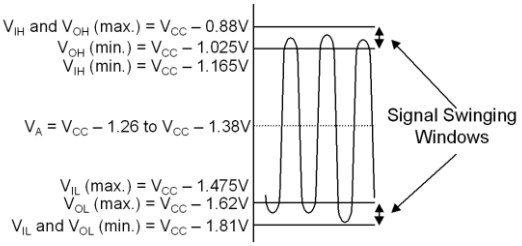
The damping resistor (R_D) is used to reduce the output signal of the CYS25G0101DX to meet the LVPECL specification. Based on Figure 5 and Table 2, it can draw a “Signal Swinging Window” as shown in Figure 6. The V_{OH} window is between V_{CC} – 1.025 V and V_{CC} – 0.88 V, and the V_{OL} is between V_{CC} – 1.81 V and V_{CC} – 1.62 V. The reduced output signal from the CYS25G0101DX must be within these windows.

In Figure 4 and Figure 7, V_O is the output voltage of the CYS25G0101DX and V_A is the middle voltage of V_{OH} and V_{OL}. When calculating the value of the resistance R_D, two cases must be considered. The first case occurs when $V_O = V_{OH}$ (V_{OH} max. and V_{OH} min.). The second case occurs when $V_O = V_{OL}$ (V_{OL} max. and V_{OL} min.)

Case 1: $V_O = V_{OH}$

$I_{VOH} + I_{R7} = I_{R8}$ Equation 5

Figure 6. Signal Swinging Window



$(V_O – V_A)/R_D + (V_{DDQ} – V_A)/R7 = V_A/R8$

Case 2: $V_O = V_{OL}$

$I_{R7} = I_{R8} + I_{VOL}$ Equation 6

$(V_{DDQ} – V_A)/R7 = V_A/R8 + (V_A – V_O)/RD$

Where V_{DDQ} is voltage at V_{DDQ} pin which is the power supply of the parallel receive data output. For an LVPECL interface, it needs to apply to 3.3 V

Using R7 = 83.3 W and R8 = 125 W (calculated from Equations 3 and 4), the results of RD in case 1 and case 2 are shown in Table 4.

Figure 7. The Current Flow Diagram

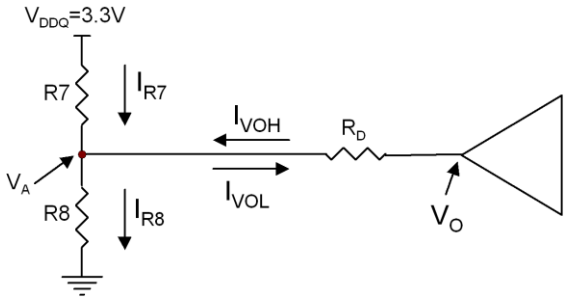


Table 3. The DC Specification of the Parallel Receive Data Outputs of CYS25G0101DX

Parameter	Description	Min	Max	Unit
V_{oHH}	Output HIGH Voltage	V_{DDQ} +0.4		V
V_{oLH}	Output LOW Voltage		0.4	V

Table 4. The Results of R_D in Case 1 and Case 2

Symbols	Case 1		Case 2	
VDDQ	3.3 V	3.3 V	3.3 V	3.3 V
VO	3.3 V (VOHH)	3.3 V (VOHH)	0.4 V (VOLH)	0.4 V (VOLH)
VA	2.275 V(Min)	2.42 V(Max)	1.49 V(Min)	1.68 V(Min)
R7	83.3 ohm	83.3 ohm	83.3 ohm	83.3 ohm
R8	125 ohm	125 ohm	125 ohm	125 ohm
RD	173.73 ohm	100 ohm	111.2 ohm	213.3 ohm

Four different values of R_D are obtained from Equations 5 and 6 and are listed in Table 4. From which, the value of R_D is picked between 111.2 Ω and 173.73 Ω. The mean can be calculated as follows:

R_D (mean) = (111.2 Ω + 173.73 Ω)/2 = 142.5 Ω.

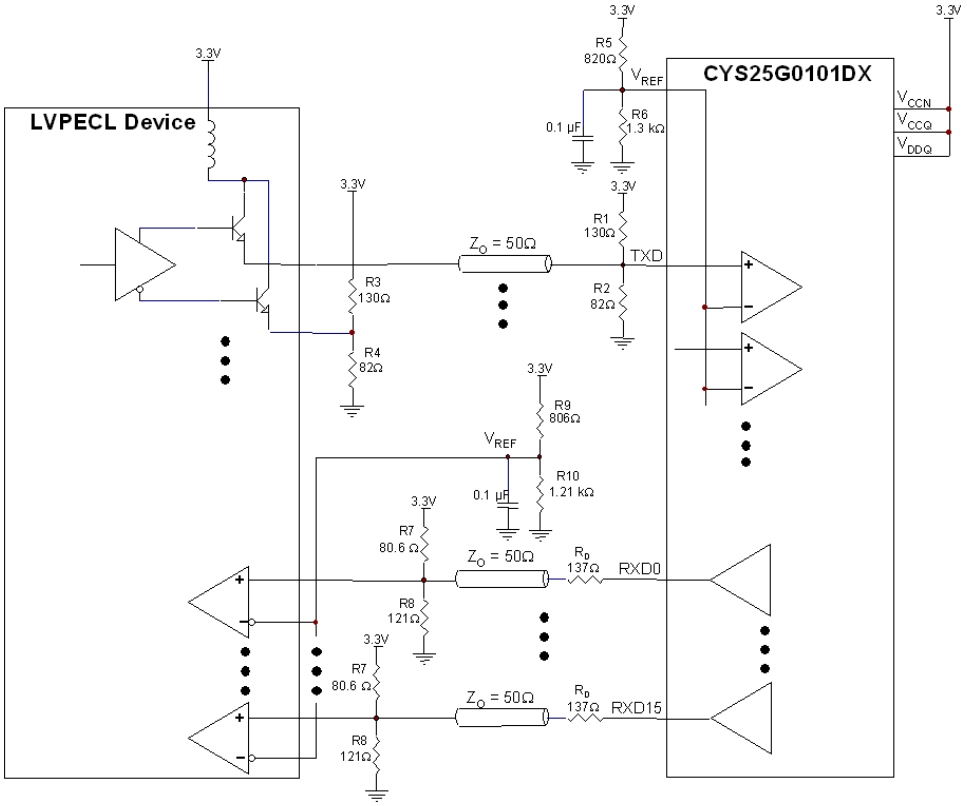
Resistors R9 and R10 form a voltage divider to generate 1.97 V (the mid-point voltage of the output of the CYS25G0101DX). The values recommended in Figure 4 and are easily obtained in the market.

CYS25G0101DX is a single ended output and it just needs one termination (composed of R7 and R8 in Figure 4 for each “receive data bit”. The differential LVPECL output to differential LVPECL input devices needs two terminations for each “receive data bit”. When both single-ended CYS25G0101DX and differential LVPECL output devices are using a Thévenin termination, the elimination of “receive data bit” termination in CYS25G0101DX will help to save about 50% of the power consumption of the termination.

Table 5. Recommended Resistance Values in the Figure 8 Example (VCC = 3.3 V, Units = ohms)

	R1	R1	R3	R4	R5	R6	R7	R8	R9	R10	R_D
Recommended	130	82	130	82	820	1.3 K	80.6	121	806	1.21 K	137
By calculation	127	82.5	127	82.5	820	1.3 k	83.3	125	806	1.21 k	142.5

Figure 8. Connection of the Parallel Transmit and Receive Output of the CYS25G0101DX to an LVPECL Device



Summary

The V_{REF} pin of the CYS25G0101DX is the voltage reference for the parallel transmit data input. It needs to be set at the mid-point of the input signal. From Table 2, the mid-point voltage range is between 1.88 V and 2.05 V, and the reference voltage in Figure 2 is 2.02 V. The V_{DDQ} is the power supply of the parallel receive data outputs. It must be connected to 3.3 V to interface with an LVPECL device. Illustrates the connections of the parallel transmit data inputs and the parallel receive data outputs to the LVPECL device. The resistances in Figure 8 may differ from the calculated values because they are easily obtained in the market. Summarizes all the recommended and calculated resistances.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1494324	CGX	09/20/2007	New spec.
*A	3390280	SAAC	09/30/2011	Updated to latest template Converted from FrameMaker to Word Added Abstract
*B	4546242	YLIU	10/22/2014	Sunset review Updated template
*C	5881042	AESATMP9	09/12/2017	Updated logo and copyright.

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