AN1111

Design and Layout Guidelines for Cypress Clock Generators

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Associated Part Family: CY254xx, CY2238x, CY2239x, CY22x50, CY27410
Software Version: NA
Related Application Notes: NA

AN1111 covers the basic schematic design and printed circuit board (PCB) layout guidelines for Cypress clock generators. General practices for power supply filtering, output terminations, and critical component placements are described in detail. Recommendations for routing clock signals are discussed in brief. Typical examples of schematic and layout are given for reference.

Contents

1 Introduction

With the increase of the speed of clock devices, signal integrity problem is also increasing. Today the demand is for reduction in design time with no errors in the first attempt. Hence, early detection and corrective measures need to be followed in the complete design cycle of a system. This application note illustrates general practices for PCB design around Cypress clock generators. These practices shall include both schematic and layout design.

In the schematic design of a clock generator, certain guidelines need to be followed for optimum device performance. These include both supply filtering and signal integrity measures. A few critical requirements of the schematic design are: power supply filtering, selection of crystal oscillator capacitors, clock output termination and routing, I^2C bus terminations, and application specific configuration.

CY254xx, CY2238x, CY2239x, CY22x50, CY27410 devices are the examples of some high performance Cypress clock generators. The brief features of these clock devices are listed in Table 1. The layout of a clock generator impacts the performance of the clock receivers and the nearby components on the circuit board. Many times a system designer has to manually implement placement and routing for devices such as clock generators, power supply and crystal oscillator capacitors, and termination resistors. This application note contains general guidelines to be followed for such PCB designs. For application specific settings, refer to the clock generator datasheet to configure it for desired functionality.

Table 1. Functional Descriptions of Some High-Performance Cypress Clock Generators

Feature	CY2544	CY22381	CY22393	CY22150	CY27410
Number of outputs	9	3	5	6	4 single ended, 8 differential
Package	24-pin QFN	8-pin SOIC	16-pin TSSOP	16-pin TSSOP	48-pin QFN
Frequency range	3 to 166 MHz	200 MHz (commercial), 166 MHz (Industrial)	200 MHz (commercial), 166 MHz (Industrial)	80 kHz to 200 MHz	25 MHz to 700 MHz differential 3 MHz to 250 MHz LVCMOS
Jitter	150 ps (Cycle-to-cycle Jitter - peak)	200 ps (Peak-to-Peak jitter)	400 ps (Peak-to-peak period jitter)	250 ps (Peak-to-peak period jitter)	50 ps (Cycle-to-cycle jitter)
SSC compatible	Yes	No	No	No	Yes
Output duty cycle	40% to 60%	45% to 55% (≤ 100 MHz) 40% to 60% (> 100 MHz)	45% to 55% (≤ 100 MHz) 40% to 60% (> 100 MHz)	45% to 55% (≤ 166 MHz) 40% to 60% (> 166 MHz)	45% to 55% (≤ 200 MHz) 40% to 60% (> 200 MHz)
PLL lock time	3 ms	3 ms	3 ms	3 ms	4 ms
Slew rate / Rise-time, Fall-time	6.8 V/ns (Measured from 20% to 80%) CLOAD = 15 pF, Drive strength [00]	0.75 V/ns (Measured from 20% to 80%)	0.75 V/ns (Measured from 20% to 80%)	1.2 V/ns (Measured from 20% to 80%)	Rise/fall time : 450 ps (Measured 20%–80% of AC levels, at 622.08 MHz - PECL, CML, LVDS standards)
Operating temperature range	-40 to 85	-40 to 85 (Industrial) and 0 to 70 (commercial)	-40 to 85 (Industrial) and 0 to 70 (commercial)	-40 to 85	-40 to 85
Multi-function pin	Pin 4 : $\overline{PD}$ / OE Pin 8 : CLK3 / FS0 Pin 9 : OE / FS1 Pin 10 : CLK4 / FS2 Pin 15 : CLK7 / SSON Pin 24 : XIN / EXCLKIN	Pin 8: FS / $\overline{SUSPEND}$ / OE / $\overline{SHUTDOWN}$	Pin 12 : SDAT / S0 Pin 13 : SCLK / S1 Pin 15: S2 / $\overline{SUSPEND}$ Pin 16: $\overline{SHUTDOWN}$ / OE	No multifunction pin.	No multifunction pin.

2 Schematic Design

This section describes the critical considerations for the schematic design.

2.1 Power Supply Filtering

The high-performance clock generators described here are susceptible to noise when they run at very high frequency. The source of the noise can be communication signals, high speed data transfer, power supply switching, or output switching of near-by ICs. The jitter and skew parameters of high-performance clock generators are largely impacted by power supply noise. The following sections explain in detail the use of decoupling and bypass capacitors, and ferrite bead filters for power supply noise reduction.

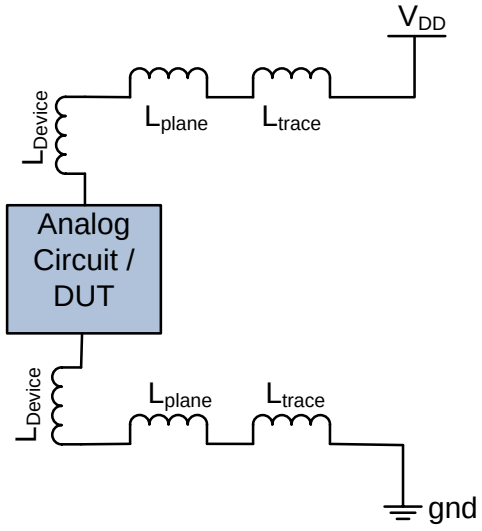
2.1.1 Why By-pass and Decoupling Capacitors?

Bypass Capacitors

Due to an increase in signal rise time, ground bounce effects begin. This happens because of the presence of lead, trace and plane inductances as sown in Figure 1. Ground bounce is the logical low as seen by a load device connected to a circuit. This is the logical low of the circuit plus the voltage spike across the lead frame inductances. As the voltage across the inductor is directly proportional to the rate of change of current, faster rise and fall time of the device results in higher voltage drop across the inductor. This leads to a current spike in the inductor that change the logical low of the device. Hence, it bounces above ground. This is called ground bounce.

On the other side, a similar negative drop in inductor near the power supply leads to lowering of the logical high value. Therefore, a load device sees a signal that bounces from ground or power supply value rather than the specified logical low or logical high. Such a situation can be handled by using bypass capacitors, which provide a regulated power supply and ground right at the package for a short time until the plane inductances are overcome. A bypass capacitor shunts a high impedance path to reduce high frequency current flow in it.

Figure 1. Different Inductances Associated with Device in PCB



This bypass capacitor also has its own noise due to its own trace and lead inductances. A longer PCB trace has higher inductance, which inhibits fast changes in current and exhibits large voltage drop. Hence, it is always suggested to place the bypass capacitors as close as possible to the device with wider traces. The package parasitic include the lead and bond wire parasitic of the package as shown in "Clock Output Terminations".

Decoupling Capacitors

Decoupling means to separate the IC's power supply from the main power supply. If it is necessary to isolate one circuit from the noise of another, one should reduce the amount of shared supply trace between them. Therefore decoupling should be used. Decoupling decreases noise transmission in two ways:

- Since decoupling always consists of a high impedance element in series with the supply line, it assists bypassing; ensuring that the noise current will flow through the low impedance bypass element rather than the supply.
- It acts as a low pass filter so that the high-frequency content of any current that does pass through the series element will be attenuated, making it more likely that the regulator will be able to react and keep the supply voltage stable.

Figure 2 shows the power supply filtering on the Cypress device CY2544. Figure 3 and Figure 4 show the effect of bypass and decoupling capacitors on the output signal.

Figure 2. Supply Filtering for CY2544

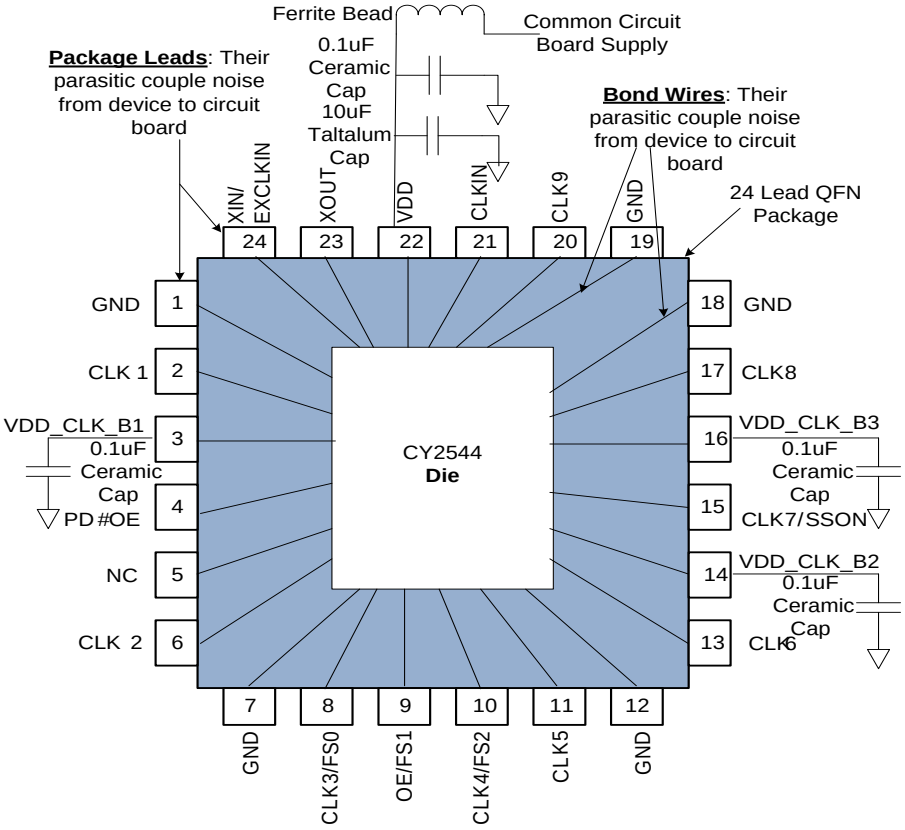


Figure 3. Output with High Impedance Bypass Capacitors

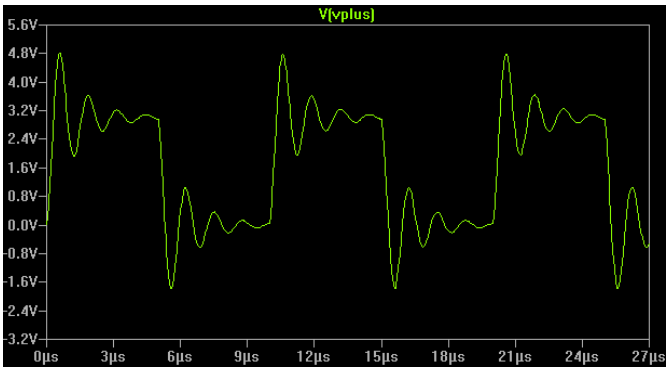
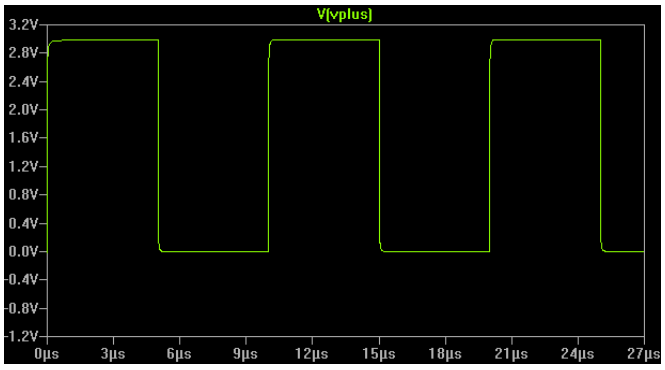


Figure 4. Output with Low Impedance Bypass Capacitors



Choice of Capacitors

To filter a wide range of frequency noise in the supply voltage, use a parallel combination of low frequency and high frequency capacitors. This provides low impedance path over the entire frequency range of operation.

- Choose larger capacitors (1 µF to 47 µF) to provide lower impedance path at low frequencies (<1 MHz)
- Choose a smaller value capacitor (0.1 µF to 1 µF) for middle frequency range of operation.
- Choose even smaller value capacitors (0.01 µF to 0.1 µF) to handle higher frequency (>200 MHz).

These capacitors are available in tantalum and electrolytic type. The equivalent series resistance (ESR) of a capacitor causes ripple in the supply voltage. Therefore, ESR should be as low as possible. A tantalum capacitor is preferable to an electrolytic capacitor due to its lower ESR. It is a good practice to design in the following way:

- One 0.1 µF or 0.01 µF ceramic capacitor on core supply pin (close to the IC pin),
- One 10 µF tantalum capacitor next to the 0.1 µF or 0.01 µF,
- One ceramic decoupling capacitor of 0.1 µF or 0.01 µF very close to the output bank supply pin.

A tantalum capacitor of 10 µF has ~16 mΩ impedance at 1 MHz and a 0.1 µF ceramic capacitor has ~8 mΩ impedance at 200 MHz. The low impedance required over a desired frequency range depends on a percentage of power supply ripple acceptable for a given change in the load current. The equation for the impedance calculation is:

$$Z_{LOW} = \frac{\Delta V}{\Delta I} = \frac{V_{DD} \times Ripple}{\Delta I}$$

Where:

- V_{DD} = Device supply voltage
- Ripple = Tolerable ripple in percentage
- ΔI = Change in supply load current

For an application, where the device supply voltage is 3.3 V and the acceptable ripple is 0.1% for a 100 mA change in the supply load current, the required low impedance is 33 mΩ over the desired frequency range.

2.1.2 Ferrite Beads

Ferrite beads eliminate noise energy over a frequency range by creating impedance for the same frequency bandwidth. Ferrite material is highly resistive, which helps in lossless transmission of signal at high frequencies. Ferrite beads can isolate the clock generator supply from the printed circuit board (PCB) power plane; multilayer PCBs have dedicated layer for power and ground plane. Due to inductive isolation, the noise from the PCB power plane cannot interfere with the device power and vice versa. The selection of a ferrite bead is based on the following two parameters:

- DC impedance (0 to 5 Ω)
- DC current (15% margin + max supply current)

DC impedance and DC current are necessary parameters to meet, but are not sufficient. If a ferrite bead has resonance at lower frequency, the supply noise may increase rather than attenuate. The following common characteristics in beads which generally do not attenuate noise are: low DC resistance (<0.1 Ω), resonance near low frequency (10–100 kHz). Typical effect of ferrite beads on an output signal are seen in Figure 5 and Figure 6.

Figure 5. Noisy Signal

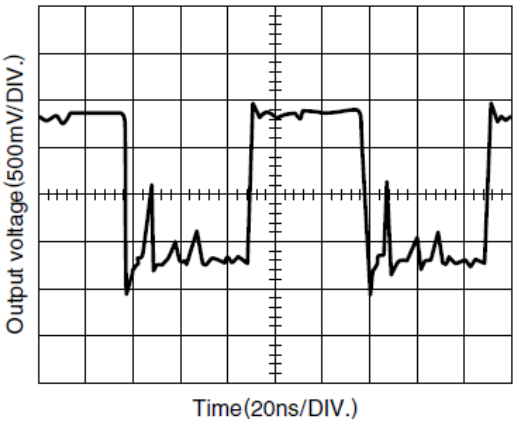


Figure 6. Signal upon Usage of Ferrite Bead

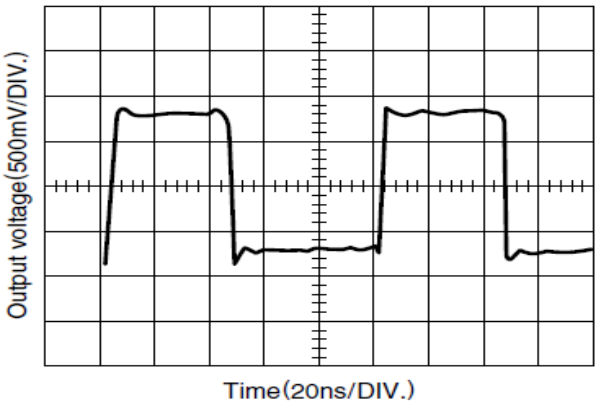
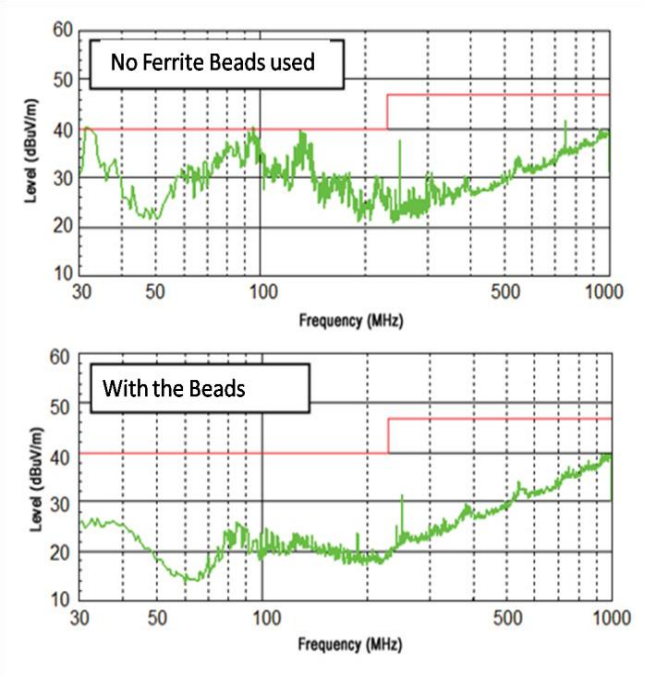


Figure 7 shows the ferrite bead effect on signals with the bandwidth of 30 to 350 MHz. the majority of the noise peaks are removed. Some peaks (>350MHz) are still visible as the material used in the ferrite bead is meant for attenuating noise at lower frequencies.

Figure 7. Effect of Ferrite Beads



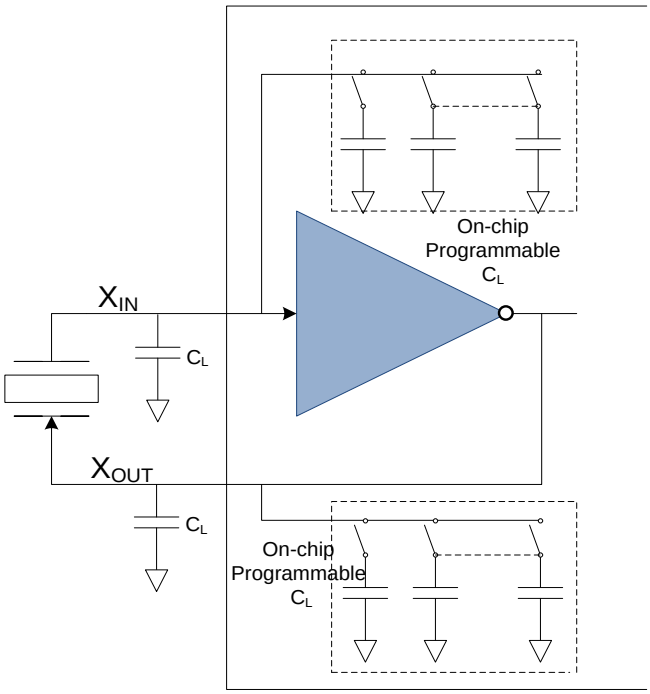
While designing power supply filter circuitry, place the bypass capacitor at the clock generator side of the ferrite bead. Ensure proper choice of ferrite beads and filtering capacitors, and proper layout design to meet system level requirements.

2.2 Ancillary Components for Crystal Oscillators

Cypress clock generators accept an external clock or crystal as a reference input.

As shown in Figure 8, the on-chip buffer amplifier with an external crystal and capacitors makes a pierce oscillator configuration. For desired oscillator functionality, a crystal must meet the specifications of the load capacitor, drive level, and motional resistance as recommended in the clock generator datasheet. A few clock generator families have an on-chip programmable load capacitor array and do not require external load capacitors. A detailed recommendation on crystal parameters is provided in the white paper, Crystal Parameters Recommendation for Cypress Frequency Synthesizers.

Figure 8. Pierce Oscillator in Cypress Clock Generators

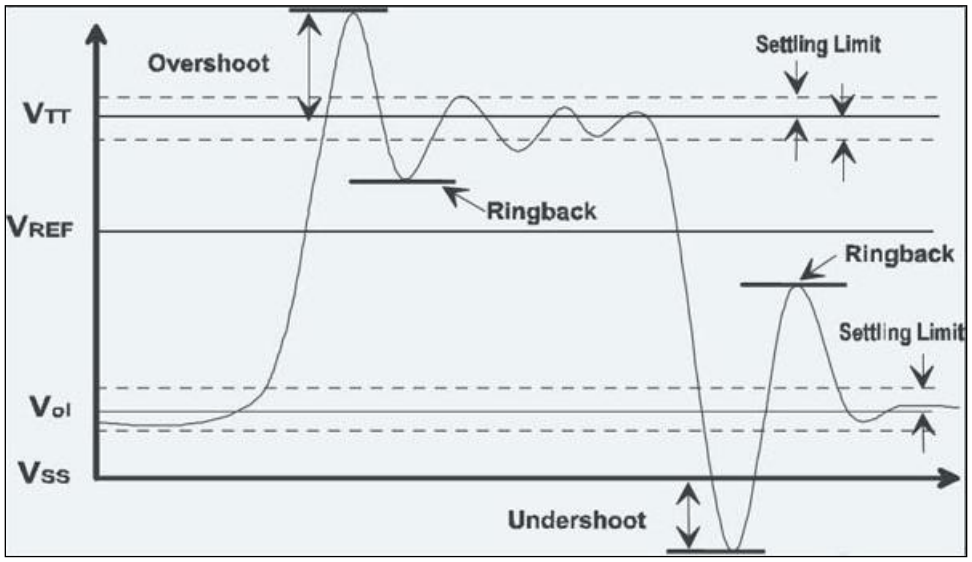


For devices CY254xx, CY2238x, CY2239x, CY22x50 have same X_{IN} pin for crystal input reference, or external clock source. To use an external clock as a reference input, keep the X_{OUT} pin unconnected, and connect the external clock to the X_{IN} pin. CY27410 device has two dedicated pins (X_{IN} and X_{OUT}) for crystal input reference, and four dedicated pins for differential input clocks.

2.3 Clock Output Terminations

According to transmission line theory, a clock signal that has a faster edge compared to twice the propagation delay of the trace (that carries the clock signal) must be terminated to avoid reflection. The maximum power transfer theorem implies that the driver impedance and the receiver impedance must match to transfer maximum signal power. When the impedance does not match, the signal power reflects from the receiver, and it appears as overshoots or undershoots at the signal discontinuities. The overshoot, or undershoot, may change the signal level significantly as shown in Figure 9. As a result, the receiver may detect it as wrong signal level. Termination techniques can match impedance and prevent overshoot and undershoot.

Figure 9. Overshoot and Undershoot Due to Reflection



A trace can terminate at the source end or at the receiver end. Each of these techniques has its own advantages and disadvantages.

2.3.1 Source Termination or Series Termination

A source of the clock signal terminates with a series resistor to match the source impedance with the trace impedance. Due to the impedance match at the source end, the reflected signal from the receiver is absorbed, and that prevents overshoots or undershoots.

The series termination resistor (R_t) can be calculated subtracting the source impedance (R_S) from the trace impedance (R_T). For a 50-Ω trace impedance and a 17-Ω source impedance, the series termination resistor should be 33 Ω. The source impedance derives from the I-V curve of the device's IBIS model. IBIS models of Cypress clock generators are available on www.cypress.com.

2.3.2 Advantages of Series Termination

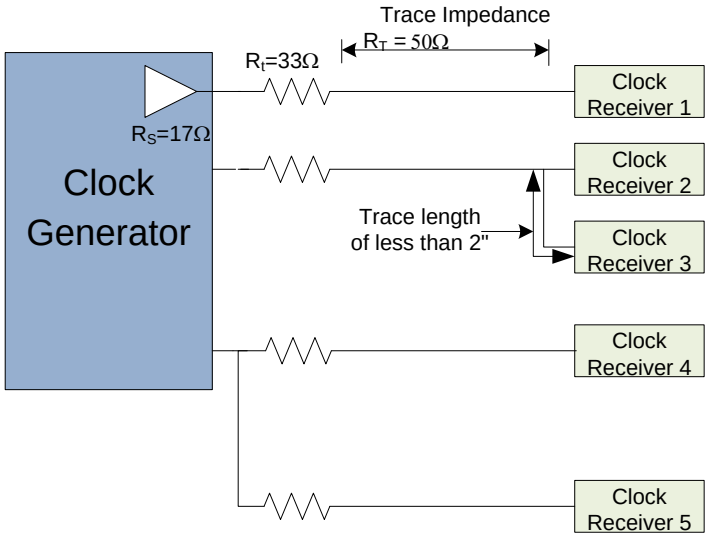
- No DC power dissipation
- Comparatively low power consumption against other termination techniques

2.3.3 Disadvantages of Series Termination

- Perfect impedance match is not possible due to variable source impedance across I-V curve
- Applicable only when a clock receiver is at the end of the trace. If a clock receiver connects along the trace, it causes a reflection.

In an application of multiple clock receivers of the same clock output, if the trace length between the receivers is less than two inches, a single termination resistor can be shared between the receivers, as shown in Figure 10. However, Cypress recommends an individual series resistor for receivers if the routing length is more than 2 inch. This has also shown in the Figure 10.

Figure 10. Source Termination



2.3.4 Trace End Terminations

In these termination techniques, a clock output terminates at the end of the trace and, hence, the signal does not reflect from the receiver. Unlike the source termination, a clock receiver can be connected along the trace without affecting the other receivers, but it should terminate to avoid reflection in the receiving clock.

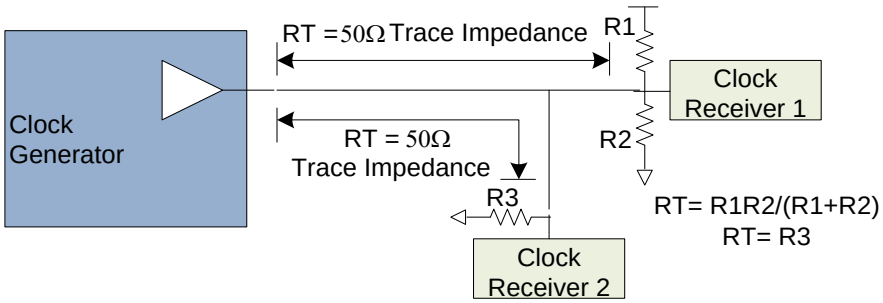
A well-known technique of the end terminations is the pull-up/pull-down termination.

2.3.5 Pull-up/Pull-down Termination

As shown in Figure 11, the pull-up and pull-down resistors (R1, R2) connect at the receiver end. The Thevenin equivalent (RT) of these resistors should be equal to the trace impedance.

RT = (R1*R2)/(R1+R2)

Figure 11. Trace End Termination



The resistance of R1 and R2 should be moderately high so that the limit of output low current (I_{OL}) and output high current (I_{OH}) specifications of the clock generator do not exceed. If I_{OL} and I_{OH} limits are the same, then select resistor R1 equal to R2 or adjust R1/R2 based on the I_{OL}/I_{OH} limit.

As DC current continuously flows through R1 and R2, the power consumption is high with the pull-up and pull-down termination technique. However, you can reduce consumption by half by using only the pull-up resistor (R1) or only the pull-down resistor (R2) to match the trace impedance.

2.4 Other General Design Guidelines

2.4.1 Unused Clock Outputs

If the application can tolerate a little variation in output to output skew (<30 ps), you can leave the unused clock outputs of a clock generator un-terminated. Un-terminated clock output pins act as antenna and radiate noise at the clock signal transition. However, the radiated noise does not contribute much in EMI for smaller packages like QFN

A clock generator with multiple clock output banks can have additional skew due to the un-terminated outputs. The un-terminated clock outputs draw much less current compared to other running clocks. This creates a difference in the current consumption of the output banks. An output bank with lower power consumption can drive a clock faster compared to a bank with relatively high power consumption. This results in an additional skew between the clock signals from the banks with different power consumption, the additional skew is less than 30 ps.

The best practice is to keep capacitors footprints on un-used outputs during design. If skew or EMI is of concern, mount 5 to 10 pF capacitors while testing.

2.4.2 Multifunction Pins

To access multiple programmable features using less pins, Cypress clock generators include multifunction pins. You can configure the multifunction pins to function as one of the multiple operations: Output Enable, Power Down, Frequency Select, and Spread ON/OFF. Please see the examples of multifunction pin feature as listed in Table 1.

To hardwire a multifunction pin, use an external pull-up or pull-down resistor. Its value should meet the V_{IH}/V_{IL} specifications of the pin. Typically, the pull-up or pull-down resistor is a 1 kΩ.

2.4.3 Pull-up resistors for I2C Bus

Cypress clock generators require external pull-up resistors on the serial clock, SCLK, and serial data, SDAT, lines of the I^2C interface. The pull-up resistor value is typically from 2 to 5 kΩ.

2.4.4 EMI Reduction using Capacitors

For EMI sensitive applications, a steep clock edge is one of the radiation sources. Use a 4.7 to 22 pF capacitor on the clock output to round out the rising and falling edge of the clock signal. This helps to reduce the radiation. Place EMI capacitors after a series termination resistor on clock outputs.

3 Layout Guidelines

Layout involves two main tasks: Placement and Routing. Placement of the critical components related to power supply filtering, crystal oscillator, and clock output termination is vital for optimum performance of clock generators. PCB routing techniques include: optimum power trace length and width, via utilization, clock trace routing disciplines, and ground and power plane usage.

3.1 Placement

Placement is the process to identify mechanical location for components on a circuit board.

3.1.1 Clock Generator Device

A clock generator should be at the center of the surrounding clock receivers, so that the clock traces do not intersect each other. Mount a clock generator directly on a circuit board without using a socket, which may add parasitic that result in noise.

3.1.2 External Components

Keep bypass or decoupling capacitors close to power pins. Keep output termination resistors close to respective clock output pins. Crystal and load capacitors should be as close as possible to the device's X_{IN} and X_{OUT} pins; crystal load capacitors must be equidistant from the X_{IN} and X_{OUT} pins to avoid extra parasitic effect. Place EMI capacitors after a series resistor on the clock outputs. Figure 12 and Figure 13 show a typical example of a schematic and the placement of a clock generator.

Figure 12. Example of Clock Generator Schematic

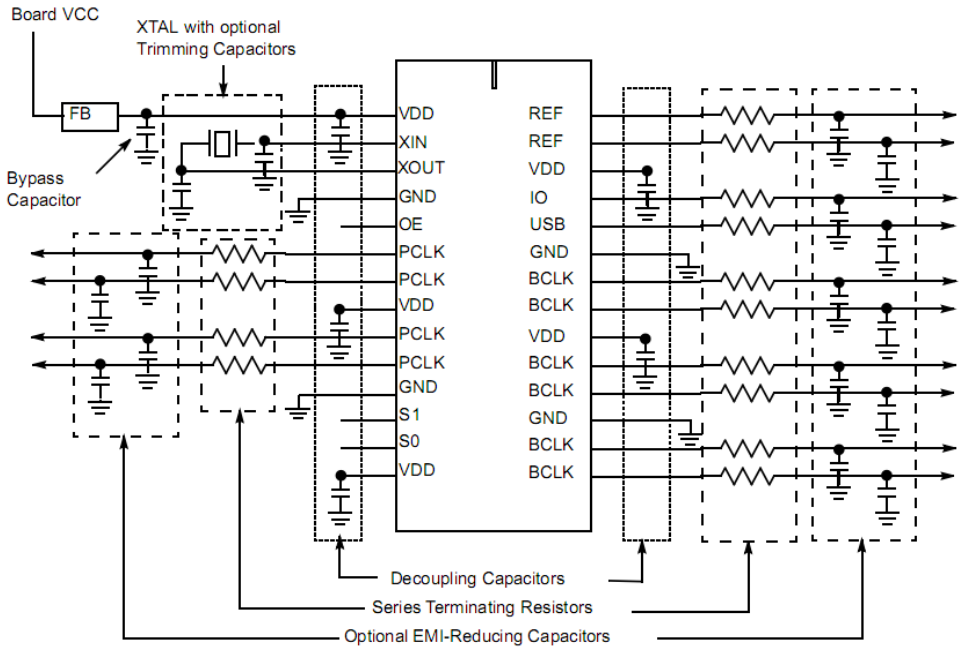
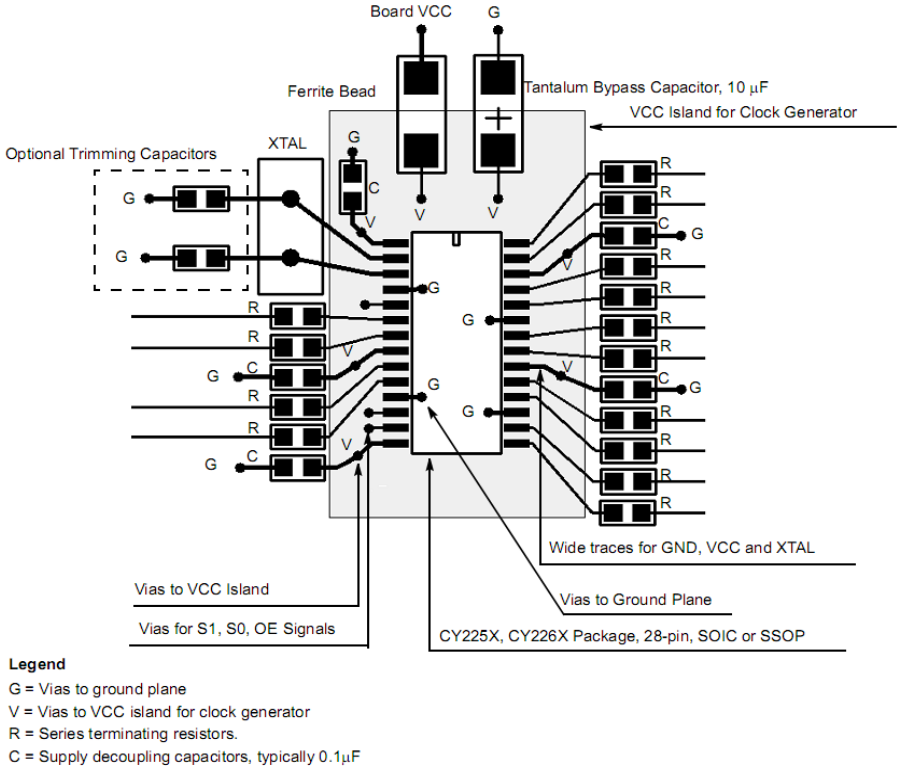


Figure 13. Example of Clock Generator Layout



For schematic and layout examples of CY22150 and CY22393, refer to Appendix A: Examples for CY22150 and CY22393.

3.2 Routing

Routing is the process to electrically connecting components on a circuit board.

3.2.1 Power and Ground Layer

Generally, the entire layer of a PCB is attributed to power, or ground layer. Thick power or ground layer has a lower DC resistance and a lower AC inductance that result in a lesser voltage drop across layer, and a lower impedance path for the signals returning through ground. Power and ground layers reduce ground loops across a circuit board, and thus, they help to reduce the EMI.

3.2.2 Localized Power or Ground Areas

Circuit boards with high speed digital and analog devices should have separate analog and digital power as well as ground areas to avoid interference. In such cases, a localized power or ground copper area is used on a component layer covering high speed devices. A localized power area should use a ferrite bead to connect to the circuit board power layer to impede noise mobility. A localized ground area should use multiple vias to connect to the ground layer for a lower impedance path.

If a clock generator package is large, use a localized area to reduce the impact of other noise sources on a circuit board as shown in Figure 13.

3.2.3 Routing Best Practices

- Use wide traces for power, and ground. Wide traces have less inductance.
- Place crystal at equidistant traces and away from clock traces or high speed traces.
- Via has high resistance and inductance compared to a copper trace. Use minimum number of vias on a clock trace. If used, keep the vias away from the power or ground layer that reduces the clock trace impedance change.
- Clock traces routed adjacent to the ground layer have low impedance return path.
- Do not route traces in a ground or power layer or below a clock generator device.
- Use equal length traces for clock signals, where a relative skew need to be minimal

4 Summary

The performance of clock generators is crucial for any electronic system. A few precautionary measures during the schematic design and layout phase can optimize clock generator performance. The key considerations for the schematic design are: power supply filtering, selection of crystal and load capacitors, termination of clock outputs, and application specific configuration. The best layout practices include the placement of clock generators, power supply filtering capacitors and crystal oscillator capacitors; and the routing disciplines for clock signals traces, power plane and ground plane.

A Appendix A: Examples for CY22150 and CY22393

A.1 CY22150 Schematic and Layout Example

Figure 14. Schematic

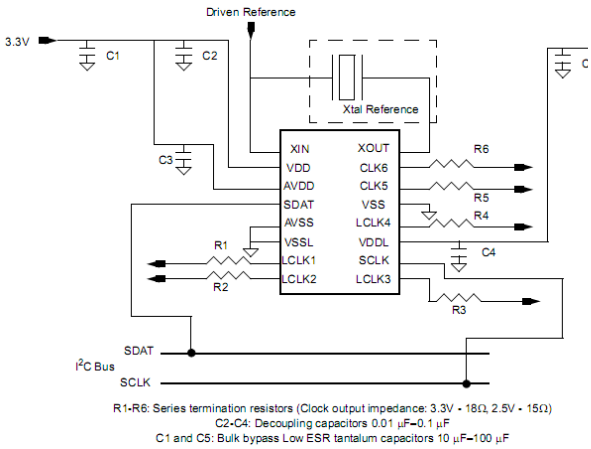


Figure 15. Layout – Top + Bottom Layer

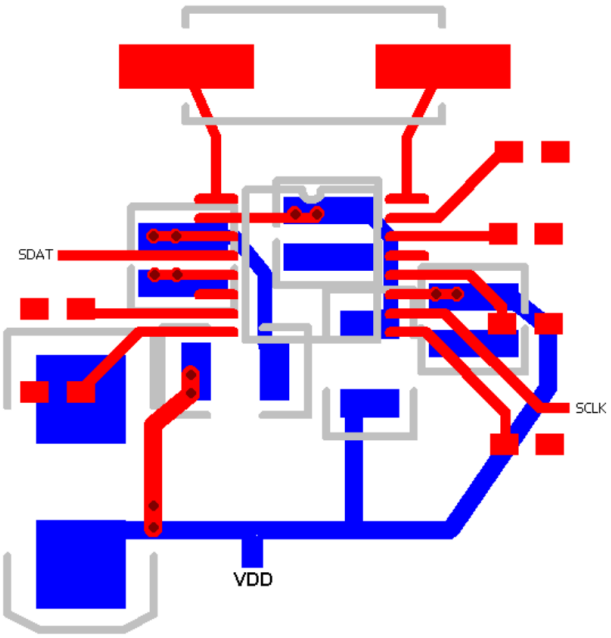


Figure 16. Layout – Top Layer

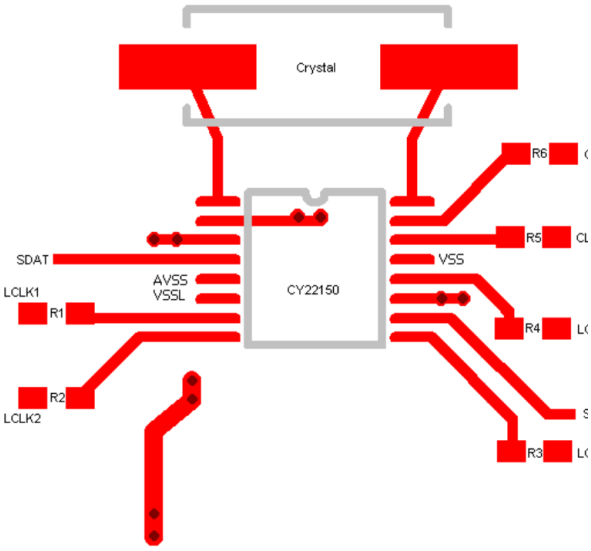
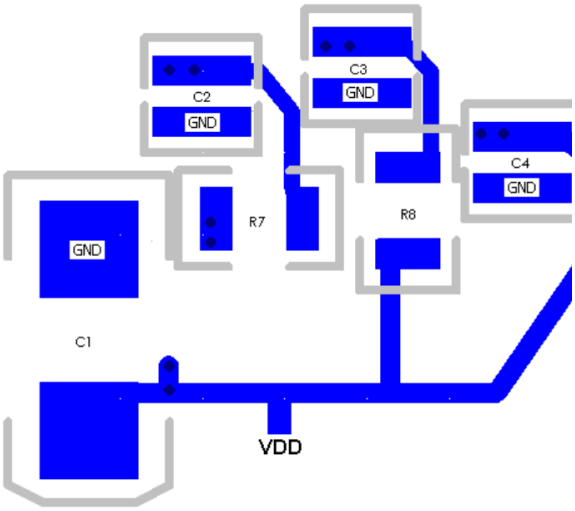


Figure 17. Layout – Bottom Layer



A.2 CY22393 Schematic and Layout Example

Figure 18. Schematic

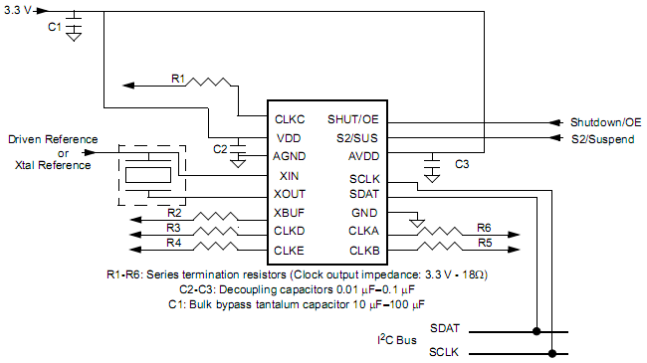


Figure 19. Layout – Top + Bottom Layer

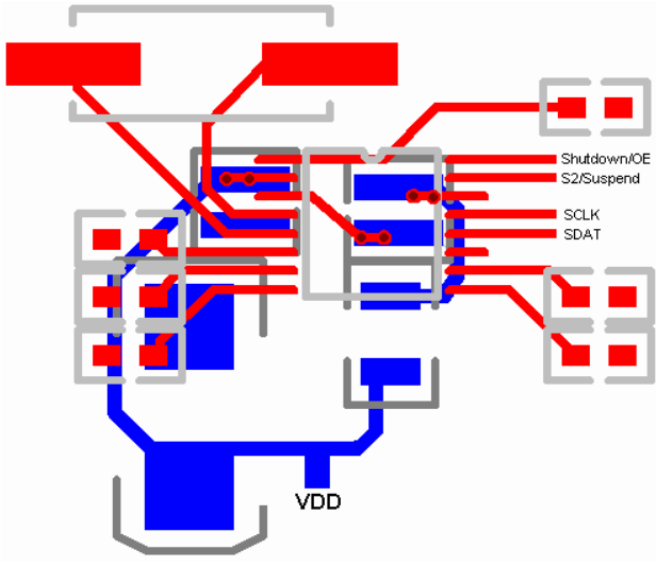


Figure 20. Layout – Top Layer

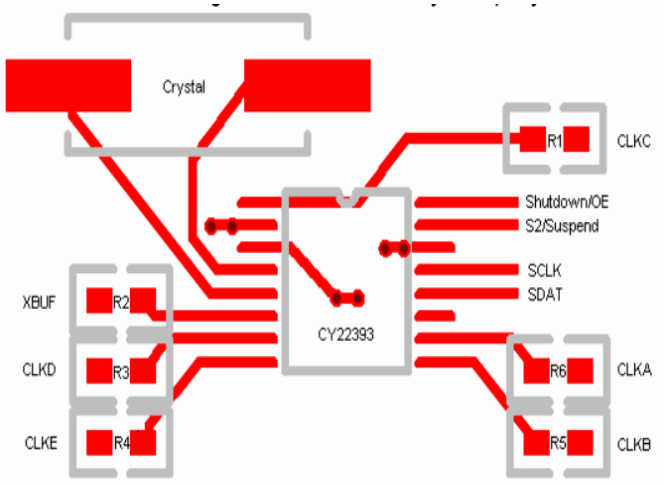
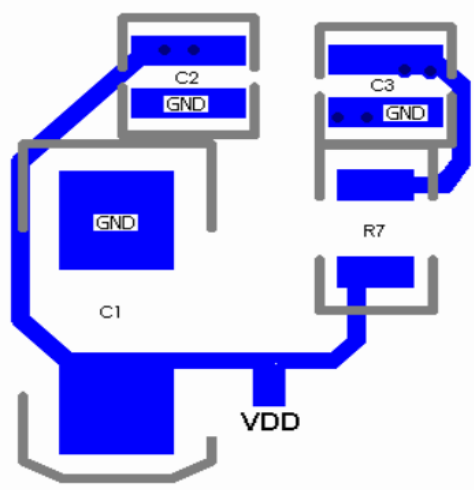


Figure 21. Layout – Bottom Layer



Document History

Document Title: AN1111 - Design and Layout Guidelines for Cypress Clock Generators

Document Number: 001-34339

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1505083	RGL	09/24/2007	Reformat document and assign document number.
*A	3058091	KVM	10/13/2010	Corrected Equation 1.
*B	3363884	PURU	09/06/2011	Updated Common Types of Transmission Lines section in Page 2 Updated hyper link in Crystal Circuitry section.
*C	3720240	BASH	08/22/2012	Changed document title. Updated template. Major rewrite.
*D	3899259	CINM	02/11/2013	Rewritten sections and subsections of the introduction, and power supply filtering. Added Figures 1, 3, 4 and 5.
*E	5035648	TAVA	01/20/2016	Updated template. Added CY27410 part number in “Associated Part Family”. Figure 1 has been updated. Table 2 is included. Minor update to the sections “Power Supply Filtering”, “Routing Best Practices” and “Unused Clock Outputs”. The section “Choice of Capacitors” has been updated.
*F	5877303	AESATMP8	09/08/2017	Updated logo and Copyright.

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