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AN1043

Understanding Synchronous Dual-Port RAMs

Associated Part Family: Dual-Port SRAMs

AN1043 discusses the basic features, operation, and expansion configurations of synchronous dual-port SRAMs. A brief note on applications of synchronous dual-port SRAMs is also included.

1 Introduction

This application note discusses the basic features of Cypress synchronous dual-port memories. A brief discussion on device operation is also included.

Synchronous dual-port devices are designed to service the need for faster devices and simpler interfaces in the next generation of high-speed applications. They offer significant advantage over asynchronous dual-port SRAMs (DPRAM).

Synchronous DPRAMs use external clocking to time read and write operations. The external clocking allows timing specifications that result in reduced DPRAM access and cycle times. Further, this enables higher system operating frequency and bandwidth. On the other hand, Asynchronous DPRAMs respond asynchronously to address and control pin changes. This operation places restrictions on input pin timings, and limits achievable system performance. This operation also restricts maximum internal operating speed of the DPRAM.

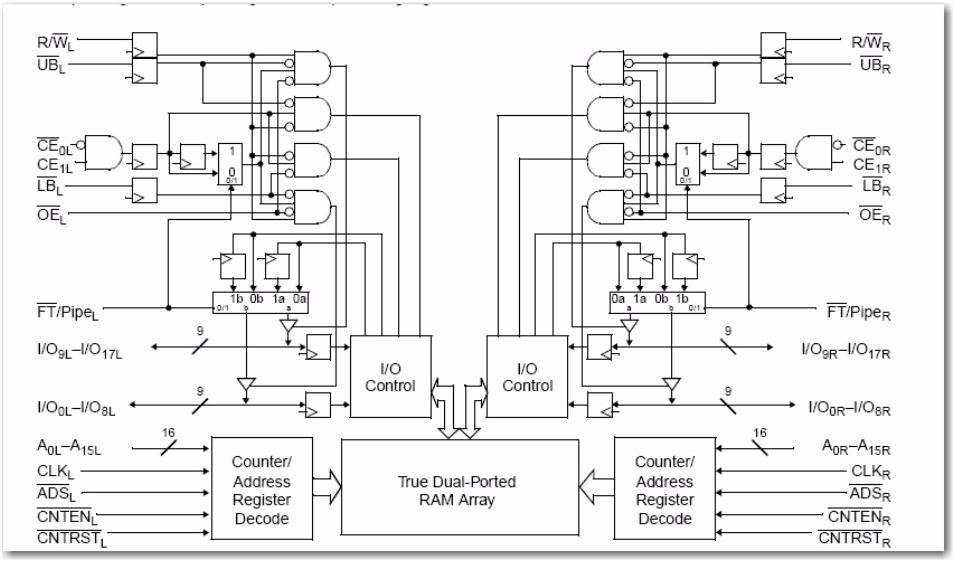
Cypress synchronous DPRAMs support three operating modes: Pipelined, Flow-Through, and Burst. Like asynchronous DPRAMS, synchronous devices also provide simultaneous access capability to any location in the memory. Either port can write or read data into/out-of any memory location.

2 Architecture

The basic architecture of sync DPRAMs is illustrated in Figure 1 overleaf. A typical 1M synchronous DPRAM (CY7C09389V) in a 64K x 18 configuration, has 18 data lines (I/O) and 16 address lines. Each port has a set of dedicated control, address, and data lines that can be used independent of each other. Operations on each port occur on the LOW to HIGH transitions of input clock signals (CLK_L for one port and CLK_R for the other). A set of external input signals ($\overline{FT}$/Pipe) selects operating mode for each port. Each port can be configured to function in an operating mode independent of the mode selected on the other port.

Dual chip enables are provided to simplify depth expansion by eliminating the need for external logic to generate multiple chip enable signals.

Figure 1. Logic Block Diagram of a Synchronous DPRAM



A burst-counter enables burst mode operation by providing address auto-increment within the device. This operation is controlled by a set of external inputs ($\overline{CNTEN}$,$\overline{CNTRST}$,$\overline{ADS}$). An interrupt generation feature is also available to signal end of count to the corresponding host controller. $\overline{ADS}$ input LOW during the clock LOW to HIGH transition. With the count enable ($\overline{CNTEN}$) asserted for a port, the address counter will increment on each LOW to HIGH transition of that port's clock signal. The counter is reset to zero on a LOW to HIGH clock transition with count reset ($\overline{CNTRST}$) asserted.

DPRAMs with bus matching capability simplify the interface between devices operating with different bus sizes. See the Tutorial on Synchronous Dual-Port SRAMs for more information.

2.1 Operating Mode

The $\overline{FT}$/Pipe pin determines the mode of operation for a port. LOW selects Flow-Through mode, and HIGH selects Pipelined mode.

In Pipelined mode, output data is stored in registers before being read out on data lines, while in Flow-Through mode, the output is read immediately from the memory array onto the data lines. The address is registered for both modes of operation.

Synchronous dual-ports also support burst mode operation. In burst mode, only the first address of a consecutive sequence of addresses is loaded on-to a burst counter. Both Flow-Through and Pipelined Cypress DPRAMs support burst.

2.2 Read Operation

A read operation requires the assertion and maintenance of several control and address signals around the clock edge that initiates a read operation. (Low → High)

The address of the memory location to be accessed must be applied to the address input pins (A). The following control signals must be setup for performing a read:

$\overline{CE_0}$ ← LOW

CE_1 ← HIGH

R/$\overline{W}$ ← HIGH

These signals must be present and valid for t_{SA}/t_{SC}/t_{SW} (setup time) before clock transitions and remain valid for t_{HA}/t_{HC}/t_{HW} (hold time) after clock transitions. At the rising edge of the clock (CLK) the address is registered and the read cycle begins. The output enable ($\overline{OE}$) is an asynchronous signal and data appears at the output lines if $\overline{OE}$ is LOW. Outputs are three-stated, and data will not appear at the outputs when $\overline{OE}$ is HIGH.

When the DPRAM is configured in Flow-Through mode, the read cycle begins after setting up the required signals and registering the address as described earlier. Data is valid t_{CD1} (clock to data valid for Flow-Through) after the rising edge of the clock as shown in Figure 2. t_{CD1} is less than one clock cycle, therefore data appears at the outputs before the next rising edge of CLK.

In Pipelined mode the output data is registered. Data from the read operation is clocked into the output register and transferred to the output lines after the second rising edge of the clock as shown in Figure 2. The output data is valid t_{CD2} (clock to data valid for pipelined) after the second clock transition. The use of registers at the output introduces a delay before the first data appears at the output lines. t_{CD1} (Flow-Through) is higher than t_{CD2} (Pipelined) and therefore the total amount of time it takes to read a complete packet of information is less in Pipelined mode. In summary, the Pipelined mode read operation involves one-cycle latency for the first access.

Only the first address of a consecutive sequence of addresses must be loaded by the sync burst DPRAMs, which accomplish subsequent accesses by using a clock to advance an address counter inside the chip. Pipelined-burst DPRAMs take the idea one step further by using a register at the output stage of the RAM to hold the next piece of data in the burst sequence, which results in an extremely fast clock-to-output time (t_{CD2}). The delay involved is the holding register's access time. Figure 3 shows burst read operation using the address counter. The external address is constantly loaded into the counter on the rising CLK edge when $\overline{ADS}$ is LOW. When $\overline{ADS}$ is HIGH and $\overline{CNTEN}$ is LOW, the internal address counter is incremented.

Figure 2. Read Operation of Flow-Through and Pipeline

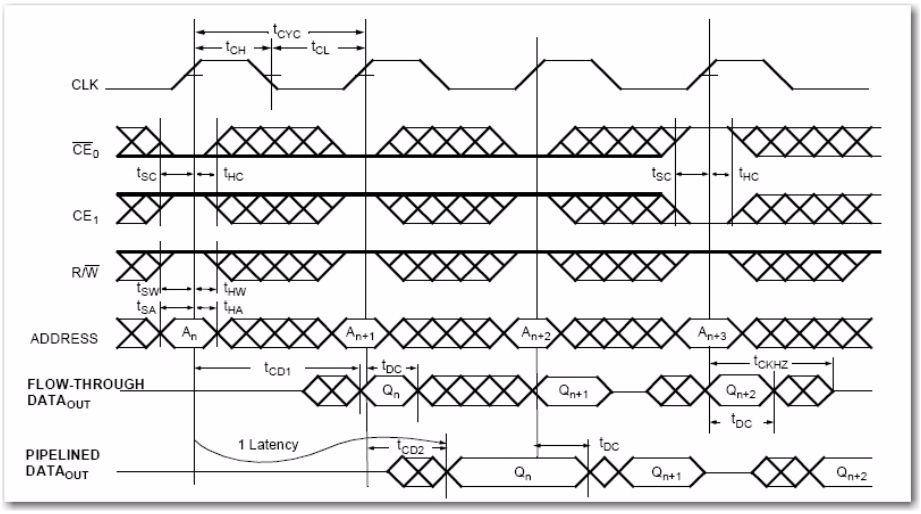
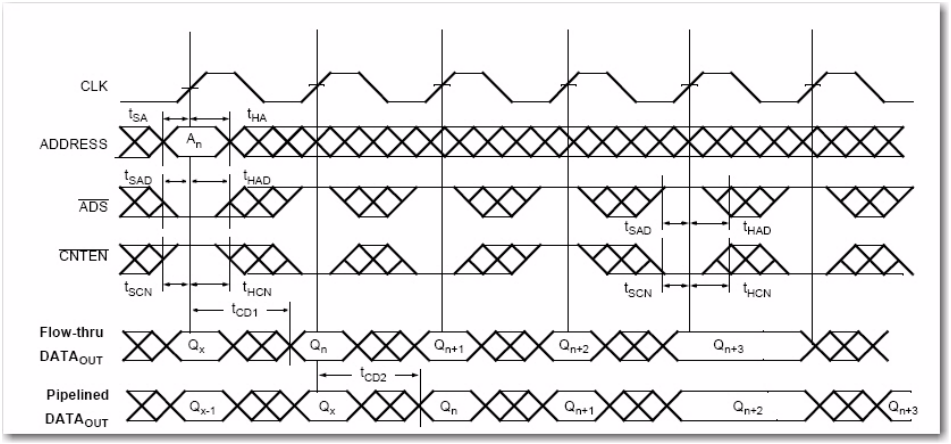


Figure 3. Flow-Through Burst vs. Pipelined Burst Read Operation



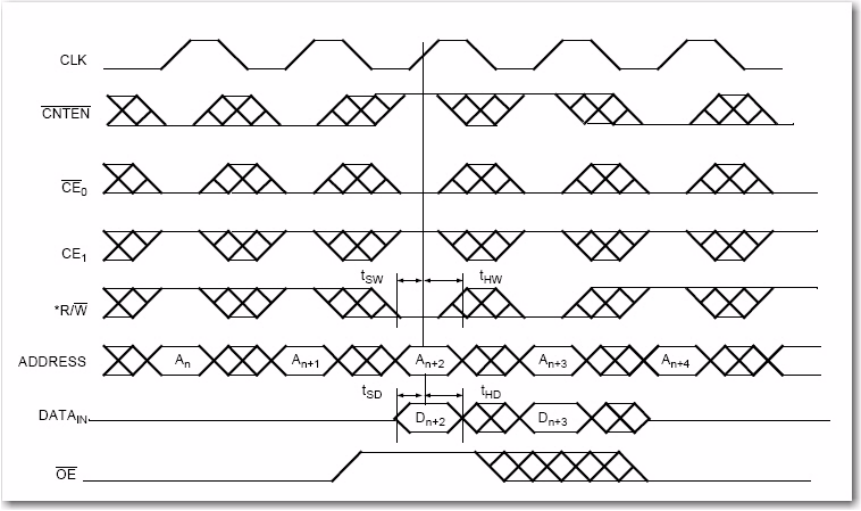
2.3 Write Operation

The write operation is identical for Flow-Through and Pipelined sync DPRAMs because the registers at the output lines in Pipelined mode affect only read operations. Write operation signal waveforms are shown in Figure 4. Write operation latency is zero. This is because after the addresses, chip enables, and write enable are set and all signals have been latched into the DPRAM, the write operation continues independent of other system operations.

When writing simultaneously to the same location by both ports, data integrity is not guaranteed. The memory location might contain new data, old data, or some transitional value. A clock-to-clock set-up time of t_{CCS} (refer to datasheet for t_{CCS} values) must be maintained between left port clock and right port clock to avoid data corruption. If the time between the two clocks is less than t_{CCS}, external logic is required to implement arbitration. The same scenario is true when writing to a location from one port and reading out that location from the other port. A t_{CWDD}.(Write port clock High to Read Data Delay) is required to assure that the read data is the newest and last piece of data written to that location.

The address counter (Burst Mode) can be used to perform a back-to-back Write or Read operation without any latency or idle cycle at the time when a new address is selected. The new address is loaded in the same way the first address is loaded. Figure 4 shows the process of loading the external addresses A_{n+2} and A_{n+3} while $\overline{ADS}$ is LOW and $\overline{CNTEN}$ is HIGH. For each external address, the internal address is incremented by deasserting $\overline{ADS}$ (HIGH) and asserting $\overline{CNTEN}$ (LOW). See datasheets of sync DPRAMs for switching waveforms of read and write operations with address counter advance.

Figure 4. Write Operation for Synchronous DPRAM (all modes)



* The same waveform for $\overline{ADS}$

There are two types of latencies associated with synchronous DPRAMs. The first is for a Pipelined read operation (one-cycle latency), as shown in Figure 2. The second type of latency happens when the R/$\overline{W}$ enable is used to do the I/O bus turnaround. A dead cycle occurs on the first Write performed immediately after a read as shown in Figure 5. This dead cycle is labeled as NO OPERATION, and occurs for both Flow-through and Pipelined operating modes. During NO OPERATION, data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity. To prevent this scenario, $\overline{OE}$ should be used to asynchronously disable the I/O drivers for bus turnaround. Figure 6 shows that by controlling $\overline{OE}$, dead cycles no longer exist.

Figure 5. Pipelined Read-to-Write-to-Read with $\overline{OE}$ = V_{IL}

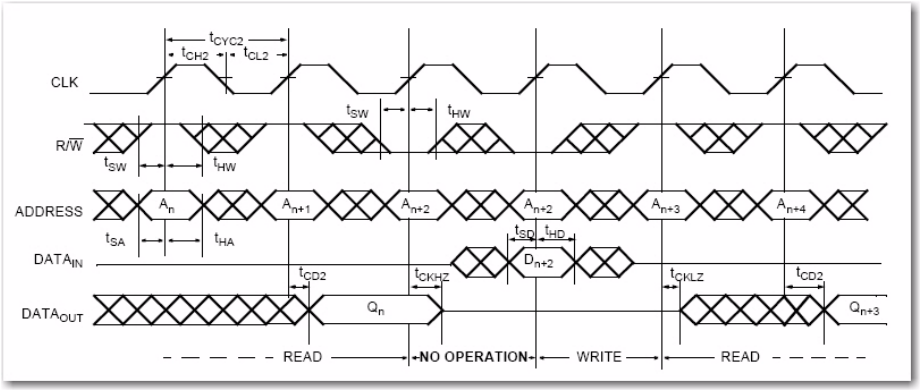
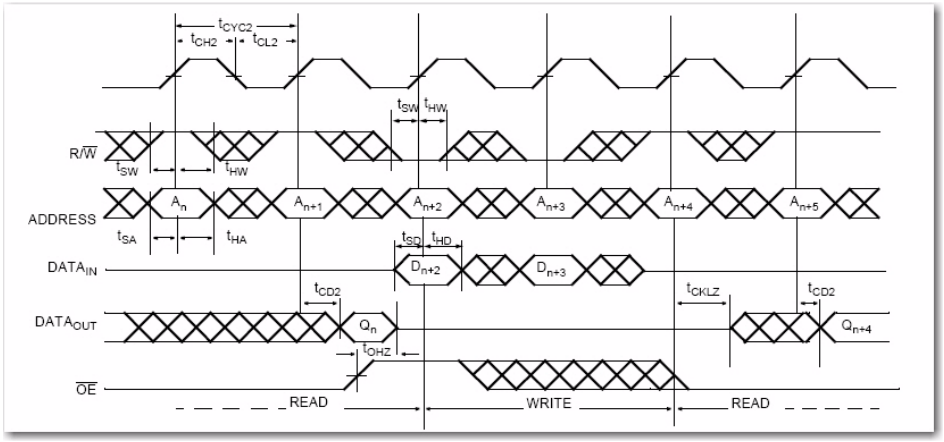


Figure 6. Pipelined Read-to-Write-to-Read with $\overline{OE}$ Controlled



2.4 Width and Depth Expansion

Cypress Synchronous dual-ports provide two chip enables, $\overline{CE_0}$ and CE_1 to simplify width and depth expansion without the need for external logic.

Figure 7 illustrates depth expansion with two 64K × 18 synchronous DPRAMs to achieve a 128K × 18 organization. The same two devices can also be width expanded to create a 64K × 36 interface. Figure 8 illustrates width expansion of synchronous DPRAMs.

Figure 7. Depth Expansion of Synchronous Dual-Port RAMs

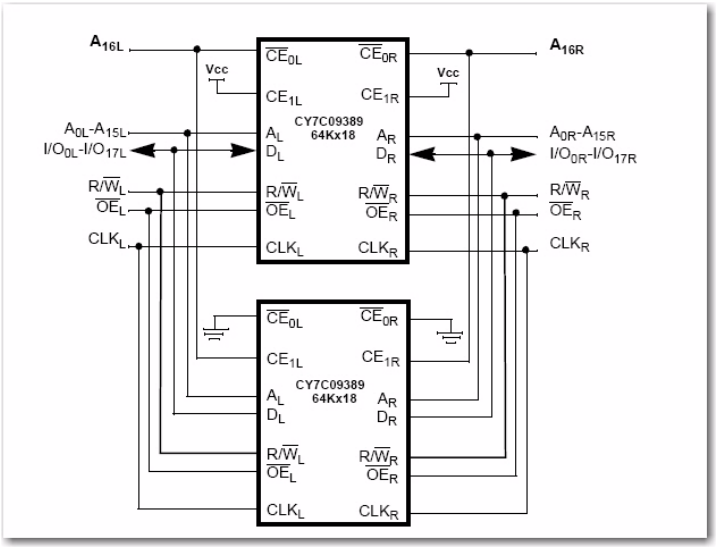
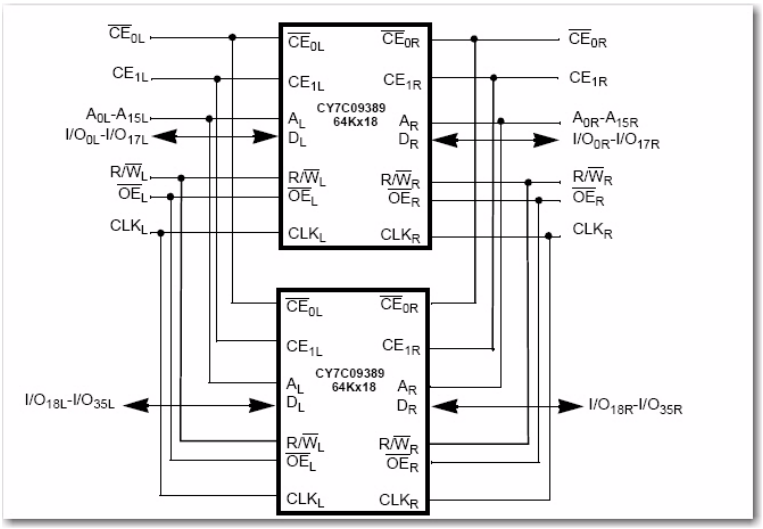


Figure 8. Width Expansion of Synchronous Dual-Port RAMs



3 Applications

Dual-ports are used in a variety of communication systems that involve multi processor designs. DPRAMs can be used in any system that requires data to be moved from one device to another. These systems include data communication/networking equipment and multiprocessor systems where the processors operate at different speeds. Synchronous DPRAMs, when operated in Pipelined sync mode are appropriate for high bandwidth applications since they provide short cycle times and fast clock to data time (t_{CD}). Burst mode operation improves the overall performance of the system since it reduces the overhead for memory accesses.

Video encoding and medical imaging applications handle large volumes of raw data and employ algorithms that are computation intensive. Such applications typically use co-processing architectures with DSPs and FPGAs. These systems benefit from the DSPs capability to handle high complexity algorithms and the FPGA's capability to support high data acquisition rates.

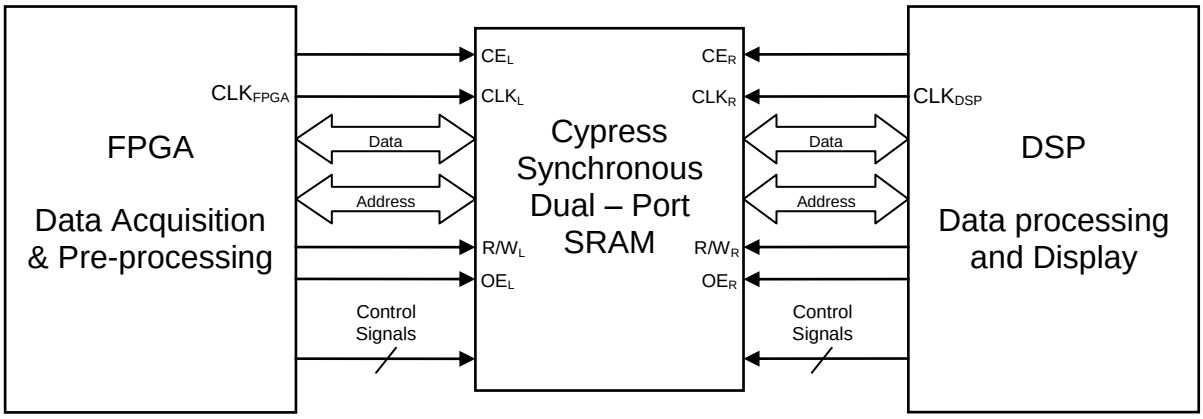
The quantum of data to be handled by the FPGA and DSP interface depends on the distribution of computation blocks between the two devices. The block RAMs in the FPGA are utilized as buffers to store the data to be sent to the DSP. The data transfer between the FPGA and DSP can be simplified using a synchronous dual-port SRAM. Each port of the DPRAM appears as a standard SRAM interface (Both the FPGA and the DSP see a simple interface).

The factors that make synchronous dual-port SRAMs an ideal interface between these systems:

- High operating speeds of up-to 200 MHz
- Densities of up-to 36 Mb
- Independent operations on both ports, eliminating the need for synchronization of memory access between the systems being interfaced
- Ability to handle two different time domains and corresponding protocols
- Capability to interface with devices working at different voltage levels on each port
- Random access to the memory locations
- Port to port message passing capability
- Mechanisms to maintain data consistency / coherence

Figure 9 is a generic block diagram of a co-processor system using a synchronous DPRAM.

Figure 9. Block Diagram of Synchronous DPRAMs in Co-Processor Architectures



4 Summary

Cypress Synchronous DPRAMs offer unmatched speed, density and flexibility and help you extract maximum performance out of multi-processor systems. Cypress Synchronous DPRAMs are the ideal choice in any system that required high speed and reliable data sharing between two bus masters. These devices available at multiple operating voltages (5 V, 3.3 V, and1.8 V) and bus width options (×8, ×16 and ×32 and in ×9, ×18 and ×36 for parity use). For a complete listing of Cypress dual-ports (densities up to 36-Mbit), visit our website http://www.cypress.com.

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*A	3118178	ADMU	01/03/2011	Updated part information. Minor edits. Updated to new template.
*B	3411411	ADMU	10/19/2011	Converted from FrameMaker to Word. Updated to new template.
*C	3544324	ADMU	03/07/2012	Updated content based feedback from on cross BU review. Updated to new template.
*D	4564162	ADMU	11/07/2014	Updated to new template.
*E	5847749	HARA	08/17/2017	Updated logo and copyright.
*F	5966346	NILE	11/14/2017	Updated template

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