AN084

SD-SDI and HD-SDI Checkfield Testing on Hotlink II™ Transceivers for SMPTE Pathological Conditions

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Associated Part Family: HOTLink II™ Video PHY
Software Version: NA
Related Application Notes: None

The purpose of this application note is to show the results of SMPTE pathological testing performed on the HOTLink II™ CYV15G0101DXB device.

Contents

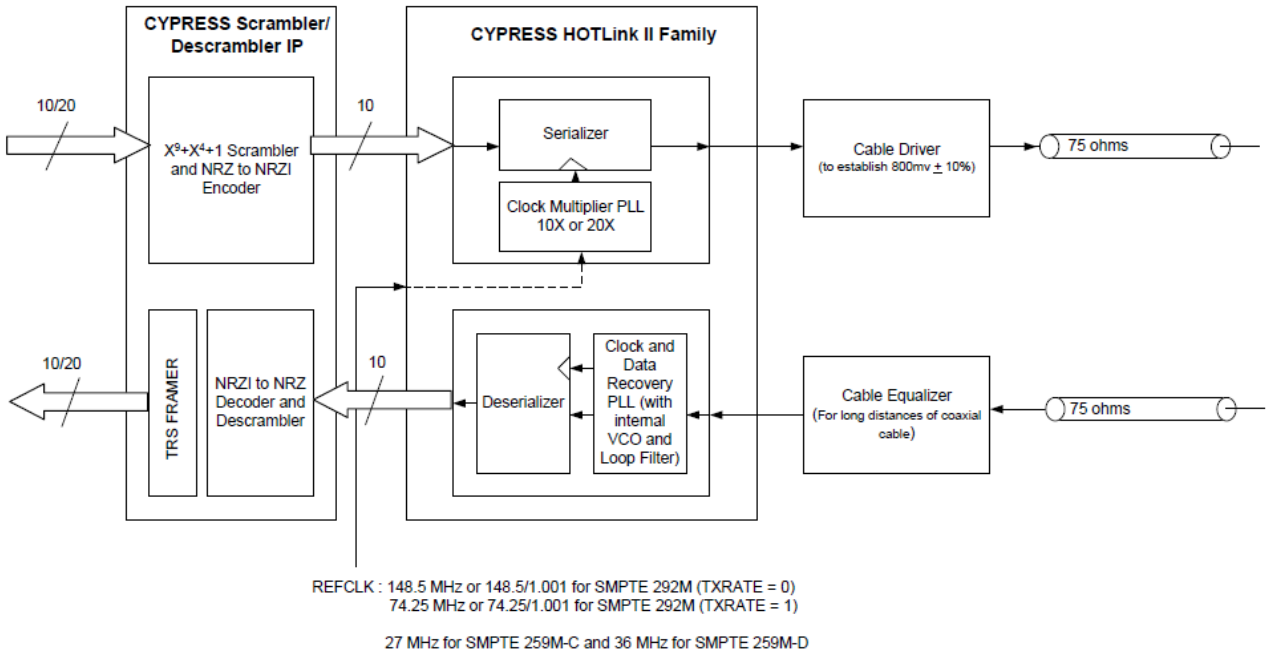
Introduction

The HOTLink II family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provides serialization, deserialization, optional 8B/10B encoding/decoding and framing functions. It can transport serial data at rates from 195 Mbps to 1.5 Gbps per channel and is compliant with communication standards such as SMPTE 259M, SMPTE 292M, DVB-ASI, Gigabit Ethernet, Fibre Channel and ESCON®.

The Society of Motion Picture and Television Engineers (SMPTE) is a professional organization that develops interface and protocol standards for the professional video industry. Two such standards are SMPTE 259M and SMPTE 292M.

The “CYV15G0x0yDXB” HOTLink II family of devices are compliant to the pathological tests defined in SMPTE EG34–1999 at both SMPTE 292M and SMPTE 259M data rates. The purpose of this application note is to show the results of SMPTE pathological testing performed on the HOTLink II CYV15G0101DXB Device. The tests were performed using industry standard test equipment that generates the pathological conditions as per SMPTE recommendations.

Figure 1. Cypress Solution for Multi-format SMPTE SDI Transport



SMPTE 259M and SMPTE 292M

SMPTE 259M documents the Standard Definition–Serial Digital Interface (SD-SDI) which is used to transport 10-Bit 4:2:2 component and 4fSC composite digital video signals across 75 W coaxial cables. This standard supports transmission of both 525 line@60 Hz and 625 line@50 Hz television signals in both 4:3 and 16:9 aspect ratio forms (Reference 5).

SMPTE 292M documents the High Definition–Serial Digital Interface (HD-SDI) which is used for serial digital transport of HDTV signal. This standard supports transmission of 1125 lines or 750 lines at both rates of 60 Hz (30 Hz for non-interlaced) and 59.94 Hz (29.97 Hz for non-interlaced) in both 16:9 and 4:3 aspect ratios (Reference 6).

Any device in the Cypress's HOTLink II family of devices is compliant to both SMPTE 259M-CD as well as SMPTE 292M. Cypress also has solutions for implementing scramblers, descramblers and TRS framers for both SMPTE 259M-CD as well as SMPTE 292M.

Block Diagram of SMPTE SDI Transport System

The illustration in shows Cypress's solution for implementing multi-format SDI transport. The parallel data input for the transmit interface can accept either 10-bit or 20-bit (10-bit Y and 10-bit C_bC_r) parallel digital video (as specified by SMPTE 125M, 244M, 260M, 274M, 295M or 296M). The data captured at these parallel inputs are then scrambled.

Scrambling

Scrambling is used to increase the transition density of the serial bit-stream, and to attempt to limit the maximum run-lengths of continuous zeros or ones that can occur when sending certain characters. The scrambler generator polynomial is listed in Equation 1.

$$G_1(X) = X^9 + X^4 + 1$$

Equation 1

Logic block diagrams of a serial implementation of a scrambler/NRZI encoder, and NRZI decoder/descrambler are shown in Figure 2. Each rectangle containing a D represents a D-type flip-flop. These flip-flops are connected to form a specialized shift register that implements the scrambler polynomial. The scrambled data is NRZI encoded to increase the transition density in the serial data stream. Moreover, it also allows the data stream to be phase independent; i.e., an inverted data stream will decode to the same signal as a non-inverted stream. The NRZI encoder polynomial is listed in Equation 2.

$$G_2(X) = X + 1$$

Equation 2

The hardware implementation of this polynomial consists of the last flip-flop and XOR gate in the transmit data path portion of Figure 2.

The Cypress Scrambling solution performs the scrambling operations on 10-bit parallel data and outputs 10-bit parallel scrambled data. If the source data is 20 bits wide, then it is multiplexed to a single 10-bit data stream before the scrambling operation. The resultant 10-bit scrambled data output is passed to the HOTLink II input register.

The input register can be clocked using the reference clock (full-rate or half-rate) or TXCLKx (operates at 10-bit character rate). This transmit data is transferred to clock domain that operates with the reference clock through the phase align buffer. This reference clock is multiplied by ten or twenty (depending on TXRATE) using a high-performance PLL to provide the bit-rate clock for the serial data path. The specific serial data rate used is dependent upon the character rate of the source video stream. The serialized data stream is fed to the coaxial cable through a cable driver. The purpose of the cable driver is to feed a single ended peak-to-peak swing of 800 mV ± 10% to the coaxial cable.

The receive path performs the opposite function of the transmit path. This starts with a high-performance PLL-based Clock and Data Recovery (CDR) circuit that captures the serial data from the coaxial cable, and extracts a bit-rate clock from the transitions in the data stream. The CDR has an internal VCO and loop filter. No external components are required for the PLL. This bit-rate clock is then divided by ten or twenty (depending on RXRATE) to generate a character-rate clock that is presented along with the output characters.

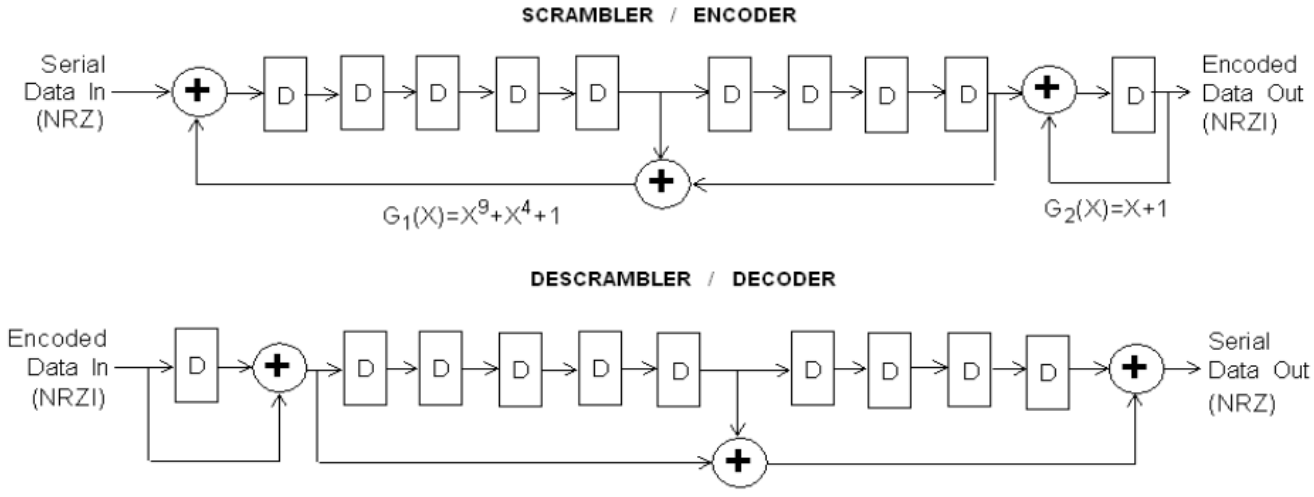
Descrambling

Following reception and deserialization, the 10-bit data is routed through an NRZI-to-NRZ converter and then descrambled. The hardware used to perform these operations is very similar to that used in the transmit portion of the interface, with two major exceptions.

First, the polynomials are reversed. Now instead of feedback operation, all the shift register XOR gates are configured for feed-forward operation. This removes the additional transitions added by the transmit data path and returns the data to its original bit-stream form.

The second major difference in the receive interface, is that the data (at this point) has no available reference to identify the start or end of each 10-bit character. The operation of finding the character boundary in the data stream is known as framing.

Figure 2. Structure of SMPTE SDI Scrambler and Descrambler



Framing

Framing is the function of determining where (in a serial data stream) characters begin and end. Framing of a SMPTE 259M video stream uses specialized hardware to detect a bit pattern known as the Timing Reference Signal (TRS) that is embedded in between the End of Active Video (EAV) and Start of Active Video (SAV) of the video line. Once the TRS is detected, the framer hardware adjusts to align the 10-bit output character with the recovered character clock.

For SMPTE 259M, the TRS consists of a three characters sequence of $3FF_h$, 000_h, and 000_h (10 bit hex) respectively. To allow this sequence to be used for framing, it must not be possible for the same bit sequence to occur at other bit offsets within characters. This is controlled within SMPTE video by making the characters in the ranges of 000_h–003_h and $3FC_h$–$3FF_h$ illegal for use in the active portion of video fields. For SMPTE 292M, the TRS consists of a six characters sequence of $3FF_h$, $3FF_h$, 000_h, 000_h, 000_h and 000_h (10 bit hex) respectively. The Cypress solution for TRS framing supports both SMPTE 259M as well as SMPTE 292M framing.

Pathological Conditions and SDI Checkfield Testing

Under normal conditions the scrambled output has high transition density with a good ratio of ones to zeros. The pathological conditions are specific high run-length patterns with very low transition density that may be generated by the SMPTE scrambler for specific combinations of the scrambler state and scrambler inputs. Although the probability of the specific inputs and specific scrambler state occurring at the same time in real video data is very low, component vendors are expected to be compliant to the specified pathological conditions. The pathological serial digital signals are often very challenging to be handled by SDI receivers. SMPTE EG34-1999 (Reference 1) documents the pathological patterns that may occur in a SMPTE scrambled system that also need to be recovered by SDI receivers with no errors. System designers need to select components that are tested to work under these pathological conditions. The various pathological conditions that could occur are the following:

1. Run-length of 44 bits with no transitions
2. Repetition of 20 ones followed by 20 zeros for a duration of entire active video line
3. Repetition of 19 ones followed by 1 zero or 19 zeros followed by 1 one for a duration of entire active video line.

SMPTE RP178 (Reference 2) documents the recommended video checkfield data that needs to be generated to test the compliance of SMPTE 259M pathological conditions. SMPTE RP198 (Reference 3) documents the recommended video checkfield data that needs to be generated to test the compliance of SMPTE 292M pathological conditions.

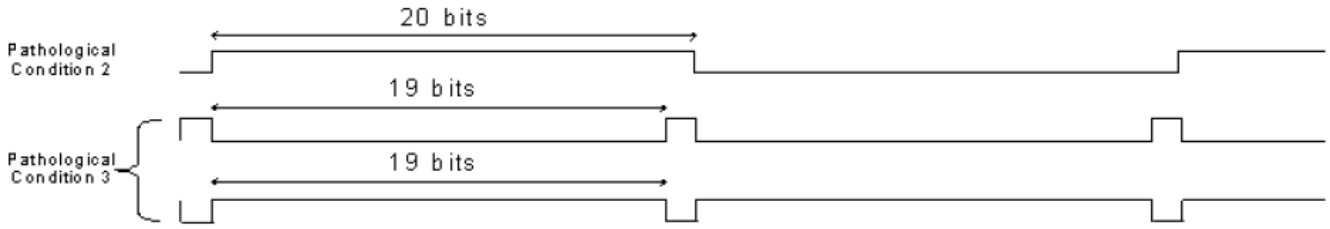
Pathological Condition 1

This condition might occur during the EAV/SAV of the video line for Component Signals and during the TRS-ID for Composite signals. Depending on the state of the scrambler the scrambled output can have a period of 44 bit times with no transitions. This pathological case will test the ability of the PLL to remain locked for a long period of no transitions. Cypress HOTLink II Transceivers are tested and found to be compliant to this pathological test case.

Pathological Condition 2

This condition might occur when flat field of specific colors (example: $Y = 110_h$; $C = 200_h$ as documented in RP-178) are scrambled. For these specific colors, the pathological condition will happen only when the scramblers are in a specific state that causes the scrambled data to be repetitions of 20 ones followed by 20 zeros, as shown in Figure 3. Whenever it occurs, the pathological pattern lasts for a duration of an entire active video scan line. In very rare cases, the condition might occur in a sequence of multiple lines. Reference 4 shows statistics that run lengths of 20 ones and 20 zeros occur about once per SD-SDI checkfield frame.

Figure 3. SDI Serial Output Data When Pathological Conditions Happen



The repetition of 20 zeros followed by 20 ones will test the ability of the Receive Clock and Data Recovery (CDR) PLL to remain locked for patterns with very low transition density. Moreover, the transition from high transition density to low transition density affects the gain and bandwidth of the PLL, making it a challenging pattern to recover with no errors. This test is commonly called the “PLL test”. Cypress HOTLink II transceivers are tested and found to be compliant to this pathological test case.

Pathological Condition 3

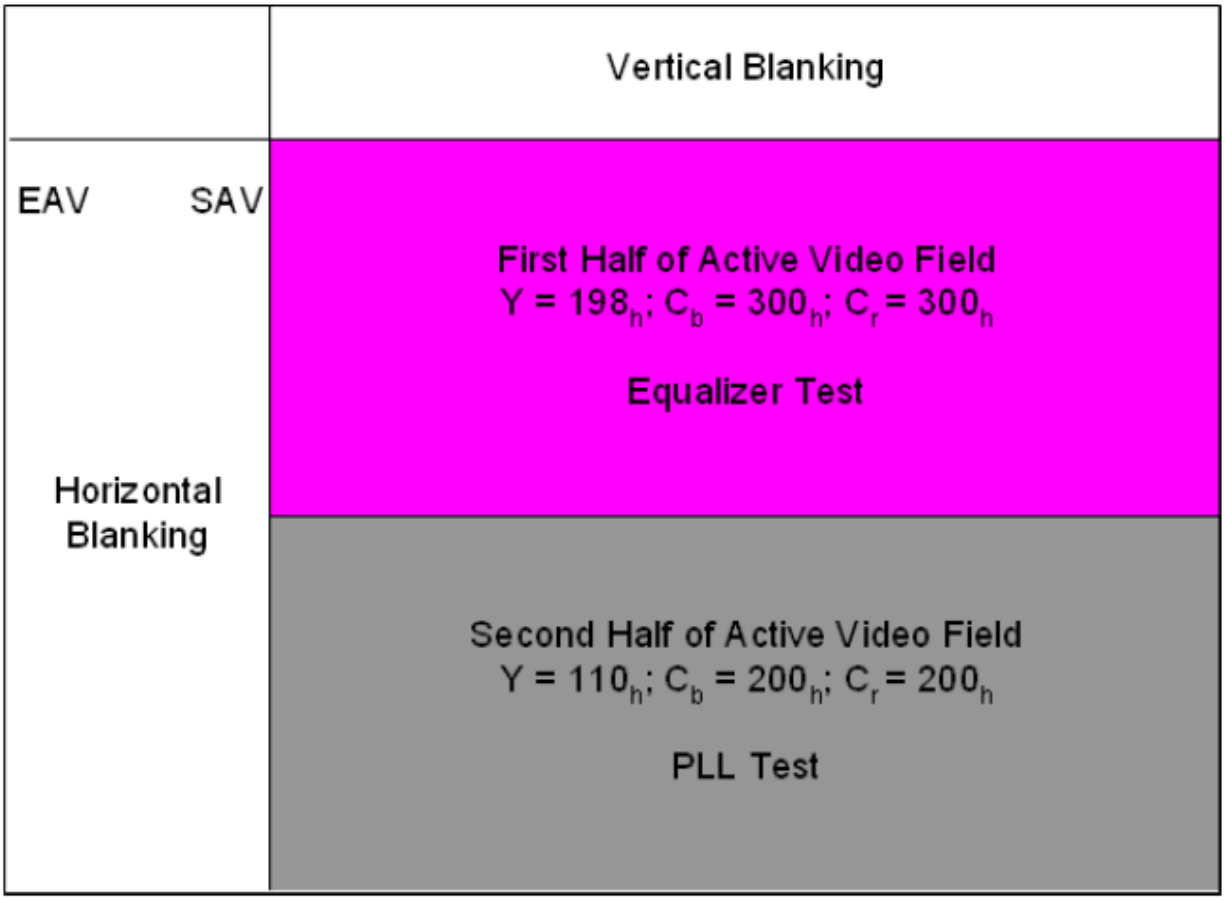
This condition might occur when flat field of specific colors, different from the colors that would generate pathological condition 2 (example: Y = 198_h; C = 300_h as documented in RP-178), are scrambled. For these specific colors, the pathological condition will happen only when the scramblers are in a specific state that causes the scrambled data to be repetitions of either 19 ones followed by 1 zero or 19 zeros followed by one 1, as shown in Figure 3. Whenever it occurs, the pathological pattern lasts for a duration of an entire active video scan line. In very rare cases, the condition might occur in a sequence of multiple lines. Reference 4 shows statistics that run lengths of 19 ones and 19 zeros occur about once per SD-SDI checkfield frame.

The repetition of 19 zeros followed by 1 one or 19 ones followed by 1 zero will test the ability of the equalizers, input buffers and coupling network (AC-coupling capacitor or transformer) to handle baseline wander and low frequency content. This test is commonly called the “Equalizer Test”. Since, this pathological signal has significant amount of DC content, the receiving equipment must have a good low frequency response to recover this signal without any errors. The effect of this pattern on the Receive Clock and Data Recovery (CDR) PLL is not as stringent as pathological condition 2, because it has two transitions every 20 bits. Cypress HOTLink II transceivers are tested and found to be compliant to this pathological test case.

SDI Checkfield

SMPTE RP 178 and SMPTE RP 198 document the SDI checkfield data for SMPTE 259M and SMPTE 292M respectively. The SDI checkfield is the recommended data pattern that needs to be used to test compliance to pathological cases 2 and 3. The structure of the SDI checkfield for SMPTE 259M and SMPTE 292M is the same with just differences in the frame/field size. The SDI checkfield is divided into two regions of approximately same size, as illustrated in Figure 4. The top half of the SDI checkfield generates the pathological condition 3 (19 ones followed by 1 zero or 19 zeros followed by 1 one) by making the active video lines in this half the same shade of pink color (Y = 198_h; Cr = 300_h; Cb = 300_h). The bottom half of the SDI checkfield generates the pathological condition 2 (20 ones followed by 20 zeros) by making the active video lines in this half the same shade of grey color (Y = 110_h; Cr = 200_h; Cb = 200_h). As per SMPTE recommendations, a component that passes the SDI checkfield without any errors is considered to be compliant to pathological conditions.

Figure 4. SDI Checkfield



Performance of HOTLink II Video Transceivers under Pathological Conditions

The HOTLink II video transceivers are compliant to all the pathological conditions defined by SMPTE for HD-SDI and SD-SDI. HOTLink II has a robust receive CDR PLL, with no external components, that will remain locked during the pathological conditions. Since HOTLink II does not need any external PLL components such as loop filter or VCO, no tweaking of components is required to achieve compliance to the pathological conditions.

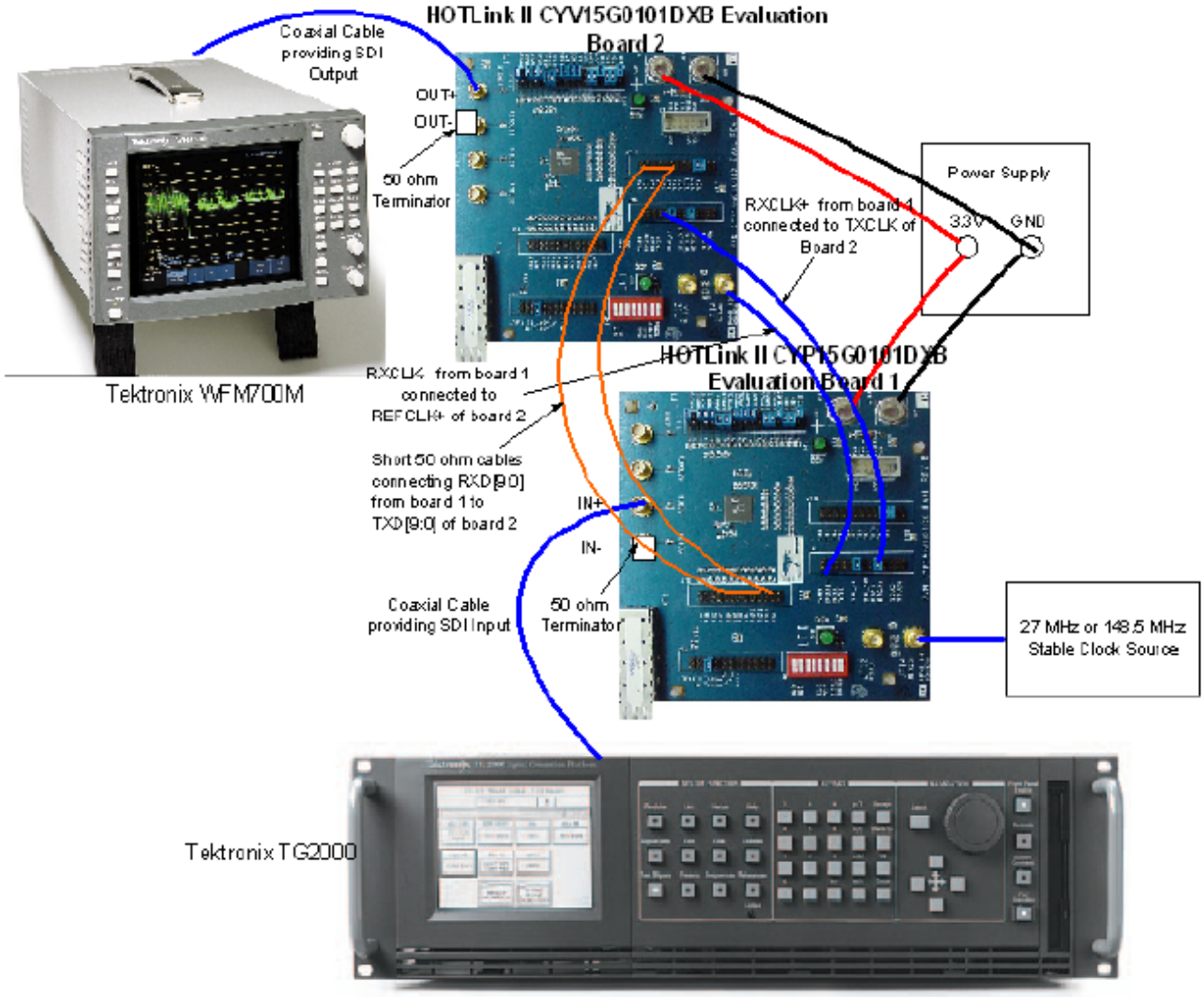
Test Set-up to Perform Pathological Testing as Recommended in SMPTE RP 178 and RP 198

Pathological testing was performed on HOTLink II Transceivers using standard test equipment used by the industry. The list of equipment used for the testing described in this section are as follows:

1. Tektronix WFM700M–SD/HD SDI Waveform monitor
2. Tektronix TG2000–SD/HD SDI Pattern generator
3. HOTLink II Evaluation Board to Receive the SDI data Note: The CYV15G0101DXB HOTLinkII Evaluation Board is Obsolete. These results apply to any Video PHY HOTLink II device.
4. HOTLink II Evaluation Board to Re-transmit the recovered SDI Data
5. 27 MHz and 148.5 MHz Clock source for the receive HOTLink II Evaluation Board
6. Power Supply (3.3 V)
7. Appropriate Coaxial cables

The test set-up is shown in Figure 5.

Figure 5. Test Set-up to Perform Pathological Error Testing



The Tektronix TG2000 is used to generate the desired pathological checkfields at the desired data rate. The module called DVG1 is used for SD-SDI Checkfield generation as per SMPTE RP 178 and the module called HDVG1 is used for HD-SDI checkfield generation as per SMPTE RP 198. The SDI data from the generator is fed to the serial input of the first HOTLink II CYV15G0101DXB Evaluation board. This test setup shows CYV15G0101DXB as the device under test. Any device in the HOTLink II family can be tested using a similar setup by simply replacing the device under test. The HOTLink II device is configured to bypass the 8B/10B encoder and 10B/8B decoder. The 10-bit deserialized data is connected to the transmit 10-bit input of the second HOTLink II Evaluation Board. The second evaluation board has to be used since the recovered clock of a given board cannot be connected to the reference clock input of the same board. This is due to the fact that the receive CDR PLL needs to see a stable reference clock to perform frequency lock. The RXCLK- output of the first evaluation board is connected to the Reference Clock input of the second evaluation board. The RXCLK+ output of the first evaluation board is connected to the TXCLK input of the second evaluation board. The serial output of the second evaluation board is connected to the inputs of Tektronix waveform monitor WFM700M. The waveform monitor is capable of displaying the received picture, eye diagram, jitter and CRC errors.

The results of pathological testing for both SMPTE 259M and SMPTE 292M showed that HOTLink II device can recover these patterns without any errors. The illustration in Figure 6 shows the testing results of the HD-SDI pathological testing performed on HOTLink II. The illustration in Figure 7 shows the testing results of the SD-SDI pathological testing performed on HOTLink II.

Figure 6. Results of HD-SDI Checkfield Testing from Tektronix WFM700M

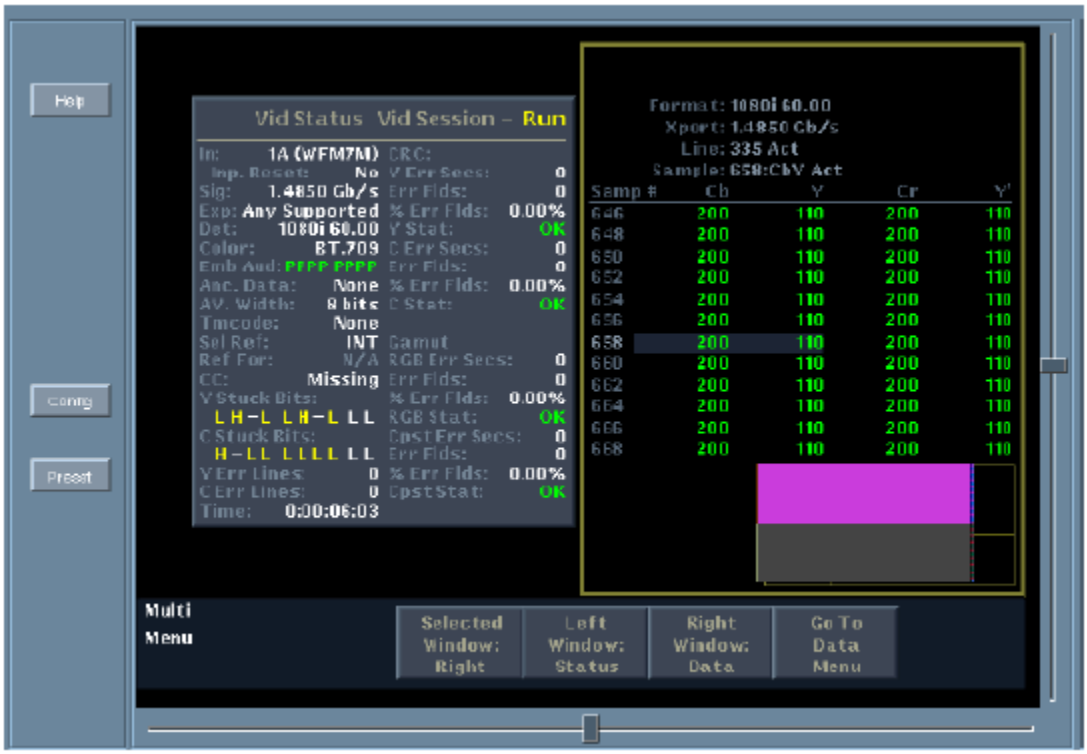


Figure 7. Results of SD-SDI Checkfield Testing from Tektronix WFM700M

Summary

Pathological Patterns with long runs of ones or zeros occur in SMPTE SDI streams for specific combinations of input to the scrambler and scrambler state. When these patterns occur, the SDI receiver components are expected to recover the data with no errors. Cypress HOTLink II family of transceivers are compliant to all pathological requirements specified by SMPTE EG34-1999. This is proven by testing the devices with standard test equipment used by the Professional Video industry.

References

1. SMPTE EG 34–1999, Pathological Conditions in Serial Digital Video Systems, SMPTE.
2. SMPTE RP 178–1996, Recommended Practice, Serial Digital Interface Checkfield for 10-Bit 4:2:2 Component Signals and 4fsc Composite signals, SMPTE.
3. SMPTE RP 198–1998, Recommended Practice, Bit Serial Interface Checkfield for Use in High-Definition Interfaces, SMPTE.
4. A Guide to Digital Television Systems and Measurements, Chapter 9, Tektronix, 1997.
5. SMPTE 259M–1997, 10-Bit 4:2:2 Component and 4fsc Composite Digital Signals–Serial Digital Interface.
6. SMPTE 292M –1998, Bit-Serial Digital Interface for High-Definition Television Systems.

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**	1009141	SAAC	04/23/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN084 file
*A	1770639	SAAC	11/26/2007	Applied new template, updated copyright, added source and revision disclaimers. No technical updates made.
*B	3147772	SAAC	01/19/2011	Added Associated Part Family as HOTLink II™ Video PHY. Added Associated Application Notes as None. Added Abstract. Updated SMPTE 259M and SMPTE 292M: Updated Block Diagram of SMPTE SDI Transport System: Updated Framing: Updated description. Updated Performance of HOTLink II Video Transceivers under Pathological Conditions: Updated Test Set-up to Perform Pathological Testing as Recommended in SMPTE RP 178 and RP 198: Updated description.
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*D	4273573	YLIU	02/06/2014	Updated in new template. Completing Sunset Review.

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