AN068

Configuring the Independent Channel Hotlink II™ Device for Digital Video Transport

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Associated Project: No
Associated Part Family: HOTLink II™ VIDEO PHY's (Independent Channel)
Software Version: NA
Related Application Notes: None

This application note describes how to configure the independent channel HOTLink II™ devices for digital video transport (DVB-ASI, SMPTE259M, or SMPTE292M).

Contents

Introduction

The HOTLink II™ family of physical layer (PHY) devices is a point-to-point or point-to-multipoint communications building block that provides serialization, deserialization, optional 8B/10B encoding/decoding and framing functions. The independent channel HOTLink II devices have independent transceivers that have separate reference clock inputs (Independent Clocking) for each channel. It can transport serial data at rates from 195 Mbps to 1.5 Gbps per channel and is compliant with communication standards such as gigabit ethernet (GbE), fibre channel, SMPTE 259M, SMPTE 292M, DVB-ASI and ESCON®. The only additional feature present in the video family of HOTLink II devices (CYV part numbers [1]) is the ability to pass pathological pattern tests as defined in SMPTE EG34-1999.

This application note will focus on configuring CYV15G0403DXB [2] for serial digital video transport protocols, specifically, Digital video broadcast—asynchronous serial interface (DVB-ASI), SMPTE 259M and SMPTE 292M. SMPTE 259M specifies Standard definition—serial digital interface (SD-SDI) and SMPTE 292M specifies High definition—serial digital interface (HD-SDI). Configuration of CYP(V)15G0403DXB for other data communication protocols (Fibre Channel, ESCON and GbE) is covered in the application note entitled Configuring the HOTLink II CYP(V)15G0403DXB Device for Multiple Protocols.

[1] The device CYV15G0403DXB is obsolete, this application note applies to any of the independent channel video devices.

[2] The device CYV15G0403DXB is obsolete, this application note applies to any of the independent channel video devices.

The first section of this application note will focus on the benefits of independent clocking and independent configuration features for serial digital video transport applications. The second section focuses on the specifics of configuring the CYV15G0403DXB [3] for operating under different serial digital video transmission protocols.

Benefits of Independent Clocking and Independent Configuration

The independent clocking and independent configuration capability of CYV15G0403DXB [4] can be used by digital video customers in three types of applications:

1. Multiple protocols over different channels: Each channel can transmit and receive traffic from a different protocol. For example, Channel A can be configured to pass SMPTE 292M data (HD-SDI), while Channel B can be configured to pass DVB-ASI (MPEG) data and Channel C can be configured to pass SMPTE 259M data (SD-SDI). An example of this application is illustrated in Figure 1.
2. Multiple data rates over different channels: Each channel can transmit and receive data at a different data rate. For example, Channel A can be configured to pass SMPTE 292M (HD-SDI) data at 1.485 Gbps while channel D is configured to pass SMPTE 259M (SD-SDI) data at 270 Mbps. Customers can use this feature to reconfigure the same channel for either SMPTE 259M transport or SMPTE 292M transport. A low-jitter programmable clock source that can be configured to output either frequency (27 MHz or 148.5 MHz) can be used as the reference clock input (REFCLKx±).
3. Multiple channels pass traffic from the same protocol but different sources: Each channel can transmit traffic from the same protocol (same data rate) but the individual channels can be referenced by different clocks that need NOT be synchronous to each other. In other words, the reference clocks for each channel can have a frequency offset with respect to each other. An example of this application is shown in Figure 2.

Figure 1. Example Showing Video Data Transfer from Multiple Protocols Over the Same CYV15G0403DXB Device

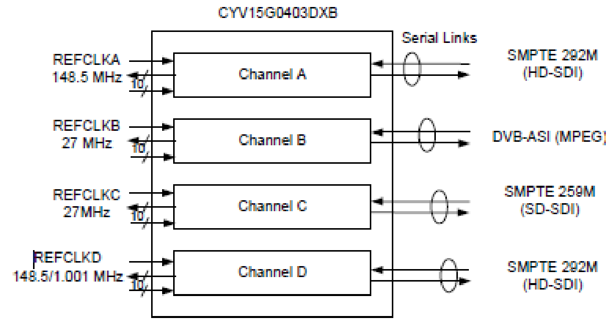
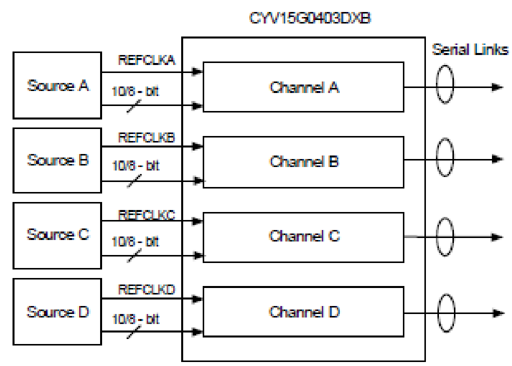


Figure 2. Example Showing Transfer of Data at the Same Data Rate but Different Reference Sources



Configuration Interface

The CYV15G0403DXB has a configuration interface that consists of a 4-bit address bus (ADDR[3:0]) and an 8-bit data bus (DATA[7:0]). The address bus selects one of 16 latch-banks. Each latch-bank has eight latches. The block level description of the configuration interface is shown in Figure 3. The 4-bit address is decoded to enable one of the sixteen latch-banks. The enable signal for each latch-bank (or row) is indicated in Figure 3 as EN_x with the associated value of ADDR[3:0] to its right. The input $\overline{\text{WREN}}$ is the write enable signal for all latch-banks. When $\overline{\text{WREN}}$ is asserted, the values of DATA[7:0] are latched into the latch-bank selected by ADDR[3:0].

[3] The device CYV15G0403DXB is obsolete, this application note applies to any of the independent channel video devices.

[4] The device CYV15G0403DXB is obsolete, this application note applies to any of the independent channel video devices.

Organization of the Latch-Banks

The first set of three latch-banks (0, 1 and 2) control the settings of Channel A. The second set three latch-banks (3, 4 and 5) control the settings of Channel B. Similarly, latch-banks 6, 7, 8 and 9, 10, 11 control the settings of Channel C and Channel D, respectively. The latch-banks 12, 13 and 14 contain the Global configuration latches that can be used for controlling all channels globally. The last latch-bank, 15, is the Mask latch-bank used for bit-by-bit configuration. The mapping of the latches in each latch bank is shown in Table 3 on page 9 in Appendix A. The definitions of these configuration bits can be found in the data sheet.

Static Latches and Dynamic Latches

There are two types of latch banks: static (S) and dynamic (D). Each channel is configured by two static and one dynamic latch banks. The S type control those settings that normally do not change during the lifetime of an application, whereas the D type controls the settings that could change during the application's lifetime. The first row of latches for each channel (address numbers 0, 3, 7, and 10) are the static receiver control latches. The second row of latches for each channel (address numbers 1, 4, 8, and 11) are the static transmitter control latches. The third row of latches for each channel (address numbers 2, 5, 9, and 12) are the dynamic control latches.

When to Use the Global Configuration Feature

The global configuration latch banks (12, 13 and 14) help limit the number of WRITE operations required when all channels in the device are to be configured with the same settings. The global update of the target latch banks occurs only when GLENx = 1 or associated FGLENx = 1. The initialization value of GLENx is 1, thereby allowing global configuration upon reset. The target latch banks for each global configuration latch bank are shown in Table 1. If all four channels are supposed to be configured with the same settings, writing to the global configuration latch banks completely configure all four channels simultaneously.

Table 1. Global Configuration

Global Configuration Latch Bank	Target Latch Banks	Conditions for global configuration
12	0, 3, 6 and 9	Associated GLENx = 1 or FGLEN0 = 1
13	1, 4, 7 and 10	Associated GLENx = 1 or FGLEN1 = 1
14	2, 5, 8 and 11	Associated GLENx = 1 or FGLEN2 = 1

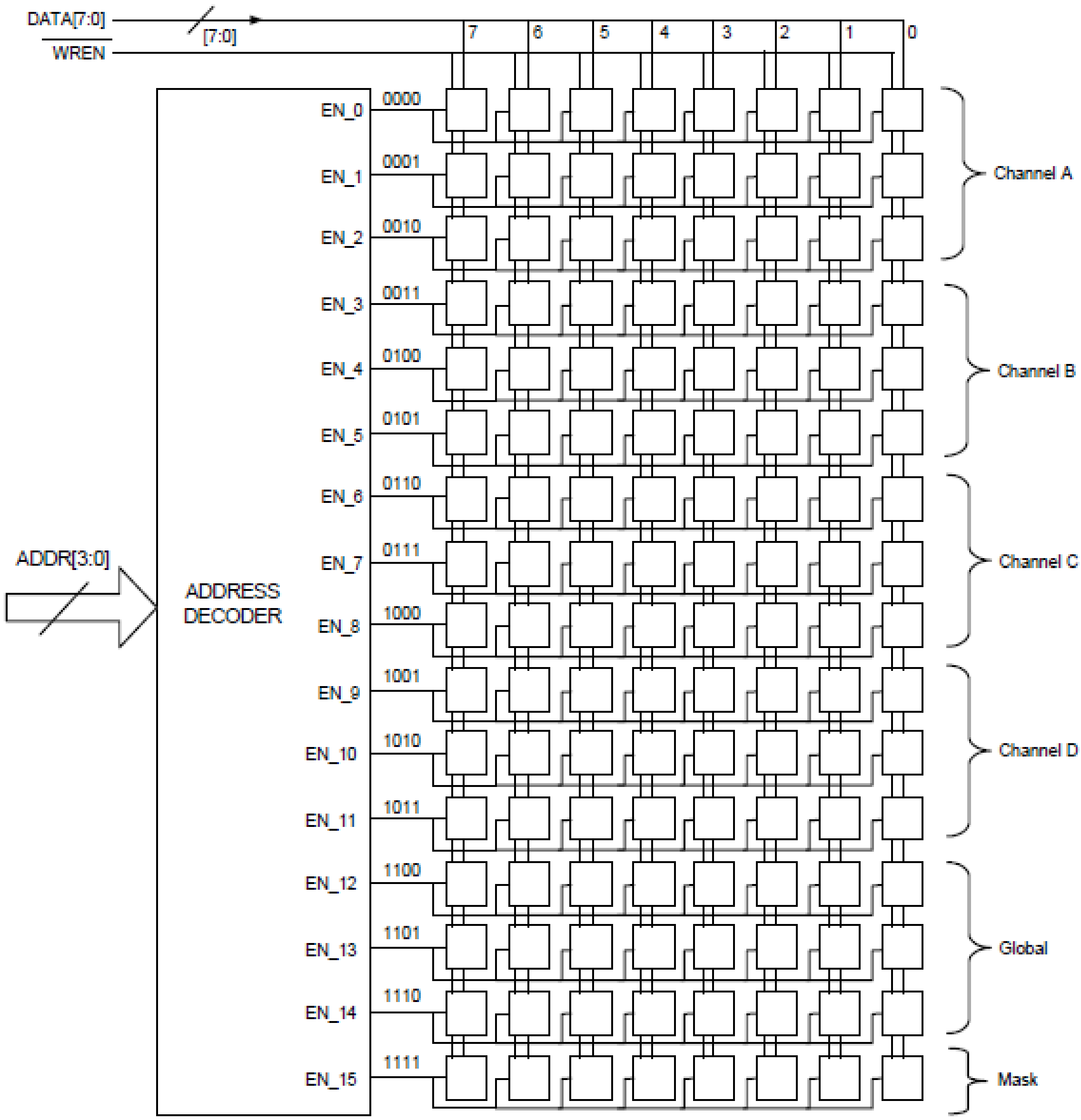
When to Use Bit-by-Bit Configuration

The bit-by-bit configuration feature should be used whenever one or more bits in a particular latch bank need to be changed without altering the contents of the other bits in that latch bank. The mask vector in latch bank 15 is used for masking the latches whose contents should remain unaltered. The masking of bits that need to remain unaltered is done by setting the associated mask bit to ‘0’. After setting the desired mask bits, subsequent write operations to any other latch bank will alter the contents of the bits for which the associated mask bit is ‘1’. The initialize value of the mask vector is “11111111,” thereby making its use optional on reset.

An example where the bit-by-bit configuration feature is useful is when performing a phase-align reset. A phase-align reset should be performed on the transmit channel after configuring the transmit channel settings. The steps needed for performing a phase align reset on channel A, for example, without altering the contents of any other configuration bits are:

1. Set all bits in the mask vector latch bank to 0, except bit DATA[1]. This done by writing “00000010” to address 15.
2. Write the data “XXXXXX0X” to latch bank 2 (channel A) where ‘X’ stands for a “don’t care” value. Note that the PABRSTx is a self-clearing latch. Therefore, there is no need to rewrite a ‘1’ to complete the reset of the phase align buffer.

Figure 3. Block Diagram of the CYV15G0403DXB Configuration Interface



Configuration for Digital Video Transport Protocols

This section of the application note covers the requirements and settings for any channel of the CYV15G0403DXB HOTLink II device to operate under a specific protocol. The protocols covered are DVB-ASI, SMPTE 259M and SMPTE 292M.

Configuration for DVB-ASI

The HOTLink II family of devices support DVB-ASI operation at a transmission rate of 270 MBaud.

Speed Settings

The operating data rate supported by HOTLink II for DVB-ASI is 270 Mbps. For this data rate, the SPDSELx for the given channel should be LOW.

Reference clock

As per DVB-ASI standard, REFCLKx± for the given channel must have a frequency stability within ±100 ppm. It should be a full-rate clock at 27 MHz. Half-rate REFCLKx± is NOT allowed for this speed range. Therefore, TXRATEx must be set to 0.

The jitter from the reference clock should be low enough to ensure that the serial output from the HOTLink II device meets the DVB-ASI Jitter specification.

Transmit Clock

If TXCLKx is selected as the input clock to latch the parallel input data into the input register (TXCKSELx = 0), TXCLKx should be synchronous in frequency to REFCLKx. The phase align buffer must be reset after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx frequency.

8B/10B Encoder and 10B/8B Decoder

The HOTLink II transmitter block has a built-in 8B/10B Encoder that should be enabled (ENCBYPx = 1) to map the raw 8-bit data characters to the corresponding 10-bit transmission character with the correct disparity as specified by DVB-ASI. The receiver block has a built-in 10B/8B Decoder that should be enabled (DECBYPx = 1) to decode the received 10-bit transmission character to the corresponding 8-bit data character.

Framer

The recommended framer for DVB-ASI data reception is the Cypress-mode Multi-Byte framer (RFMODEx[1:0] = “10”). In this framing mode, the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

All transport packets in DVB-ASI must be preceded by two successive K28.5 characters. When this is detected by the HOTLink II receiver, it meets the framer requirements for the Cypress-mode Multi-Byte framer to frame to the correct character boundaries.

Framing Character

For the reasons mentioned in the previous section on Framer, the framing character should be set to K28.5 by setting FRAMCHARx = 1.

Receive Clock Source (Local Receiver Clock)

The received data can be clocked out of the output register to upstream logic either using the recovered clock (RXCKSELx = 0) or the local reference clock REFCLKx± (RXCKSELx = 1).

When REFCLKx± is used as the output clock for the output register, the data is read out of the elasticity buffer. The elasticity buffer inserts or deletes K28.5 characters from the transport stream to accommodate for the frequency differences between the incoming stream and the local reference clock. Therefore, sufficient K28.5 characters should be interspersed within the transport stream to allow insertion and deletion.

Receive Clocking Rate

The receive clocking rate must be set to full-rate clocking (RXRATEx = 0). The received characters will be latched every rising edge of RXCLKx+ or every falling edge of RXCLKx-.

Configuration for SMPTE 259M and SMPTE 292M

CYV15G0403DXB supports the transport of serial digital video streams of both SMPTE 259M (SD-SDI) as well as SMPTE 292M (HD-SDI). Any channel can be configured/reconfigured to either SMPTE 259M or SMPTE 292M by setting SPDSELx to LOW or HIGH, respectively.

Speed Settings

HOTLink II can operate at SMPTE 259M data rates (270 Mbps and 360 Mbps) and SMPTE 292M data rates (1.485 Gbps or 1.485/1.001 Gbps).

For SMPTE 259M data rates (270 Mbps and 360 Mbps), SPDSELx should be LOW.

For SMPTE 292M data rates (1.485 Gbps and 1.485/1.001 Gbps), SPDSELx should be HIGH.

Reference Clock

As per SMPTE standards, REFCLKx± must have a stability within ±100 ppm. For SMPTE 259M, it is recommended to use a full-rate (TXRATEx = ‘0’), stable source as the reference clock.

For SMPTE 292M, the REFCLKx± source must be either a 148.5 MHz ± 100 ppm or 148.5/1.001 MHz ± 100 ppm. The HOTLink II receiver Clock and Data Recovery PLL can lock to incoming serial streams at either of the two data rates (1.485 Gbps or 1.485/1.001 Gbps) with either of the two reference clocks.

The jitter from the reference clock should be low enough to ensure that the serial output from the HOTLink II device meets the SMPTE jitter specification for the applicable standard (SMPTE 259M or SMPTE 292M).

Transmit Clock

If TXCLKx is selected as the input clock to latch in the parallel input data (TXCKSELx = ‘0’) into the input register, the TXCLKx should be synchronous in frequency to REFCLKx. The phase align buffer must be reset after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx frequency.

8B/10B Encoder and 10B/8B Decoder

For both SMPTE 259M and SMPTE 292M, the 8B/10B Encoder and the 10B/8B Decoder must be bypassed (ENCBYPx = 0 and DECBYPx = 0). The raw 10-bit data provided by the upstream scrambler to the parallel inputs is serialized and transmitted through the serial outputs. The received serial data is deserialized as raw 10-bit data and provided as inputs to the upstream descrambler. Cypress has its own scrambler and descrambler solutions that can interface with HOTLink II devices.

Framer

For SMPTE 259M as well as SMPTE 292M, the HOTLink II framer should be permanently disabled by setting RFENx = 0.

Enabling the HOTLink II framer leads to misframing and the loss of a few bits of data whenever a sequence that matches the framing sequence is detected. This leads to bit errors in the descrambled video data. Framing to Timing Reference Sequence (TRS) should be performed in the upstream device. The descrambler solution offered by Cypress has a built-in framer that frames to the TRS sequence.

When the framer is disabled, RFMODEx[1:0] is not interpreted. It could be set to any mode EXCEPT the mode that is reserved for test, RFMODEx[1:0] = 11.

Framing Character

When the framer is disabled, the selection of framing character, FRAMCHARx, is not interpreted. Hence it is a “Don’t Care.”

Receive Clock Source (Local Receiver Clock)

The received data should be clocked to upstream logic using the recovered clock by selecting RXCKSELx = 0.

Receive Clocking Rate

The receive clocking rate must be set to full-rate clocking (RXRATEx = 0). The received characters will be latched every rising edge of RXCLKx+ or every falling edge of RXCLKx-.

Summary

The Independent Clocking feature of independent channel HOTLink II devices can be used in applications that need to transport protocols at different data rates as well as applications that need to transmit data from different reference clock domains. The flexible configuration interface allows both global and independent configuration. The configuration interface can be used to configure a particular channel to any particular video protocol (DVB-ASI, SMPTE 259M or SMPTE 292M). The settings of all control latches and control signals for DVB-ASI, SMPTE 259M and SMPTE 292M are tabulated in Table 2.

References

1. Cabled Distribution Systems for Television, Sound and Interactive Multimedia Signals, Part 9: Interfaces for CATV/SMATV Headends and Similar Professional Equipment for DVB/MPEG-2 Transport Streams. European Standard EN 50083-9: March 1997.
2. SMPTE 259M. 10-Bit 4:2:2 Component and 4FSC Composite Digital Signals—Serial Digital Interface. 1997.
3. SMPTE 292M. Bit-Serial Digital Interface for High-Definition Television Systems. 1998.
4. Independent Clock Quad HOTLink II™ Transceiver Data Sheet (38-02065). Cypress Semiconductor Corporation.
5. Pathological Conditions in Serial Digital Video Systems. SMPTE Engineering Guideline EG34–1999.

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Table 2. Recommended Configuration for Different Protocols

Control Latch/ Control Signal	DVB-ASI (270 MBaud)	SMPTE 259M (270 Mbps and 360 Mbps)	SMPTE 292M (1.485 Gbps and 1.485/1.001 Gbps)
RFMODEx[1:0]	"10": Selects Cypress-mode Multi-Byte framer.	Any setting EXCEPT "11": Framer should be disabled by setting RFENx = 0.	
FRAMCHARx	1: Selects K28.5 as framing character.	Don't Care when RFENx = 0	
DECMODEx	User selectable 1: Selects Cypress Decoding Mode for special characters 0: Selects Alternate Decoding Mode for special characters	Don't care when DECBYPx = 0	
DECBYPx	1: Enables 10B/8B Decoder in the receiver block.	0: to bypass10B/8B Decoder in the receiver block	
RXCKSELx	User selectable 0: Selects recovered clock to clock output register 1: Selects REFCLKx± to clock output register, with insertion/deletion of K28.5 characters to absorb the frequency difference between incoming serial data and REFCLKx±	0: Selects recovered clock to clock output register	
RXRATEx	0: RXCLKx+ and RXCLKx- are full-rate complementary clocks operating at the character rate.	0: RXCLKx+ and RXCLKx- are full-rate complementary clocks operating at the character rate.	
SDASEL1x[1:0]	User selectable "00": Analog signal detector disabled "01": Typical p-p differential voltage threshold level is 140 mV "10": Typical p-p differential voltage threshold level is 280 mV "11": Typical p-p differential voltage threshold level is 420 mV	User selectable "00": Analog signal detector disabled "01": Typical p-p differential voltage threshold level is 140 mV "10": Typical p-p differential voltage threshold level is 280 mV "11": Typical p-p differential voltage threshold level is 420 mV	
SDASEL2x[1:0]	User selectable "00": Analog signal detector disabled "01": Typical p-p differential voltage threshold level is 140 mV "10": Typical p-p differential voltage threshold level is 280 mV "11": Typical p-p differential voltage threshold level is 420 mV	User selectable "00": Analog signal detector disabled "01": Typical p-p differential voltage threshold level is 140 mV "10": Typical p-p differential voltage threshold level is 280 mV "11": Typical p-p differential voltage threshold level is 420 mV	

ENCBYPx	1: Enables 8B/10B Encoder in transmitter block	0: bypasses 8B/10B Encoder in transmitter block	
TXCKSELx	User selectable 0: Recommended. Selects TXCLKx to clock input register. Use TXCLKx synchronous to REFCLKx± to clock input registers. 1: Selects REFCLKx to clock input register	User selectable 0: Recommended. Selects TXCLKx to clock input register. Use TXCLKx synchronous to REFCLKx± to clock input registers. 1: Selects REFCLKx to clock input register	
TXRATEx	0: A full-rate reference clock at 27 MHz must be provided as REFCLKx±	0: A full-rate reference clock at 27 MHz for 270 Mbps bit rate and at 36 MHz for 360 Mbps bit rate must be provided	User selectable 0: 148.5 MHz or 148.5/1.001 MHz source must be used as reference clock 1: 74.25 MHz or 74.25MHz/1.001 source must be used as reference clock
RFENx	Could be left as 1 if recommendations for RFMODEx[1:0] are followed. This will keep the framer continuously enabled, making reframing possible whenever there is loss of framing.	0: Disables Framing permanently.	
RXPLLPDx	1: Enables CDR PLL in the receiver block. Set to 0 only when the receive block of the channel is not used	1: Enables CDR PLL in the receiver block Set to 0 only when the receive block of the channel is not used	
RXBISTx	1: Receiver BIST function is disabled	1: Receiver BIST function is disabled	
TXBISTx	1: Transmitter BIST function is disabled	1: Transmitter BIST function is disabled	
OE1x	User selectable 0: Disables Serial Output Buffer OUT1x± 1: Enables Serial Output Buffer OUT1x±	User selectable 0: Disables serial output buffer 1: Enables serial output buffer	
OE2x	User selectable 0: Disables Serial Output Buffer OUT2x± 1: Enables Serial Output Buffer OUT2x±	User selectable 0: Disables serial output buffer OUT2x± 1: Enables serial output buffer OUT2x±	
PABRSTx	If TXCLKx± is used as input clock, this latch should be rewritten with a 0 after the completion of device configuration, after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx± input frequency.	If TXCLKx± is used as input clock, this latch should be rewritten with a 0 after the completion of device configuration, after the presence of TXCLKx and after the TXPLL has locked to the REFCLKx± input frequency.	

LDTDEN	User selectable HIGH: range controller, Transition density detector and signal level detector are enabled to determine if RXPLL tracks REFCLKx± LOW: Only range controller is used to determine if RXPLL tracks REFCLKx±	User selectable HIGH: range controller, Transition density detector and signal level Detector are enabled to determine if RXPLL tracks REFCLKx± LOW: Only range controller is used to determine if RXPLL tracks REFCLKx±	
ULCx	User selectable LOW: RXCLKx± follows reference clock. Assert this input when there is no serial data present at the serial inputs. HIGH: RXCLKx± follows clock selected by RXCKSELx	User selectable LOW: RXCLKx± follows reference clock. Assert this input when there is no serial data present at the serial inputs. HIGH: RXCLKx± follows clock selected by RXCKSELx	
SPDSELx	LOW. Use strong pull-down resistor (like 100 ohms). Do not provide LVTTL or LVCMOS stimulus.	LOW. Use strong pull-down resistor (like 100 ohms). Do not provide LVTTL or LVCMOS stimulus.	HIGH. Use strong pull-up resistor (like 100 ohms). Do not provide LVTTL or LVCMOS stimulus.
INSELx	User selectable HIGH: IN1x± is selected as input buffer for the associated receive channel LOW: IN2x± is selected as input buffer for the associated receive channel	User selectable HIGH: IN1x± is selected as input buffer for the associated receive channel LOW: IN2x± is selected as input buffer for the associated receive channel	
LPENx	LOW. Setting to HIGH routes the serialized output of the associated channel internally to the Clock and Data Recovery circuit of the same channel.	LOW. Setting to HIGH will route the serialized output of the associated channel internally to the clock and data recovery circuit of the same channel.	

Appendix A

Table 3. Device Control Latch Configuration Table

ADDR	Channel	Type	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Reset Value
0 (0000b)	A	S	RFMODE A[1]	RFMODE A[0]	FRAMCHAR A	DECMODE A	DECBYP A	RXCKSEL A	RXRATE A	GLEN0	10111111
1 (0001b)	A	S	SDASEL2 A[1]	SDASEL2 A[0]	SDASEL1 A[1]	SDASEL1 A[0]	ENCBYP A	TXCKSEL A	TXRATE A	GLEN1	10101101
2 (0010b)	A	D	RFEN A	RXPLLPD A	RXBIST A	TXBIST A	OE2 A	OE1 A	PABRST A	GLEN2	10110011
3 (0011b)	B	S	RFMODE B[1]	RFMODE B[0]	FRAMCHAR B	DECMODE B	DECBYP B	RXCKSEL B	RXRATE B	GLEN3	10111111
4 (0100b)	B	S	SDASEL2 B[1]	SDASEL2 B[0]	SDASEL1 B[1]	SDASEL1 B[0]	ENCBYP B	TXCKSEL B	TXRATE B	GLEN4	10101101
5 (0101b)	B	D	RFEN B	RXPLLPD B	RXBIST B	TXBIST B	OE2 B	OE1 B	PABRST B	GLEN5	10110011
6 (0110b)	C	S	FMODE C[	FMODE C[	FRAMCHAR C	DECMODE C	DECBYPC	XCKSEL (	RXRATE C	GLEN6	10111111
7 (0111b)	C	S	DASEL2C[	DASEL2C[	SDASEL1 C[1]	SDASEL1 C[0]	ENCBYPC	XCKSEL (	TXRATE C	GLEN7	10101101
8 (1000b)	C	D	RFEN C	RXPLLPD (	RXBIST C	TXBIST C	OE2 C	OE1 C	PABRST C	GLEN8	10110011
9 (1001b)	D	S	RFMODE D[1]	RFMODE D[0]	FRAMCHAR D	DECMODE D	DECBYP D	RXCKSEL D	RXRATE D	GLEN9	10111111
10 (1010b)	D	S	SDASEL2 D[1]	SDASEL2 D[0]	SDASEL1 D[1]	SDASEL1 D[0]	ENCBYP D	TXCKSEL D	TXRATE D	GLEN10	10101101
11 (1011b)	D	D	RFEN D	RXPLLPD D	RXBIST D	TXBIST D	OE2 D	OE1 D	PABRST D	GLEN11	10110011
12 (1100b)	GLOBAL	S	RFMODE GL[1]	RFMODE GL[0]	FRAMCHAR GL	DECMODE GL	DECBYP GL	RXCKSEL GL	RXRATE GL	FGLEN 0	N/A
13 (1101b)	GLOBAL	S	SDASEL2 GL[1]	SDASEL2 GL[0]	SDASEL1 GL[1]	SDASEL1 GL[0]	ENCBP GL	TXCKSEL GL	TXRATE GL	FGLEN1	N/A

14 (1110b)	GLOBAL	D	RFEN GL	RXPLLP GL	RXBIST GL	TXBIST GL	OE2 GL	OE1 GL	PABRST GL	FGLEN2	N/A
15 (1111b)	ALL MASK	D	D7	D6	D5	D4	D3	D2	D1	D0	11111111

Document History

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**	1770639	SAAC	11/30/2007	New Spec
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