TLE6389-x – Using the Demo Board

TLE6389-2GV50
TLE6389-3GV50
TLE6389-2GV

DC-DC Buck Converter

Z8F52274261

Application Note

Rev. 1.01, 2015-07-27

Automotive Power

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1 Abstract

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note provides information on using the demo board of the switched mode regulators TLE 6389-2GV50, TLE 6389-3GV50 and TLE 6389-2GV. The reader should be enabled to understand the dimensioning of the components and change them in order to adapt the function for his application needs.

2 Introduction

Selection of appropriate external components as well as the layout of the PCB is a key factor when designing DC-DC applications in automotive environment. The goal is to achieve optimum functionality with minimum output voltage ripple and good EMC performance. This application note gives a proposal for selecting components and recommendations for layout with an example.

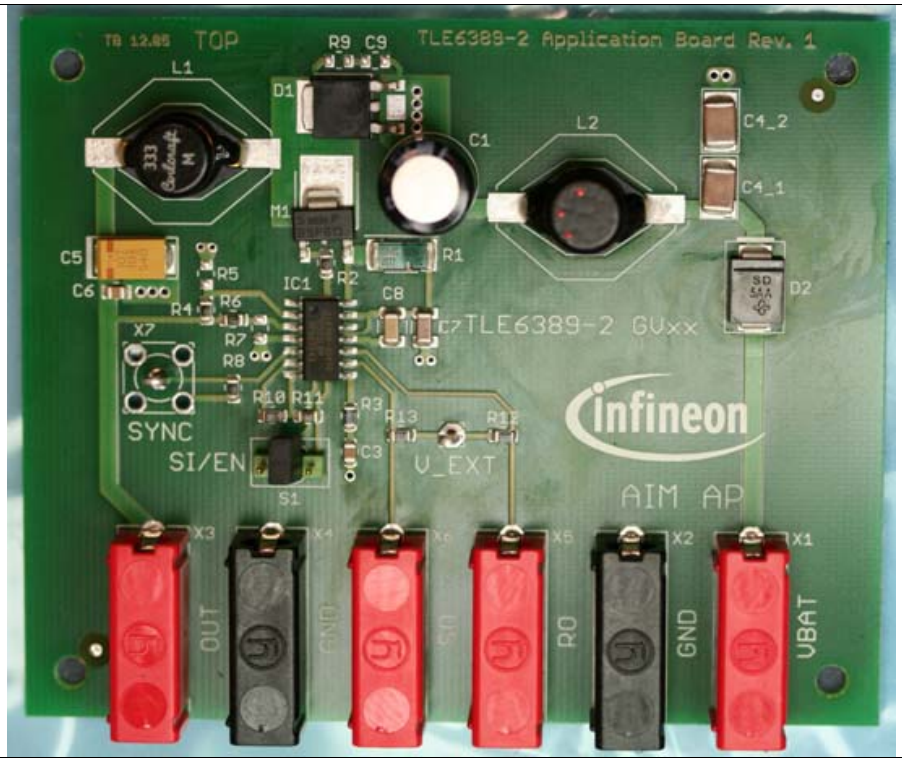

Figure 1 Demo Board with the TLE 63689-2GV50

3 Application Schematic for 5 V Output Versions

Figure 2 shows the minimum application circuit as proposed in the TLE6389 datas heet which applies for to 5 V output versions TLE6389-2GV50 and TLE6389-3GV50.

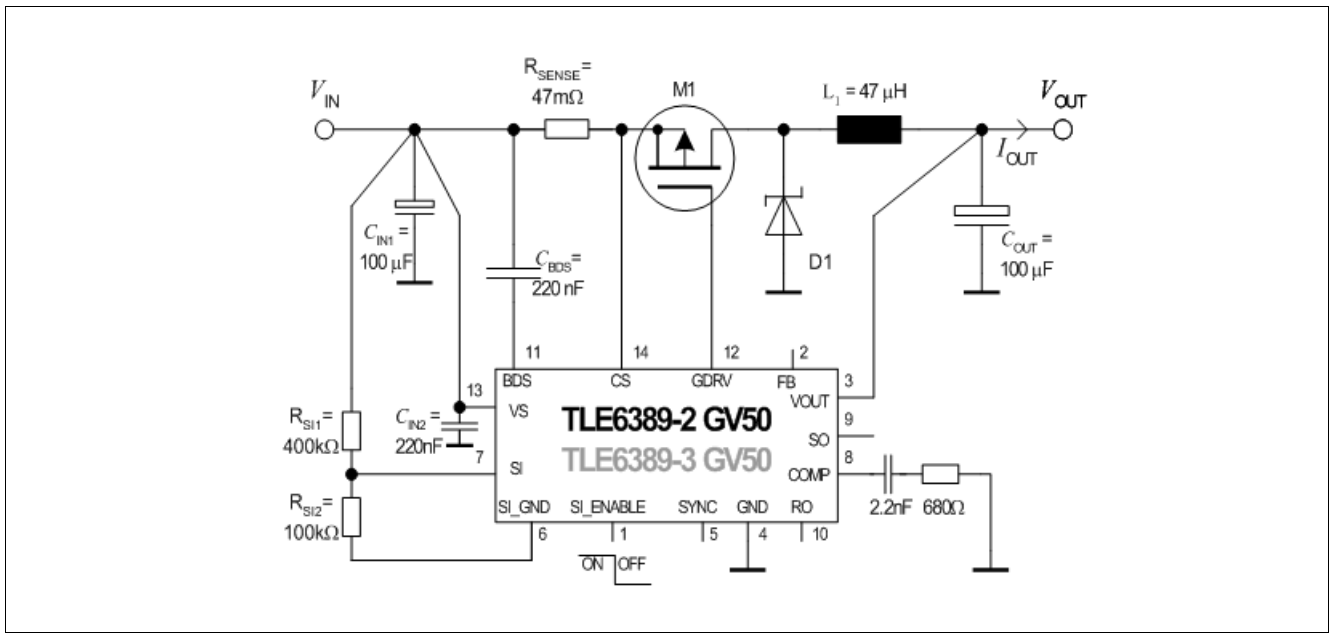

Figure 2 Minimum Application Circuit for TLE6389-2GV50 and TLE6389-3GV50

The circuitry of the demo board is extended slightly. **Figure 3** shows the complete circuitry of the demo board.
The circuitry of the demo board ...

- covers a wider load current range
- improves EMC performance
- allows using only one PCB, also applicable for the variable device TLE6389-2GV (see **Chapter 4**).

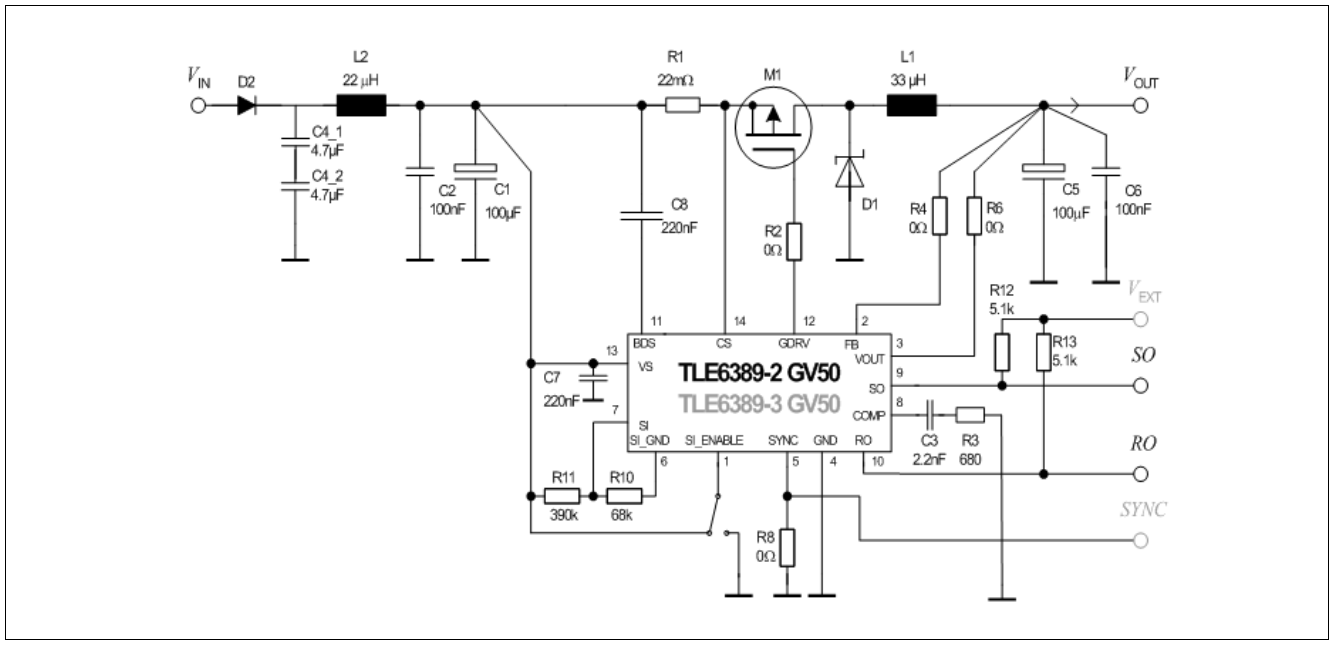

Figure 3 Schematic of the Demo Board for TLE6389-2GV50 and TLE6389-3GV50

Table 1 Recommended Components - BOM for TLE6389-2GV50 and TLE6389-3GV50

Device	Supplier	Type	Value & Remark
L1	Coilcraft	DO-3340P-333	33 µH, 2.0 A, 80 mΩ
L2	Coilcraft	DO-3340P-223	22 µH, 2.5 A, 66 mΩ
C1	Various	Al-Electrolytic capacitor	100 µF, 63 V
C2		Ceramic capacitor	X7R, 100 nF, > 60 V[1)]
C3		Ceramic capacitor	X7R, 2.2 nF, 16 V
C4_1, C4_2	TDK	Ceramic capacitor C4532X7R1H475M	X7R, 4.7 µF, 50 V
C5	EPCOS	Tantalum electrolytic capacitor B45010D1076M506	Low ESR, 'Speed Power'
C6		Ceramic capacitor	X7R, 100 nF, 16 V
C7	TDK	Ceramic capacitor C3216X7R2A224	X7R, 220 nF, 100 V
C8	various	Ceramic capacitor	X7R, 220 nF, 16 V
C9	not assembled		
R1		Resistor	22 mΩ, ±1 %
R2, R4, R6, R8			0 Ω
R3		Resistor	68 0Ω
R5, R7, R9	not assembled		
R10		Resistor	68 Ω
R11		Resistor	390 Ω
R12, R13		Resistor	5.1 Ω
D1	ON	Schottky Diode	MBRD 360, 3 A, 60 V
D2	various	Diode, S3D	3 A
M1		P-channel MOSFET	BSP 613P[2)]

1) Mounted on PCB back side

2) Pin 2 (GND) to be cut before assembly on demo board

3.1 Notes on the 5V Demo Boards

TLE6389-2GV50 and TLE6389-3GV50 have an integrated pull up resistor of typically 20 kΩ at the outputs RO and SO. The integrated pull up resistor connects RO, respectively SO, to the 5 V output voltage present at the VOUT pin. Therefore the resistors R12 and R13 are optional for these devices. On the demo board these resistors are connected to the VEXT connector. The VEXT connector can be left open. In case a reduced pull up resistance is desired, VEXT can be connected externally to VOUT. **VEXT should not be connected to other voltage sources.** The synchronizing function is disabled by the 0ΩΩ resistor R8 connecting pin 5 directly to GND. In case the synchronizing function is needed **make sure R8 is removed before connecting a TTL-Level frequency source to the SYNC connector of the demo board.** On the demo board the feedback input FB is connected via R4 (0 Ω) to the output voltage, whereas the basic circuitry shows an open FB pin. The feedback pin connection is optional for the 5 V devices since the voltage feedback of the error amplifier is connected to the VOUT pin in the TLE6389-2GV50 and TLE6389-3GV50.

4 Application Circuit of the Variable Output Voltage Version

TLE6389-2GV shows the minimum application circuit as proposed in the TLE6389 data sheet for the variable output voltage version TLE6389-2GV.

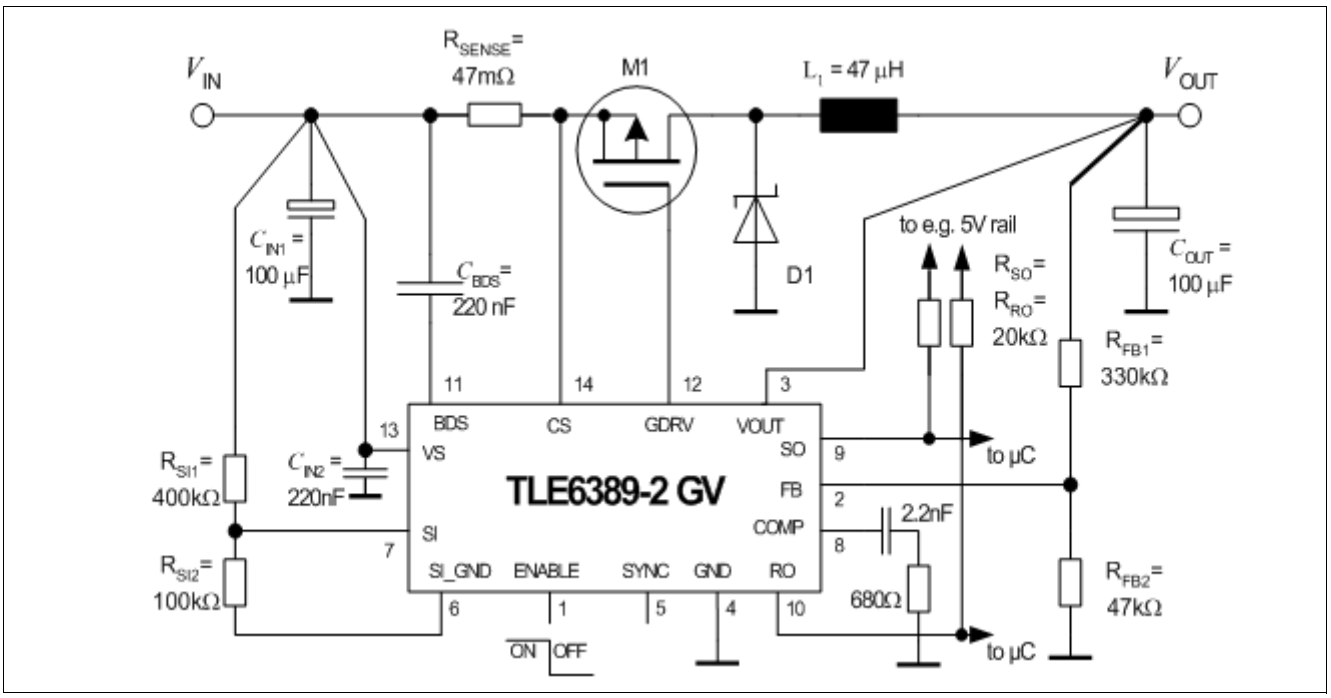

Figure 4 Minimum Application Circuit for TLE6389-2GV

Similar to the fixed 5 V output voltage version, the circuitry of the TLE6389-2GV demo board is extended slightly. Thus a wider load current range and improved EMC performance of the application can be achieved. **Figure 5** shows the schematic of the demo board.

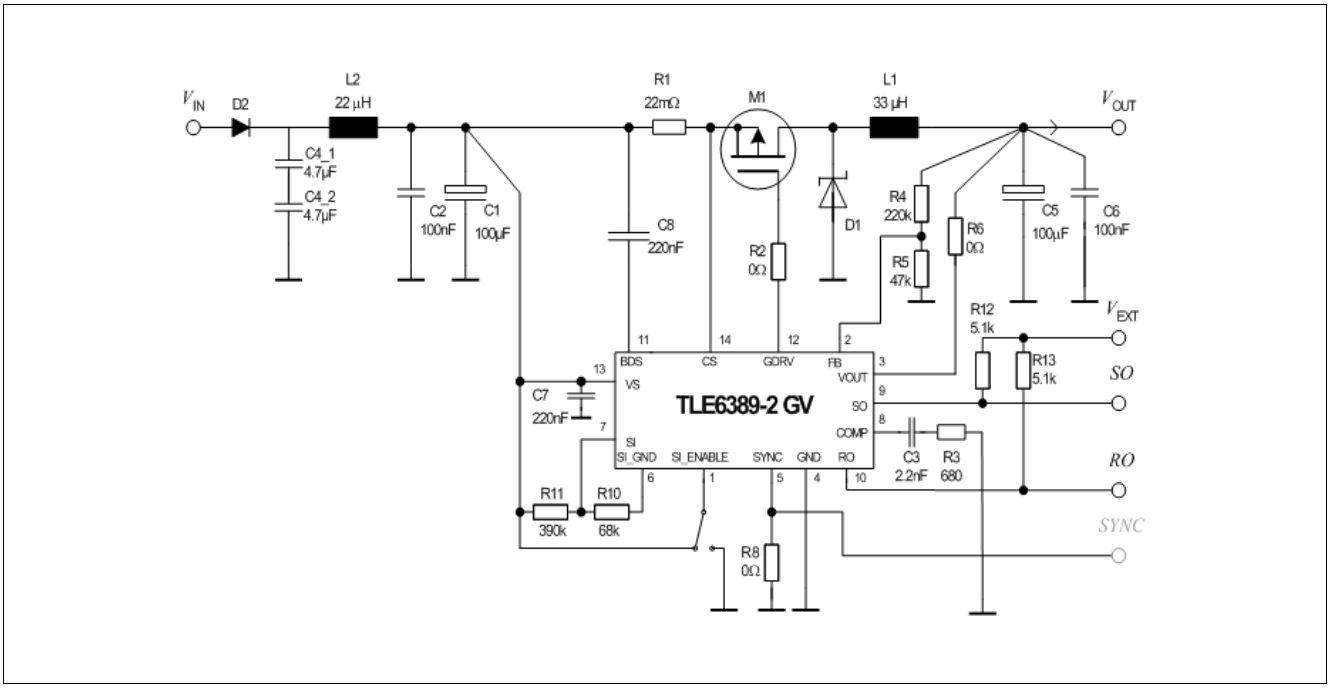

Figure 5 Schematic of the Demo Board for TLE 6389-2GV

Table 2 Components recommendation - BOM for TLE 6389-2GV

Device	Supplier	Type	Value & Remark
L1	Coilcraft	DO-3340P-333	33 µH, 2.0 A, 80 mΩ
L2	Coilcraft	DO-3340P-223	22 µH, 2.5 A, 66 mΩ
C1	Various	Al-Electrolytic capacitor	100 µF, 63 V
C2		Ceramic capacitor	X7R, 100 nF, > 60 V[1)]
C3		Ceramic capacitor	X7R, 2.2 nF, 16 V
C4_1, C4_2	TDK	Ceramic capacitor C4532X7R1H475M	X7R, 4.7 µF, 50 V
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C7	TDK	Ceramic capacitor C3216X7R2A224	X7R, 220 nF, 100 V
C8	various	Ceramic capacitor	X7R, 220 nF, 16 V
C9	not assembled		
R1		Resistor	22 mΩ, ±1 %
R2, R4, R6, R8			0 Ω
R3		Resistor	680 Ω
R5, R7, R9	not assembled		
R10		Resistor	68 Ω
R11		Resistor	390 Ω
R12, R13		Resistor	5. 1Ω
D1	ON	Schottky Diode	MBRD 360, 3 A, 60 V
D2	various	Diode, S3D	3 A
M1		P-channel MOSFET	BSP 613P[1)]

1) Pin 2 (GND) to be cut before assembly on demo board

4.1 Notes on the Variable Voltage Demo Board

The TLE6389-2GV has open drain outputs at the pins RO and SO. The pull up resistors R12 and R13 on the demo board are connected to the V_EXT pad. V_EXT should be connected to an appropriate pull up voltage source (usually the microcontroller I/O voltage source). The pull up resistors have a value of R11 = R12 = 5.1 kΩ. This resistor value should be checked in respect to the actual I/O voltage and microcontroller requirements. The driving capability of the reset output and sense output are described in the data sheet (electrical characteristics, items 4.52, 4.53, 4.69 and 4.70).

The synchronizing function is disabled by the 0 Ω resistor R8 connecting pin 5 directly to GND. In case the synchronizing function is needed, **make sure R8 is removed before connecting a TTL frequency source to the SYNC connector of the demo board.**

5 Dimensioning of the external components

The equations for dimensioning of the external components L1, R1 are given in the data sheet in chapter 7. Data sheet, chapter 7 also discusses the dimensioning of the feedback divider resistors R4 and R5.

This Application Note shows a practical approach on how to apply these equations for given application requirements.

5.1 5 V-Versions

The maximum operating supply voltage at VBAT connector of the application board should be up to 58 V. Therefore all components connected to VBAT have to withstand 60 V, leaving some room for voltage ripple caused by switching: C1, C4 (sum of rated voltage C4_1 +C4_2), C7, M1, D1.

In the first step the right value of the current sensing shunt resistor R1 is determined. The application board is designed to supply a permanent output current of up to 2.0 A at 13.5 V input voltage with a target current of 1.0 A. The (worst case = lowest) maximum current of 2.0 A is allowed to be in the foldback range of the output current characteristic (see Fig. 5).

The data sheet, chapter 7.10.2 delivers the equation:

$$R1 = \frac{V_{LIM}}{2 \times I_{Peak,PWM}} \tag{5.1}$$

V_{LIM} is specified in the electrical characteristics as item 4.36 ‘peak current limit threshold voltage’, 50 mV …. 90 mV. To get the worst case (lowest) current the equation above is used, but without the factor 2, as entering the foldback part of the current characteristic is accepted:

$$R1_{max} = \frac{50\ mV}{2.0\ A} = 25\ m\Omega \tag{5.2}$$

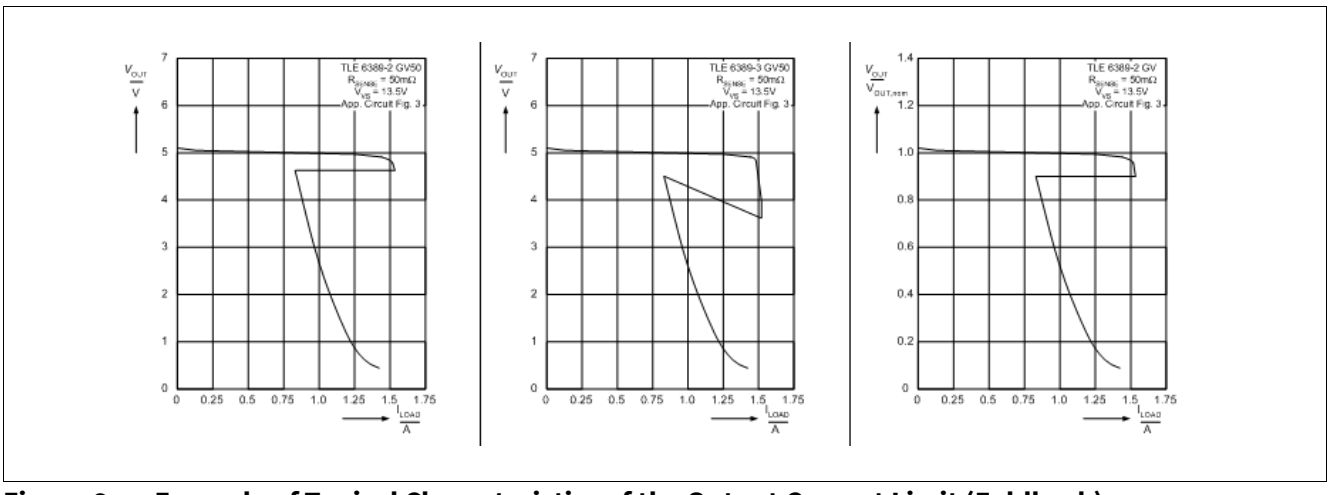

Figure 6 Example of Typical Characteristics of the Output Current Limit (Foldback)

Dimensioning of the external components

The following equation takes into account the current ripple which reduces the maximum load current available:

(5.3)

$$I_{Peak,PWM} = I_{LOAD} + 0.5 \times \Delta I$$

In the next step R1 is selected:

(5.4)

$$R1 = 22\ m\Omega$$

Using this value, the maximum current ripple allowed can be calculated, still assuming a load current of 2.0 A:

(5.5)

$$\Delta I_{max} = \frac{50\ mV/22\ m\Omega - 2.0\ A}{0.5} = 545\ mA$$

In order to keep the output voltage ripple as low as possible, a current ripple of 300 mA in the typical operation condition with 13.5 V VBAT is chosen, corresponding to 15 % of the 2.0 A maximum load current. The data sheet, chapter 7.10.1 delivers the following equation:

(5.6)

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_{SW} \times V_{IN} \times L1}$$

This equation is now used to define the buck inductance L1:

(5.7)

$$L1 = \frac{(13.5\ V - 5.0\ V) \times 5.0\ V}{370\ kHz \times 13.5\ V \times 300\ mA} = 28\ \mu H$$

A matching IEC 60063 E6 value is selected:

(5.8)

$$L1 = 33\ \mu H$$

The following equation serves to check if the stability conditions arising from the slope compensation are fulfilled:

(5.9)

$$\frac{R_{SENSE}}{L1} = 667\ \Omega H^{-1}$$

The result matches the allowed range of 500 Ω/H to 1000 Ω/H (data sheet, chapter 7.10.1).

5.2 Variable Output Voltage

For the TLE6389-2GV variable device demo board we use the same output current target as for the fixed voltage version: 2.0 A, with permission to be in the foldback current limit range (see Fig. 5). The desired output voltage should be typically 7.10 V.

Now the feedback output voltage divider should be fixed. The data sheet (chapter 7.3) allows a range from 5 kΩ to 500 kΩ for R5 (corresponds to RFB2) of 5 kΩ to 500 kΩ. We have selected a value of R5 = 47 kΩ.

R4 can be calculated using the feedback voltage value of 1.25 V (item 4.17 of the electrical characteristics in the data sheet):

(5.10)

$$R4 = 47\ k\Omega \times \left(\frac{7.10\ V}{1.25\ V} - 1\right) = 220\ k\Omega$$

The following procedure is quite the same as for dimensioning the 5 V versions . The shunt resistor is given by the current limitation target.

The data sheet, chapter 7.10.2 provides the following equation:

(5.11)

$$R1 = \frac{V_{LIM}}{2 \times I_{Peak,PWM}}$$

V_{LIM} is specified in the electrical characteristics as item 4.36 ‘peak current limit threshold voltage’, 50 mV …. 90 mV. To get the worst case (lowest) current the equation above is used, but without the factor 2, as entering the foldback part of the current characteristic is accepted:

(5.12)

$$R1_{max} = \frac{50\ mV}{2.0\ A} = 25\ m\Omega$$

The following equation takes into account the current ripple which reduces the maximum load current available:

(5.13)

$$I_{Peak,PWM} = I_{LOAD} + 0.5 \times \Delta I$$

In the next step R1 is selected:

(5.14)

$$R1 = 22\ m\Omega$$

Using this value, the maximum current ripple allowed can be calculated, still assuming a load current of 2.0 A:

(5.15)

$$\Delta I_{max} = \frac{50\ mV/22\ m\Omega - 2.0\ A}{0.5} = 545\ mA$$

Dimensioning of the external components

In order to keep the output voltage ripple as low as possible, a current ripple of 300 mA in the typical operation condition with 13.5 V VBAT is chosen, corresponding to 15 % of the 2.0 A maximum load current. The data sheet, chapter 7.10.1 delivers the following equation:

(5.16)

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_{SW} \times V_{IN} \times L1}$$

This equation is now used to define the buck inductance L1:

(5.17)

$$L1 = \frac{(13.5\,V - 5.0\,V) \times 5.0\,V}{370\,kHz \times 13.5\,V \times 300\,mA} = 28\,\mu H$$

The best matching IEC 60063 E6 value is selected:

(5.18)

$$L1 = 33\,\mu H$$

The following inequation serves to check if the stability conditions arising from the slope compensation are fulfilled:

(5.19)

$$[(2.0 \times 10^{-4}\,\frac{s}{V}) \times V_{OUT} \times R_{SENSE}] < L1 < [(4.0 \times 10^{-4}\,\frac{s}{V}) \times V_{OUT} \times R_{SENSE}]$$

$$[(2.0 \times 10^{-4}\,\frac{s}{V}) \times 7.1\,V \times 22\,m\Omega] < L1 < [(4.0 \times 10^{-4}\,\frac{s}{V}) \times 7.1\,V \times 22\,m\Omega]$$

$$31\,\mu H < L1 < 62\,\mu H$$

Thus, the inductance selected is good for maintaining stability.

6 Components placement and PCB layout

For EMC optimization the demo board comes with an input Π-Filter (C4, L2, C1). Thus emission from the VBAT line is largely suppressed.

For both proper operation and avoiding stray inductance paths, the external catch diode, the Buck inductance and the input capacitor CIN1 have to be connected to the PMOS device as close as possible. Also the path from the GDRV pin of the controller to the switching transistor should be as short as possible. A small area located next to the drain of the PMOS is best suitable for the connection of the catch diode's cathode to one terminal of the inductance.

The GND connection of the catch diode also must be as short as possible. In general the GND level should be implemented as surface area over the whole PCB in a second layer.

The most sensitive points to coupled switching noise are the feedback path to the pins FB and VOUT and the input path. Switching noise coupled back to the SYNC input must be avoided also. These paths should be kept away from the switching node. On the demo board also the ceramic capacitor C6 helps suppress potential noise on the feedback line.

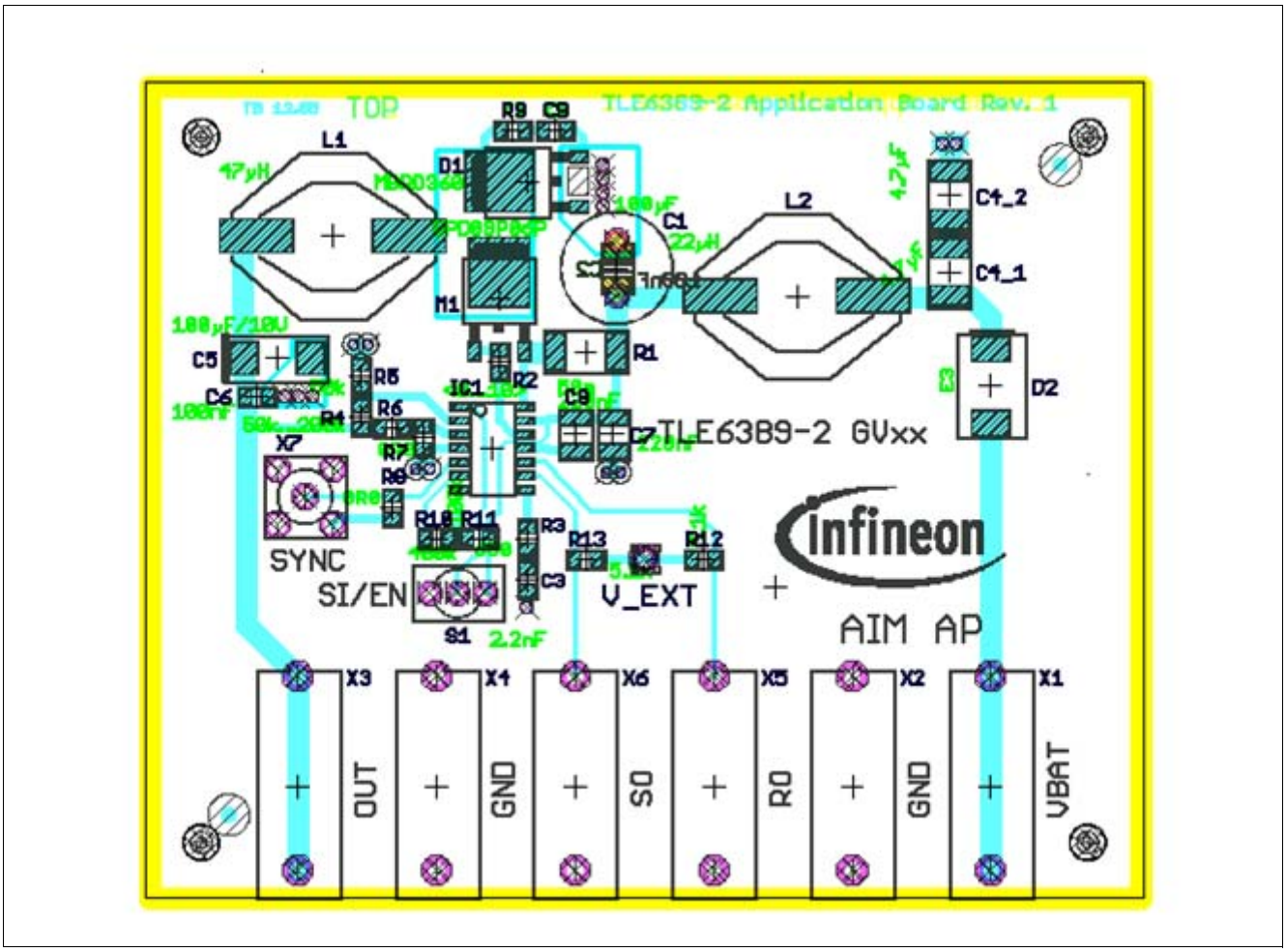

Figure 7 PCB Layout

7 Layout Recommendations

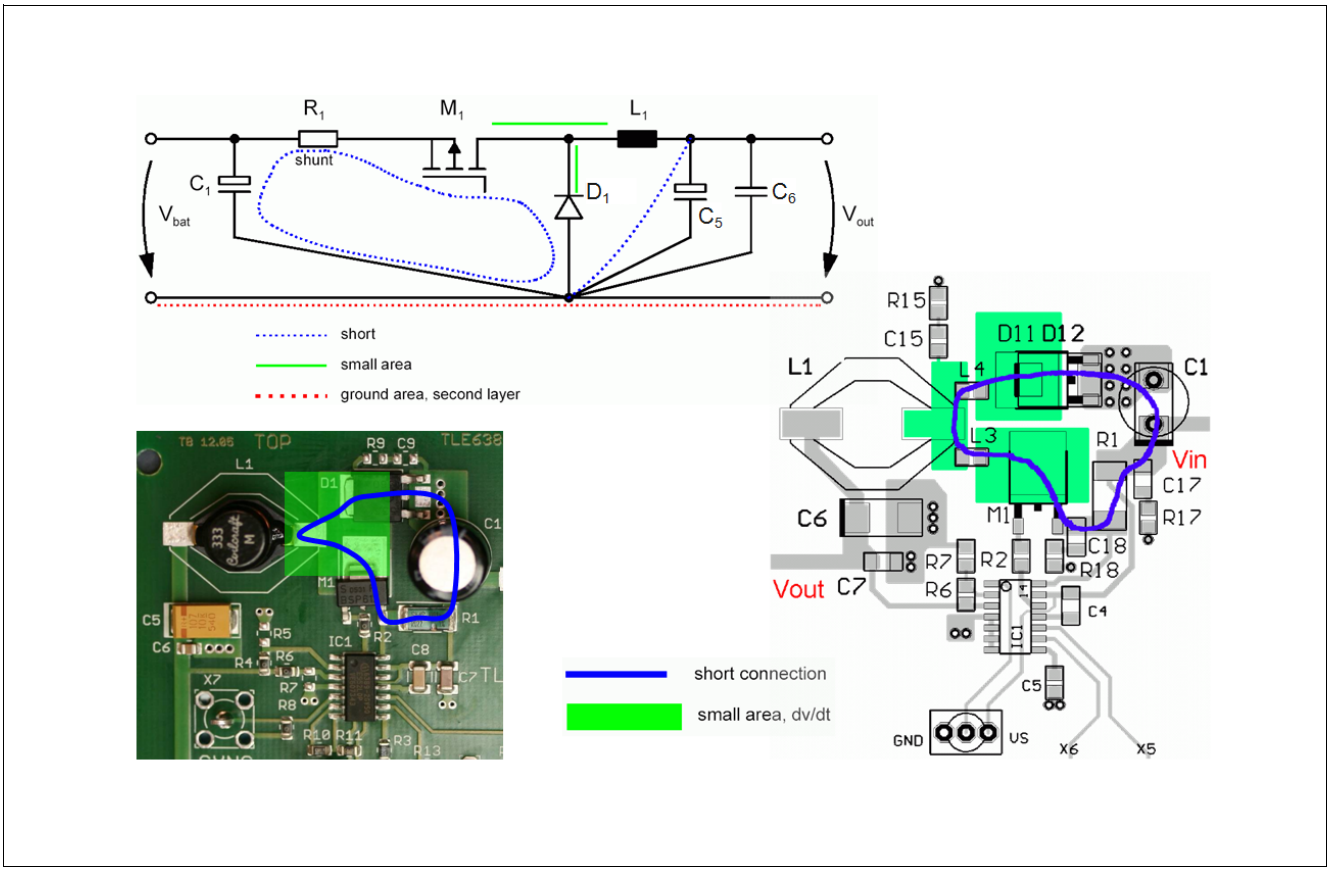

Figure 8 Layout Recommendations

- The commutating circuit input capacitor (C1), PMOS (M1) and free-wheeling diode (D1) shall be as compact as possible for having low inductance.
- The area of the connection M1-L1-D1 (alternating potential) shall be as small as possible.
- Input and Output capacitors shall have a short link for low inductance.
- Forced routing of RF currents: The supply voltage should be routed via the pins of the input capacitors, and the output voltage should be routed via the pins of the output capacitors.
- Design the ground as a ground area in a second layer.
- Directly connect all GND terminals of input caps, D1, output caps, IC RC elements and filter caps.
- Separate ground system, connection to external wiring ground via only one trace.
- Star-shaped design for the ground link to avoid ground looping.
- Connect the current sensing IC terminals (pin 13, 14) directly to the shunt (R1), designed to be short.

Keep the following pins free from any switching noise:

- Pin 8 [COMP]
- Pin 13 [VS]
  - Spikes at VS may influence bandgap reference. → Positive feedback might cause instability
  - Use low ESR input capacitance, additional ceramic C (220 nF ... 1 µF) at VS

Layout Recommendations

- Pin 2 [FB]
  - Keep PCB traces far from switching nodes to prevent from coupled switching noise
  - Use low-ESR output capacitance, additional ceramic recommended
- Pin 2 [VOUT]
  - Use low-ESR output capacitance, additional ceramic recommended
- Pin 5 [SYNC]

8 TLE6389 vs. TLE6389-2 and TLE6389-3

- Functional Change of Pin 8:
  - External Loop Compensation [COMP] instead of Adjustable Reset Delay Time [RD]

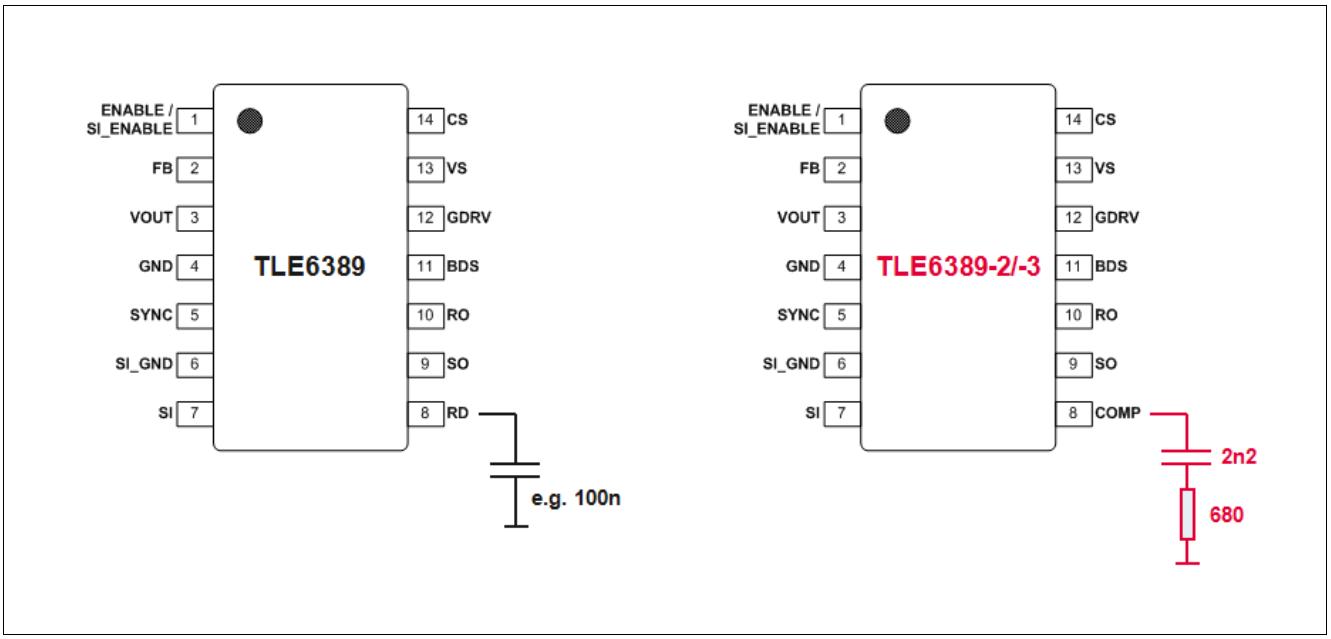

Figure 9 Functional Change of Pin 8

- Problem: PCB not prepared fortwo2 components at pin #8
  - Modifying PCB (recommended)
  - Use 2n2 or 3n3 only (still some loop stability improvement)

9 Foldback Current Limitation

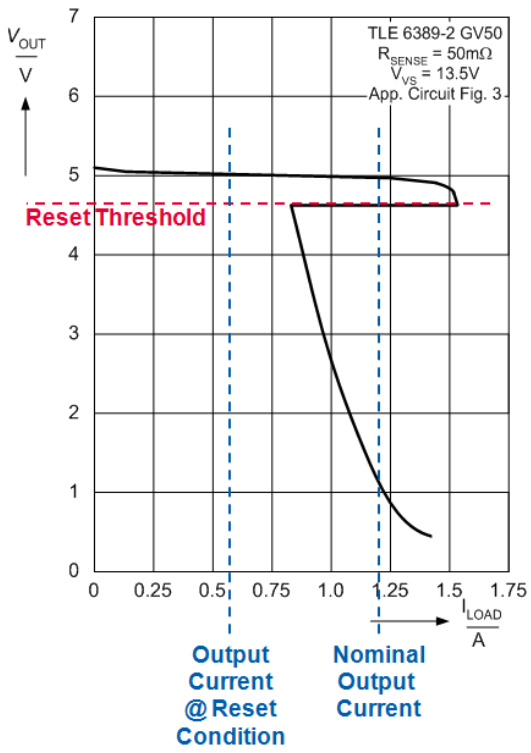

Figure 10 Foldback Current Limitation

- Safe Operation:
  - $I_{MAX} \geq (2 \times I_{NOM}) \rightarrow R_{SENSE} = V_{LIM} / (2 \times I_{Peak,PWM})$
- Assuming that the load current at reset condition is only half of the nominal output current
  - $R_{SENSE} = V_{LIM} / I_{Peak,PWM}$

10 Additional Information

- For further information you may contract **http://www.infineon.com/**

11 Revision History

Revision	Date	Changes
1.01	2015-07-27	Infineon Style Guide update. Editorial changes.
1.0	2006-08-31	Application Note initial revision.

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