

TLE6368 – Overvoltage at the Buck Converter Output

Multi Voltage Processor Power Supply

Z8F52274260

Application Note

Rev. 2.01, 2015-07-09

Automotive Power

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Abstract

1 Abstract

During application tests a certain failure mode may be observed with the TLE6368 – the increase of the Buck converter output voltage up to battery voltage levels resulting in damage of the device. This Application Note is intended to provide some details on the failure mechanisms and show workaround solutions to avoid destruction with proper operation of the TLE6368.

Detailed problem description

2 Detailed problem description

2.1 Relevant TLE6368 operation principle

In order to understand the failure in detail, a brief explanation of the TLE6368's operation principle is necessary. The internal circuit blocks that need to be considered for this failure are the internal biasing and wake up block, the Buck converter control block, the gate driver supply block and the external charge pump block. Internal biasing, e.g. the reference and the logic supply, as well as the step down control block are supplied in the TLE6368 from the battery line directly in order to ensure startup and operation at very low battery voltages. Those biasing and logic blocks are enabled and disabled by the internal wake up block. The wake up block itself has two inputs, the Wake pin and the sleep-bit in the SPI. In order to activate the TLE6368, a signal higher than the wake up threshold has to be applied at the Wake pin. For device shutdown, the appropriate bit in the SPI has to be set by the microcontroller and the Wake signal must be below the wake up threshold. A simple low signal at the Wake pin only will not turn off the device. This means that if the microcontroller is not powered, the TLE6368 cannot be shutdown without disconnecting the battery supply voltage. The gate driver supply is generated under normal operation (except at startup) by the help of the external charge pump circuit, i.e. the bootstrap capacitor providing the charge to enhance the internal DMOS is powered from this external charge pump circuit. The charge pump itself is operating from the Buck output voltage rail, which means it is operating independently from the input voltage. Therefore, once the output of the Buck converter has powered up, the charge pump is operating and able to provide the gate driver supply even if the input voltage had decreased to zero again.

2.2 Buck regulator control failure at bouncing battery

The main simplified blocks of the Buck control loop, which are relevant for this failure are shown below in **Figure 1**. The PWM signal to drive the power DMOS is generated in the current mode control block with inputs "Buck output voltage, FB/L_IN" and "main switch current, ISWITCH". In addition to the control block, there is also a refresh block in order to reset (i.e. turn off) the main switch in case the Buck control loop fails. The refresh signal is generated with a delay of eight clock cycles after a loop failure.

Detailed problem description

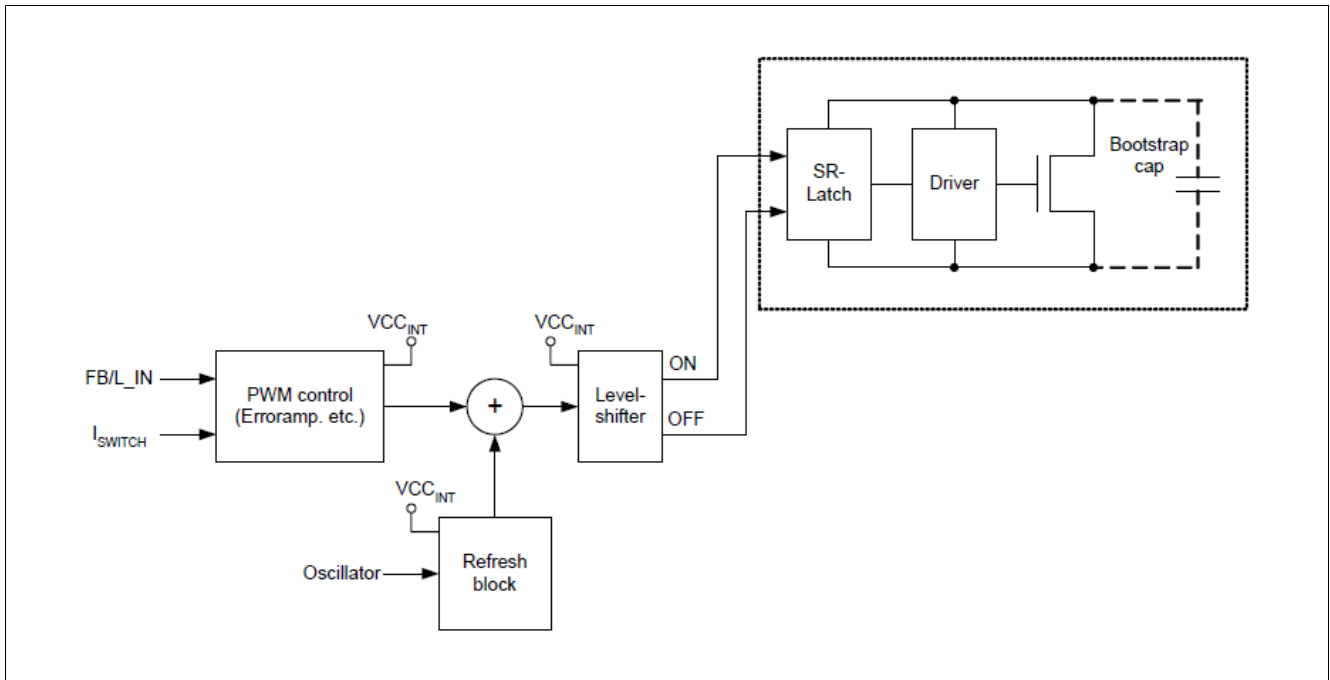


Figure 1 Simplified internal circuit blocks

The level shifter transforms the logic signals generated by the PWM control and the refresh logic to the high side driver block, which includes the latch and the driver for the Power DMOS itself. The high side driver block is moving up and down according to the Bootstrap supply voltage independent from the internal 5 V VCC logic supply voltage which is biasing the PWM and Refresh block. Now if the input voltage collapses, the control loop assumes low battery and sets the latch in the high side driver block, which means the main switch is completely turned on. Even when the voltage at the input is too low to supply the logic blocks PWM and Refresh, the latch is still set and the DMOS is still on (remember that the gate driver supply block is supplied by the bootstrap capacitor and the external charge pump).

If the battery decreases down to zero and remains there, the Buck output voltage would also decrease to a certain level, thus disabling the external charge pump. With the charge pump disabled, the Bootstrap voltage will not be maintained so the main switch will also be turned off. To power the device up again, the battery has to be at minimum 5.5 V and the Wake signal has to be above the wake up threshold. During TLE6368's control loop failure, the scenario is that the input voltage at the device is oscillating, not remaining long enough at the low level in order to allow the Bootstrap capacitor to discharge. The internal logic supply cannot be established immediately with the battery recovery because of internal delays caused by the power up procedure of the internal supply. Due to this fact, the PWM logic and Refresh logic are not supplied, therefore, they cannot send a turn off command to the driver circuitry. The main switch of the Buck converter stays on with 100% duty cycle allowing the Buck output voltage to follow the input voltage. This error condition will continue to occur until the PWM/Refresh logic supply is established. The worst case, i.e. the highest possible output voltage occurs, when the refresh circuit has to reset the power switch. Measurements on ceramic samples have shown delays (or loop "dead times") up to 50µs.

Note: *In applications, the failure of the TLE6368 as described above is most likely to happen only at very low input capacitor configuration. The diagram below shows a typical input configuration of the input line on the TLE6368. At the module input, there's the reverse polarity protection followed by the input Pi-filter with storage capacitors at the input pins of the TLE6368. In the timing diagrams,*

Detailed problem description

voltages with bouncing are shown for various load currents at the battery and at the input of the device. This bouncing could occur, e.g. when plugging a biased connection to the TLE6368.

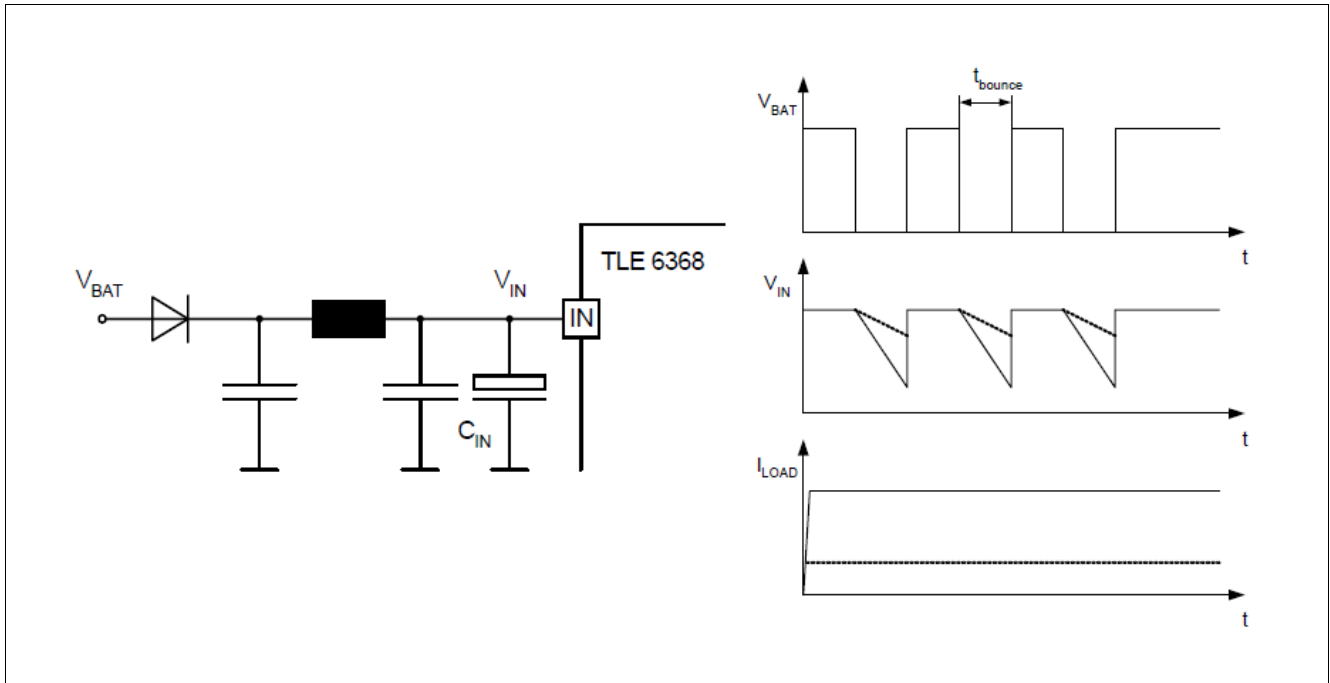


Figure 2 Input configuration and timing

The voltage at the input of the TLE6368 (which acts as the supply line for the internal blocks) can be approximated to:

(2.1)

$$V_{IN} = V_{BAT} - \left(I_{LOAD} \cdot \frac{t_{bounce}}{C_{IN}} \right)$$

As long as the input voltage at the TLE6368 does not decrease below 5 V, the failure described above can never happen because the internal blocks are still supplied. For example, with a battery voltage of 13.5 V, a bouncing time of 300 μs, an input capacitor configuration of 47 μF and a load current at the Buck converter of 1 A, a minimum battery voltage at the input of roughly 7.1 V would be obtained, without a failure of the device. Another component helping to avoid destruction after the control loop’s black out during low battery is the Buck output inductance. Applications using inductors with high saturation currents can overcome the “dead time”. The Buck output cannot follow the input immediately due to the inductance effect, which is still present at high (and increasing) currents. With the control loop taking over again, i.e. turning off the main switch, a non destructive overshoot at the output is recognized. However the choice of the inductor cannot prevent the primary failure, i.e. the control loop’s failure.

2.3 Buck regulator control failure at SPI turn-off command

Another identified mechanism which may cause the Buck regulator output voltage to exceed the maximum ratings can happen when the Boost pin is connected directly to the input (battery line) and an SPI turn off command is sent at hot temperature. As described in the datasheet, the high side power switch consists of two

Detailed problem description

power stages, a low ohmic main power stage and a higher ohmic secondary stage. This two Power DMOS approach was chosen to improve the switching behavior (EME) of the high side stage. Each of the two high side switching blocks contains its own level shifter which receives the signals from the Buck converter control loop to turn on and off the individual power stage. Both high side blocks are supplied from the same high side driver supply, the Bootstrap capacitor. A more detailed block diagram is shown in **Figure 3**. It is recognized that the high ohmic driver block is simpler than the main power stage as the high ohmic power stage was intended to be connected to the Buck output. (Compare to datasheet, application diagram, the Boost pin is connected to the Buck output by a diode configuration.)

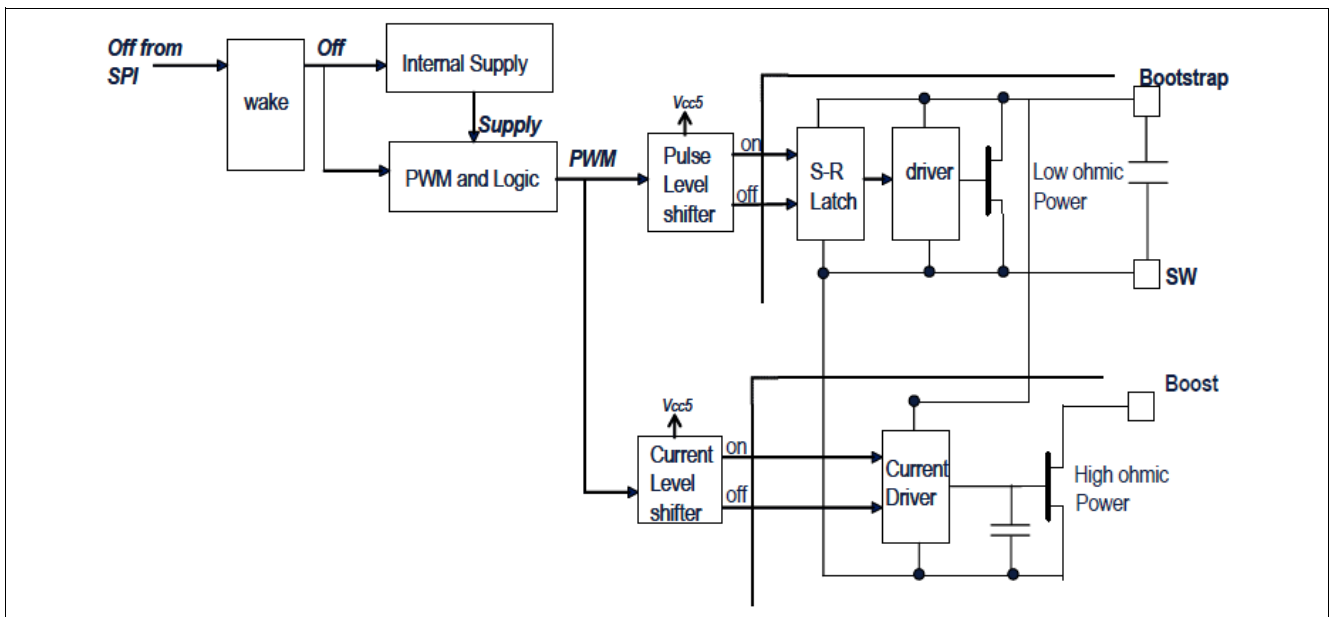


Figure 3 Input configuration and timing

The SPI turn off command disables the internal logic supply Vcc5 as well as it resets the Buck converter control block. As soon as the Buck converter control block receives the turn off command from the SPI, it sends the off command to the level shifters of the two high side switches. Due to signal delay times it can occur that the level shifter of the high ohmic power DMOS receives the turn off command too late, i.e. when its supply voltage Vcc5 had collapsed already. Not being supplied, the high ohmic power stage’s level shifter is not able to transfer the off command to the switch, which means in case the high ohmic power stage was turned on it will not be turned off and the output can reach battery voltage level.

2.4 Buck regulator control failure due to disturbances at the FB input

In applications where the Buck converter output isn’t fed back to the TLE6368 FB/LIN pin exclusively but is used to supply other circuits on the PCB, the Buck converter overvoltage failure mode could potentially be observed. It is recognized that high frequency noise on the FB/LIN pin, e.g. induced by other switching elements on the board, can mislead the internal Buck control loop. The main switch is turned on permanently causing the overshoot at the Buck converter output. Once the Buck converter switch is turned on by noise, the reset / turn off of this main switch is forced only by the refresh block within the Buck control loop (see **Figure 1**). At high input voltage / low buck inductance configured systems the failure mode is more likely to occur, because the refresh cycle is too long to avoid overvoltage at the Buck output. **Chapter 3.3** gives some guidelines for proper layout in order to avoid disturbances at the FB/LIN input of the TLE6368.

Proposed solutions

3 Proposed solutions

3.1 Workaround circuit for bouncing battery

In order to prevent a failure of the Buck converter output voltage, the following workaround circuit is suggested. The main purpose of this circuitry is to discharge the gate driver supply (i.e. the bootstrap capacitor), dependent on the input voltage in order to avoid the voltage overshoot at the output. **Figure 4** shows one possible solution on how to discharge the bootstrap capacitor.

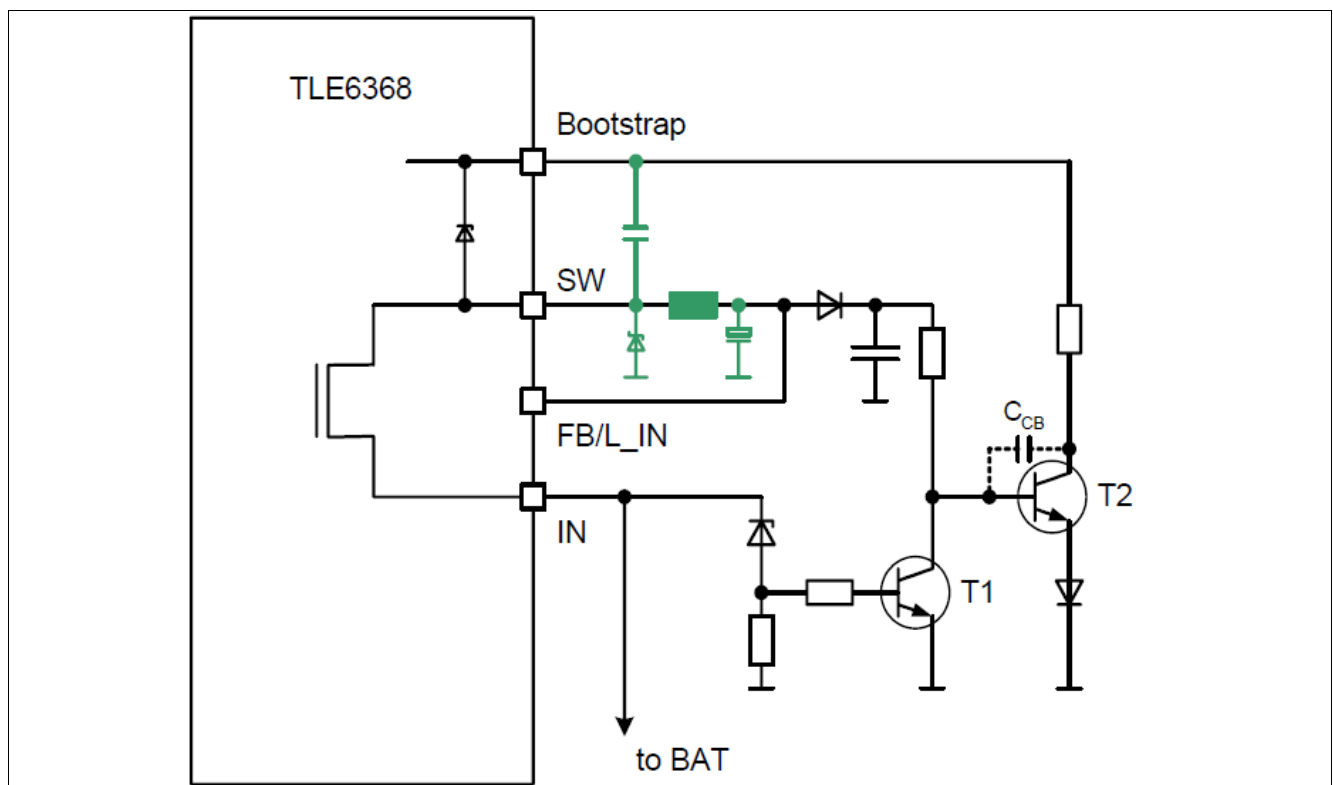


Figure 4 Patch circuit TLE6368

With an undervoltage condition at the input pin (i.e. battery voltage lower than the Zener voltage), the base of T1 is kept low and the base of T2 is set to the Buck converter output voltage level, which enables T2 and discharges the Bootstrap capacitor. In order to discharge the Bootstrap capacitor without destroying the internal ESD protection diode between the Bootstrap and the SW pins (which would cause a permanent short between SW and Bootstrap), if the SW pin is not GND level when discharging, the discharge current has to be limited to 20 mA by a resistor. The maximum voltage at the bootstrap pin to calculate the resistor value is obtained by adding the maximum bootstrap voltage (10.5 V) to the maximum battery voltage. The diode from the emitter of T2 to GND avoids unwanted turning on of T2 (which is the discharge of the bootstrap capacitor) at high temperature when the saturation voltage of T1 is close to the base emitter enable voltage of T2. Care has to be taken when selecting transistor T2 in terms of its parasitic collector base coupling capacitance (marked as CCB in **Figure 4**). As the collector voltage of T2 is increasing and decreasing along with the voltage at the bootstrap pin, the base might be affected through this coupling capacitance to turn on T2. Therefore, low parasitic coupling capacitor values are preferred. The diode at the output of the Buck converter is for decoupling, and the resistor to the base of T2/collector of T1 is for limiting the current through T1 during normal battery operation.

Proposed solutions

3.2 Solution to avoid overshoots at SPI turn-off commands

To overcome the risk that SPI turn off commands may not turn off the high ohmic power stage and cause a voltage overshoot at the Buck output, it is recommended that the Boost pin is left open when its intention of usage was to be connected directly to battery. When the Boost pin is fed from the output by the diode and capacitor configuration as recommended in the datasheet, a disconnection of this pin is not necessary, no overshoot can occur in this case.

3.3 Layout recommendation to avoid noise induced failure

When considering the layout of a Buck converter circuit, some general guidelines have to be taken into consideration. **Figure 5** shows a simplified example of the components used for Buck converter circuits, the input capacitors, the switch, the catch diode, the Buck inductance and the output capacitors.

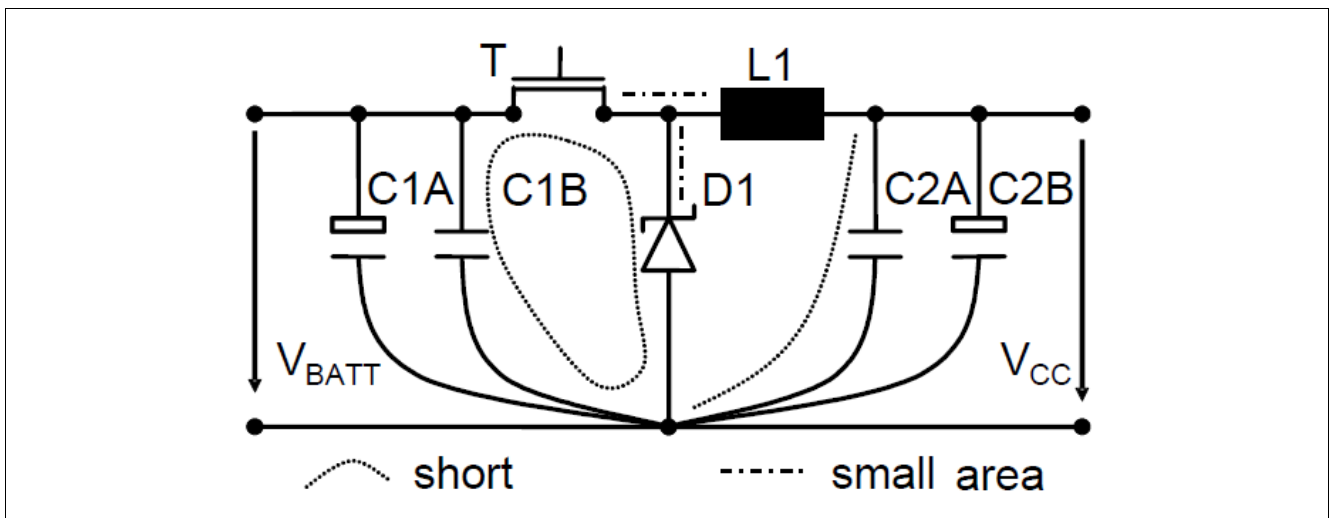


Figure 5 Main components in a Buck converter circuit

Referring to **Figure 5** the following guidelines should be considered:

- The loop containing $C1B$, T and $D1$ where currents with high di/dt occur, should be as small as possible (or as low inductive as possible) to avoid interfering voltages.
- The connection between T , $D1$ and $L1$ where high dv/dt occurs should be as short as possible (or as low capacitive as possible, small area)
- $C1A$, $C1B$, $C2A$ and $C2B$ have to be connected by short lines (low inductive) to be effective in the high frequency range
- To guide high frequency current: The strip lines from V_{BATT} should pass the pins of $C1A$ and $C1B$ before being connected to the switch, the same applies to the output of the Buck inductance for $C2A$ and $C2B$ before reaching V_{CC} .
- The application circuit should have a ground plane below it on the other side of the PCB
- On the top layer, there should be a star type of GND connection which then goes to the GND layer. Connecting input capacitors, output capacitors and the catch diode at one point avoids large high-frequency currents on the GND plane.
- The GND pins of TLE6368's should be connected directly to the GND plane.
- The GND plane below the Buck application circuit should be also "star" connected to the GND connectors of other networks.

Proposed solutions

An example for those recommendations above is given in **Figure 5**. It is recognized that the loop consisting of C1s, T and D1 is as small as possible, also the area connecting T, D1 and L1. The strip lines are guided from battery to C1s - T - D1 - L1 - C2s and finally back to the feedback input of the IC. The bottom side of the PCB is the GND plane.

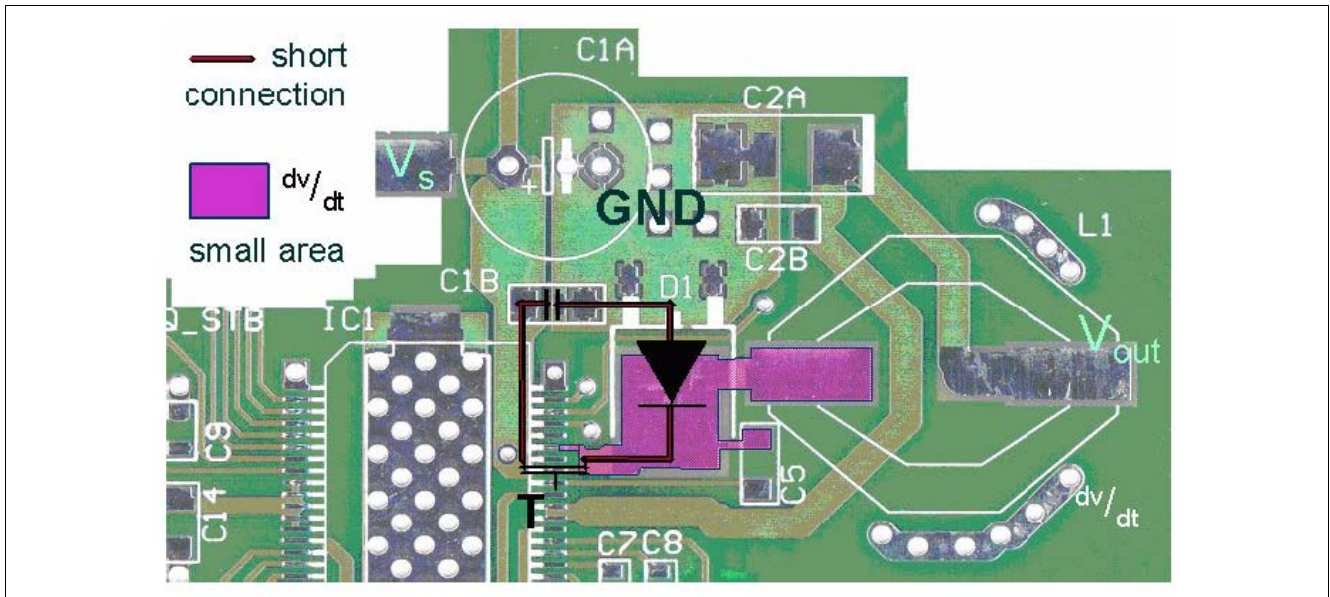


Figure 6 Layout example TLE6368

When feeding additional, potentially noisy, circuitry on the PCB (others than just the FB/ L_IN input of the TLE6368) from the Buck regulator output, it should be avoided to tap off this Buck supply line at the FB/LIN pin. The capacitors located at the Buck converter output would not filter the signals, i.e. noise coming in from this supply line into the FB/ LIN pin. **Figure 7** shows the layout with two examples of connecting additional circuitry. When feeding the additional circuitry close to the control loop feedback input, behind the filter capacitors C2A and C2B, the line to the IC is not filtered. Therefore noise can enter the IC and disturb the system. Tapping off the Buck output rail just at the Buck inductance ensures proper noise filtering of the output capacitors C2A and C2B, the control loop of the IC is not influenced.

Proposed solutions

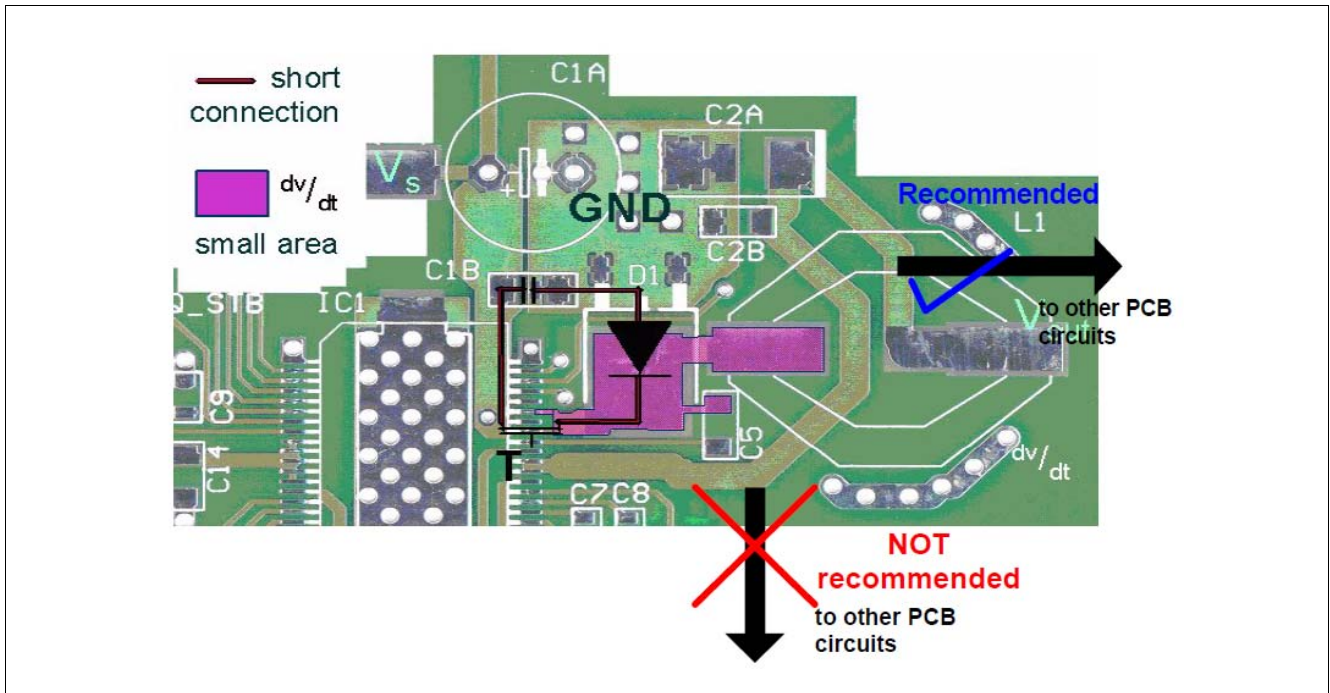


Figure 7 Possibilities of connecting additional circuitry

3.4 Additional patch proposal

The solutions in the previous sections discuss preventive measures which avoid excessive Buck output voltage. However, there is also the possibility to create a patch circuit which reacts (by monitoring the Buck output voltage) on the failure itself. In the case where the Buck output voltage starts to increase to unallowed values, the patch must quickly discharge the Bootstrap capacitor (by shortening the Bootstrap pin to the SW pins, e.g. with a PMOS transistor). Due to undervoltage at the Bootstrap the main switch is then turned off and the Buck output voltage cannot increase further.

Revision History

4 Revision History

Revision	Date	Changes
2.01	2015-07-09	Infineon Style Guide update (EDD41). Editorial changes.

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