

# Overmolded Packages

PG-HBSOF-4 and PG-HB1SOF-4

## Packages PG-HBSOF-4 and PG-HB1SOF-4

Recommendations for Circuit Board Assembly

Application Note

### About this document

#### Scope and purpose

An Application Note providing guidelines for testing and installation of Infineon High Power RF devices in packages PG-HBSOF-4 and PG-HB1SOF-4, including information about selection of appropriate materials and processes.

#### Intended audience

Anyone using Infineon's products in overmolded packages PG-HBSOF-4 and PG-HB1SOF-4.

## Table of Contents

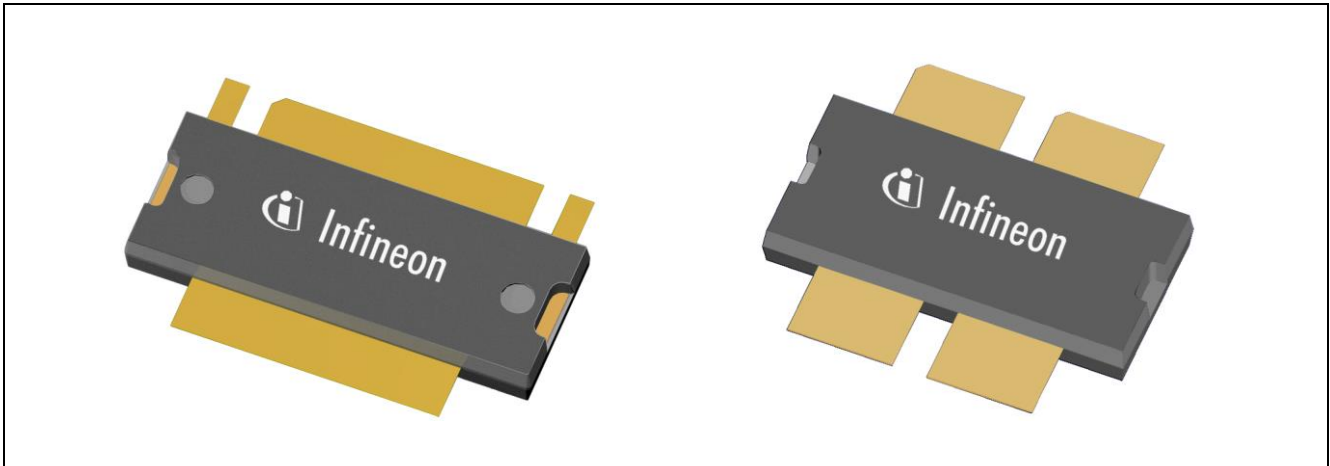
<b>About this document .....</b>	<b>1</b>
<b>Table of Contents .....</b>	<b>2</b>
<b>1 Introduction .....</b>	<b>3</b>
<b>2 Package Description .....</b>	<b>4</b>
<b>3 Package Handling .....</b>	<b>5</b>
3.1 ESD Protective Measures .....	5
3.1.1 Protective Measures in the Workplace .....	5
3.1.2 Equipment for Personnel .....	5
3.1.3 Production Installations, Processing Tools, and Conditions .....	5
3.2 Packing of Components .....	6
3.3 Storage and Transportation Conditions .....	6
3.4 Internet Links to Standards Institutes .....	6
<b>4 Printed Circuit Board (PCB) .....</b>	<b>7</b>
4.1 General Remarks .....	7
4.2 PCB Pad Design .....	7
4.3 Solder Mask Layer .....	8
4.4 Metal Coin, PCB Assembly .....	10
4.5 PCB Pad Finishes .....	11
<b>5 Board Assembly .....</b>	<b>12</b>
5.1 General Remarks .....	12
5.2 Solder Stencil .....	12
5.3 Solder Paste and Preform .....	12
5.4 Component Placement .....	12
5.5 Soldering .....	13
5.5.1 Reflow Process .....	13
5.6 Cleaning .....	15
5.7 Inspection .....	15
5.8 Special notes for inspection of lead-free solder joints: .....	16
<b>6 Rework .....</b>	<b>17</b>
6.1 Tooling .....	17
6.2 Device Removal .....	17
6.3 Site Redressing .....	17
6.4 Reassembly and Reflow .....	18
<b>7 Appendices .....</b>	<b>19</b>
<b>8 Revision History .....</b>	<b>20</b>

## **1 Introduction**

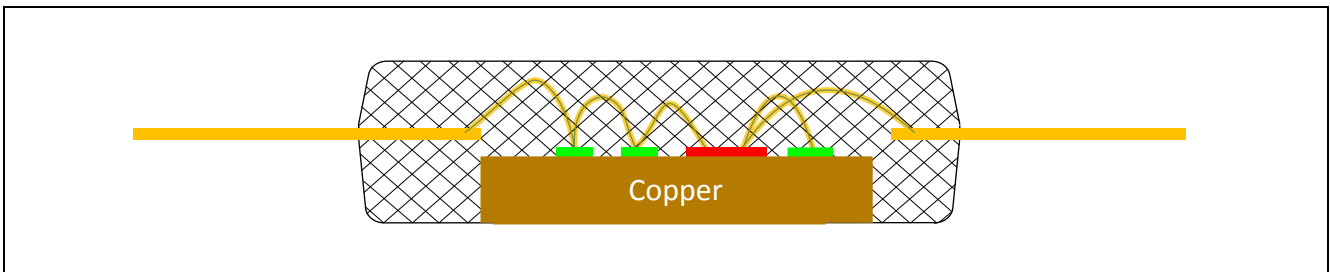
This Application Note will provide guidelines supporting our customers to test and install our devices in their products. It contains information about selecting appropriate materials, and effectively installing our parts for performance and ongoing stability in their builds. Additional studies at the manufacturing site may be necessary for optimization, taking into account the actual printed circuit board, the customer's board assembly equipment, and product-specific requirements.

## 2 Package Description

Infineon's packages PG-HBSOF-4 and PG-HB1SOF-4 are overmolded plastic RF packages with enhanced thermal characteristics. They feature a copper-based flange that serves as a heat sink (**Figure 1**), providing excellent thermal dissipation and electrical conductivity. This heat sink is typically soldered to the printed circuit board to get optimum electrical and thermal performance.



**Figure 1** Packages PG-HBSOF-4 (left) and PG-HB1SOF-4 (right)



**Figure 2** Cross section view of a PG-HBSOF-4 or PG-HB1SOF-4 package

## **3 Package Handling**

### **3.1 ESD Protective Measures**

Semiconductor devices are normally electrostatic-discharge sensitive (ESDS), requiring specific precautionary measures regarding handling and processing. The discharging of electrostatically charged objects near these devices, including those in a PG-HBSOF-4 or PG-HB1SOF-4 package, caused by human touch or by processing tools, may cause high voltage energy transfer, which may damage or even destroy the sensitive semiconductor structures. On the other hand, some devices may themselves become charged during processing. If a discharge takes place too quickly (a “hard” discharge), it may also cause load pulse damages to the device. ESD protective measures must therefore prevent not only contact with other, possibly charged parts, but also the charging of these devices as well. Protective measures against ESD include procedures for handling, processing and packing of ESDS devices. A few hints are provided below on handling and processing.

#### **3.1.1 Protective Measures in the Workplace**

- Standard marking of ESD and non-ESD protected manufacturing and handling areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Earth bonding point for wrist strap
- Trolleys with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields.

#### **3.1.2 Equipment for Personnel**

Along with regular training, the assembly staff should be provided with the following:

- Dissipative/conductive footwear or heel straps
- Suitable smocks
- Wrist strap with safety resistor
- Volume-conductive gloves or finger cots

#### **3.1.3 Production Installations, Processing Tools, and Conditions**

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers for sliding tracks

## Package Handling

- All parts reliably connected to ground potential
- No difference in potential between individual machine and tool parts
- No sources of electrostatic fields

Detailed information on ESD protective measures may be obtained from Infineon's ESD Specialist through Area Sales Offices. These recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

## 3.2 Packing of Components

Infineon packs according to the IEC 60286-\* series. For a list of relevant standards to consider, see Appendix A.

### Other references

EIA-783

Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)

EIA-481-2-A

16 mm, 24 mm, 32 mm, 44 mm & 56 mm Embossed Carrier Taping of Surface Mount Components for Automatic Handling

## 3.3 Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination and package cracking effects. For a list of relevant standards to consider, see Appendix B.

## 3.4 Internet Links to Standards Institutes

[American National Standards Institute \(ANSI\)](#)

[Electronics Industries Alliance \(EIA\)](#)

[Electronic Components Industry Association \(ECIA\)](#) (manages EIA Standards)

[Association Connecting Electronics Industries \(IPC\)](#)

[Electrostatic Discharge \(ESD\) Association](#)

[JEDEC](#)

## 4 Printed Circuit Board (PCB)

### 4.1 General Remarks

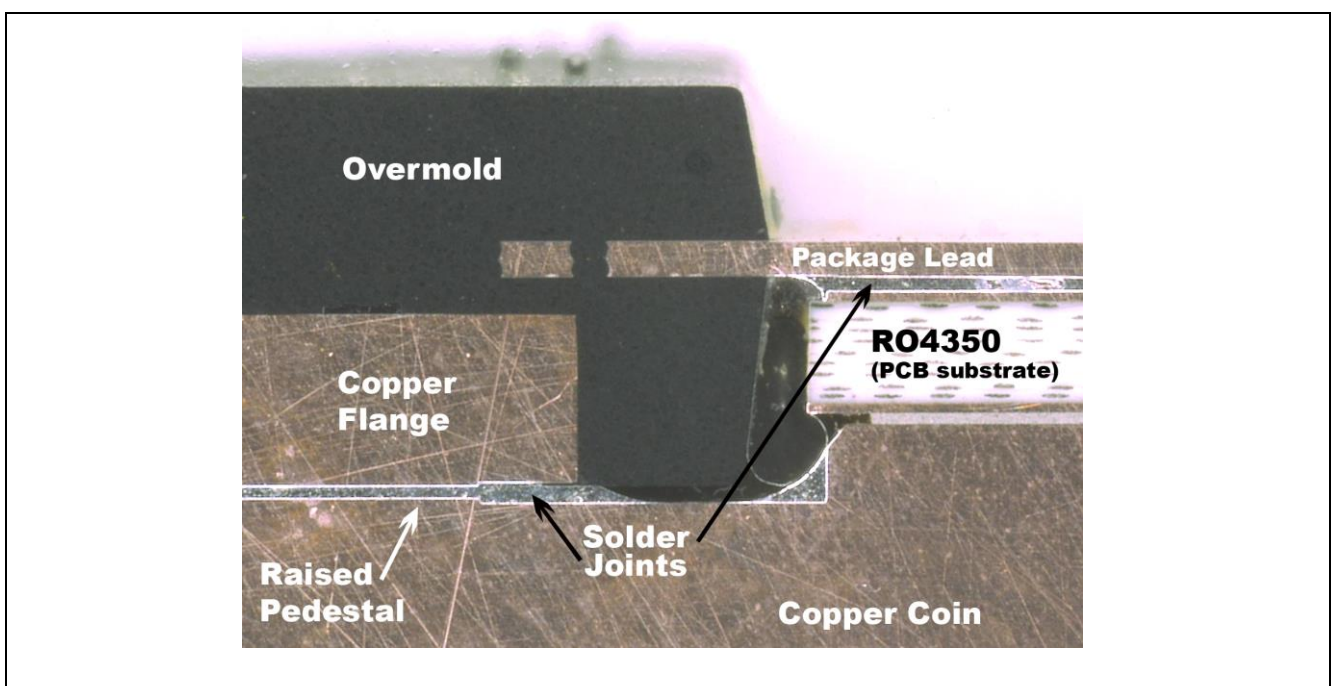
The printed circuit board (PCB) design and construction are key factors in achieving a high board assembly yield and sufficient reliability. For example, the metal coin, PCB pads for the leads, and the board finish should all be considered. In addition, soldering the package's heat sink to the PCB structure is generally recommended for optimum thermal, electrical, and board level reliability and performance, and this should be taken into account.

This Application Note provides guidelines to support our customers' board design. Additional studies by the customer may be necessary for optimization, which must take into account the actual PCB manufacturer's capability, the customer's SMT process, and product-specific requirements.

### 4.2 PCB Pad Design

PG-HBSOF-4 and PG-HB1SOF-4 packages have a copper heat sink (flange). This package heat sink allows direct transfer of large amounts of heat to the heat sink of the PCB; soldering the package heat sink to the heat sink of the PCB (Section 4.4) provides very effective heat removal.

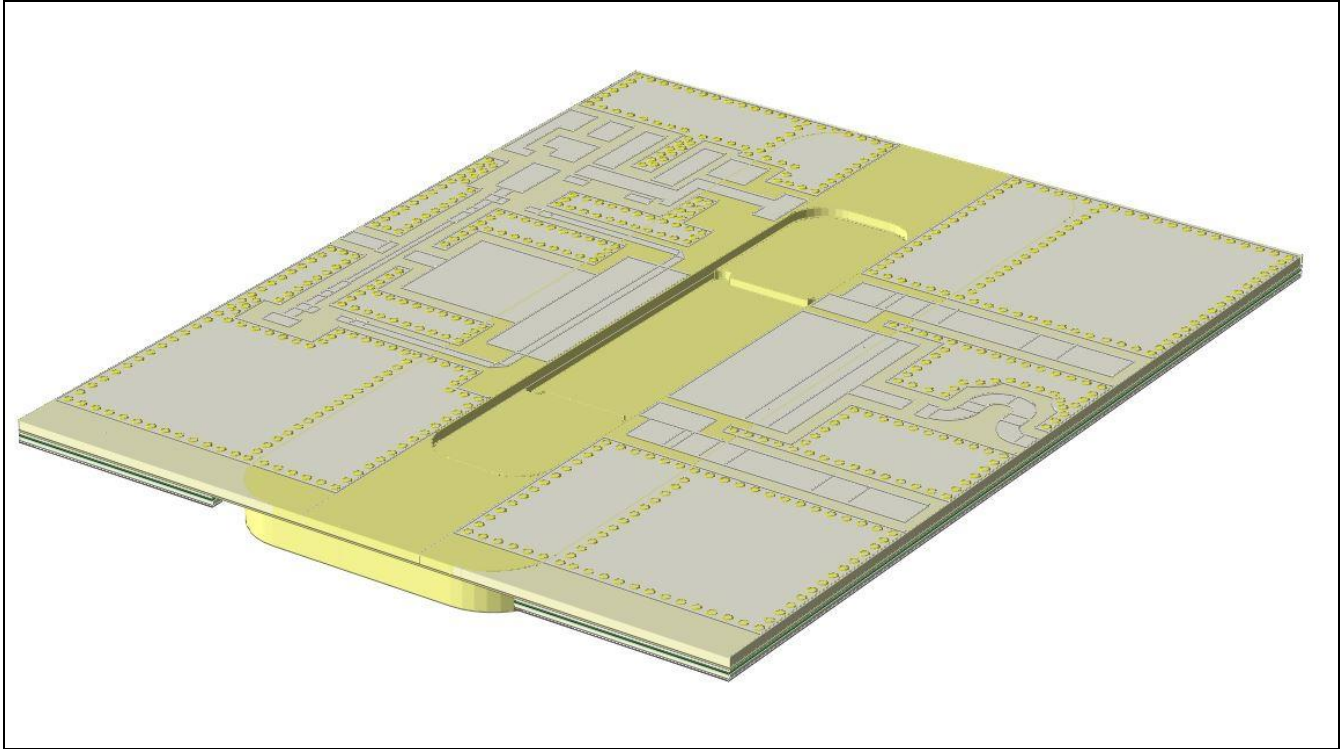
**Figure 2** shows a cross section of solder joints through a lead and the package heat sink. We recommend extending the PCB pad beyond and all around the leads. This extension of the PCB pad can help to develop a solder joint fillet at the side wall of the leads. However this cannot be guaranteed, as this area is not plated. Other influencing factors for fillet formation are package exposure to environment, solder paste material, and reflow process. If fillets are formed, this will additionally be beneficial for solder joint reliability. Also recommended is a low pedestal in the PCB heat sink to coincide with the raised bottom of the flange. This leaves a channel into which excess solder can flow plus ensures better seating.



**Figure 3** Cross section showing solder joints

**Printed Circuit Board (PCB)**

The illustration in **Figure 4** shows a PCB design example which includes perimeter pads and a metal coin heat sink.

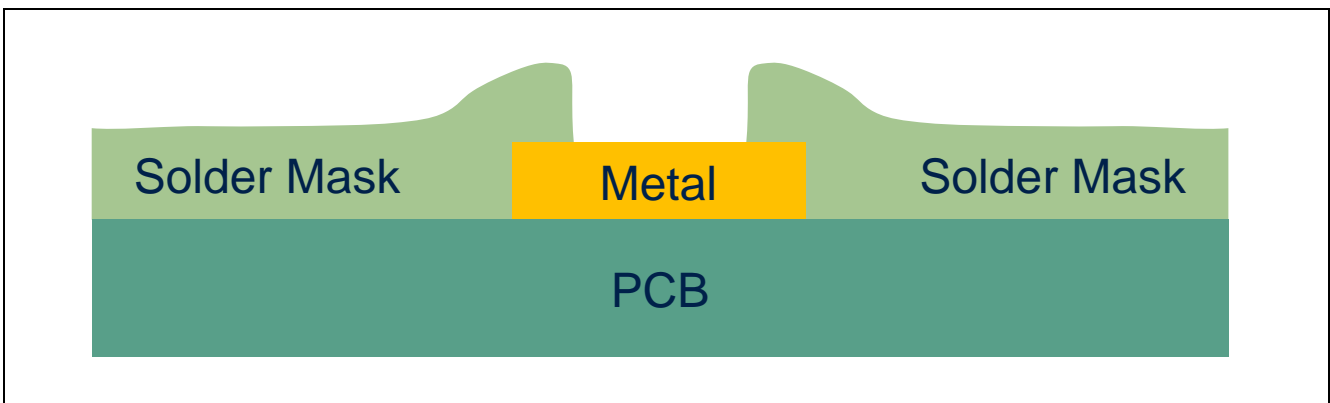


**Figure 4 Example of a PCB design (top view) showing metal coin heat sink placement**

### **4.3 Solder Mask Layer**

Generally, two basic types of solder pads are used: solder mask-defined (SMD) and non-solder mask-defined (NSMD). For this package, NSMD type solder pads for the perimeter are recommended.

- a) Solder mask-defined (SMD) pad (**Figure 5**): The copper metal pad is larger than the solder mask opening above this pad. Thus the pad area is defined by the opening in the solder mask.

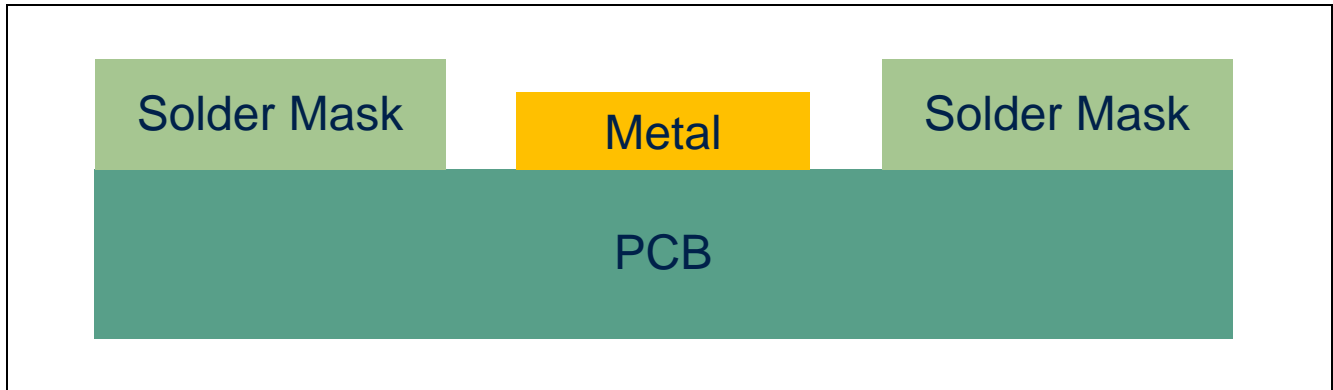


**Figure 5 Solder-mask defined (SMD) pad**



**Printed Circuit Board (PCB)**

b) Non-solder mask–defined (NSMD) pad (**Figure 6**): Around each copper metal pad there is solder mask clearance. Dimensions and tolerances of the solder mask clearance have to be specified in order that no overlapping of the solder pad by the solder mask occurs. The dimensions specified will depend on the PCB manufacturer’s tolerances; 75 µm is a widely used value.



**Figure 6 Non solder-mask defined (NSMD) pad**

#### 4.4 Metal Coin, PCB Assembly

Some products/applications require that a metal “coin” be connected to ground or source layers of the PCB ([Figure 7](#)). One reason for doing so is to maximize the electrical performance, especially for products operating at high frequency. Another reason is to optimize the thermal performance of products having high thermal power dissipation.

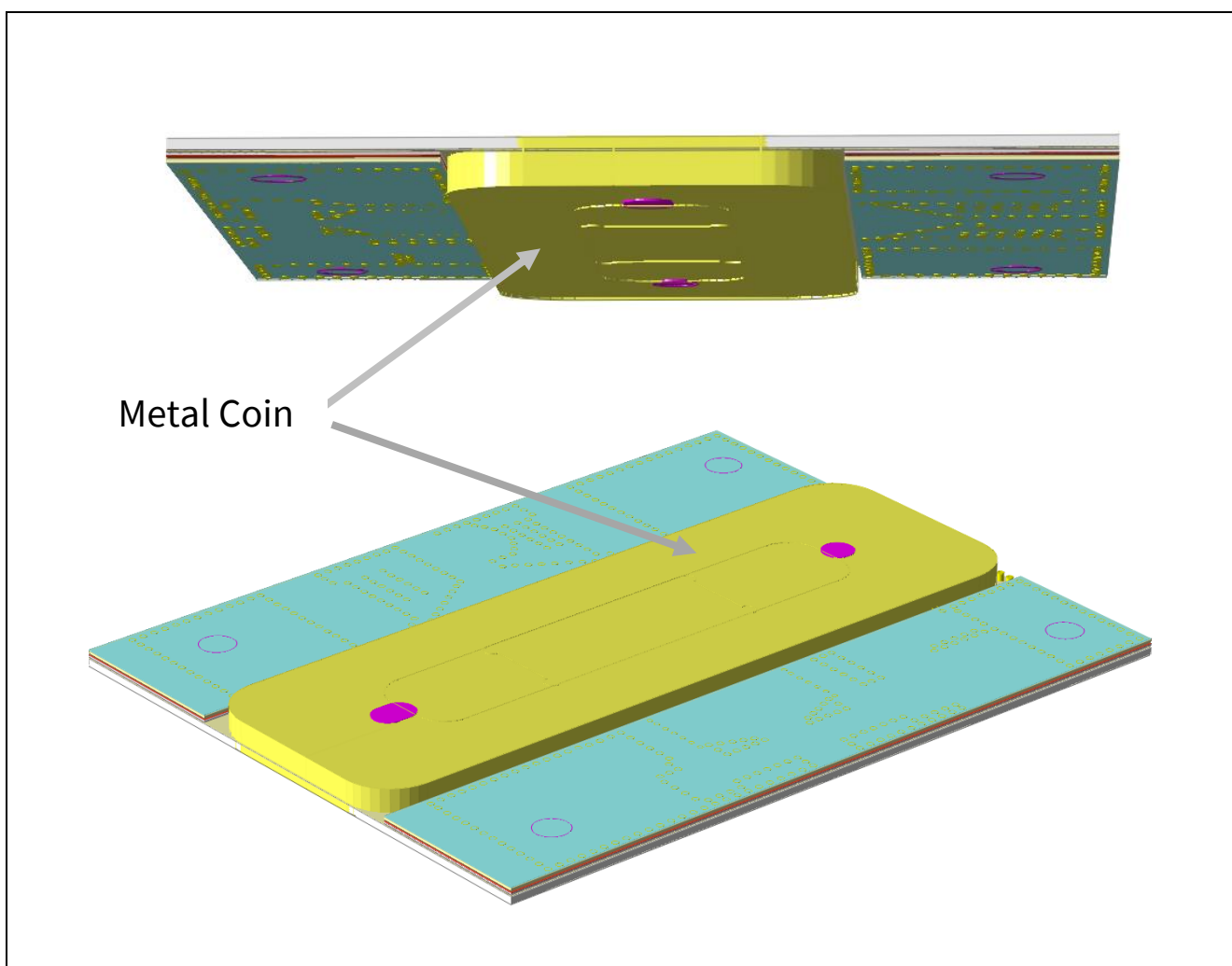


Figure 7 PCB shown with metal coin, two bottom-side views

**Printed Circuit Board (PCB)**

**4.5 PCB Pad Finishes**

The solder pads must be easy for the soldering material (solder paste) to wet. All finishes listed here are well proven for board assembly. In addition, pad flatness must be taken into account in order to achieve a high quality solder joint. The properties of some finishes are listed in [Table 1](#).

**Table 1 Properties of Some Solderability Finishes on PCBs**

<b>Finish</b>	<b>Typ. Layer Thickness [µm]</b>	<b>Properties</b>	<b>Concerns</b>
Hot Air Solder Leveling (SnAg) (HASL)	> 5	cheap, widely used, established know-how in fabrication	uneven surface, formation of humps, flatness of single pads has to be good for fine pitch applications
Electroless Tin	0.3 - 1.2	solder joint consists only of copper and solder; no further metal is added to the solder joint	long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Silver	0.2 - 0.5	solder joint consists only of copper and solder, no further metal is added to the solder joint	long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Ni /Immersion Au (ENIG)	3 - 7 / 0.05 - 0.15	good solderability protection, high shear force values	expensive, concerns about brittle solder joints
Galvanic Ni/Au	> 3 / 0.1 - 2	only for thicker layers, typically used for connectors	expensive
Organic Solderability Preservatives (OSP)	typical 1	cheap, simple, fast and automated fabrication	must be handled carefully to avoid damaging the OSP; not as good long-term stability as other coatings; at double-sided reflow only suitable with inert gas reflow

The question about the best solder pad finish cannot be answered in general terms. It depends strongly on one or more of the following: board design, pad geometry, components on board, and process conditions. In literature, the test results of solderability, wetting force and wetting time for several preservative layers are not always coincident.

## **5 Board Assembly**

### **5.1 General Remarks**

Many factors within the board assembly process have influence on assembly yield and board-level reliability. These may include the design and material of the solder stencil, the solder paste material and printing process, component placement, and the reflow process. The plating finish on PG-HBSOF-4 and PG-HB1SOF-4 packages allows assembly with either SnPb-based or lead-free SnAgCu-based solder paste and reflow processes.

### **5.2 Solder Stencil**

The solder paste is applied onto the PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For PG-HBSOF-4 and PG-HB1SOF-4 packages, the recommendation is to use 100  $\mu\text{m}$  to 150  $\mu\text{m}$  thick stencils. If this does not match with the requirements of the other components' packages on the same PCB, then a step-down stencil should be considered. To ensure a uniform depth and volume of solder paste transfer to the PCB, stencils which are laser-cut and electroformed, usually made from stainless steel or nickel electroformed stencils are preferred. Rounding the corners of the apertures (radius  $\sim 50 \mu\text{m}$ ) can support good paste release.

### **5.3 Solder Paste and Preform**

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux. In term of mass this means approximately 90 wt% alloy and 10 wt% flux system. One of the functions of the flux system is to remove the contaminations from the solder joints during the soldering process. The capability of removing contaminations is given by the respective activation level. A lead-based solder paste metal alloy has to be of leaded eutectic or near-eutectic composition (SnPb or SnPbAg). A lead-free solder paste metal alloy composition (typically SnAgCu with Ag 3 – 4%, Cu 0.5 – 1%) can also be applied. A “no-clean” solder paste is preferred, because cleaning under the soldered package may be difficult. The paste must be of suitable consistency for printing the solder stencil aperture dimensions. Solder paste is sensitive to storage time, temperature and humidity. Please notice the handling recommendations of the paste manufacturer.

Solder preform is used under the heat sink of the package as it is not possible to screen print solder paste into a cavity. Thickness of the preform is determined by the solder paste thickness of the perimeter leads and the cavity depth of the metal coin with respect to the seating plane height of the package.

### **5.4 Component Placement**

PG-HBSOF-4 and PG-HB1SOF-4 packages have to be placed accurately according to their geometry. Positioning the packages manually is not recommended.

Component placement accuracies of  $\pm 50 \mu\text{m}$  can be obtained with modern automatic component placement machines using vision systems. With these systems both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or additionally on individual

### Board Assembly

mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling correct placement.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB for non-solder-mask defined pads. As a consequence, for PG-HBSOF-4 and PG-HB1SOF-4 packages, the device-pad-to-PCB-pad misalignment has to be less than 50 µm in order to assure a robust mounting process. Generally this is achievable with a wide range of placement systems.

The following remarks are important to consider:

- Especially on large boards, local fiducials close to the device can compensate for the larger PCB tolerances.
- It is recommended to use the lead recognition capabilities of the placement system, not the outline for part centering.
- To ensure the identification of the packages by the vision system, adequate lighting as well as the correct choice of measuring mode is necessary. The optimal settings can be determined from the equipment manuals.
- Too much placement force can lead to squeeze out of solder paste, which can cause solder-joint shorts. On the other hand too little placement force can lead to insufficient contact between package and solder paste, which can lead to open solder joints or badly centered packages.

## 5.5 Soldering

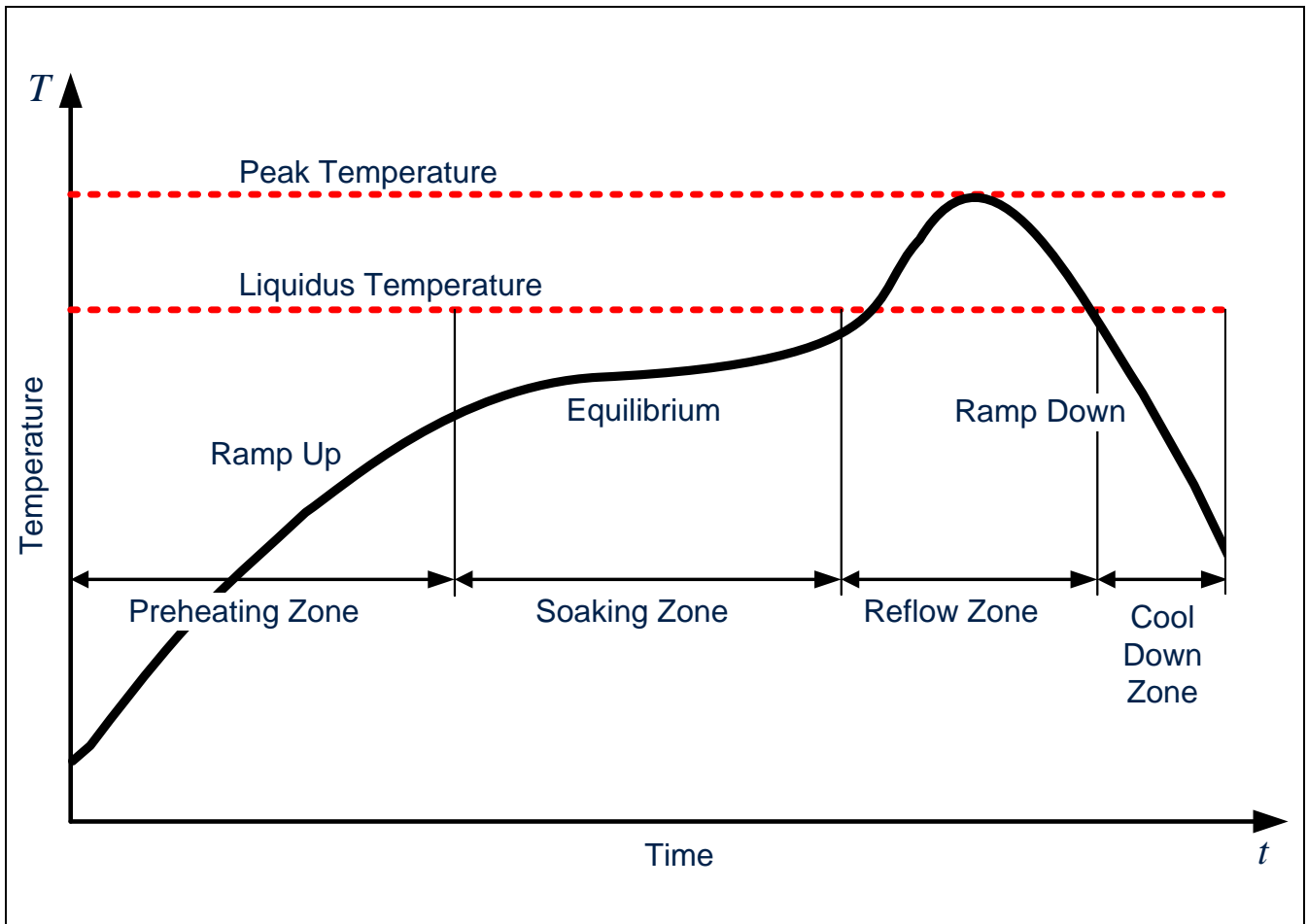
Soldering determines the yield and quality of board fabrication to a very large extent. Generally all standard reflow soldering processes—including forced convection, vapor phase, and infrared (with restrictions)—and typical temperature profiles are suitable for board assembly with the PG-HBSOF-4 and PG-HB1SOF-4 package. Wave soldering is not possible.

### 5.5.1 Reflow Process

At the reflow process each solder joint has to be exposed to temperatures above solder liquidus for a sufficient time in order to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the component's packing for the peak package body temperature. It is important that the maximum temperature of the PG-HBSOF-4 and PG-HB1SOF-4 package during the reflow does not exceed the specified peak temperature.

When using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints of the assembly, especially on large, complex boards using components with differing thermal masses. Products using PG-HBSOF-4 and PG-HB1SOF-4 packages may be used on boards of this type. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering tin-lead metal alloys. For the lead-free process with higher reflow temperatures, nitrogen atmosphere may reduce oxidation and improve the solder joint quality.

The temperature profile of a reflow process is one of the most important factors in the soldering process. This profile can be divided into several phases, each with a special function. **Figure 8** shows a typical forced air convection reflow temperature profile for soldering PG-HBSOF-4 and PG-HB1SOF-4 packages.



**Figure 8 Typical forced-air convection solder reflow temperature profile**

**Table 2** shows an example of possible parameter values which could be used to create solder profiles either for tin-lead or for lead-free alloys. Each parameter is influenced not only by the package, but also by various other factors. It is essential to follow first the solder paste manufacturer’s application notes. In addition, the position and the surroundings of the device on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly.

Most board assemblies incorporate more than one package type and therefore the reflow profile has to be matched to the demands of all components and materials. Considering that components with large thermal masses do not heat up at the same rate as lighter-weight components, developing an effective temperature profile can be expedited by using thermocouples placed beneath the respective components to measure the temperature of the solder joints.

The following table is an example only, to be used for reference purposes, and is not a recommendation.

**Table 2 Example of key parameters describing a forced-air convection solder reflow profile**

Parameter	Minimum value	Typical value	Max value (acc. JEDEC J-STD-020)	Main influence
Preheating rate	1.0 K/s	2.5 K/s	3.0 K/s	Flux system (solder paste)
Soaking temperature	140 – 170°C	140 – 170°C	150 – 200°C	Flux system (solder paste)
Soaking time	50 s	80 s	120 s	Flux system (solder paste)
Peak temperature	230°C	245°C	260°C	Alloy (solder paste)
Reflow time above melting point (liquidus)	40 s	60 s	150 s	Alloy (solder paste)
Cool down rate	1.0 K/s	2.5 K/s	8.0 K/s	

## 5.6 Cleaning

After the reflow soldering process some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. Be aware that cleaning beneath a PG-HBSOF-4 or a PG-HB1SOF-4 package is difficult because of the small gap between package and PCB, and is therefore not recommended. However if the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution have to be selected with consideration given to the packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and environmental and safety aspects. Removing or drying of even small residues of the cleaning solution itself should also be done very thoroughly. Contact the solder paste manufacturer for recommended cleaning solutions.

## 5.7 Inspection

A visual inspection of the solder joints with conventional automatic optical inspection (AOI) systems is limited to the outer surface of the solder joints. Since the non-wetting of the package lead side walls is not a reject criterion (**Figure 9**), the significance of an optical inspection is questionable.

Cross sectioning (**Figure 10**) or dye penetrant analysis of a soldered package can serve as tools for sample monitoring only, because of their destructive character. Scanning Acoustic Microscopy (SAM), however, is a quick, less-destructive analysis technique. Also, CSAM can be a more-effective tool for finding voids.





Figure 9 Non-wetting of the lead side walls is not a reject criterion

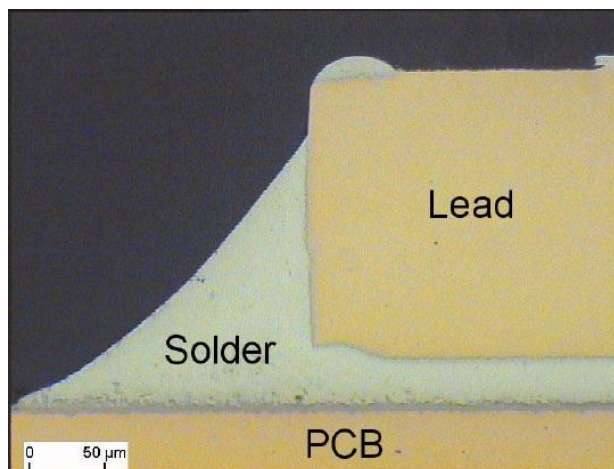


Figure 10 Cross section of a perimeter lead solder joint

## 5.8 Special notes for inspection of lead-free solder joints:

Lead-free solder joints look different than tin-lead (SnPb) solder joints. Tin-lead joints have typically a bright and shiny surface; lead-free (SnAgCu) solder joints typically do not have this bright surface. Lead-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder, as the solder alloys used are not exactly eutectic (as is the 63Sn37Pb solder alloy). This means that SnAgCu solders do not have a melting point but rather a melting range of several degrees. Although lead-free solder joints have this dull surface, this does not mean that lead-free joints are of lower quality or weaker than the SnPb joints. It is therefore necessary either to instruct the inspection staff how these lead-free joints will look and the difference between the two, or to adjust optical inspection systems, if used, to identify and evaluate lead-free solder joints.



## 6 Rework

If a defective component is observed after board assembly, a PG-HBSOF-4 or PG-HB1SOF-4 package can be removed and replaced with a new one.

### 6.1 Tooling

The rework process is commonly done on special rework equipment. There are many such systems available on the market; for processing these packages the equipment should fulfill the following requirements:

- Heating: Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With easily programmable temperature profiles (e.g. by PC controller) it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from underside is recommended. Infrared heating can be applied, especially for preheating the PCB from underside, but it should be only in addition to the hot air flow from the upside. Instead of air, nitrogen can also be used.
- Vision system: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB a split optic should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- Moving and additional tools: Tooling should be able to reach the entire PCB area. Placement accuracy is recommended to be better than  $\pm 100 \mu\text{m}$ . The system should have the capability of removing solder residues from PCB pads (special vacuum tools).

### 6.2 Device Removal

If a defective component is to be sent back to the supplier, further defects must not be introduced into the device during the removal process as this may hinder the failure analysis by the supplier. The following points should be observed when removing components:

- Temperature profile: During the soldering process, ensure that the package peak temperature is not higher than, and temperature ramps are not steeper than, those during the standard assembly reflow process (Section 5.5).
- Mechanics: Be aware not to apply high mechanical forces for removal. Otherwise failure analysis of the package may become impossible or the PCB can be damaged. For large packages, pipettes can be used. Pipettes are usually implemented on most rework systems.

### 6.3 Site Redressing

After removing the defective component, any solder residues have to be cleaned from the pads on the PCB.

Do not use steel brushes because steel residues can lead to bad solder joints. Before placing a new component, it is recommended to apply solder paste on each PCB pad by printing (special micro stencil) or dispensing. It is also recommended to use only no-clean solder paste.

**Rework**

**6.4 Reassembly and Reflow**

After preparing the site, the new package can be placed onto the PCB. As in the original assembly, zero-force placement should be used, with the package is positioned exactly above the PCB pads, at a height such that there is no contact between the package and the prepared PCB. Then drop the package onto the printed or dispensed flux or solder paste deposit with no further pressure. During the soldering process the package peak temperature should not be higher than, and temperature ramps should not be steeper than, those during the standard assembly reflow process (Section 5.5).

## 7 Appendices

### Appendix A Packaging of Components

Infineon packs components according to the IEC 60286-\* series.

#### List of relevant standards to consider

- IEC 60286-1 Packaging of components for automatic handling - Part 1: Tape packaging of components with axial leads on continuous tapes
- IEC 60286-2 Packaging of components for automatic handling - Part 2: Tape packaging of components with unidirectional leads on continuous tapes
- IEC 60286-3 Packaging of components for automatic handling - Part 3: Packaging of surface mount components on continuous tapes
- IEC 60286-5 Packaging of components for automatic handling - Part 5: Matrix trays
- IEC 60286-6 Packaging of components for automatic handling - Part 6: Bulk case packaging for surface mounting components

### Appendix B Storage and Temperature Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination and package cracking effects.

#### List of relevant standards to consider

- IEC 60721-3-0 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; introduction
- IEC 60721-3-1 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 1: Storage
- IEC 60721-3-2 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 2: Transportation
- IEC 62258-3 Semiconductor Die Products - Part 3: Recommendations for good practice in handling, packing and storage
- ISO 14644-1 Clean rooms and associated controlled environments Part 1: Classification of airborne particulates

## **8 Revision History**

### **Major changes since the last revision**

<b>Date</b>	<b>Reference</b>	<b>Description of change</b>
2014-10-16	All pages	First Publishing

#### Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOST™, CIPURSE™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBLADE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SiL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ™, TRENCHSTOP™, TriCore™.

#### Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. ANSI™ of American National Standards Institute. AUTOSAR™ of AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. HYPERTERMINAL™ of Hilgraeve Incorporated. MCS™ of Intel Corp. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ of Openwave Systems Inc. RED HAT™ of Red Hat, Inc. RFMD™ of RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2014-07-17

[www.infineon.com](http://www.infineon.com)

**Edition 2014-10-16**

**Published by**

**Infineon Technologies AG**

**85579 Neubiberg, Germany**

**© 2014 Infineon Technologies AG.**

**All Rights Reserved.**

**Do you have a question about any aspect of this document?**

**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

**Document reference**

**B154-I0045-V1-7600-NA-EC-P**

#### Legal Disclaimer

THE INFORMATION GIVEN IN THIS APPLICATION NOTE (INCLUDING BUT NOT LIMITED TO CONTENTS OF REFERENCED WEBSITES) IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

#### Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.