Advantages of coreless-transformer gate drivers over gate drive optocouplers

About this document

Infineon strives to enhance electrical systems with comprehensive semiconductor competence. One of these areas with high competence is the power electronics. Power electronics applications employ power device switches used in applications like battery-driven power tools, small and major home appliances, computing and telecom servers, EV charging, solar, and robotics. And power device switches require optimum gate drive solutions. Gate driver ICs are the interface between control signals (digital or analog controllers) and power switches (IGBTs, MOSFETs, SiC MOSFETs, and GaN HEMTs). The integrated gate driver solutions reduce the design complexity, development time, bill of materials (BOM), and board space while improving reliability over gate drive solutions implemented with discretes.

In an industrial environment where high voltages, magnetic fields and noise are present everywhere, reliability is critical to avoid downtime and ensure consistent data. In this environment, circuit designers use galvanically isolated CT gate driver to insulate high voltages and isolate unwanted signals.

Infineon coreless transformer (CT) technology is a magnetically coupled, galvanically isolated technology which uses semiconductor manufacturing processes to integrate an on-chip transformer consisting of metal spirals and silicon oxide insulation. The on-chip coreless transformers are used for transmitting switching signal between the input chip and output chip(s) and other information.

Another well-known isolation technology is the optical coupling, from which the galvanically isolated gate drive optocouplers were later developed.

Scope and purpose

- Why galvanically isolated gate drivers are used
- Amplify the main differences of gate drive optocouplers versus CT gate drivers
- Review of application-level impact of long cables
- Provide design guidelines on how to match longer cables used between microcontroller outputs and gate driver inputs in the context of high switching frequencies and fast rise- and fall-times

Intended audience

- Engineers who want to learn how to use the Infineon EiceDRIVER™ isolated gate driver ICs
- Experienced design engineers designing circuits with Infineon EiceDRIVER™ gate driver ICs, IGBTs, CoolSiC™ MOSFETs and MOSFETs
- Design engineers designing power electronic devices, like inverters and drives

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1 Galvanically isolated gate driver

Galvanically isolated gate drivers are useful in applications where signals need to be transferred from one module to another in the presence of a large potential difference or induced noise between the ground or common points of these modules.

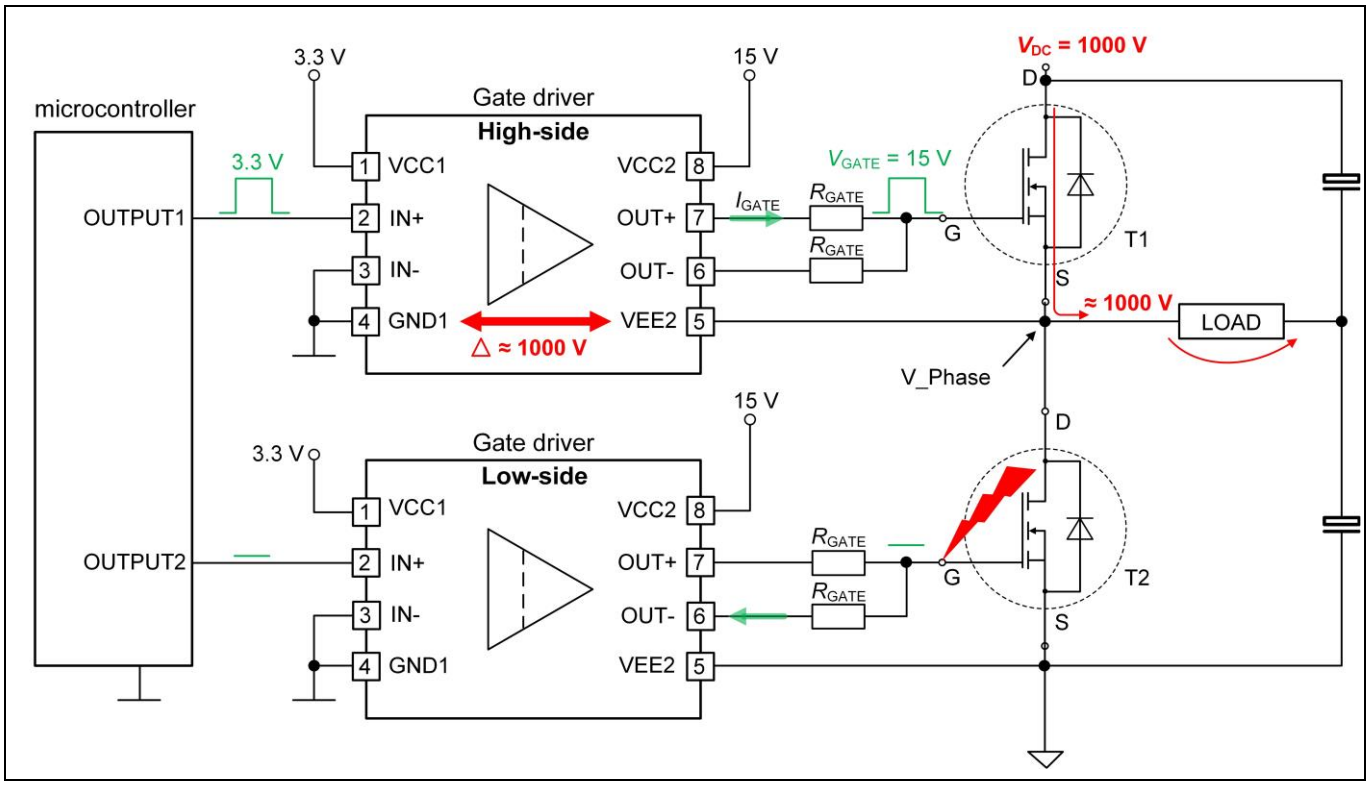

Figure 1 Typical half-bridge application including microcontroller, isolated gate driver and power switches

Figure 1 shows the challenges when operating with high voltages. There are two possible scenarios:

- Scenario 1: High-side gate driver switching on, normal operation
- Scenario 2: Worst-case scenario, a defect in power switch T2 or T1

Scenario 1: This is a normal operation in a half- or full-bridge configuration. The high-side gate driver switches on. According to the example in Figure 1 there are 15 V on gate from power switch T1, and T1 is fully conducting. The full voltage of around 1000 V can then be measured at the node V_Phase, which is directly connected with VEE2 of the high-side gate driver. There is now a big potential difference between the secondary side (VCC2, OUT+, OUT-, VEE2) and the primary side of the gate driver (VCC1, IN+, IN-, GND1). This voltage difference, which is almost the full DC-bus voltage, should never lead to breakthrough. In this case, the high voltage would be applied to the microcontroller. The application would be destroyed and people could be in **mortal danger of their lives**. **This means that the gate driver must withstand this voltage difference (V_{DC} + V_{GATE}) over the entire life time.**

Scenario 2: There is a breakthrough between drain and gate of the power switch T2 or T1, caused by an error in the application/device (worst case error). Even in the error condition the result will be the same: the driver has to withstand the full voltage difference!

To prevent accidental current from high voltages that could cause bodily harm, a galvanic isolation is mandatory. In this application note, the two most common methods of electrical isolation in context with gate drivers are briefly described and compared.

These two methods are:

- Galvanic isolation by using gate drive optocoupler
- Galvanic isolation by using transformer implemented on chip - CT gate driver

1.1 Gate drive optocoupler

1.1.1 Introduction

An optocoupler (also called photo coupler or optical isolator) is an electronic component that transfers electrical signals between two isolated circuits by using light. Figure 2 shows the general overview of a gate drive optocoupler.

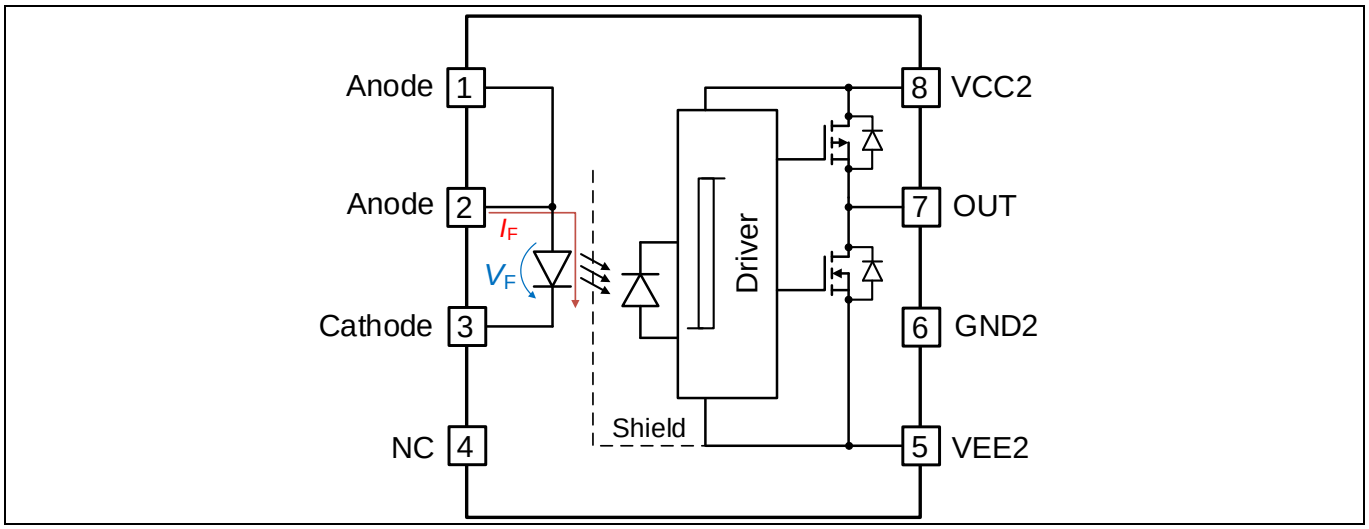

Figure 2 Structure of gate drive optocoupler

Most types of optical isolators consist of an LED (emitting the light energy) and a phototransistor (receiving the light energy), coupled by an opaque material for light transmission. A dielectric barrier layer (shield) is mounted between the LED and the phototransistor. The optical energy is absorbed by the phototransistor and converted with the help of an internal driver in such a way that two output transistors can be operated.

Figure 3 shows the transfer characteristics from the gate drive optocoupler ACNU-3430. This indicates the amount of energy which is required to turn on the optocoupler.

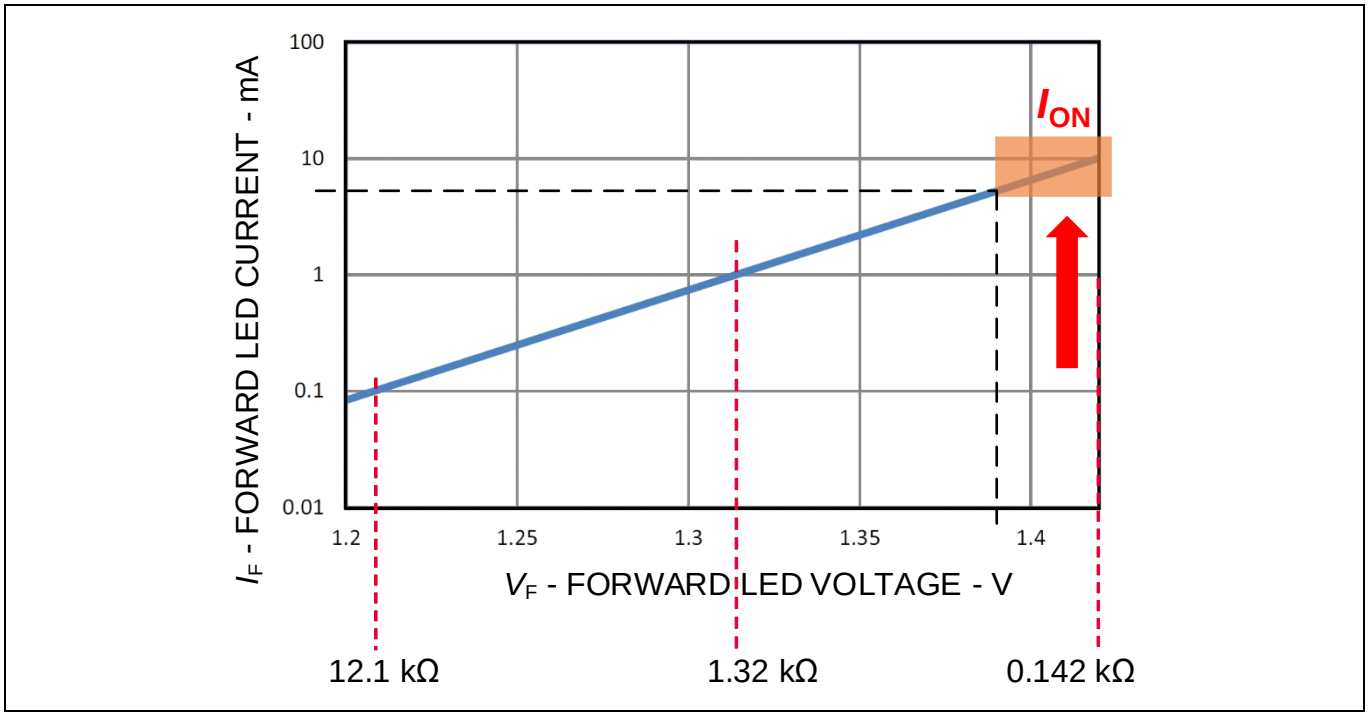

Figure 3 Transfer characteristic of gate drive optocoupler ACNU-3430

Two further essential properties of the gate drive optocoupler can be derived from this transfer-characteristic curve. First, the input resistance is non-linear. It falls very sharply within a relatively small voltage swing, in this case from approx. 12 kΩ down to 142 Ω. Second, the driver only switches on from a threshold value, in this case at approximately 8 mA.

1.1.2 Mode of operation of gate drive optocoupler

Figure 4 shows a basic circuit of a gate drive optocoupler in cooperation with a microcontroller.

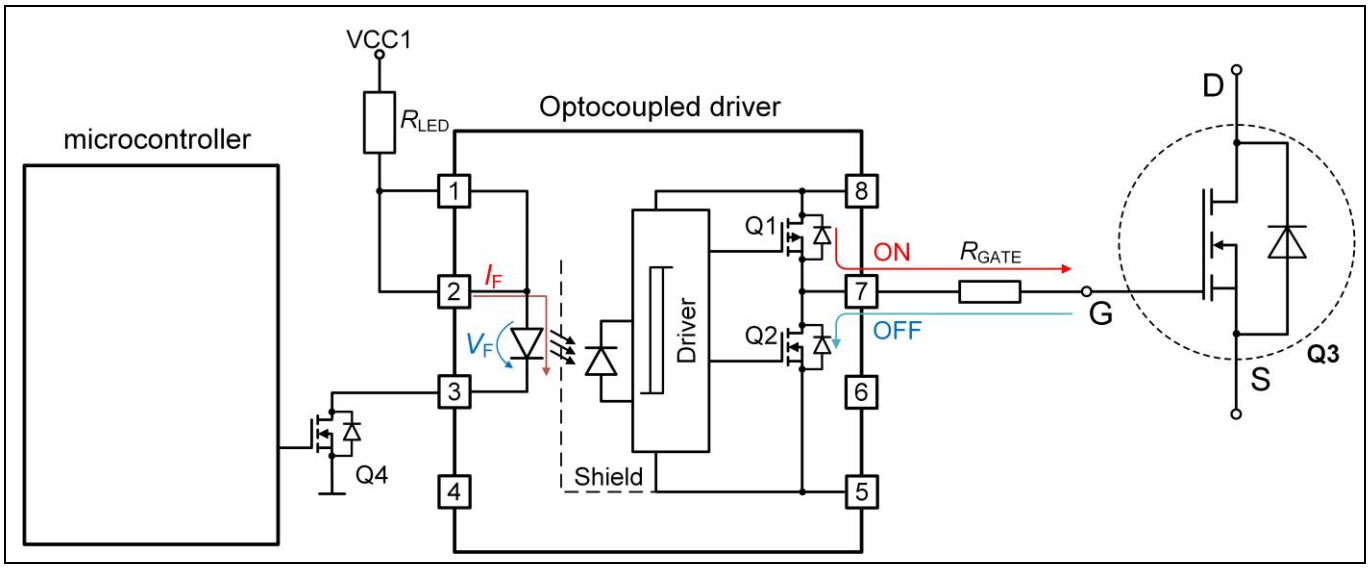

Figure 4 Basic circuit of gate drive optocoupler with microcontroller and SiC MOSFET

In this example, the driver is not switched directly by the microcontroller, but via an extra transistor Q4. This is necessary in the case that the microcontroller output is not able to switch the required diode current I_F or several channels are switched, so that there is a risk of overloading the microcontroller.

As soon as Q4 turns on (conductive), an electric current (I_F) flows through the LED, and it emits light. This emitted light passes through an optical transparent shield and reaches the photodetector. Here the light energy is converted into electrical energy and fed to the internal driver of the optocoupled gate driver. The output transistor Q1 switches on (conductive), and Q2 switches off (not conductive).

If Q4 is turned-off (not conductive), no electric current (I_F) flows through the LED, and no light is emitted. In this case, the output transistor Q1 turnes off (not conductive), and Q2 turnes on (conductive).

1.2 Coreless transformer (CT) gate driver

1.2.1 Introduction

Infineon coreless transformer (CT) technology is a magnetically coupled, galvanically isolated coupler technology. It is based on a semiconductor manufacturing process that integrates an on-chip transformer consisting of metal spirals and silicon oxide insulation. By using the well-known complementary metal-oxide-semiconductor (CMOS) process, many other functions can be integrated, such as filters, protection functions, a second transformer and other functions. The on-chip coreless transformers are used for transmitting switching information between the input chip and output chip(s) and other signals.

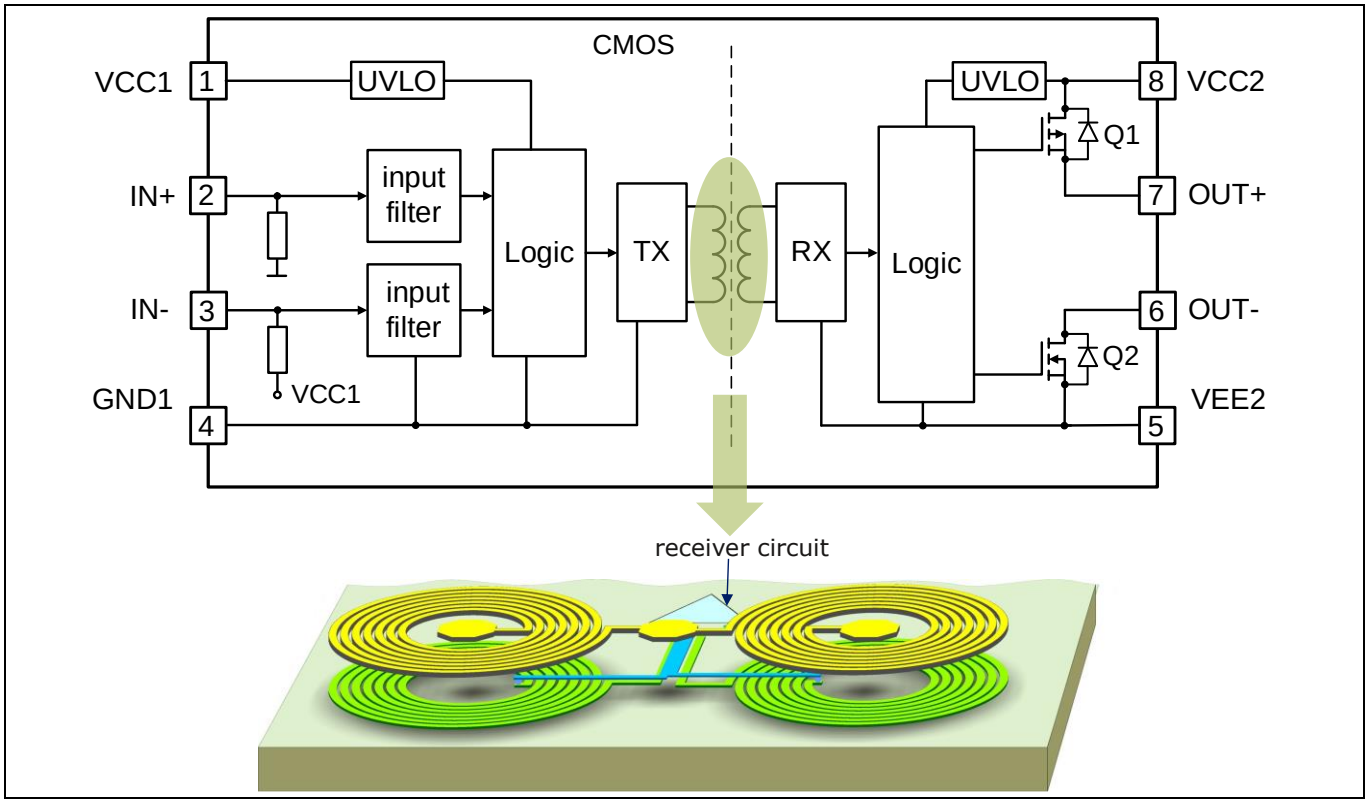

Figure 5 CT gate driver equivalent circuit and simplified structure of coreless transformer

The incoming signals are processed by input filters to prevent unexpected switching due to interferences. In the transmitter unit (TX) the logic signals are converted into an RF carrier signal. This RF signal is then transmitted

via the transformer and converted back into logical signals in the receiver unit (RX). The undervoltage lockout units (UVLO) protect the application from distortions in the power supplies. As soon as the supply voltages drop below a certain value (please see corresponding data sheet information), the gate driver is switched off (Q1 not conducting, Q2 conducting). The information transfer via the transformer occurs instantaneously and cannot be influenced from outside.

1.2.2 Mode of operation of CT gate driver

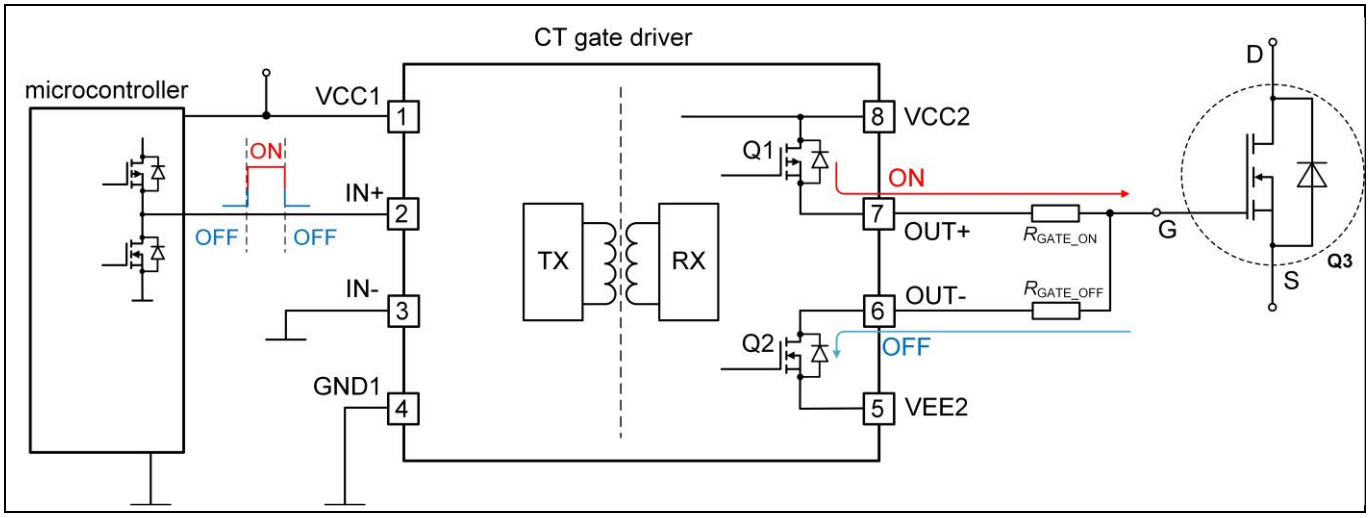

Figure 6 Basic circuit of CT gate driver with microcontroller and SiC MOSFET

Figure 6 shows a basic circuit of a CT gate driver connected with a microcontroller and a SiC MOSFET. There are two possible input modes to control the power switch. At non-inverting mode, the input IN+ controls the driver output while IN- is set to low. At inverting mode, IN- controls the driver output while IN+ is set to high. A minimum input pulse width is defined to filter occasional glitches (40 ns at CT gate driver 1ED3124MC12H). It is implemented using the integrated filters; please see previous section. According to the circuit in Figure 6, as soon as the input IN + goes to logic “High”, the driver switches on (Q1 – conductive, Q2 – not conductive). As soon as the input IN + goes to logic “Low”, the driver switches off (Q1 – not conductive, Q2 – conductive).

2 Advantages enabled by coreless-transformer based gate drivers

The following Table 1 lists some key features, that are important for various applications. Summarizing all the features, it can be seen that the coreless-transformer-based gate drivers of the new generation, like X3 Compact (1ED31xx), 2L-SRC Compact (1ED32xx), X3 Analog (1ED34xx), X3 Digital (1ED38xx) and 1ED-F3 (1ED332x) as well are excellently suited for the majority of currently used applications. The following sections discuss these features in more detail.

Table 1 Typical design parameter of an opto-based and CT-based gate driver

	Example CT gate driver	**Example opto gate driver**
Typical design parameter	**1ED3124MC12H**	**ACNU-3430**
Input to output offset voltage	**2300 V**	n.a.
Maximum repetitive insulation voltage V_{IORM}	**1767 V**	1414 V
Input current for switch "ON"	70 µA	7 mA…12 mA
Input voltage for switch "ON"	2.5 V	1.45 V
Input capacitance CIN	<< 1 pF	≈25 pF
Integrated input filter	Yes - 30 ns	No
Input to output Propagation delay ON	100 ns	150 ns
Input to output Propagation delay OFF	100 ns	150 ns
Input to output, part to part propagation delay	±7 ns	±90 ns
Maximum power supply voltage output side (VCC2 - VEE2)	35 V	30 V
Peak output current from Q1 and Q2	Q1 = 14 A ; Q2 = 14 A	Q1 = 5 A ; Q2 = 5 A
CMTI	200 kV/µs	100 kV/µs

2.1 Input-to-output isolation voltage

As discussed in Chapter 1, galvanically isolated gate drivers are useful in applications where signals need to be transferred from one module to another in the presence of a large potential difference. This large potential difference is specified as “Input-to-output isolation voltage” in the data sheet. Figure 1 illustrates the term “Input-to-output”, for example the potential difference from GND1 to VEE2.

For household applications with voltages around 230 V_{RMS} (V_{PEAK} to GND ≈ 325 V), an insulation voltage of 600 V would be sufficient if a certain margin is included.

In other applications, like solar, the voltages can be much higher. Figure 7 illustrates a very simplified setup of a solar application.

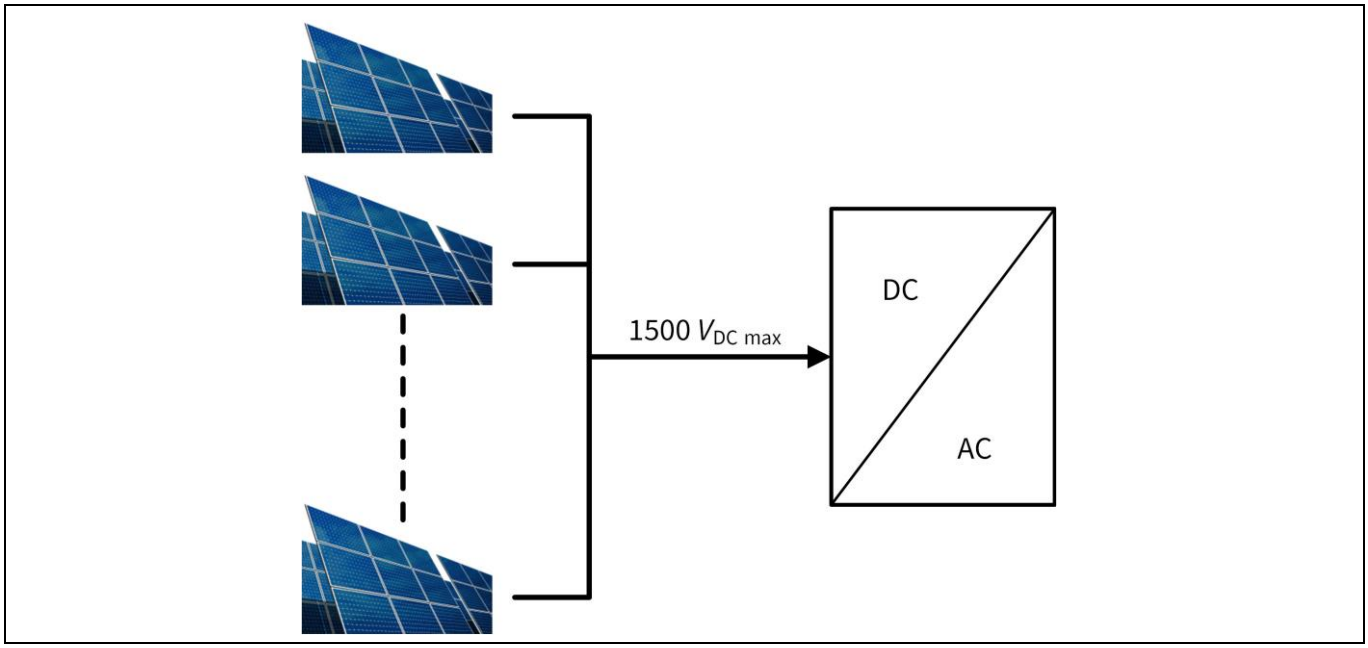

Figure 7 Simplified setup of solar application

The voltages of different solar panels are transformed to 1500 V to reduce the cable cross section while maintaining the same electrical power. This saves copper and also reduces the weight of the setup.
If a certain margin is now added, the power switches should have a break down voltage of at least 1700 V. However, the trend leans more towards 2000 V power switches. The gate driver must of course have the same voltage range, in this case at least the input to output isolation voltage of 1700 V or 2000 V.

2.2 Electrical input characteristics

2.2.1 Input voltage and current for switch-on

In many applications, including power applications, microcontrollers or Field Programmable Gate Arrays (FPGAs) are used, which in the first stage control the gate driver, which actuates the power switch. Figure 1 shows one of these application scenarios. The outputs of these microcontrollers are standardized, i.e. they provide clearly defined digital output voltages. In most cases, this is 3.3 V or 5 V, with trend being 3.3 V.

The CT gate drivers, like the 1ED3124MC12H, are produced in CMOS technology and no extra effort is required to be controlled by the microcontroller or FPGA. A typical connection can be seen in Figure 6. Table 2 shows the main electrical parameters for the input stage of the 1ED3124MC12H. The maximum input-voltage at the IN+ or IN- pin should be 5.5 V, the input current is with 100 µA very low. Looking at an edge coming from 0 V to 3.3 V, the switch-on level is 2.5 V. This is a much higher level compared to the opto gate driver ACNU-3430, given with a starting value of about 1.4 V, see Figure 3. The distance to noise, which is present on every electrical line, is thus much greater with the CT gate driver.

Much worse is the higher input current from the opto gate driver, which is, in the range of 7 mA up to 12 mA depending on the type. This leads on the one hand to bigger power losses in the gate driver stage. On the other

hand, not all microcontrollers can drive this amount of electrical current, especially when multi-channel applications like half- or full- bridge applications are present and the currents add up.

Table 2 shows the main values of the input characteristics for CT-based gate driver as discussed.

Table 2 Electrical input characteristic for CT-based gate driver 1ED3124MC12H

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Logic input voltages (IN+, IN-)	V_{IN}	-0.3		5.5	V
IN+, IN- low input threshold voltage	$V_{IN,L}$			1.1	V
IN+, IN- high input threshold voltage	$V_{IN,H}$	2.5			V
IN+, IN- low/high hysteresis	$V_{IN,HYS}$	0.5	0.8		V
IN+, IN- input current	I_{IN}			100	µA

At higher switching frequencies, the effect is amplified even further, as there are even higher switching losses. At the end the power losses of the microcontroller become too high.

Some of these input characteristics, namely the input current and the input voltage, in qoutient the input impedance, determine the electrical behavior of the gate driver in operation over long transmission lines. For this, of course, the output stage of the transmitter (i.e. microcontroller) must be considered at the same time. The next section will provide some short summaries about this topic.

2.3 Transmission line termination

The transmission line termination is a key point, especially in harsh environments. In addition to the noise and interference signals, the line reflections are added, which in total prevents a clean and accurate switching behavior. The intention is to make the reflection factor zero at the signal source by inserting a series resistor, which makes the (apparent) output impedance of the signal source (transmitter + R_P) equal to the line impedance. All electrical lines longer than the critical length of $l > t_r / (2^* \tau)$ and on which high-frequency signals are transmitted, should be terminated! The factor τ is the signal runtime and t_r the rise time of the signal.

You will find more information on this topic in the application note:

AN-2022_pulses_and_transmission_line_theory

2.3.1 Line termination of single-channel gate drive optocoupler via series damping

The series attenuation is the most economical option and is achieved by choosing the value of resistor R_P as close as possible to the value of the characteristic impedance of the transmission line. Assuming the microcontroller can drive the LED current, such a circuit could resemble the one in Figure 8.

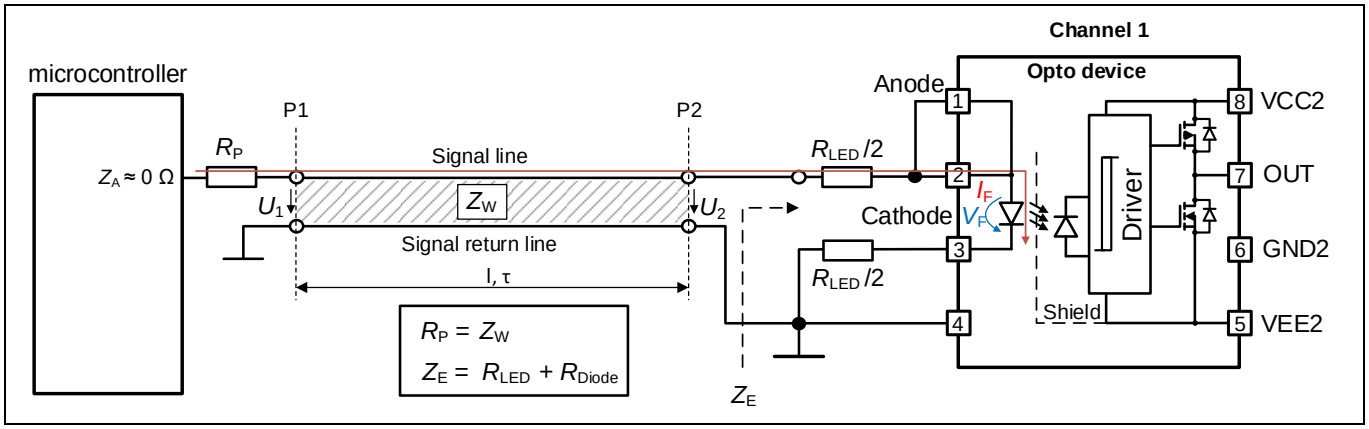

Figure 8 Transmission line termination with gate drive optocoupler

Due to the higher input current and the associated small input resistance RLED (about 150 Ω in a 3.3 V system), a certain degree of line matching is already present. But an exact fit is not easy. It depends on the LED current I_F, and it will not be easy to adapt the R_P to the Z_W.

2.3.2 Line termination of multi-channel gate drive optocoupler via series damping

In applications such as half-bridge or full-bridge, in which several drivers have to be operated, it can be assumed that a microcontroller cannot drive several opto devices at the same time without being overloaded. With a much greater effort, e.g. an additional buffer, such an application can work well, see Figure 9.

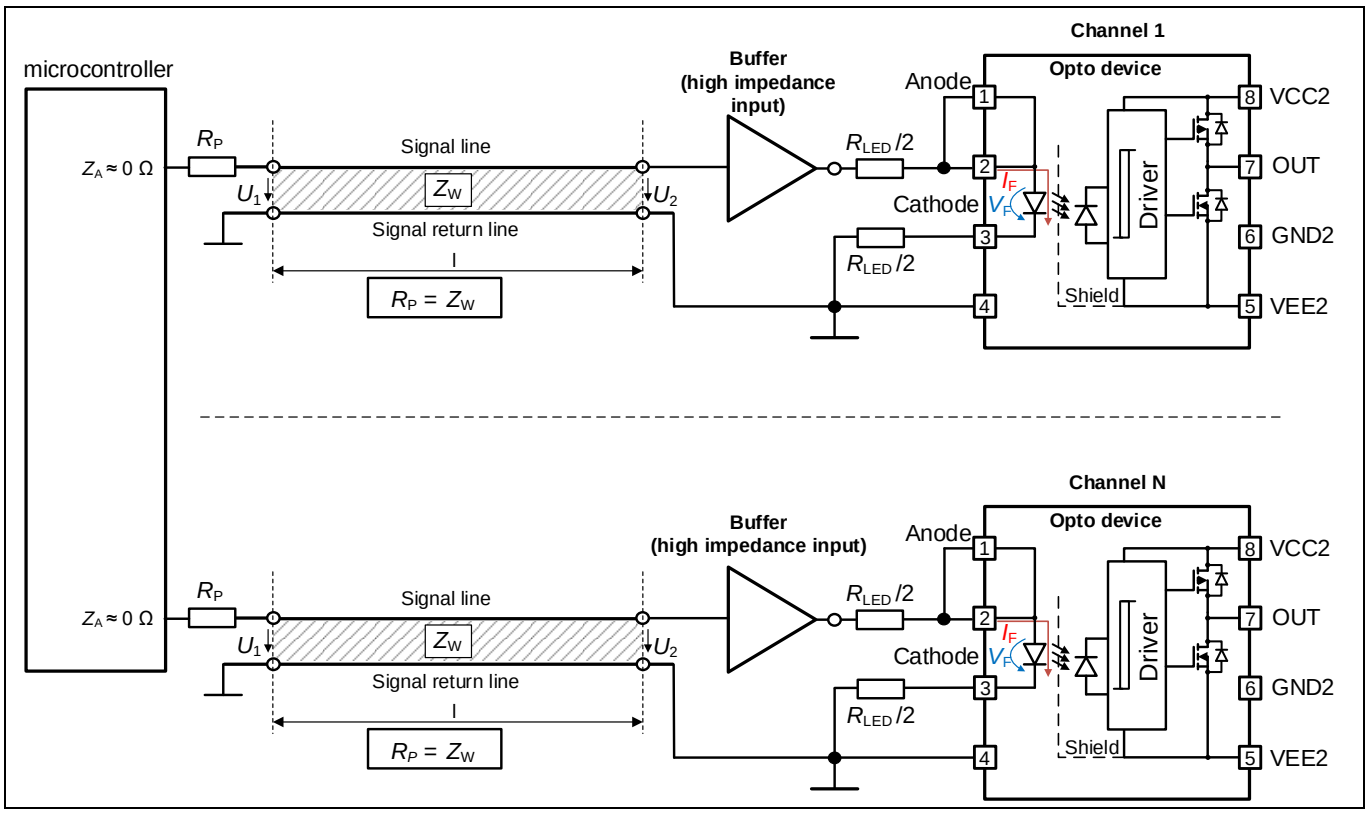

Figure 9 Multi-channel transmission line termination with gate drive optocoupler

2.3.3 Line termination of single-channel CT drivers via series damping

The same applies here that, series attenuation is the most economical option. Due to the fact that CT gate drivers have a high-resistance input, the wiring is very simple, see Figure 10.

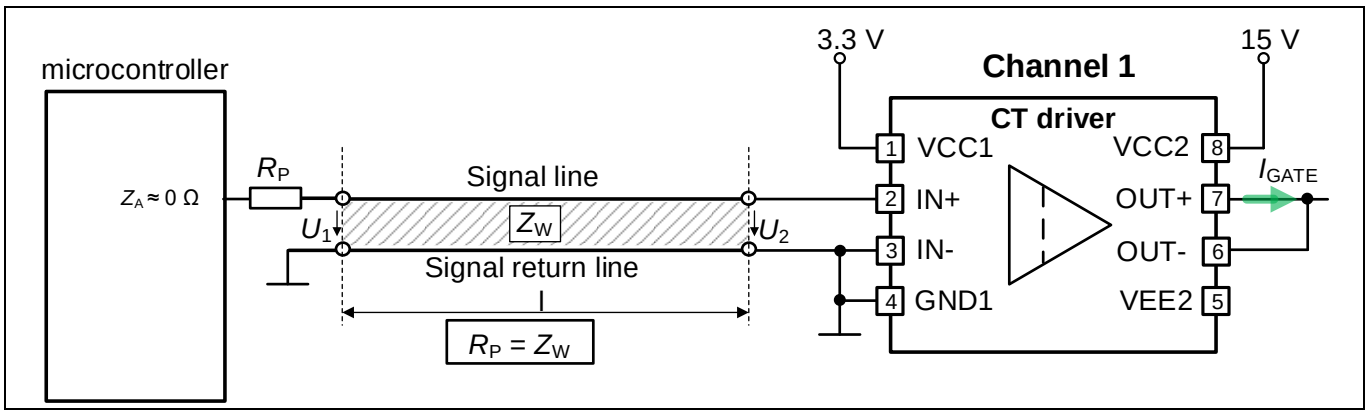

Figure 10 Single-channel transmission line termination with CT gate driver

Due to the high input impedance of the CT gate driver, the line matching is done with only one resistor!

2.3.4 Multi-channel CT via series damping

Figure 11 shows a multi-channel application with CT gate driver.

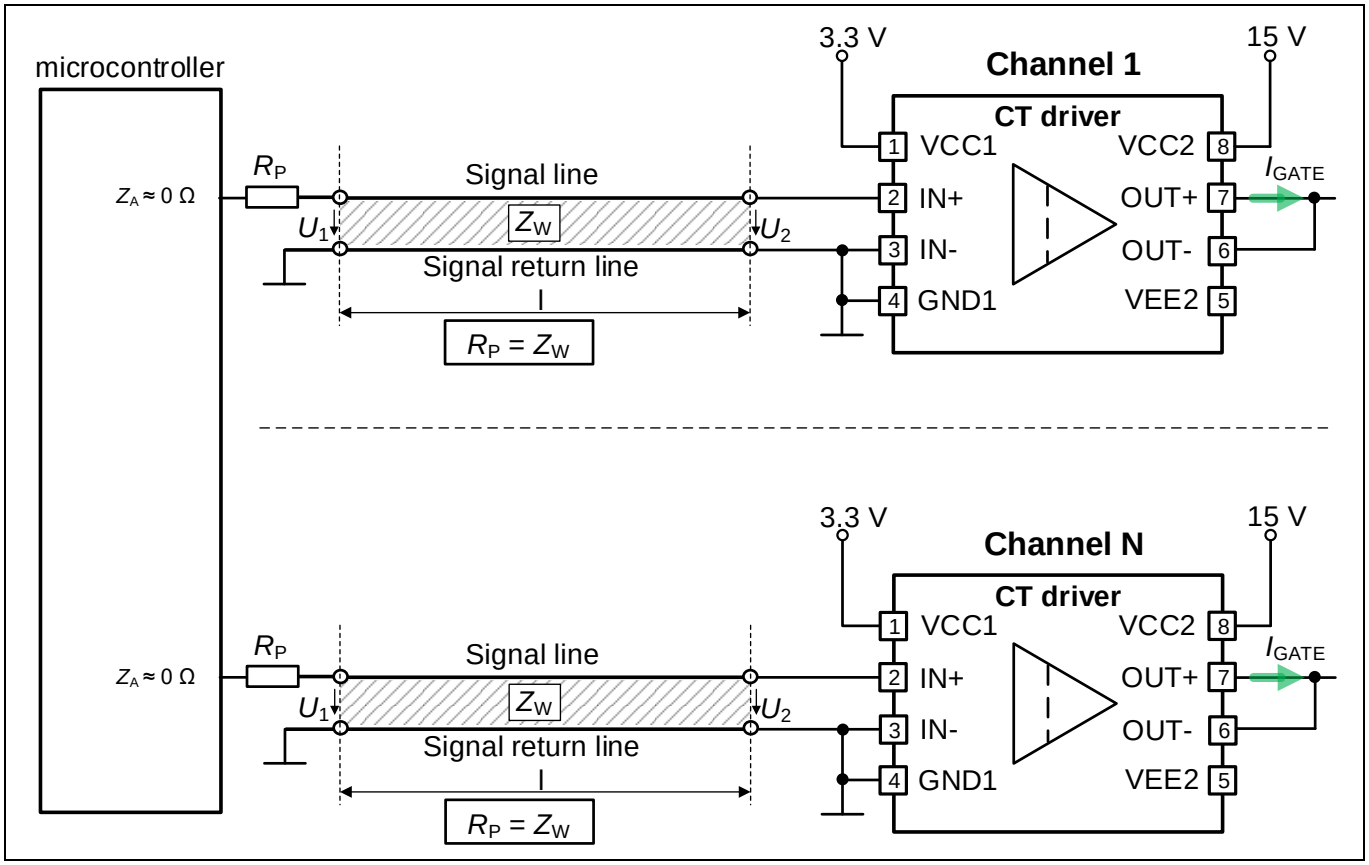

Figure 11 Multi-channel transmission line termination with CT gate driver

The transmission line termination with CT gate driver is very easy in both single- or multi-channel application.

Due to the high impedance resistances of the CT gate driver, the CT gate drivers are very interesting for multi-channel applications, such as drives, EV charging, etc.

2.4 Integrated input filter

In order to protect the application against high-frequency interference signals, filters have been integrated in the CT gate drivers 1ED312xMC12H, through which the input signals require a certain length (time length – t_{MININ} ≈ 40 ns) before the input signal is allowed to pass.

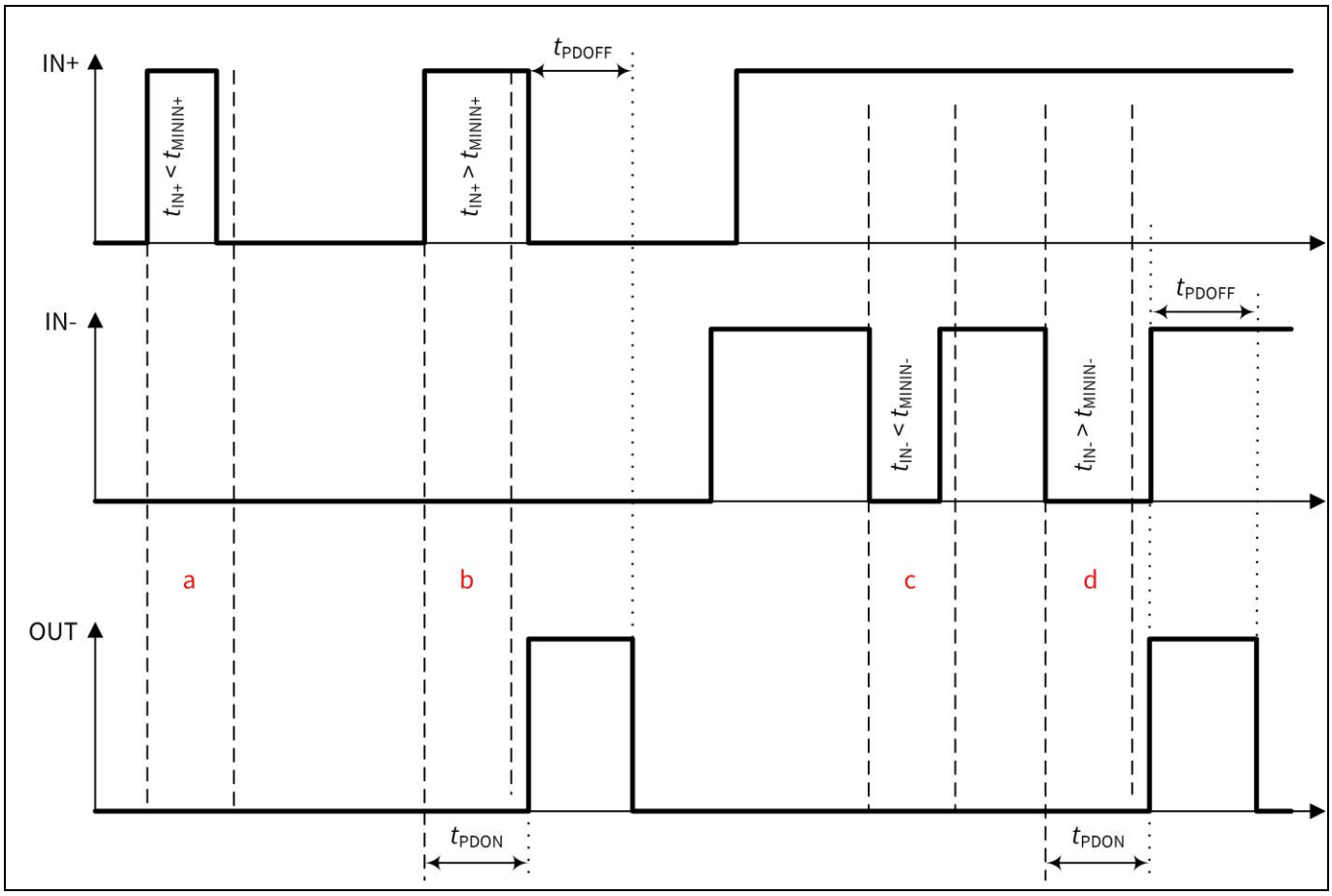

Figure 12 Input-pulse suppression and turn-on / turn-off propagation delay

Every pulse at IN+ shorter than the input pulse suppression time for pin IN+ (t_{MININ+}) will be filtered and won't be transmitted to the output chip (cases a and c). Longer pulses will be sent to the output with the shown propagation delay t_{PDON} and t_{PDOFF} (cases b and d). The same behavior is implemented at IN-. Every pulse shorter than the input- pulse suppression time for IN- (t_{MININ-}) will be omitted, and longer pulses transmitted with the same propagation delay.
This is one of the big differences, the gate drive optocoupler has no integrated filter compared to the CT gate driver and is therefore more prone to false triggering.

2.5 Input capacitance

The CT gate driver 1ED3124MU12H has a very small input capacitance (< 1 pF) as opposed to gate drive optocoupler ANCU-3430 with ≈ 23 pF. Due to the smaller capacitance, the input has a smaller low-pass characteristic and higher switching frequencies can be achieved. Furthermore, the extra delay for the signal caused by this external low-pass filter is much smaller.

2.6 Timings

2.6.1 Propagation delay

The propagation delay from the gate driver is defined as the delay from an incoming signal from the input to the output of the gate driver. The propagation delay is often specified with two values, when switching-on (input- to- output propagation delay on - t_{PDON}) and when switching-off (input-to-output propagation delay off - t_{PDOFF}). Figure 13 illustrates the relation.

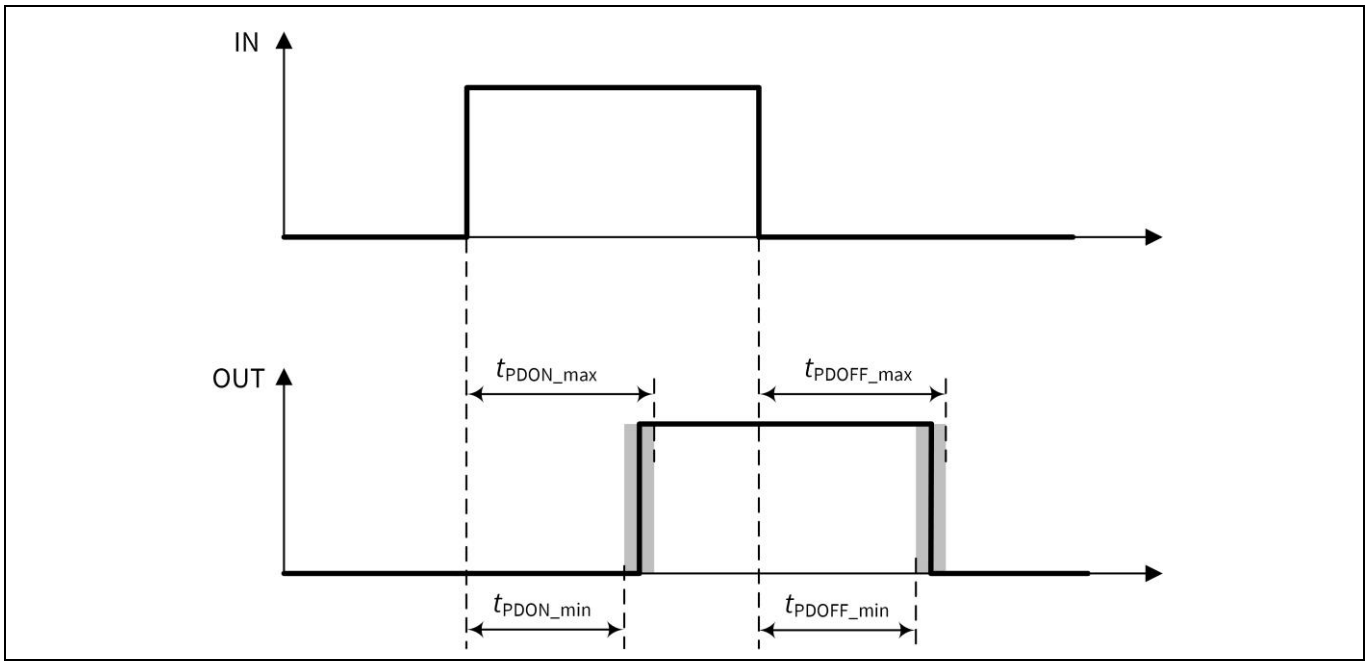

Figure 13 Propagation delay on and propagation delay off

In addition, the minimum (min) and maximum (max) values are also displayed in Figure 13. The input to output propagation delay on is the time after which the rising edge of the input signal is transmitted to the output. Similar is the case with input-to-output propagation delay off, which is the time delay after falling edge.

The propagation delay must be considered in the applications, as well as the delay caused by the power switch; see Figure 14 and Figure 16.

Figure 14 shows the delay chain in a half-bridge application. Starting from the view point of the output of the microcontroller (low-side or high-side) with starting point t_0, the first delay can be expected in the electrical bus between microcontroller and gate driver, and depends on the length of the electrical bus and its material properties. The time difference between t_{d1} (input of gate driver) and t_{d2} (output of gate driver) can be considered as the propagation delay time from the gate driver. A more detailed definition can be found in the corresponding data sheets.

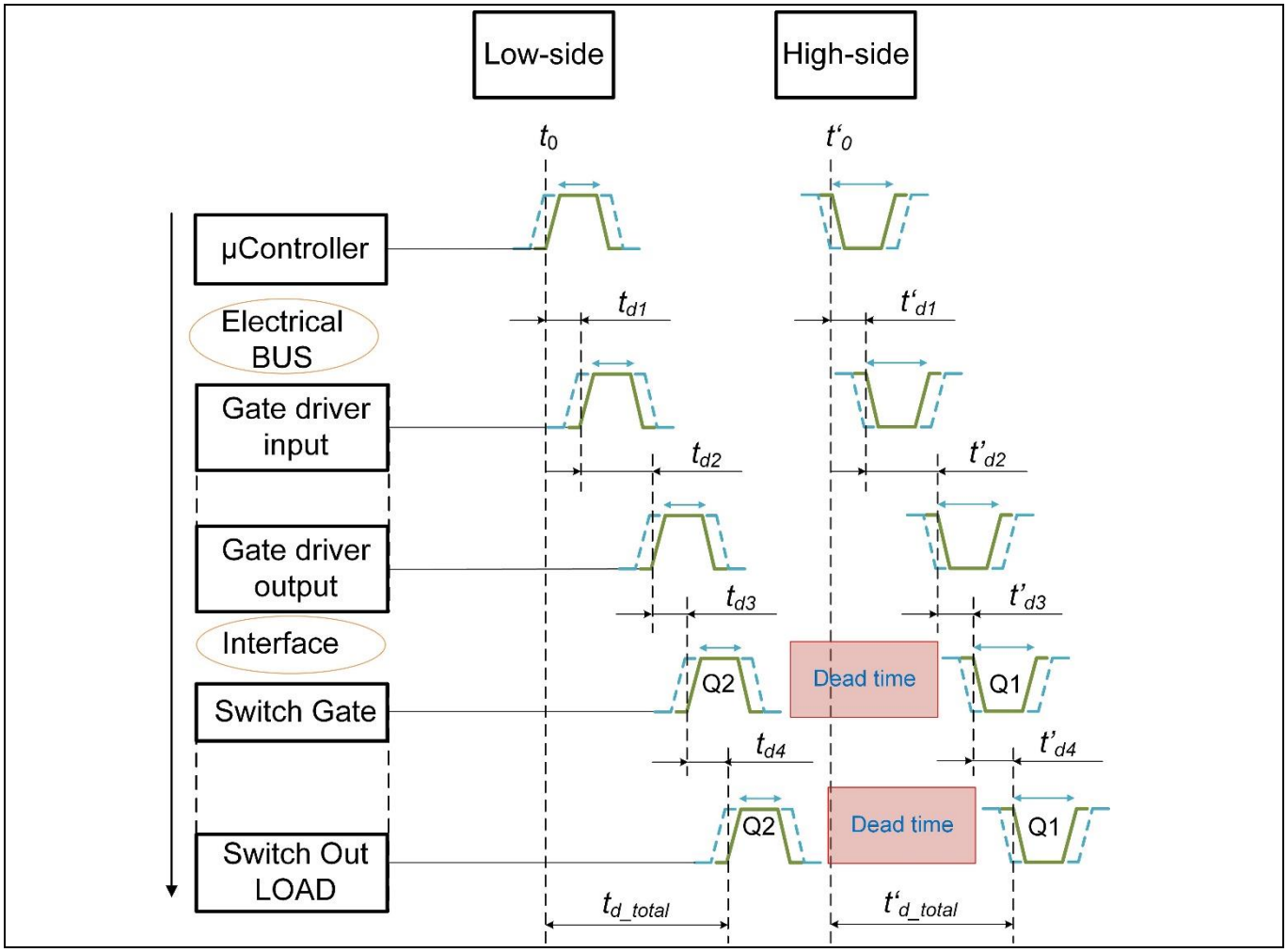

Figure 14 Delay chain from microcontroller up to the load

Also, the power switch itself has a propagation delay, to be seen in Figure 14 as the time difference between t_{d3} and t_{d4}. At the end of the chain, there is a summation of the delay times, here denoted by t_{d_total}, which must of course be considered in the switching process. The blue dashed lines indicate possible tolerances.

A worst-case scenario can be seen in Figure 16. Here the low-side switch turns on, while the high-side switch is not yet completely off. Power switch Q1 and power switch Q2 are now conducting at the same time. The result is a short circuit, and the application can be destroyed.

If the microcontroller is fast enough, it can compensate the propagation delays in most cases. A so-called dead time is introduced into the switching process, see also Figure 17. This is an artificially inserted delay which ensures that the switches are never conducting at the same time. This, of course, delays the entire switching process.

Therefore, the shorter the propagation delay, the better for the application, especially for high-speed applications. The CT gate driver definitely has advantages here.

For the CT gate drivers, the integrated filters are the dominating factor for the propagation delay, not the technology as for the opto gate drivers. This means that if the CT gate driver did not integrate the filters, it would be even faster.

2.6.2 Input to output, part-to-part propagation delay (skew)

This feature is especially important as soon as two or more gate drivers are used in a half or full- bridge application. It is defined as the difference between edges of two different channels reacting to the same input and operation conditions. Figure 15 shows the principle definition of the propagation delay skew. The input edge is rising, the outputs from gate driver 1 and gate driver 2 thus have different values of propagation delays. This can lead to worst-case conditions in real applications. Figure 16 illustrates a possible scenario based on a half-bridge circuit. The measuring point 1 shows that the input off the high-side driver switches off, and the input off the low-side driver 1 switches on after the high-side is exactly off. The high-side driver has a longer delay than the low-side driver. The result can be seen at measuring point 2. The low-side driver starts with the switch-on process, while the high-side driver is not yet switched off.

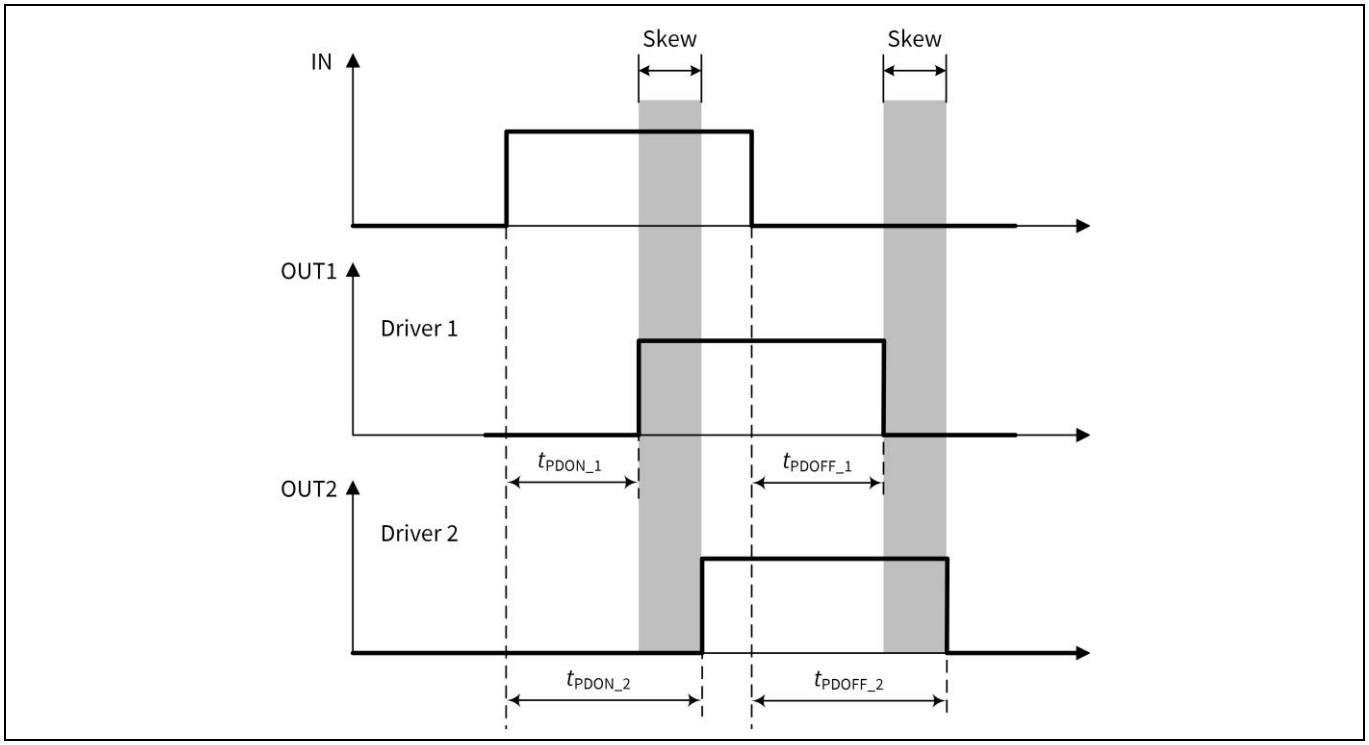

Figure 15 Propagation delay skew

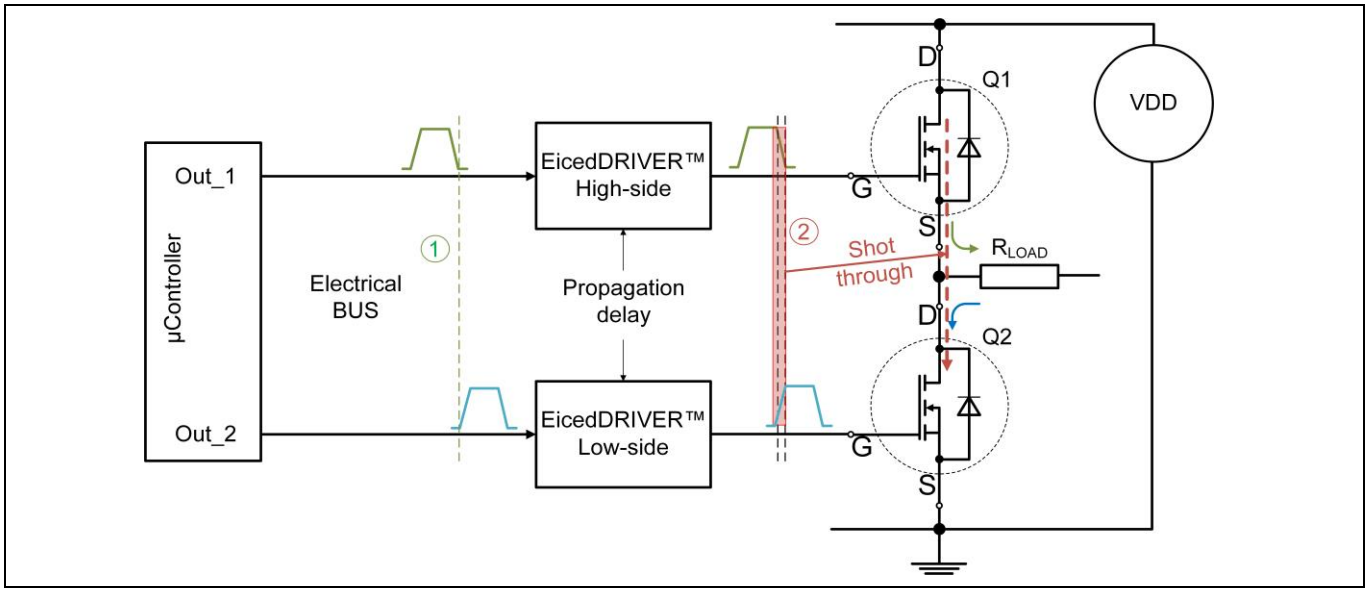

Figure 16 Half-bridge application illustrating possible shoot through caused by propagation delay skew

Power switch Q1 and power switch Q2 are now conducting at the same time. As a result, a very high electrical current can flow through both power switches and destroy the entire application. Therefore, it is important to know this feature and take it into account in the design. The microcontroller has to compensate the time differences with the introduction of the so-called dead time, see Figure 17. The shorter the skew, the smaller the dead time, and the better for the application.

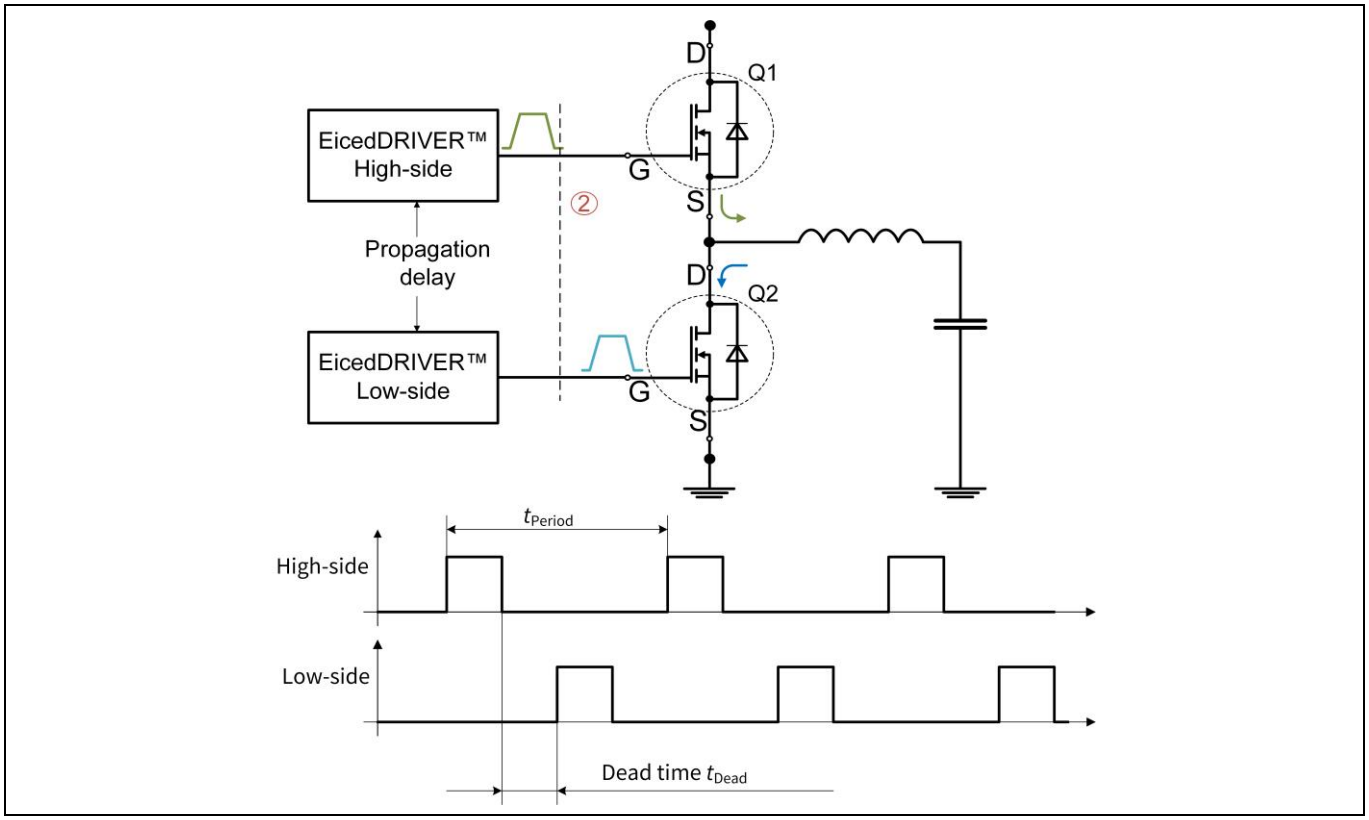

Figure 17 Half-bridge application driven with pwm-signal and a dead time to mitigate the skew

The dead time mitigates the skew, but has some disadvantages in the application. The reason is that during the dead time both power switches Q1 and Q2 are off. This could reduce the output power and efficiency could suffer, as depicted in Figure 18.

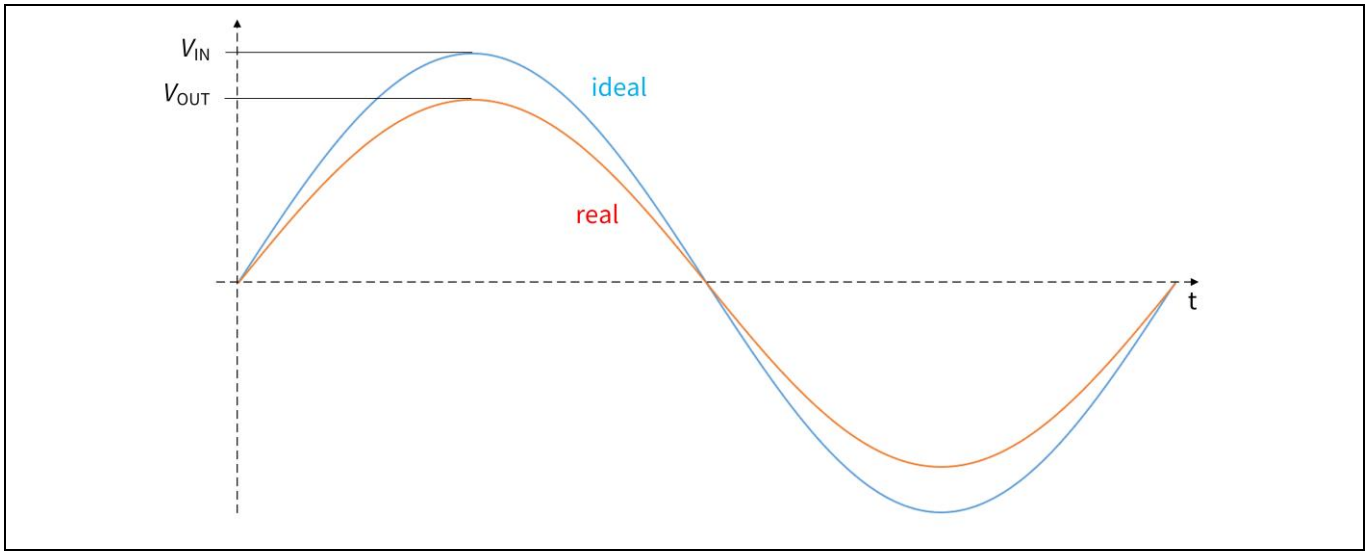

Figure 18 Reduced output voltage due to dead time

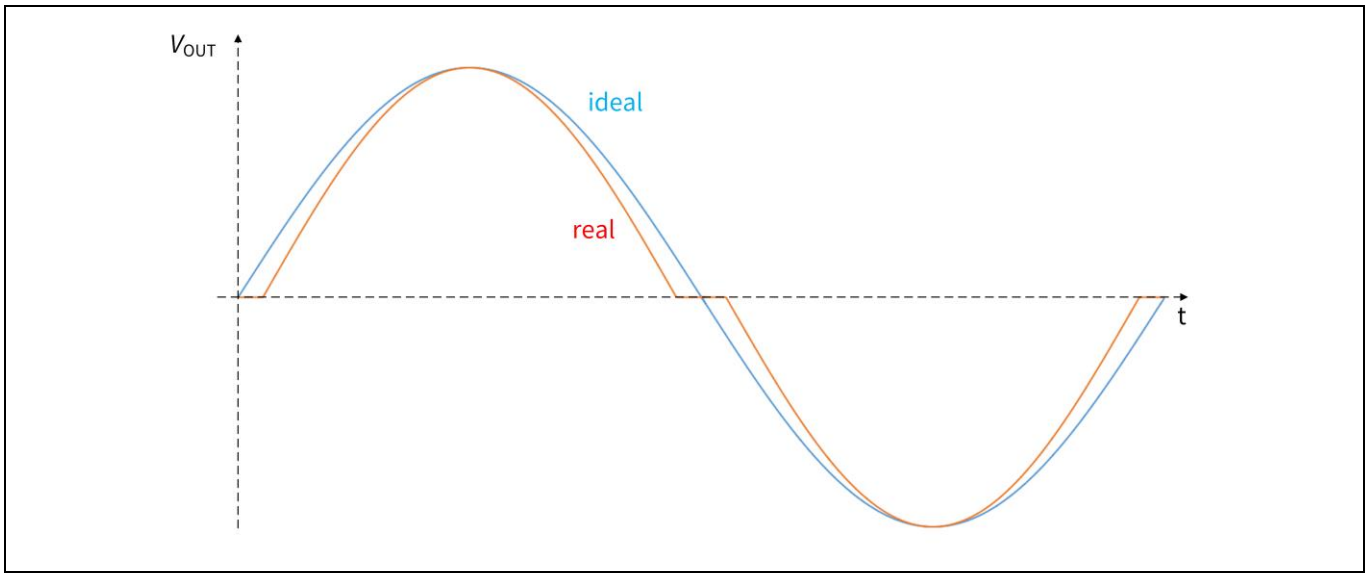

Figure 19 Increased harmonics due to dead time

If the dead time too long in relation to the period time, as in high-frequency applications, the switching process may ultimately deviate from the ideal line and generate unwanted frequency components, as shown in Figure 19.

Another application scenario is the parallel connection of power switches. Here, too, the propagation delay skew must be as small as possible so that all power switches are loaded as evenly as possible.

All the examples given here show the importance of a close part-to-part matching or a small skew. The CT gate drivers show best results here.

2.7 Electrical output characteristics

2.7.1 Maximum power supply voltage output side (VCC2-VEE2)

The power-supply voltage on the output side (VCC2-VEE2) shows the types of power switches that can be operated. VCC2 indicates the positive gate voltage, and VEE2 indicates the negative gate voltage, if needed.

Of course, the maximum difference should not be exceeded. For example, overshoots that occur more frequently due to switching operations could cause this difference to be exceeded. This can reduce the lifetime of the gate drivers. Table 3 shows some typical gate voltages for various power switches.

Table 3 Typical gate voltages for different kind of power switches

	IGBT	MOSFET	SiC MOSFET
VCC2	+15 V	+10 V / +15 V	+18 V / +15 V
VEE2	-15 V	0 V	0 V / -2 V
VCC2 - VEE2	30 V	15 V	20 V

With its maximum value of VCC2-VEE2 from about 40 V, the CT gate driver is able to drive all these various power switches without reaching the limit values.

2.7.2 Peak output current from Q1 and Q2 of the gate drivers

An important key figure is the maximum output current from Q1 and Q2, the output transistors of the gate drivers, see Figure 4 and Figure 6. These values determine the power classes of the power switches that can be operated by these gate drivers. Available in three gradations, the CT gate driver 1ED3124MU12H can supply an electrical current of up to 14 A maximum for a short time. This is sufficient to drive even large IGBT or SiC MOSFET modules with nominal electrical currents of several hundred amperes. Of course, this depends on the respective gate charge and the switching frequency.

2.8 Common-mode transient immunity (CMTI)

As mentioned in Chapter 1, with the increasing number of applications using the new generation of power switches, such as SiC and GaN, the customer end equipment and applications require higher switching frequencies. The transients can reach more than 2X the dv/dt and over 5X the di/dt during turn on/off transients compared to conventional MOSFETs or IGBTs. Therefore, CMTI is one of the key characteristics associated with isolation technologies such as isolated gate drivers or optocouplers.

High-slew-rate (high-frequency) transients can corrupt data transmission across the isolation barrier. Understanding and measuring the susceptibility to these transients is critical. The capacitance across the barrier (i.e., between the isolated ground planes) provides the path for these fast transients to cross the isolation barrier and corrupt the output waveform.

Figure 20 shows a simplified measurement circuit for CMTI.

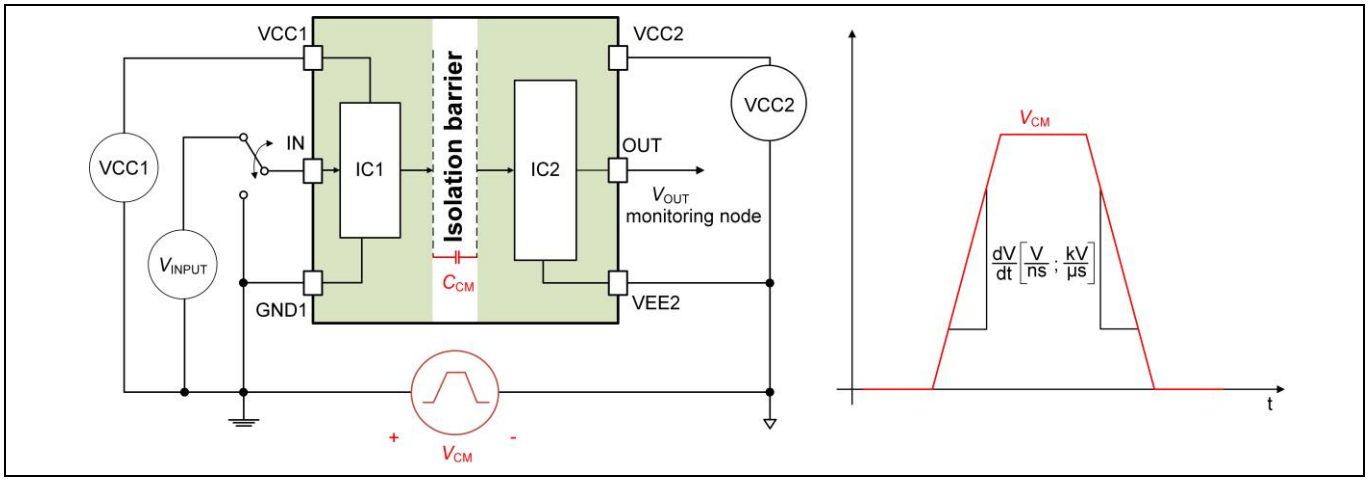

Figure 20 Simplified CMTI measurement circuit and typical common-mode pulse waveform

The CMTI is defined as the maximum tolerable rate of the rise or the fall of the common mode voltage (VCM) applied between two isolated circuits. This means that for example two isolated circuits, transmitter side and receiver side, work well within the datasheet specifications without error when striking the insulation barrier with high-rise (positive) slew rate or high- fall (negative) slew rate (dv/dt). The higher the value of CMTI, the better the immunity to interference at high switching frequencies. The physical unit is given in kV/µs or V/ns.

The test conditions for the static CMTI are defined in such a way that while the input is tied to either logic high or logic low, the output state is monitored during the occurrence of CMT strike. The output should stay in the specified high or low state within the CMTI specifications over the variation of the process, voltage and temperature. Figure 21 shows an example of static CMTI measurements, including CM_H and CM_L. For digital isolators that primarily concern the signal integrity, the output should remain at the specified logic-high level or logic-low level. For isolated gate driver applications where the output voltage is tied to the power semiconductors, such as MOSFETs or GaNs, $V_{OH\,(min)}$ and $V_{OL\,(max)}$ are typically defined as 80% and 20%, respectively, the output VDD power supply. In this case, the power transistor should remain off or on during the common-mode pulse transient.

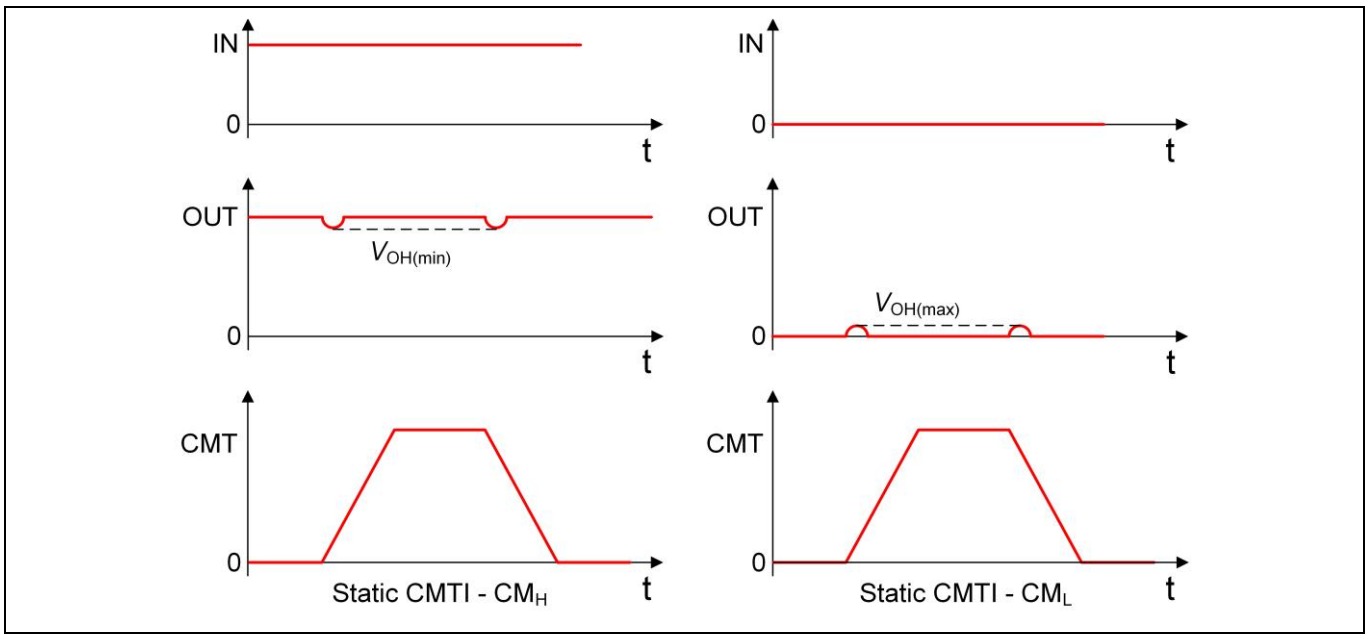

Figure 21 Static CMTI measurement

2.8.1 CMTI for gate drive optocouplers

To understand the CMTI an interference circuit model as shown in Figure 22 is considered.

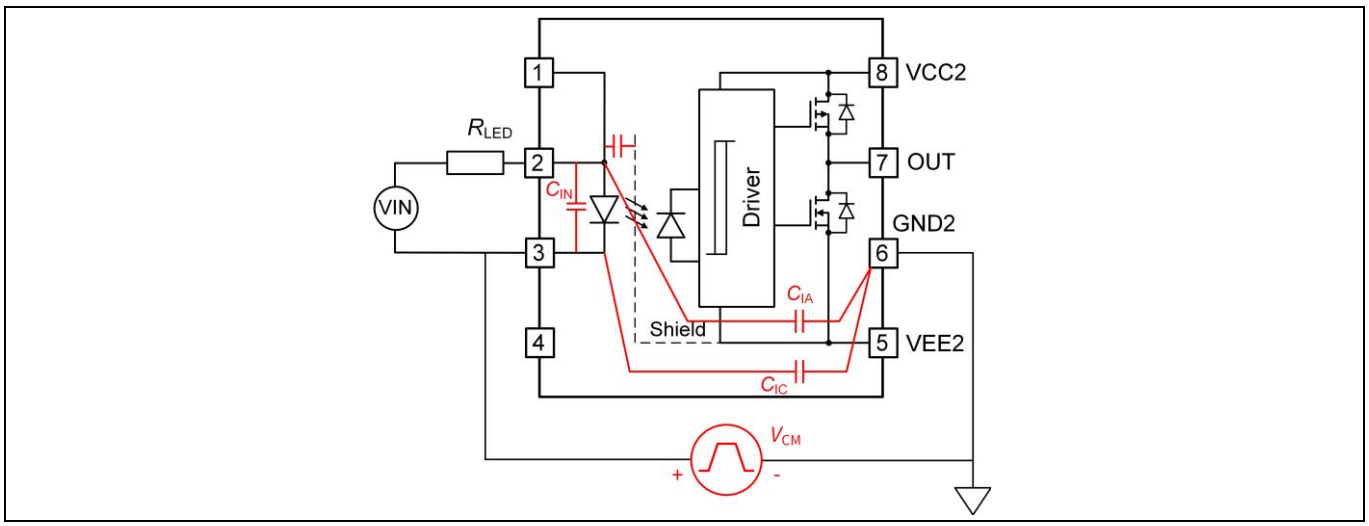

Figure 22 Example of Interference Circuit Model for gate drive optocoupler

The VCM represents a voltage spike across the opto-isolation path between the output-side ground and the input-side ground. Due to internal parasitic capacitances inside the gate drive optocoupler, there is a current flow, which can disturb the signal transmission between input and output.

A small improvement for optocoupled devices can be obtained by using the so called quasi-differential connection as shown in Figure 23.

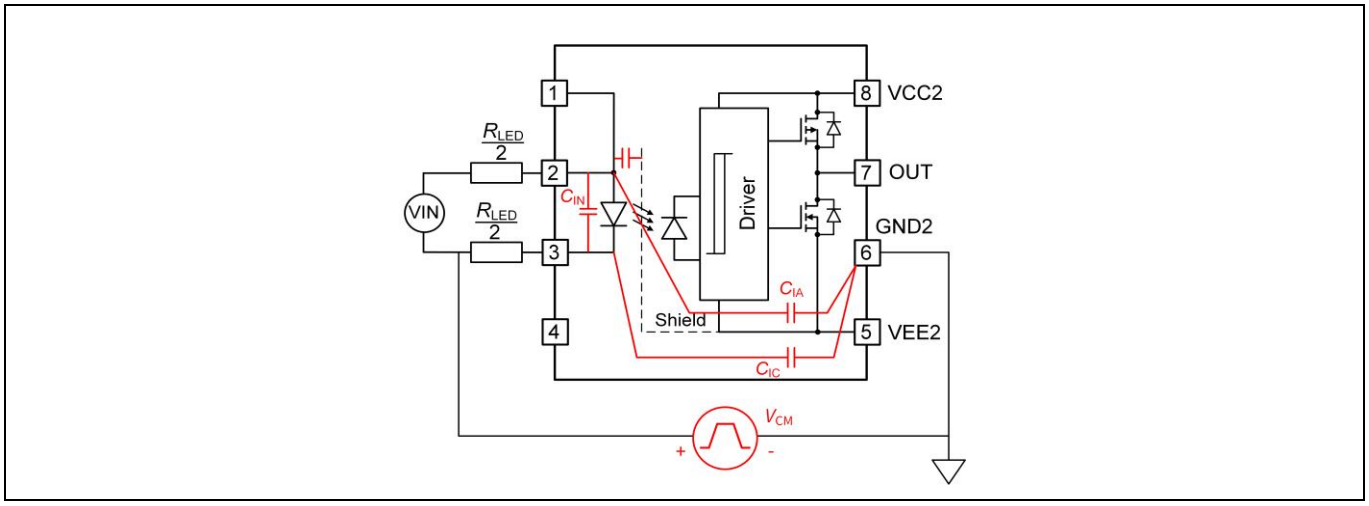

Figure 23 Example of "Improved Interference Circuit Model" for gate drive optocoupler

The current-limit resistor R_{LED} is split in two parts and placed at the anode and the cathode as well. With this extra effort, values of about 100 kV/µs or more can be reached.

2.8.2 CMTI for CT gate driver

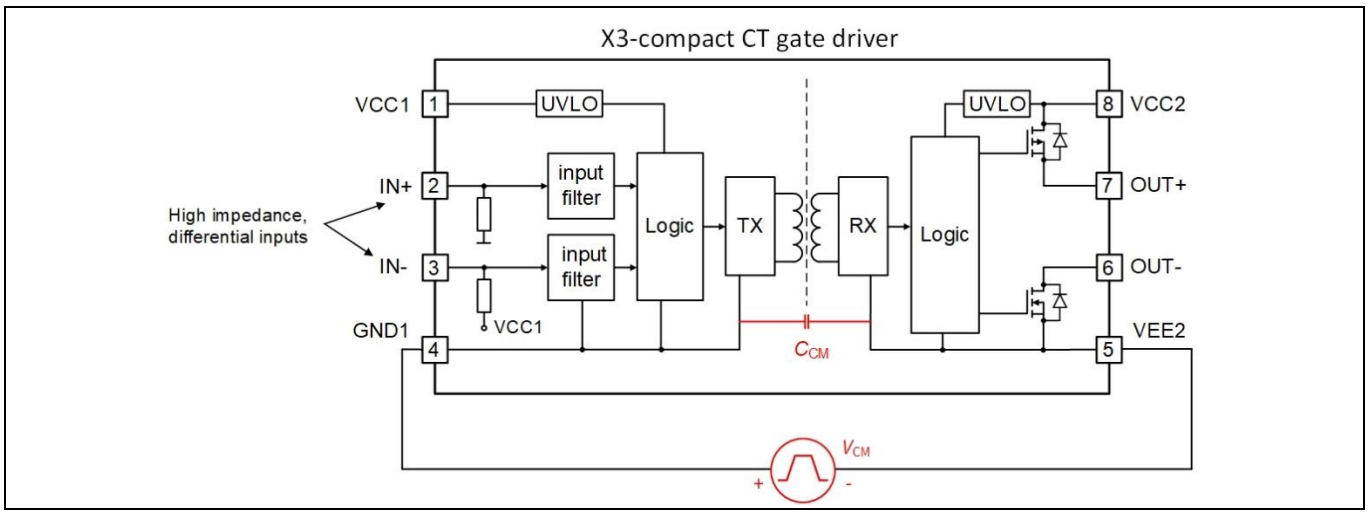

Figure 24 Example of Interference Circuit Model for X3-compact CT gate driver

Figure 24 shows the interference circuit model for X3-compact CT gate driver. Similar to the description in the previous chapter, a VCM source is connected between the ground at the input-side and the ground at the output-side. The largest proportion of the parasitic capacitance can be expected from the integrated transformer. The differential inputs also reject common-mode voltages. No extra effort is needed. Values ≥ 200 kV/µs can be reached (example 1ED31XXMC12H).

Due to the technological structure, the CT gate drivers are very robust against high-frequency transients.

2.9 Product lifetime and VDE 0884-11

For certain safety-sensitive applications, special tests according to the reinforced isolation standard are required. The tests required for this are found in the VDE-0884-11 standard, which will be replaced by the IEC-60747-17 standard, for which the VDE 0884-11 was used as a submission. This isolation standard is valid for the coreless-transformer-based gate drivers of the new generation, like X3 Compact (1ED31xx), 2L-SRC Compact (1ED32xx), X3 Analog (1ED34xx), X3 Digital (1ED38xx) and 1ED-F3 (1ED332x). In any case, both standards cover the particular breakdown mechanisms of CT couplers and are very difficult to meet. A short overview is shown in Table 4.

Table 4 Overview of standards and their tests

Test		VDE-0884-11 IEC-60747-17 (Magnetic coupling)	UL-1577 (Optocoupling and all others)	IEC60747-5-5 (Optocoupling)
Type	V_{IOTM} / V_{ISO}	Yes	Yes	Yes
	Partial discharge	Yes	N / A	Yes
	V_{IOSM}	Yes	Only in case of double isolation	Yes
	Lifetime test	**Yes**	N / A	No standards
Safety factors		Yes	N / A	N / A
Sample		Yes	Yes	Yes
Quarterly monitoring		Yes	N / A	Yes

Due to the fact that the Infineon`s CT gate drivers meet all these tests; the lifetime of these products is proven by a lifetime model and high safety margins.

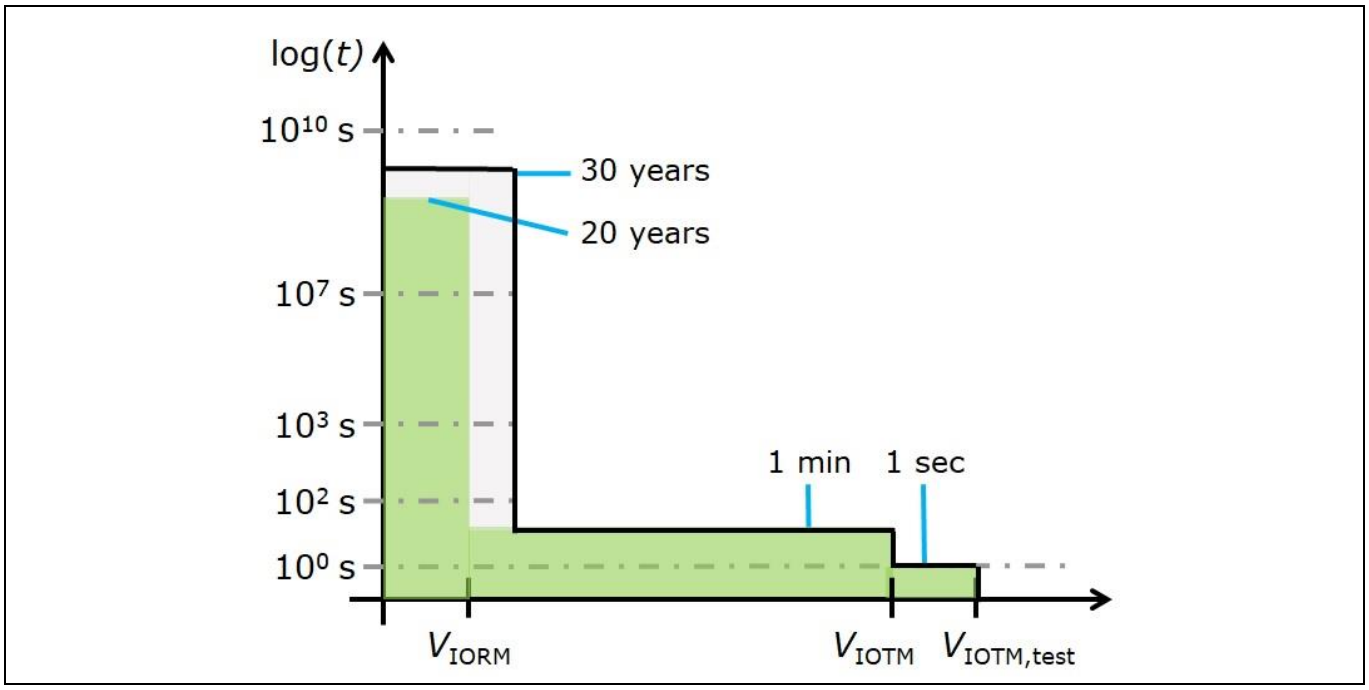

Figure 25 Lifetime testing

The new standard IEC 60747-17 assumes an application lifetime of 20 years by default. Additionally, the standard demands 100% test coverage for isolation in terms of transient overvoltages (V_{IOTM}). The test is performed at 1 second at a 20% higher test voltage.
These two requirements are shown in the green area. Infineon has additional margins and tests at 9.6 kV (peak) for a rating of V_{IOTM} equals to 8 kV (peak).
On top of that, the IEC 60747-17 imposes a safety factor of 1.5 in lifetime, while assuming an intrinsic failure rate of 1 ppm during this time.
This means that a CT gate driver runs up to 30 years without an isolation failure.

Opto coupled gate drivers do not have a lifetime model!

3 Summary of features

- The EiceDRIVER™ CT gate driver ICs from Infineon Technologies AG are solutions that are well suited for high- voltage applications
- Due to the good insulation properties of the coreless transformer technology, the CT gate drivers can currently be used in voltage classes of 2300 V
- Due to the high current carrying capability for example, the 14 A EiceDRIVER™ CT gate driver ICs are able to switch a wide variety of power switches, like IGBTs, Power MOSFETs and CoolSiC™ MOSFETs as well
- CT gate CT driver do not need extra effort for attaining high CMTI robustness
- A low input-current and CMOS-compatible inputs make the CT gate driver easy to use in single- and multichannel systems with lower BOM when longer transmission lines are used compared to optocoupled gate driver devices

Table 5 Summary of feature comparison

Lifetime, quality and reliability	**CT: FiT = 35** Opt: FiT = 1000	- No customer return for > 15 Mpcs / year over 15 years - Best industry FiT rate at Tj = 125 °C
Temperature drift & operating temperature	**CT: I: 35%, t: 5%** Opt: I: 128%, t: 35%	- Simplified gate driver power supply - Reduced control effort for timing - Best fit for driving SiC
Tight propagation delay matching & high output current (typ.)	**CT: < +/- 7 ns, 14 A** Opt: > 80 ns, 5 A	- Tight dead time values - Efficient driving of SiC in fast switching applications - Reduce losses in SiC based applications based on optimized dead times
Low input current consumption	**CT: 70 µA (typ.)** Opt: 7 mA [typ.)	- Multiple channel gate drive directly from a microcontroller - Reduced circuit complexity (BOM) & timing impact
Low input capacitance	**CT: << 1 pF** Opt: ≈ 25 pF	- Higher possible switching frequencies due to better low-pass behavior - Less sensitive to interference peaks
Input to output isolation voltage	**CT: 2300 V** Opt: 1414 V	- Better usability in applications with higher voltages - Higher margins against voltage peaks (over shoots)
Integrated input filter	**CT: Yes (35 ns)** Opt: No	- Better protection against false triggering due to interference spikes
Maximum power supply voltage output side (VCC2 - VEE2)	**CT: 35 V** Opt: 30 V	- Better application possibilities when using a wide range of power switches in terms of necessary gate voltages - Better protection against overvoltage's due to switching operation
Better common-mode transient immunity (CMTI)	**CT: ≥ 200 kV/µs** Opt: ≥ 100 kV/µs	- Highest resilience against large voltage spikes (dv/dt robustness) - Fast switching designs

4 How to change from gate drive optocoupler design to CT gate driver design

To use the advantages of the CT gate driver as described in Chapter 2 and summarized in Table 5, only a few minor changes are necessary for an existing design with a gate drive optocoupler to be converted into a new design with a CT gate driver. In the first step, of course, the PCB must be changed. The electrical circuits of both designs are shown in Figure 26 and Figure 27 and are similarly structured.

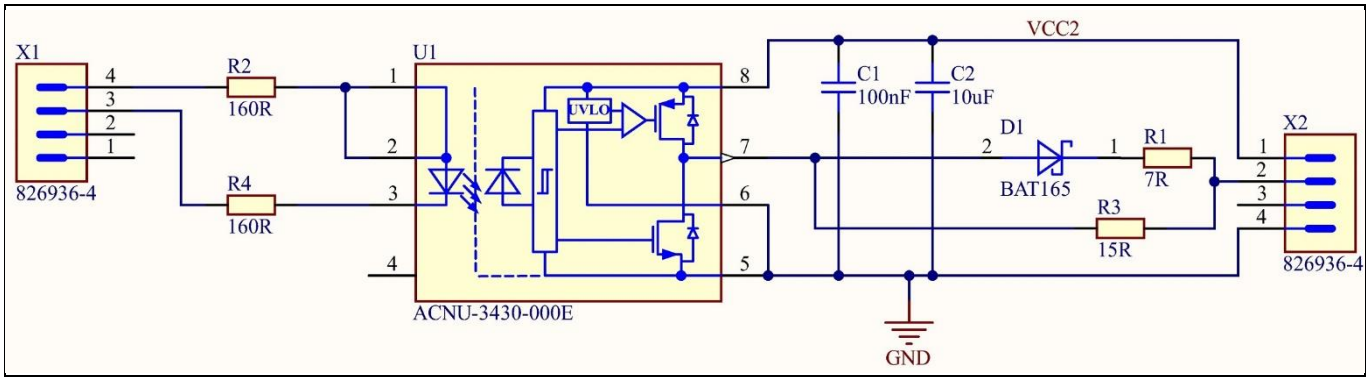

Figure 26 Example circuit for gate drive optocoupler ACNU-3430

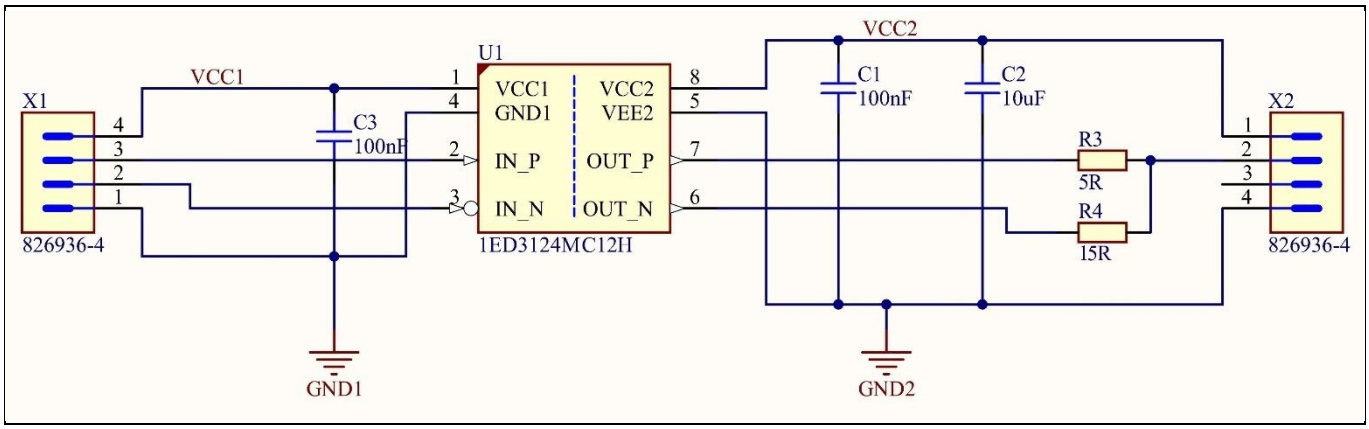

Figure 27 Example circuit for CT gate driver 1ED3124MC12H (X3 Compact)

Connector X1 (on each circuit) is the input side where the signals arrive from the microcontroller. The output side, connector X2 (on each circuit), connects the corresponding gate driver to the power switch.

The input side difference between both designs is mainly in the two input resistors, which have been wired according to Chapter 2.8.2 (Figure 23) to achieve a better CMTI behavior for the gate drive optocoupler. This is not necessary for the CT gate driver. Only a small capacitor (C3, Figure 27) is recommended here to absorb any voltage peaks that may occur. Also, in the CT gate driver design, both inputs were led out to allow differential driving. If this is not needed, for example the input IN_N could be connected directly to signal-ground (GND1).

The output side circuitry of the two designs is almost the same. The difference is due to the CT gate driver 1ED3124MC12H, because it has two outputs (OUT_P and OUT_N, see Figure 27). This feature makes it possible to separate the switch-on and switch-off behavior in the application due to the different values of the gate resistors R3 and R4. This is increasingly required in various applications, for example in drives applications.

Corresponding to the circuits in Figure 26 and 27, the boards are similar as shown in Figure 28 and Figure 29.

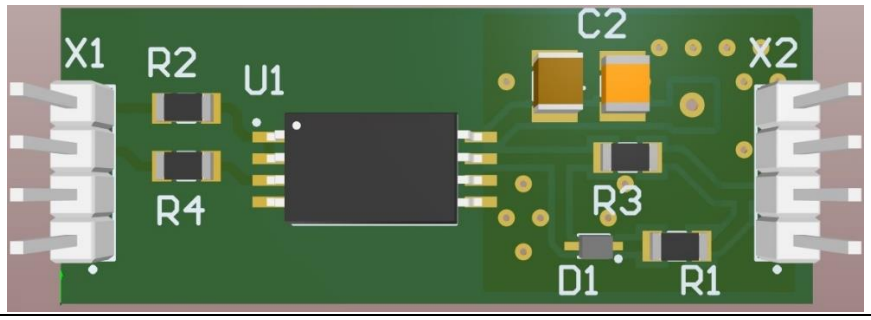

Figure 28 3D PCB view for gate drive optocoupler design with ACNU-3430

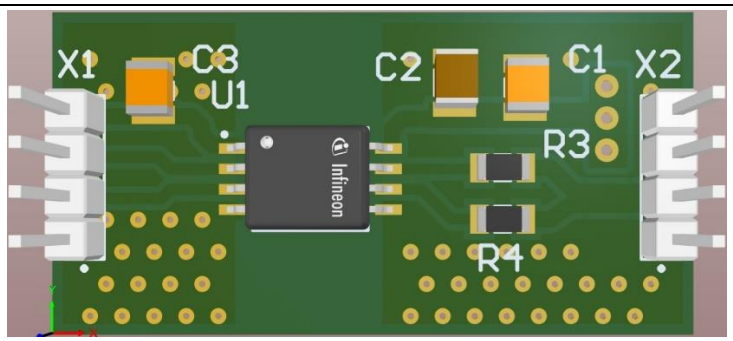

Figure 29 3D PCB view for CT gate driver design with 1ED3124MC12H (X3 Compact)

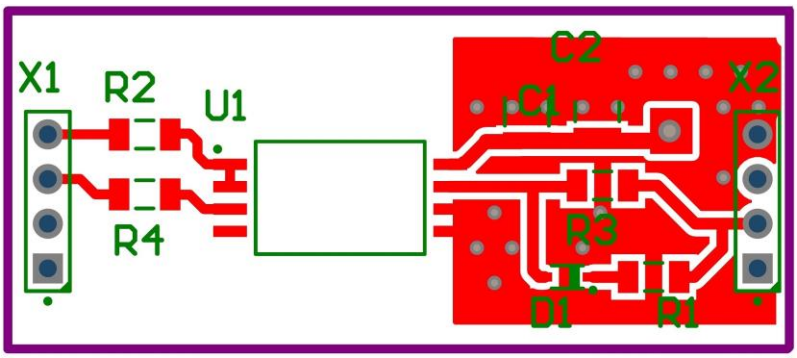

Figure 30 Top view of PCB for gate drive optocoupler design with ACNU-3430

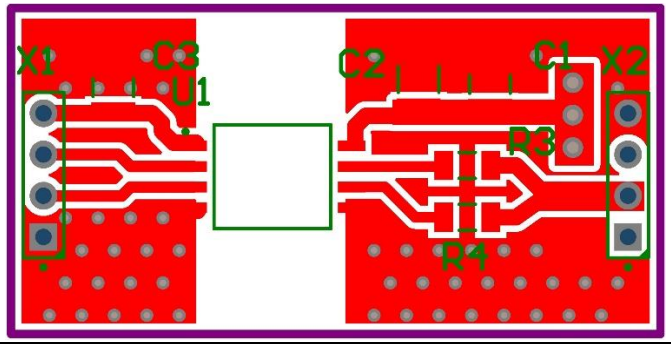

Figure 31 Top view of PCB for CT gate driver design with 1ED3124MC12H (X3 Compact)

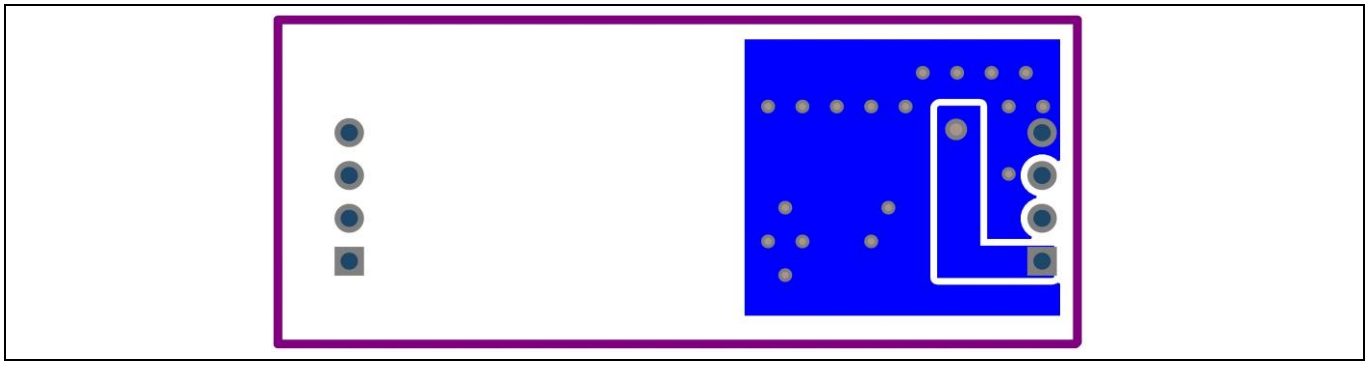

Figure 32 Bottom view of PCB for gate drive optocoupler design with ACNU-3430

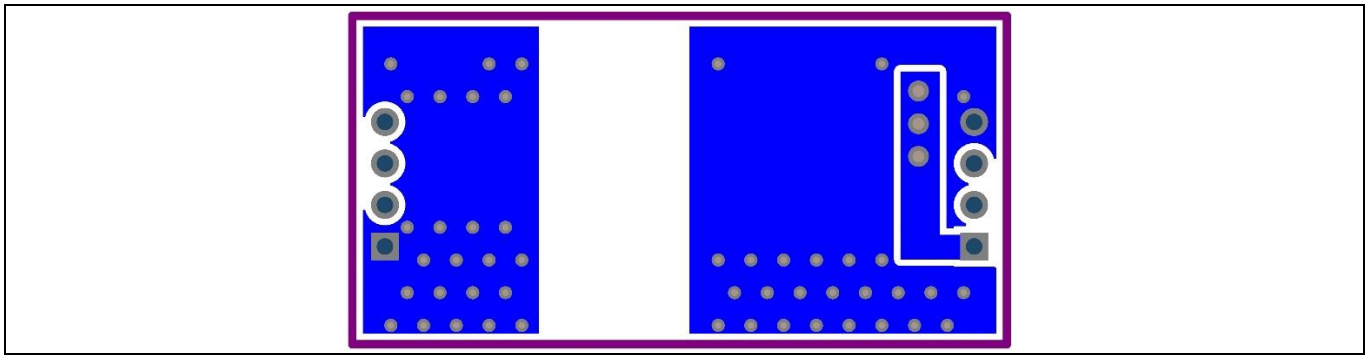

Figure 33 Bottom view of PCB for CT gate driver design with 1ED3124MC12H (X3 Compact)

There is no ground-shield on the entrance side of the design with the gate drive optocoupler (see Figure 30 and Figure 32), since there is no signal-ground (GND1) at the ACNU-3430. This signal could of course be obtained from the input cable, but is not necessary in this simple application.

It can be clearly shown that the electrical circuit and the PCB design of a gate driver unit with CT gate drivers is quite similar to that of a gate driver unit with gate driver optocouplers. For applications in the high- frequency range, the effort required for designs with gate drive optocouplers can increase considerably when long transmission lines are used between microcontroller and gate driver or for multi-channel applications.

If the advantages of the CT gate drivers described in Chapters 2.1 to 2.8 are also considered, it is fair to say that these gate drivers can be used to build robust and reliable gate driver units for all kinds of markets and applications.

5 References and appendices

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