

Application Note AN-1136

Discrete Power Quad Flat No-Lead (PQFN) Board Mounting Application Note

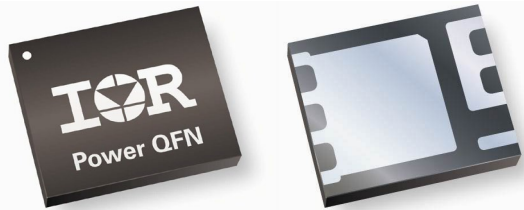
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The Discrete PQFN package family comprises efficient devices with a wide range of input voltages, all of which are lead-free as indicated by the PbF suffix after the part number (for example, [IRFH5300PbF](#)). There are various sizes and outlines. The main text of this application note contains guidance applicable to the whole range, while Appendix A contains device outlines, substrate layouts and stencil designs for each device. For more detail about individual devices, refer to the relevant product data sheet and package outline drawing. To simplify board mounting and improve reliability, International Rectifier manufactures PQFN devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

Introduction

Power Quad Flat No-Lead (PQFN) is a surface mount semiconductor technology designed primarily for board-mounted power applications. It eliminates unnecessary elements of packaging that contribute to higher inductance and resistance, both thermal and electrical, so that its power capabilities exceed those of comparably sized packages.



The PQFN package family includes various sizes and device outlines. The main text of this application note contains guidance applicable to the whole range, while Appendix A contains device outlines, substrate layouts and stencil designs for each device.

All recommendations are based on PCB-mounted devices that have been X-rayed and subjected to detailed analysis of post-reflow alignment and design feasibility. Devices with new outline designs, such as [IRFH7911PbF](#), were subject to more extensive study, including placement positions from ideal through various degrees of skew to erroneous.

To simplify board mounting and improve reliability, International Rectifier manufactures PQFN devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

For information about the SupIRBuck™ PQFN, refer to [AN-1132](#) and [AN-1133](#).

Device construction

PQFN devices are surface mounted and use current plastic-molding techniques with wire bond interconnects, as shown in Figure 1.

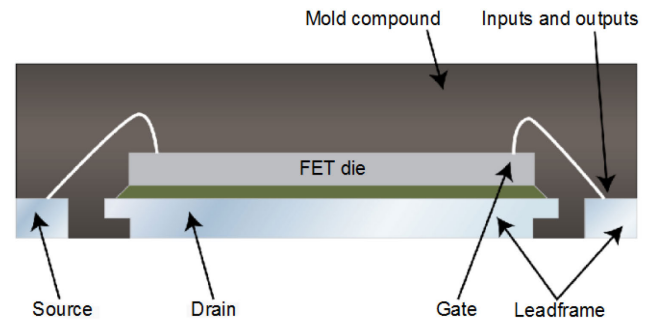


Figure 1 Sectional view

Figure 2 shows a sample contact configuration for a PQFN device. Specific pad assignments are shown in the data sheet for each product.

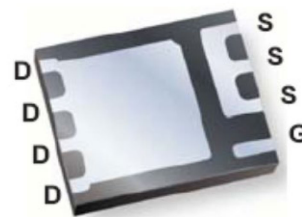


Figure 2 Sample PQFN contact pad configuration

Figure 3 shows how PQFN devices are labeled. Part number, batch number and date code are provided to support product traceability. The position of Pin 1 is indicated in two ways:

- A dot on the top side (Figure 4).
- A half-moon marking on the underside (Figure 5).

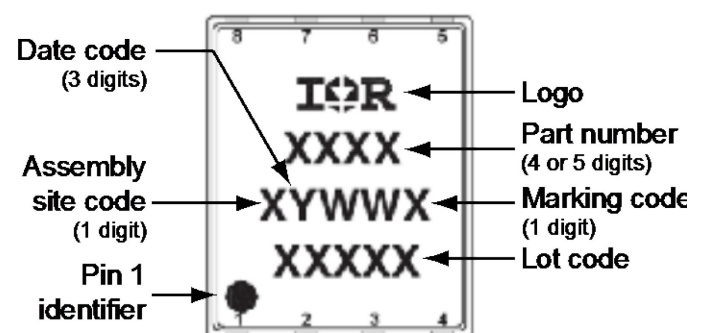


Figure 3 Device markings



Figure 4 Pin 1 indicator on an IRFH5300PbF

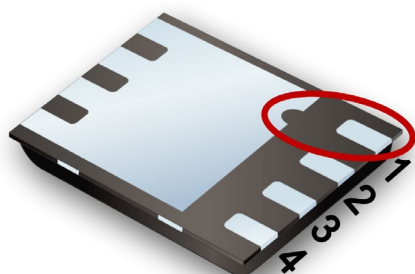


Figure 5 Pin 1 indicator on an IRFH5300PbF

Design considerations

Substrates

The PQFN was originally developed and evaluated for use with epoxy glass-woven substrates (FR-4). The test substrates were finished in Organic Solderability Preservative (OSP), but any of the numerous surface finishes available are suitable.

The substrate finish can affect the amount of energy required to make solder joints; this can in turn be a factor in solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids.

Substrate designs

To achieve low-loss track layouts, PQFN devices were designed for use with layouts that use solder-mask-defined (SMD) pad lands and non-solder-mask-defined (NSMD) lead lands. The devices were also evaluated with entirely NSMD layouts. The device outlines and the use of solder-mask-defined pads contribute to efficient substrate design. Large-area tracks optimize electrical and thermal performance.

If pad numbering is required to produce a component outline in the library of a CAD system, International Rectifier recommends that the conventions shown in Figure 6 are adopted. This makes it easier to discuss any issues that may arise during design and assembly.

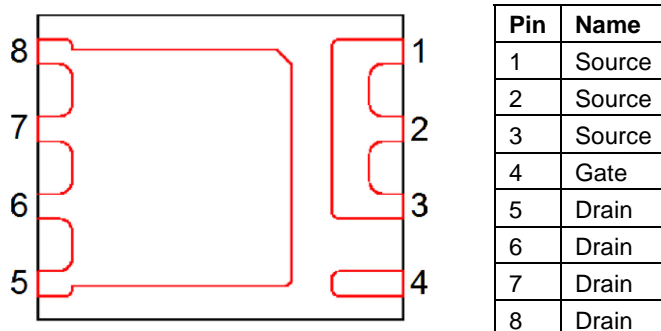


Figure 6 Recommended pad numbering

PQFN devices can be placed in parallel using simple layouts (Figure 7). International Rectifier recommends a minimum separation of 0.500mm (0.020"). The separation can be adjusted to reflect local process capabilities but should allow for rework. Micro-screen design and desoldering tool type may affect how closely devices are placed to each other and to other components.

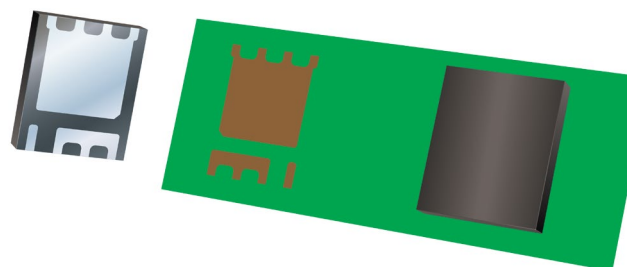


Figure 7 Placing PQFN devices in parallel

Refer to Appendix A for device outlines, substrate layouts and stencil designs for each package size and device outline in the PQFN range.

Assembly considerations

International Rectifier designed PQFN devices to be as easy as possible to assemble using standard surface mounting techniques. However, procedures and conditions can have a profound influence on assembly quality. It is therefore necessary to develop an effective process based on the individual requirements for the application.

Packaging

PQFN devices are supplied in tape and reel format (Figure 8).

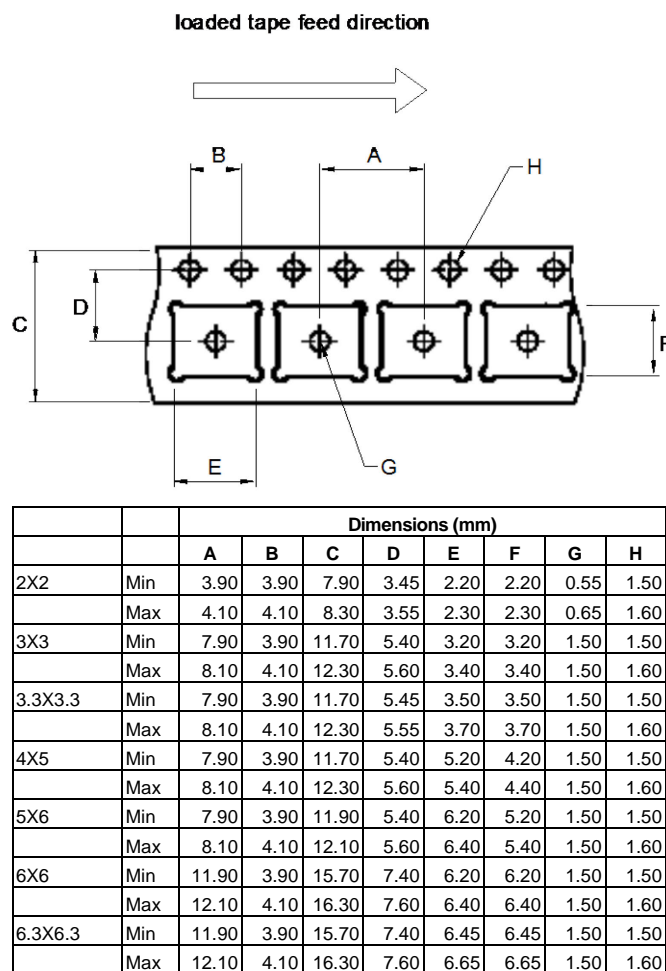


Figure 8 Tape and reel packaging

Storage requirements

PQFN devices are packed in sealed, nitrogen-purged, antistatic bags. The sealed bags provide adequate protection against normal light levels but it is prudent to avoid prolonged exposure to bright light sources. The bags also provide protection from the ambient

atmosphere. Devices in sealed, unopened bags have a shelf life of one year.

The package labeling shows whether devices should be treated as Moisture Sensitivity Level (MSL) 1, 2 or 3 after a bag has been opened. Appropriate storage is important to guarantee good solderability.

International Rectifier recommends that, when not in use, reels of devices should be resealed into the protective bags in which they were supplied.

Solder pastes

International Rectifier evaluated different types of solder paste from various manufacturers. The properties of pastes vary from manufacturer to manufacturer, meaning that some perform better than others. In general, high slumping pastes tend to suffer more from solder balling than slump-resistant pastes. In addition, some pastes appear to be more prone to voiding than others.

Solder alloys, metal contents and flux constituents all influence the rheology of the solder paste. This in turn influences how the paste reacts during processing. The assembly and board-level reliability of the PQFN package have only been evaluated using lead-free pastes (Sn96.5 Ag3.0 Cu0.5).

Evaluations of lead-free devices used a reflow profile that conforms to IPC/JEDEC standard J STD 020C (July 2004 revision). As devices may be subjected to multiple reflows when PCBs are double-sided or reworked, the evaluations used up to three reflows. International Rectifier recommends that customers should conform to J STD 020C in setting reflow profiles and should not exceed three reflows.

Stencil design

The stencil design is instrumental in controlling the quality of the solder joint. Appendix A shows stencil designs that have given good results with the recommended substrate outlines. These are based on reductions of 25% for the pad lands and 20% for the lead lands, which is equivalent to printing 75% and 80% of the area respectively using a stencil thickness of 0.127mm (0.005"). The design should be revised for other stencil thicknesses.

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

Post-reflow evaluations can help to assess how a stencil is performing within a given process. Two main problem areas can be addressed by improving stencil design:

- **Solder balling around the perimeter of the die.**
This can be caused by too much solder paste, in which case the stencil might need to be reduced by more than 25%. The reduction can be symmetrical but biasing it unevenly may help to prevent solder balling; the stencil designs in Appendix A have apertures moved further from the die edge for this reason. Solder balling can result from other external factors, such as the moisture content of the board and incorrect ramp rates or insufficient soak times in the reflow profile. Leadless packages like PQFN can sometime accentuate existing deficiencies within a process.
- **Misshapen joints.** If the joints are smaller or seem to be only partially made, this might suggest that there is insufficient solder to make the joint. If, however, the joints have what appear to be additional areas extending from their edges, they are usually the result of too much solder; this is almost certainly the case if solder balls are also present. Insufficient solder can also cause voiding but this is more likely to arise from other factors, including surface finish, solder paste and substrate condition.

Device placement

Inaccurate placement may result in poor solder joints or in devices being tilted and/or misaligned. Ideally, PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes but, during evaluations, devices centered themselves from placement inaccuracies of more than 0.300mm. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Reflow equipment

PQFN devices are suitable for assembly using surface mount technology reflowing equipment and are recommended for use with convection, vapor phase and infrared equipment. PbF qualified devices have a good resistance to short-term exposure to high temperatures, making them suitable for reflow profiles of up to 260°C (measured by attaching a thermocouple to a PQFN device).

There are no special requirements for successful assembly, but all reflow processes used in evaluation and qualification complied with the recommendations of solder paste suppliers. Using incorrect reflow profiles can cause solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids; if such problems arise, the reflow profile should be checked.

The PQFN package is designed to have superior thermal resistance properties. For this reason, it is essential that the core of the substrate reaches thermal equilibrium during the pre-heating stage of the reflow profile to ensure that adequate thermal energy reaches the solder joint.

Inspection

For comprehensive information on inspecting board-mounted PQFN devices, refer to the PQFN Inspection Application Note ([AN-1154](#)).

As with all QFN packaging, the best way to inspect devices after reflow is through a combination of visual inspection of the peripheral solder joints and X-ray imaging of the connections directly under the package.

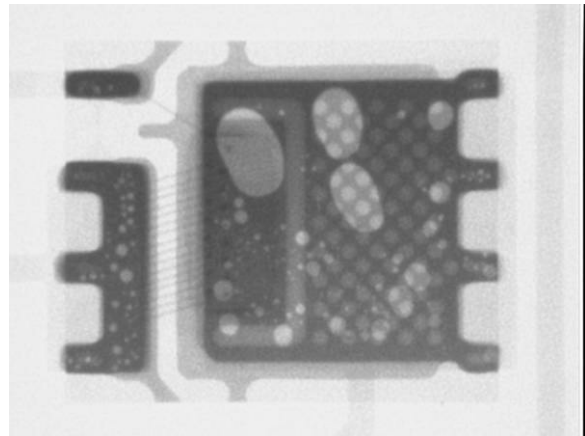


Figure 9 X-rays of PQFN

Figure 9 is a typical X-ray image of a board-mounted PQFN device, which shows the solder joints, device alignment and solder voiding level. Regarding solder joint voiding, most customers use 25–30% as the acceptable limit, often citing industry standards such as IPC-A-610 or IPC-7093. However, having tested board-mounted devices deliberately voided up to 45%, International Rectifier has been unable to detect any deterioration in electrical or thermal performance in application compared with devices voided to 5–10%.

Rework guidelines

Modern rework stations for ball grid array and leadless packages often use two heating stages:

- The first stage heats the substrate, either with a conventional hot-plate or a hot-air system. This reduces the amount of heating required from the hot-air de-soldering tool, which in turn reduces the risk of damaging either the substrate or surrounding components.
- The second stage uses a hot-air system for localized heating, often with the option of unheated air for faster cooling of the solder interconnections on the replaced device; this improves the solder grain structure.

The device placement mechanism or arm usually has a hot-air de-soldering gun as part of the pick head, equipped with a vacuum cup and thermocouple. Once the solder reflow temperature has been reached, the vacuum is automatically engaged to allow the device to be removed from the substrate. This reduces the risk of causing damage by premature removal.

Most rework stations have the facility to attach a micro-stencil supplied by the vendor, with the aperture design being supplied by the user. The apertures are aligned with the pads on the board before manually screening the solder paste. Alternatively, it is possible to use a standalone micro-stencil and squeegee to apply the paste.

The objective of rework is to remove a non-functional device and replace with a functional device. International Rectifier does not recommend reusing devices removed from a substrate. To permit subsequent failure analysis, take care when removing devices not to exacerbate the existing failure.

To replace a PQFN device:

Note: If you usually bake to remove residual moisture before rework, insert your normal procedure here.

1. Heat the site to approximately 100°C (150°C for lead-free assembly) using the substrate heating stage.

Note: Pb devices are qualified for a maximum reflow peak temperature of 240°C (260°C for PbF devices). To avoid overheating the device or substrate, adjust the settings on your equipment to achieve a maximum air temperature of 300°C.

2. Lower the placement arm to bring the de-soldering tool into contact with the device. When the device and the solder interconnects reach reflow temperature, lift the placement arm to remove the device from the substrate. Discard the device.
3. Clear residual solder from the site using a blade-type de-soldering tool and de-soldering braid. Clear residual flux using a flux-reducing agent. Take care in cleaning the site: damage to the solder-resist may produce undesirable results.
4. When the site is ready, apply new solder paste with a micro-stencil and squeegee.
5. Position a new device on the vacuum tip of the placement head and lower the placement arm until the device is in contact with the solder paste.
6. Switch off the vacuum on the placement head and retract the placement arm, leaving the device in place.
7. Heat the site to approximately 100°C (150°C for lead-free assembly) using the substrate heating stage.
8. Use the de-soldering tool to heat both device and solder interconnects to reflow temperature, waiting until all the solder has reflowed.
9. Retract the arm, leaving the device in place. Cool as quickly as possible.

Mechanical test results

International Rectifier has subjected board-mounted PQFN devices to extensive mechanical tests, conducted in accordance with industry standards and practices. The devices tested were 5x6mm. Given that all PQFN devices are made in the same way, other devices should perform to the same high standard.

This section contains summarized results for bend tests, drop tests and vibration tests.

Standards

JEDEC JESD22B113 Board Level Cyclic Bend Test

JEDEC JESD22B111 Board Level Drop Test

MIL-STD-810F Method 514 Proc. 1. Random Vibration

Bend tests

Method

Cycling bend testing was carried out in accordance with JEDEC JESD22B113, Board Level Cyclic Bend Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Products.

Boards were designed as specified in JESD22B113 with nine PQFN devices per board. Board thickness was maintained to 0.75mm (0.030"). The span of the support anvils was 110mm and the span of the load anvils was 75mm. The sinusoidal load was cycled at 3Hz with a 2mm displacement. Boards were cycled for 200,000 cycles.

Results

Figure 10 shows the results from cyclic bend testing.

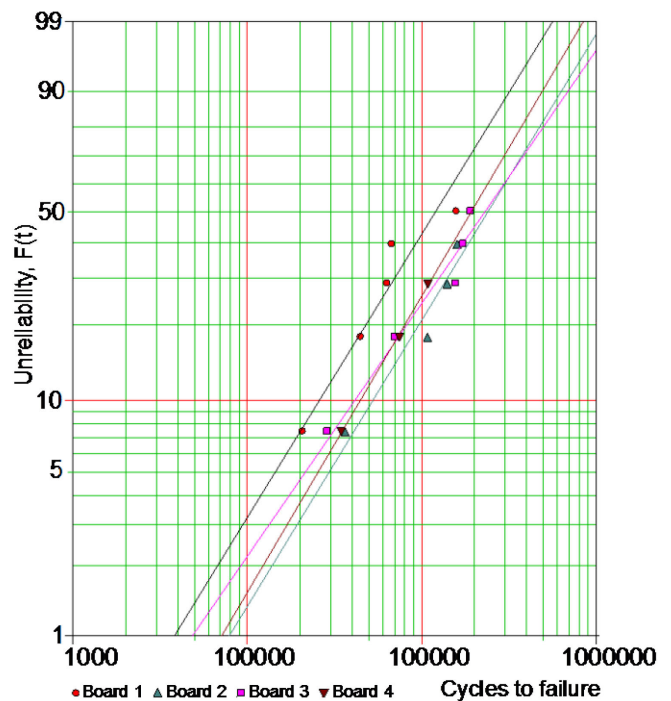


Figure 10 Cyclic bend test results for PQFN devices

It is important to note that no qualification requirements are imposed in JESD22B113. As stated in the specification, "The test duration of 200,000 cycles should not be construed as an expectation of reliability; it is only a recommendation to get enough component failures to generate a valid probability failure plot or to limit the duration of testing. The reliability requirements should be separately determined between the supplier and customer." In some respects, the PQFN can be considered relatively robust as fewer than 60% of the components, as called out in JESD22B113, failed before the test limitation of 200,000 cycles.

Drop tests

Method

Drop testing was carried out in accordance with JEDEC JESD22B111, Board Level Drop Test Method of Components for Handheld Electronic Products.

Boards were designed as specified in JESD22B111 with fifteen PQFN devices per board. Board thickness was maintained to 0.75mm (0.030"). The populated assemblies weighed 22g. The calibrated acceleration was 1500G, 0.5 millisecond duration, half-sine pulse which resulted from a 15.5" drop onto a steel block. Figure 11 shows the shock pulse. Each drop was measured with an accelerometer. Each board was dropped 30 times.

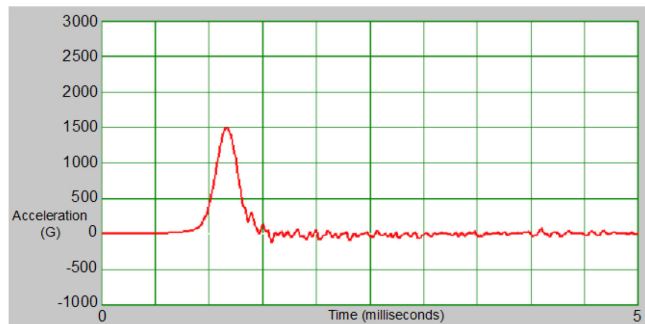


Figure 11 Shock pulse for shock test

Results

60 devices were tested and there were no failures.

Vibration tests

Method

Vibration testing was carried out as per MIL-STD-810F (Method 514, Proc. 1, Cat. 20 – composite wheeled vehicle). The board design used in vibration testing was equivalent to the design specified in JEDEC JESD22B111, with fifteen PQFN devices per board. A total of four boards were subjected to vibration testing.

The PQFN boards were subjected for four hours to random vibration from 5Hz to 500Hz, experiencing $1.9g_{rms}$ ($18.6ms^{-2}_{rms}$) with an acceleration spectral density value of $0.005g^2Hz^{-1}$ ($[0.48ms^{-2}]^2Hz^{-1}$). Figure 12 shows the bandpass filter frequency chart.

Based on experience with the interconnect failure behavior of similar packages, the devices were only subjected to out-of-plane loading (Z-direction). The test is a pass-fail test and the PQFN devices were tested after the vibration was completed.

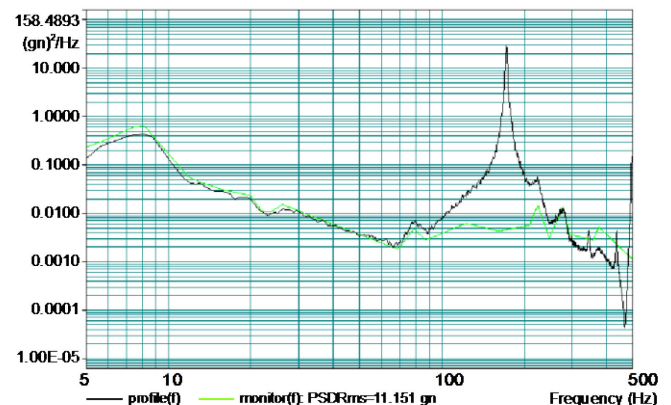


Figure 12 Bandpass filter frequency chart

Results

60 devices were tested and there were no failures.

Appendix A Model-specific data

This appendix contains the following information about various PQFN devices:

- Device outline drawing
- Recommended substrate/PCB layout
- Suggested designs for stencils of 0.127mm (0.005") thickness

The footprint and stencil designs are recommendations only, and may need to be adjusted to specific requirements. During a study conducted on various package types, International Rectifier found the designs gave repeatable device alignment and proper solder connections.

For more details about individual devices, and to find out their size and outline, refer to the relevant product data sheet.

Interchangeability

Devices of different sizes are not interchangeable.

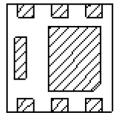
For 5x6mm devices, the A, B, E and G outlines are similar except for their Source pads. The A outline has one E-shaped pad, while the B, E and G outlines have three separate pads. These outlines have been reviewed for footprint compatibility and are excellent substitutes for each other. The C outline is application-specific and cannot be used in designs for other outlines.

Acknowledgements

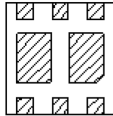
International Rectifier would like to thank DfR Solutions for providing the studies needed to develop the substrate/PCB layouts and stencil designs.

2x2mm and 3x3mm outlines

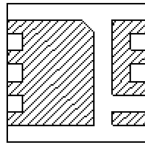
2x2 Single



2x2 Dual

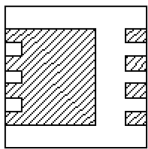


3x3 A

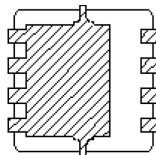


3.3x3.3mm outlines

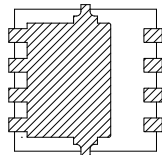
3.3x3.3 Single A



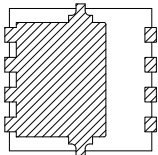
3.3x3.3 Single B



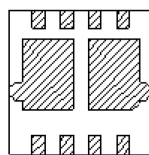
3.3x3.3 Single C



3.3x3.3 Single G

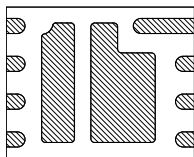


3.3x3.3 Dual



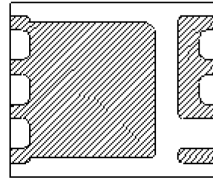
4x5mm outlines

4x5 Dual

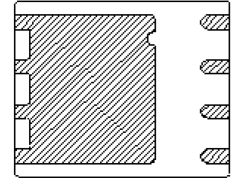


5x6mm outlines

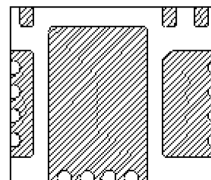
5x6 A



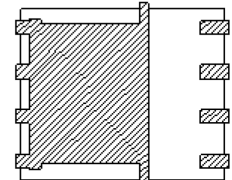
5x6 B



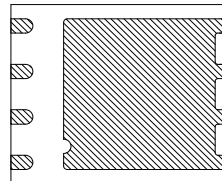
5x6 C



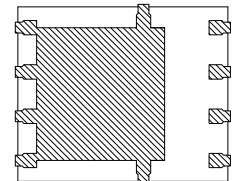
5x6 E



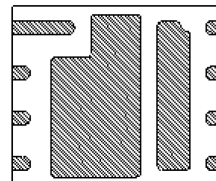
5x6 F



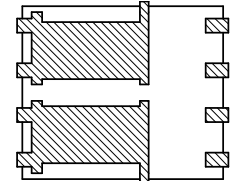
5x6 G



5x6 H

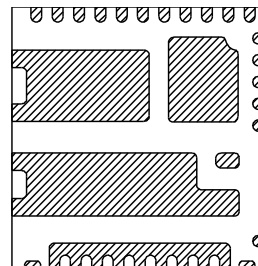


5x6 Dual



6x6mm outlines

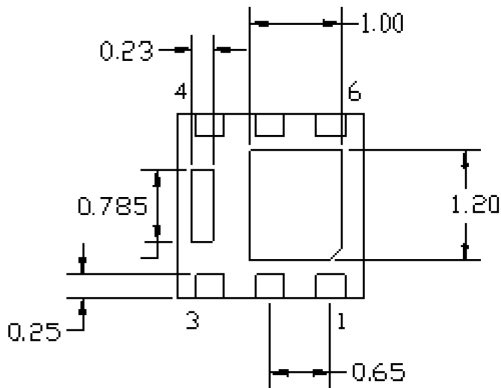
6x6



Appendix A.1 2x2 Single devices

Device outline

Figure A.1.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

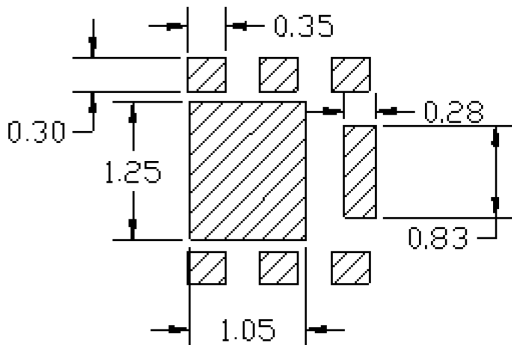


(dimensions in mm)

Figure A.1.1 2x2 Single device outline

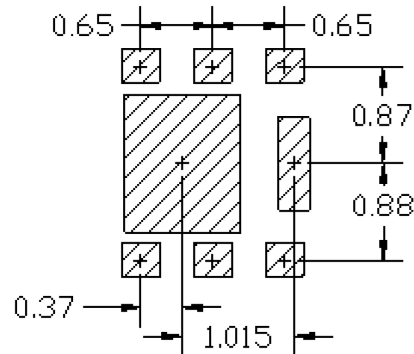
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.1.2 (a and b).



(dimensions in mm)

Figure A.1.2(a) 2x2 Single substrate/PCB layout



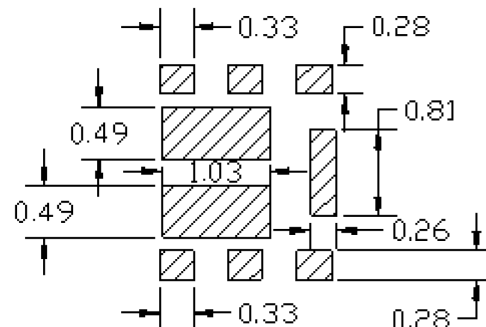
(dimensions in mm)

Figure A.1.2(b) 2x2 Single substrate/PCB layout

Stencil design

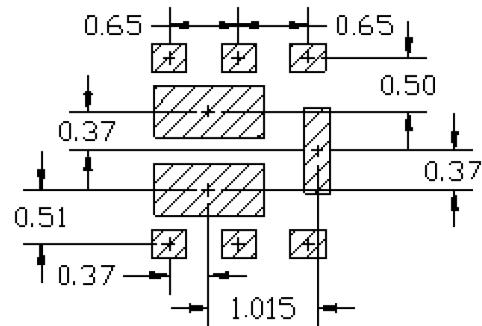
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.1.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.1.3(a) 2x2 Single stencil design



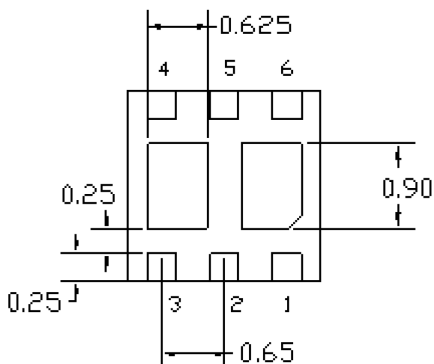
(dimensions in mm)

Figure A.1.3(b) 2x2 Single stencil design

Appendix A.2 2x2 Dual devices

Device outline

Figure A.2.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

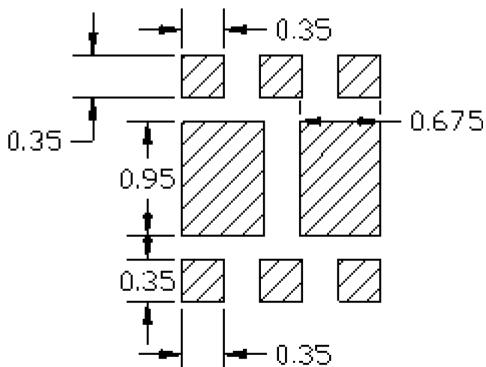


(dimensions in mm)

Figure A.2.1 2x2 Dual device outline

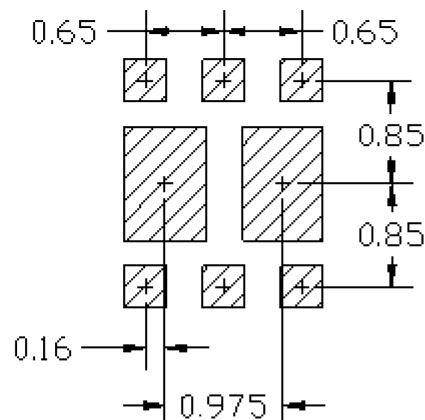
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.2.2 (a and b).



(dimensions in mm)

Figure A.2.2(a) 2x2 Dual substrate/PCB layout



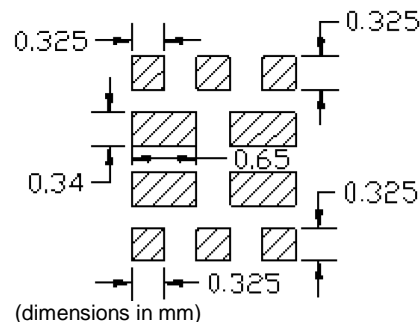
(dimensions in mm)

Figure A.2.2(b) 2x2 Dual substrate/PCB layout

Stencil design

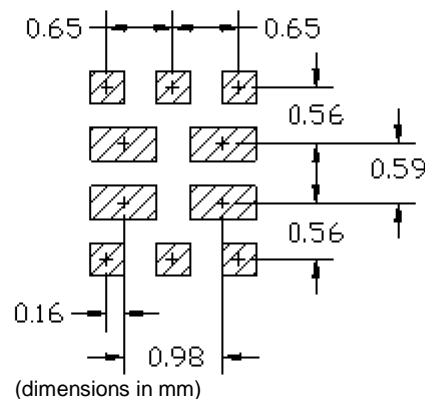
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.2.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.2.3(a) 2x2 Dual stencil design



(dimensions in mm)

Figure A.2.3(b) 2x2 Dual stencil design

Appendix A.3 3x3 A devices

Device outline

Figure A.3.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

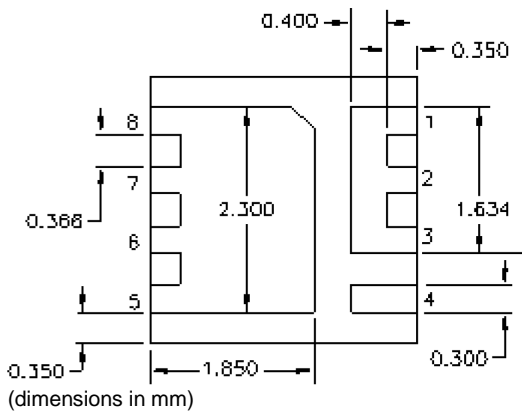


Figure A.3.1 3x3 A device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.3.2 (a and b).

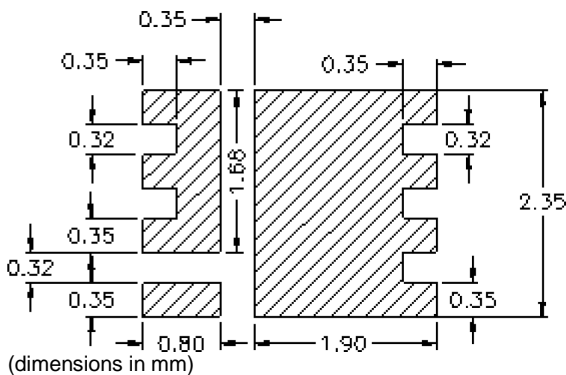


Figure A.3.2(a) 3x3 A substrate/PCB layout

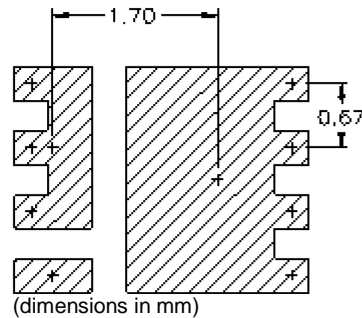


Figure A.3.2(b) 3x3 A substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.3.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

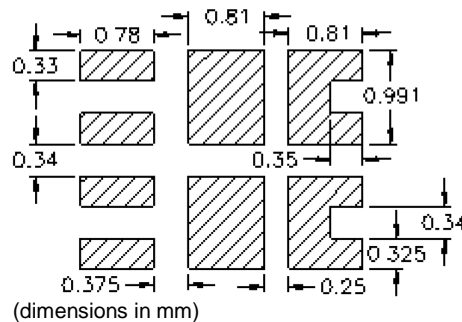


Figure A.3.3(a) 3x3 A stencil design

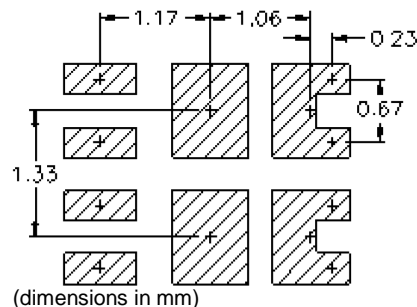


Figure A.3.3(b) 3x3 A stencil design

Appendix A.4 3.3x3.3 Single A devices

Device outline

Figure A.4.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

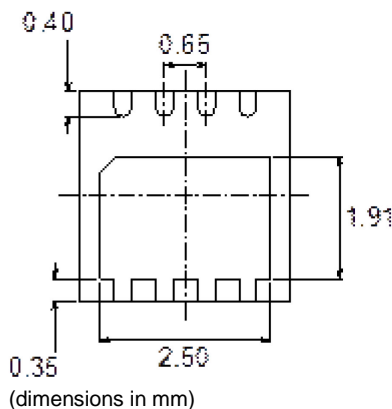


Figure A.4.1 3.3x3.3 Single A device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.4.2 (a and b).

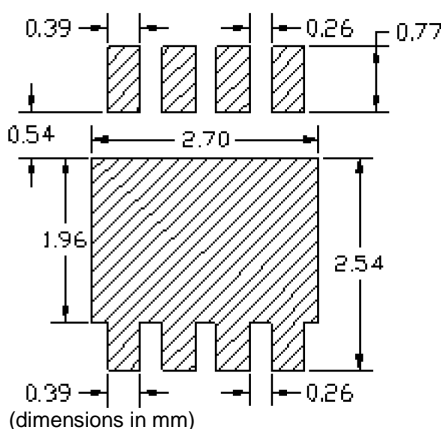


Figure A.4.2(a) 3.3x3.3 Single A substrate/PCB layout

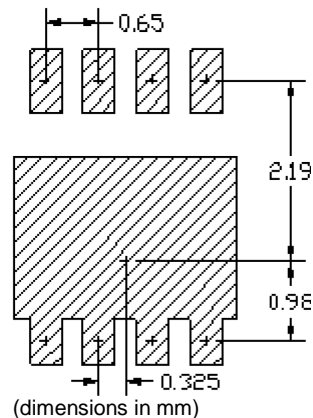


Figure A.4.2(b) 3.3x3.3 Single A substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.4.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

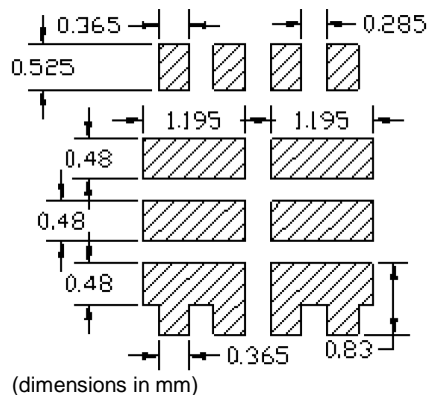


Figure A.4.3(a) 3.3x3.3 Single A stencil design

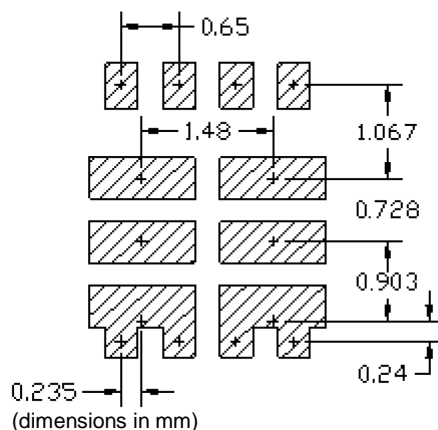


Figure A.4.3(b) 3.3x3.3 Single A stencil design

Appendix A.5 3.3x3.3 Single B devices

Device outline

Figure A.5.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

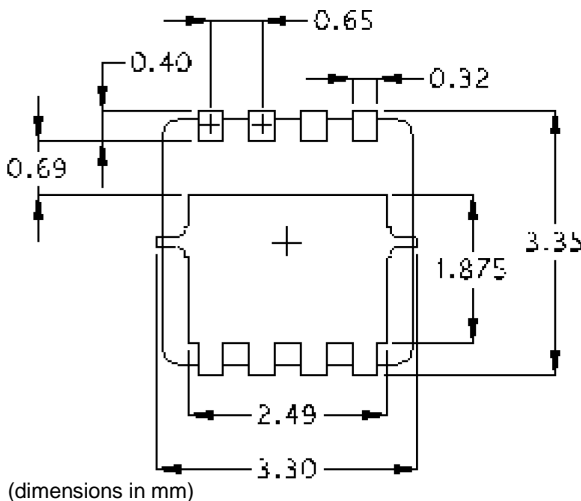


Figure A.5.1 3.3x3.3 Single B device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.5.2 (a and b).

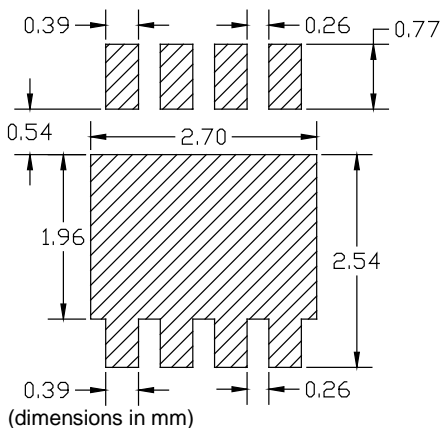


Figure A.5.2(a) 3.3x3.3 Single B substrate/PCB layout

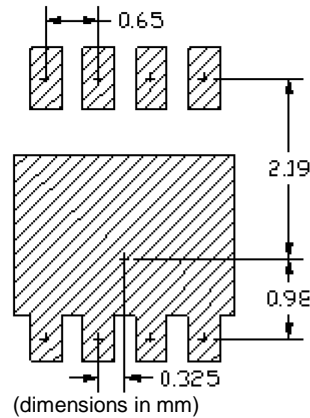


Figure A.5.2(b) 3.3x3.3 Single B substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.5.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

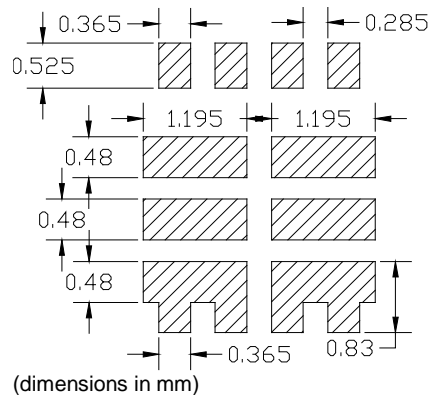


Figure A.5.3(a) 3.3x3.3 Single B stencil design

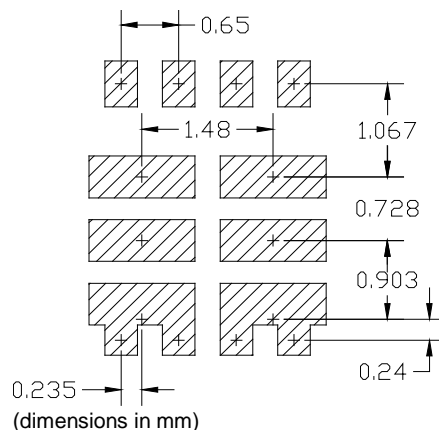


Figure A.5.3(b) 3.3x3.3 Single B stencil design

Appendix A.6 3.3x3.3 Single C devices

Device outline

Figure A.6.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

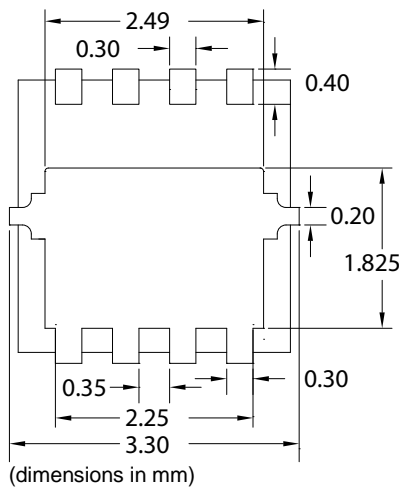


Figure A.6.1 3.3x3.3 Single C device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.6.2 (a and b).

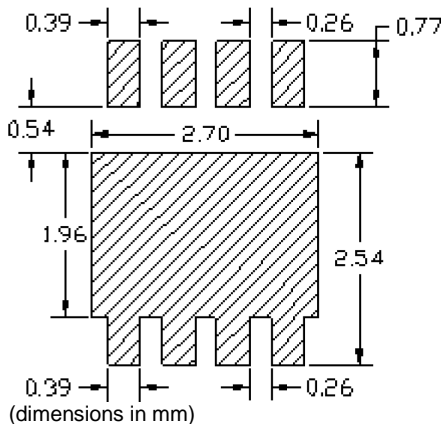


Figure A.6.2(a) 3.3x3.3 Single C substrate/PCB layout

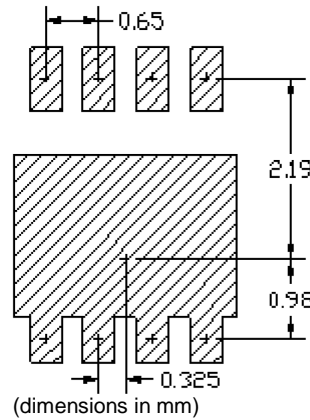


Figure A.6.2(b) 3.3x3.3 Single C substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.6.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

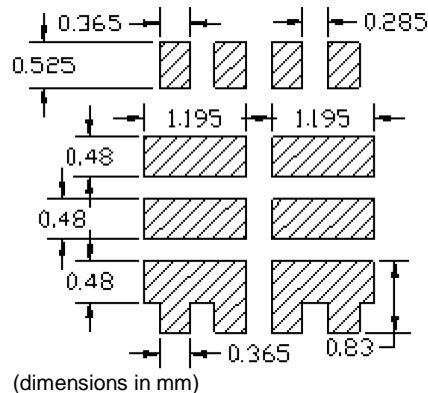


Figure A.6.3(a) 3.3x3.3 Single C stencil design

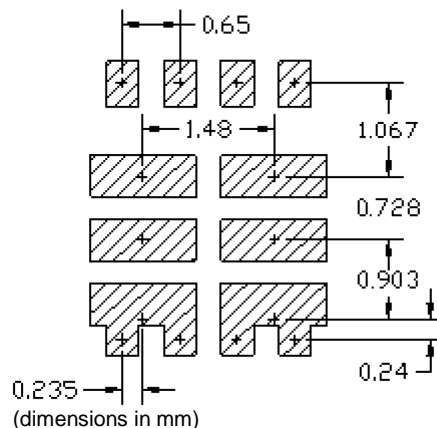


Figure A.6.3(b) 3.3x3.3 Single C stencil design

Appendix A.7 3.3x3.3 Single G devices

Device outline

Figure A.7.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

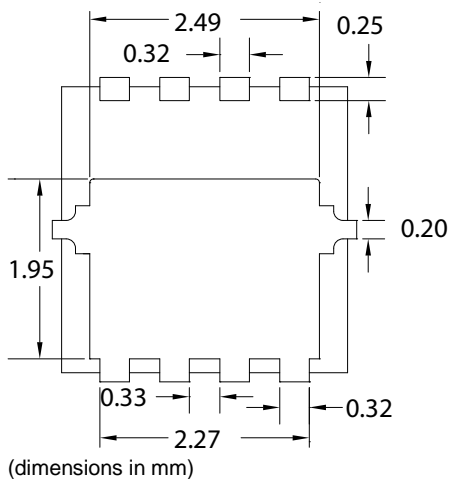


Figure A.7.1 3.3x3.3 Single G device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.7.2 (a and b).

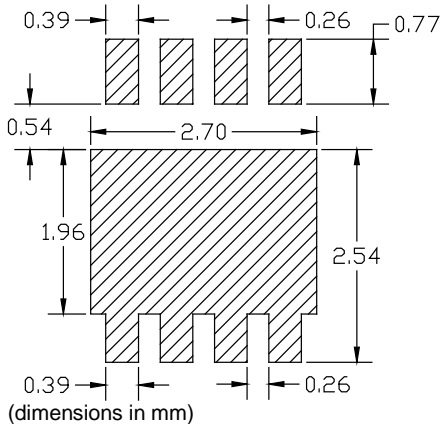


Figure A.7.2(a) 3.3x3.3 Single G substrate/PCB layout

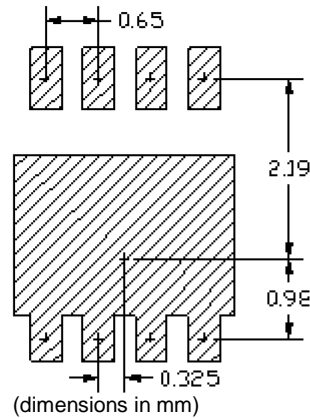


Figure A.7.2(b) 3.3x3.3 Single G substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.7.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

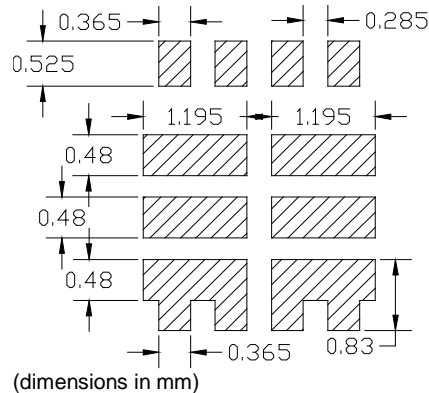


Figure A.7.3(a) 3.3x3.3 Single G stencil design

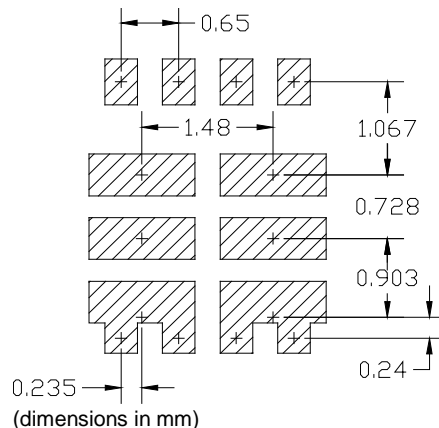
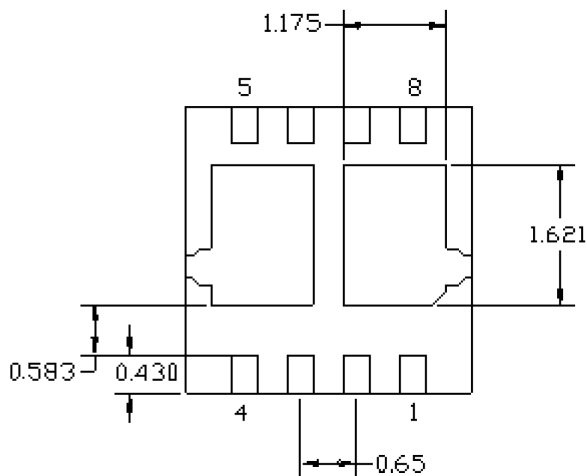


Figure A.7.3(b) 3.3x3.3 Single G stencil design

Appendix A.8 3.3x3.3 Dual devices

Device outline

Figure A.8.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

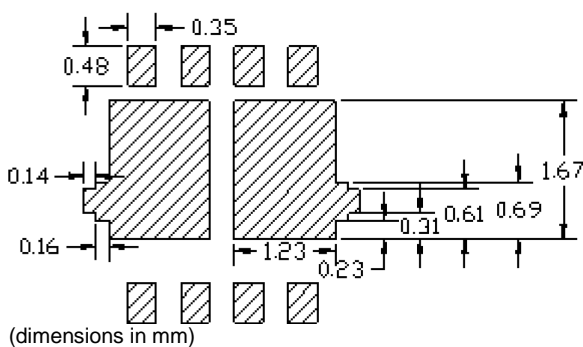


(dimensions in mm)

Figure A.8.1 3.3x3.3 Dual device outline

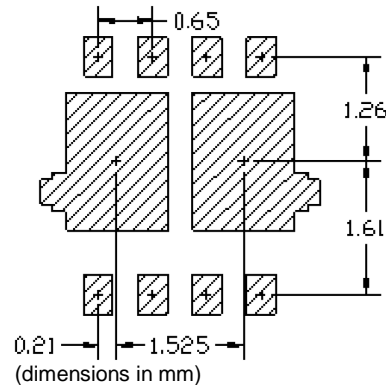
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.8.2 (a and b).



(dimensions in mm)

Figure A.8.2(a) 3.3x3.3 Dual substrate/PCB layout



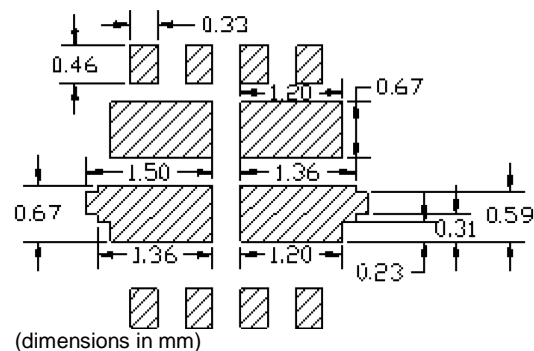
(dimensions in mm)

Figure A.8.2(b) 3.3x3.3 Dual substrate/PCB layout

Stencil design

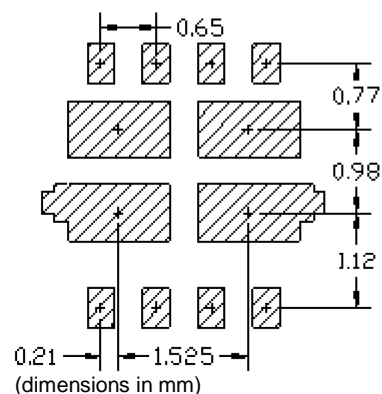
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.8.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.8.3(a) 3.3x3.3 Dual stencil design



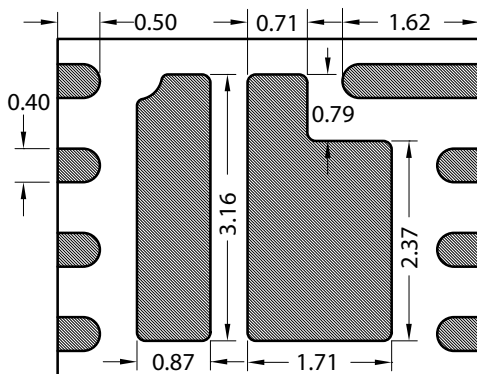
(dimensions in mm)

Figure A.8.3(b) 3.3x3.3 Dual stencil design

Appendix A.9 4x5 Dual devices

Device outline

Figure A.9.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

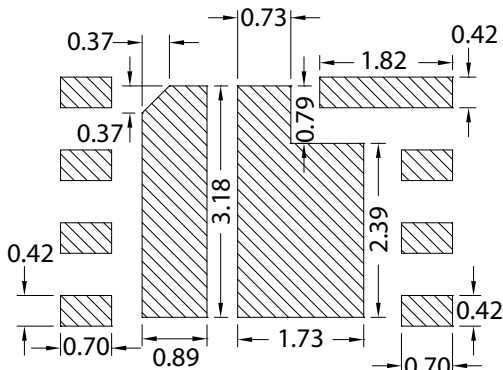


(dimensions in mm)

Figure A.9.1 4x5 Dual device outline

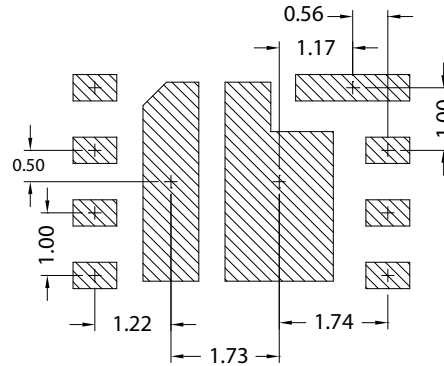
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.9.2 (a and b).



(dimensions in mm)

Figure A.9.2(a) 4x5 Dual substrate/PCB layout



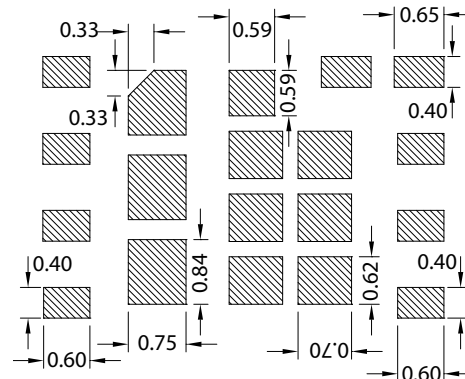
(dimensions in mm)

Figure A.9.2(b) 4x5 Dual substrate/PCB layout

Stencil design

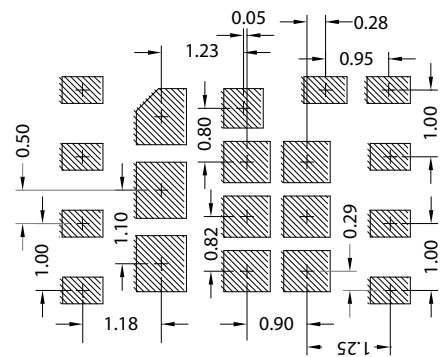
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.9.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.9.3(a) 4x5 Dual stencil design



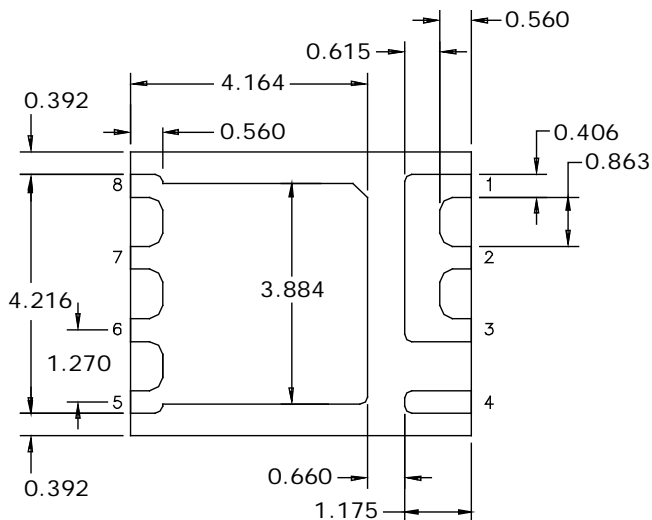
(dimensions in mm)

Figure A.9.3(b) 4x5 Dual stencil design

Appendix A.10 5x6 A devices

Device outline

Figure A.10.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

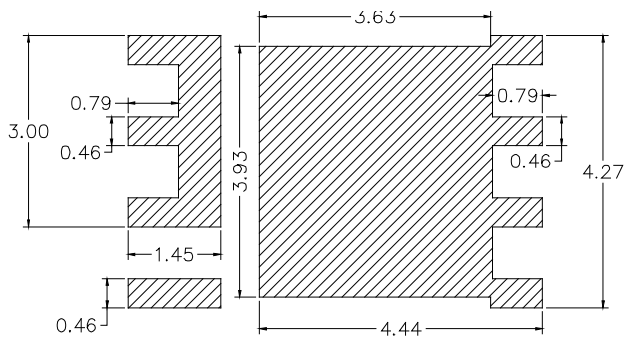


(dimensions in mm)

Figure A.10.1 5x6 A device outline

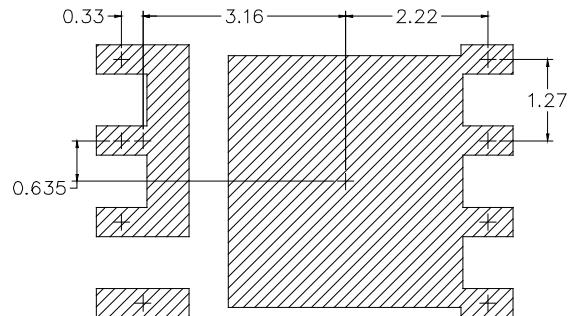
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.10.2 (a and b).



(dimensions in mm)

Figure A.10.2(a) 5x6 A substrate/PCB layout



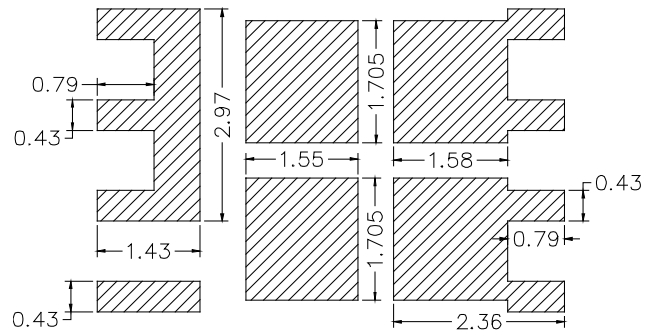
(dimensions in mm)

Figure A.10.2(b) 5x6 A substrate/PCB layout

Stencil design

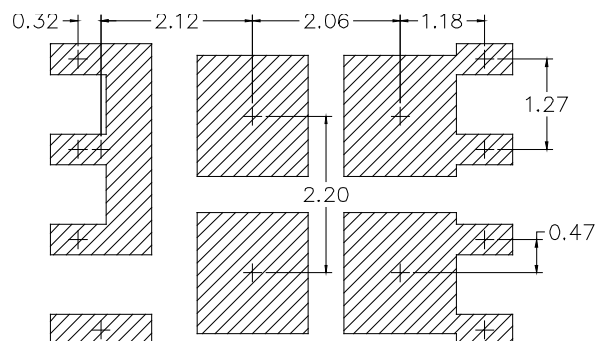
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.10.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.10.3(a) 5x6 A stencil design



(dimensions in mm)

Figure A.10.3(b) 5x6 A stencil design

Appendix A.11 5x6 B/E/G devices

Note: These devices may be supplied as B, E or G devices. They share common substrate/PCB layouts and stencil designs.

Device outline

Figure A.11.1 (a, b and c) show the outlines for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

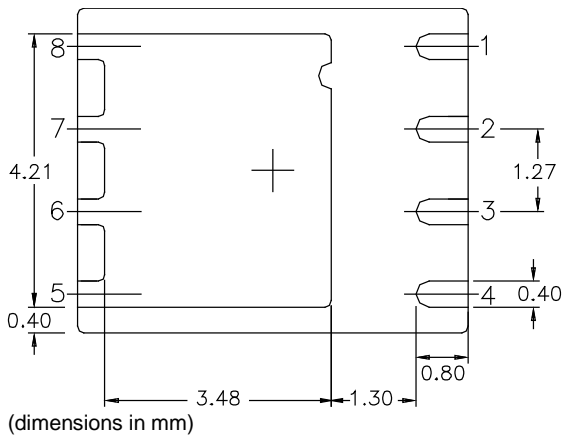


Figure A.11.1(a) 5x6 B device outline

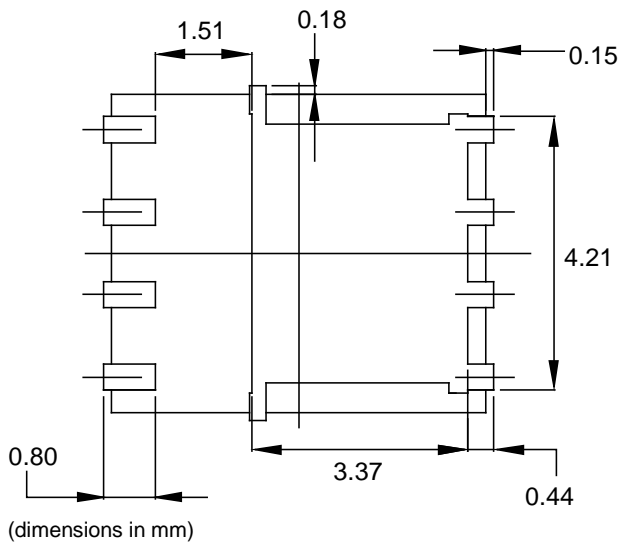


Figure A.11.1(b) 5x6 E device outline

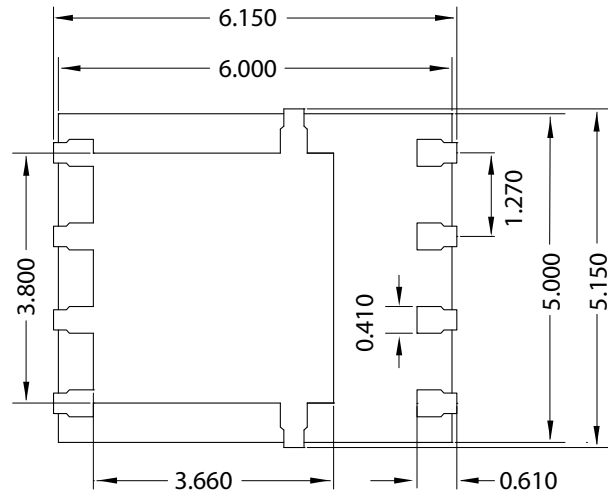


Figure A.11.1(c) 5x6 G device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.11.2 (a and b).

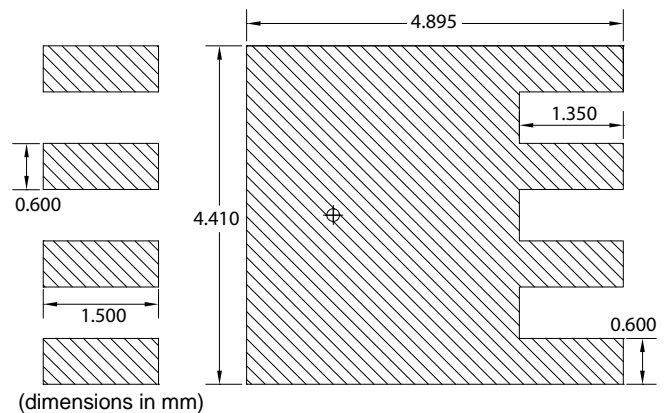


Figure A.11.2(a) 5x6 B/E/G substrate/PCB layout

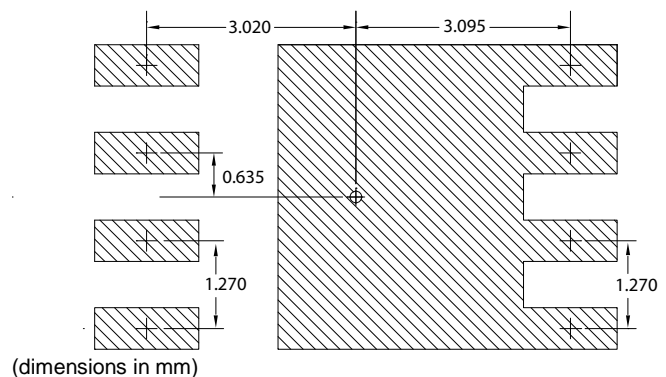


Figure A.11.2(b) 5x6 B/E/G substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.11.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

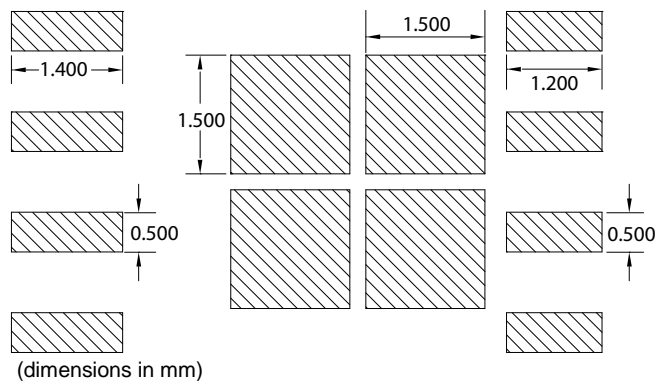


Figure A.11.3(a) 5x6 B/E/G stencil design

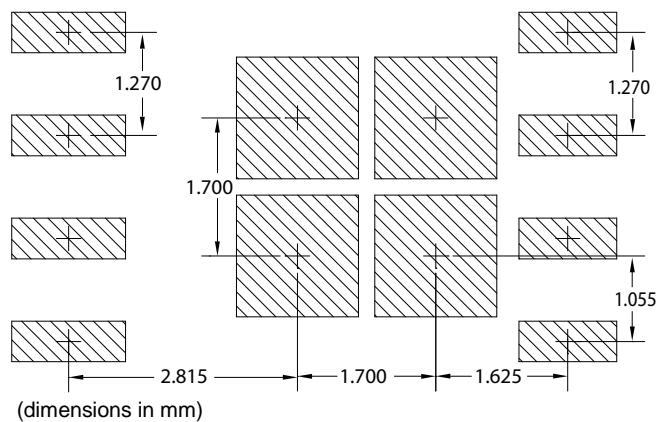


Figure A.11.3(b) 5x6 B/E/G stencil design

Appendix A.12 5x6 C devices

Device outline

Figure A.12.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

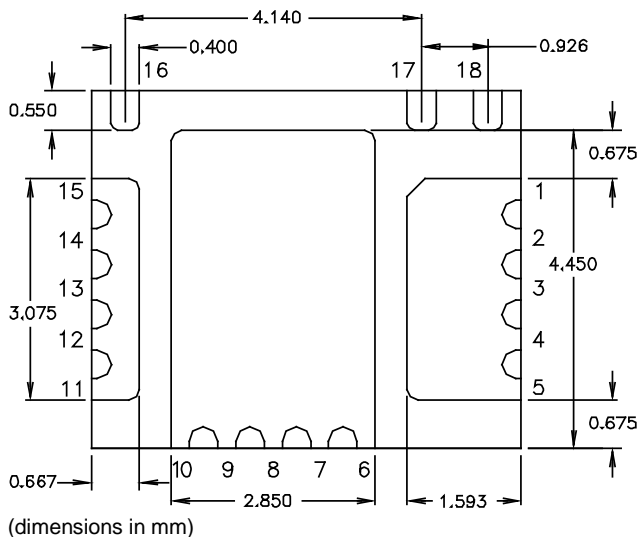


Figure A.12.1 5x6 C device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.12.2 (a and b).

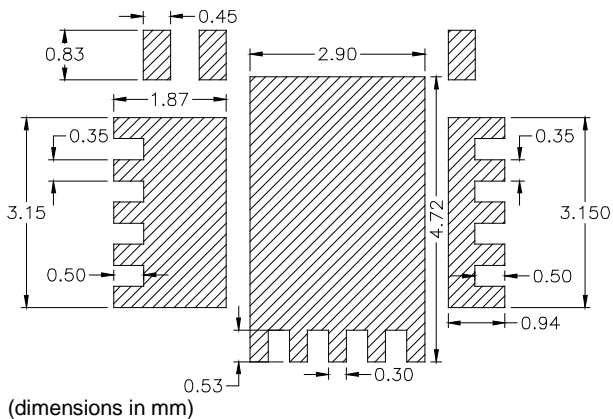
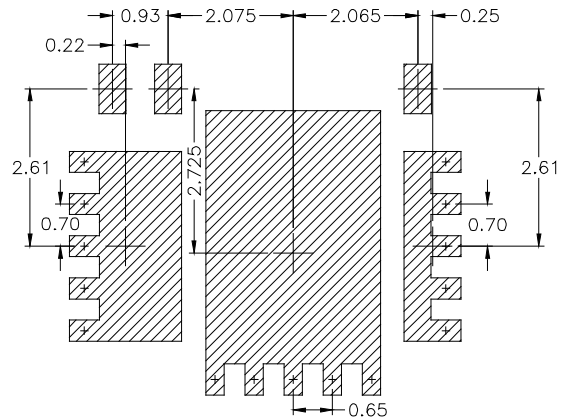


Figure A.12.2(a) 5x6 C substrate/PCB layout



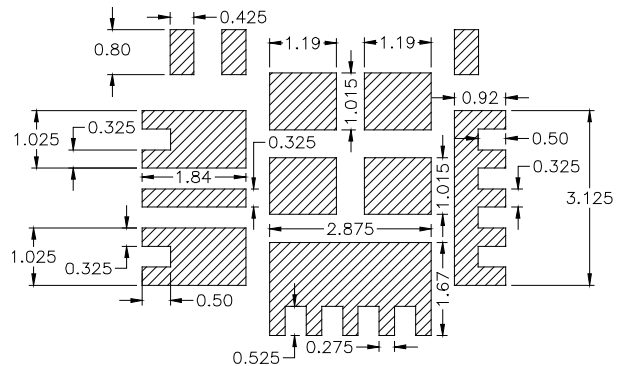
(dimensions in mm)

Figure A.12.2(b) 5x6 C substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.12.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.12.3(a) 5x6 C stencil design

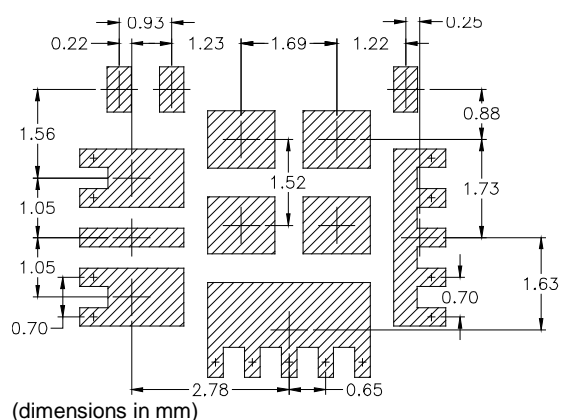


Figure A.12.3(b) 5x6 C stencil design

Appendix A.13 5x6 F devices

Device outline

Figure A.13.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

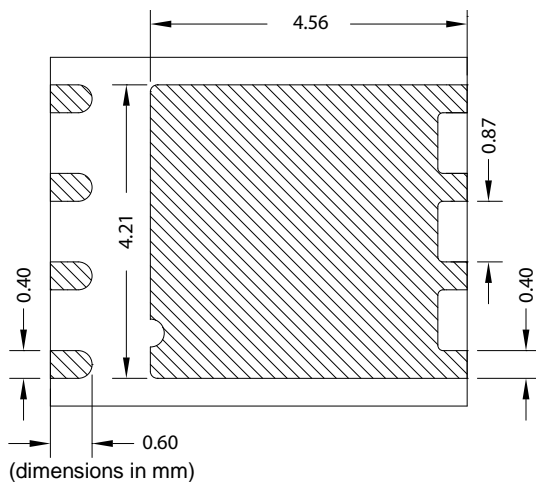


Figure A.13.1 5x6 F device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.13.2 (a and b).

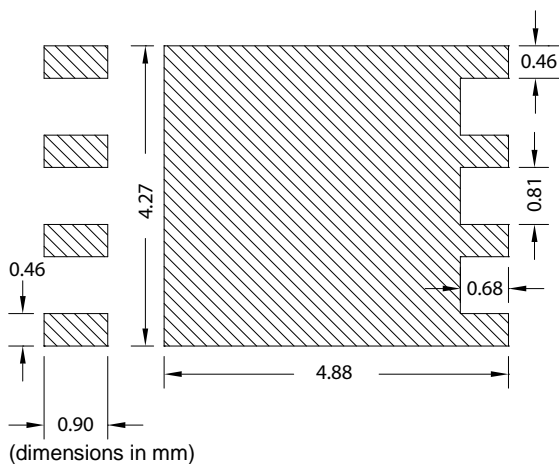


Figure A.13.2(a) 5x6 F substrate/PCB layout

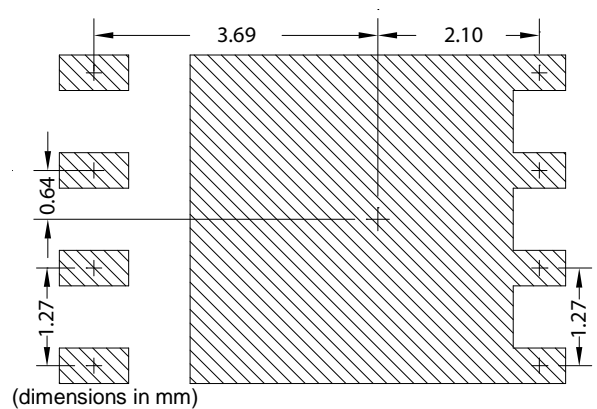


Figure A.13.2(b) 5x6 F substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.13.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

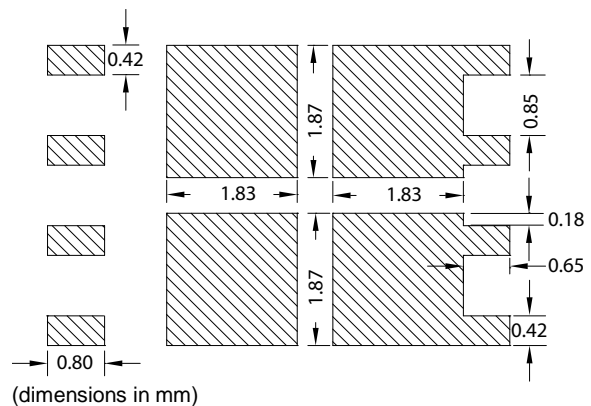


Figure A.13.3(a) 5x6 F stencil design

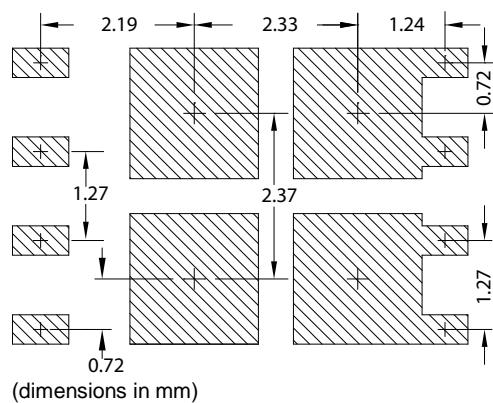


Figure A.13.3(b) 5x6 F stencil design

Appendix A.14 5x6 H devices

Device outline

Figure A.14.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

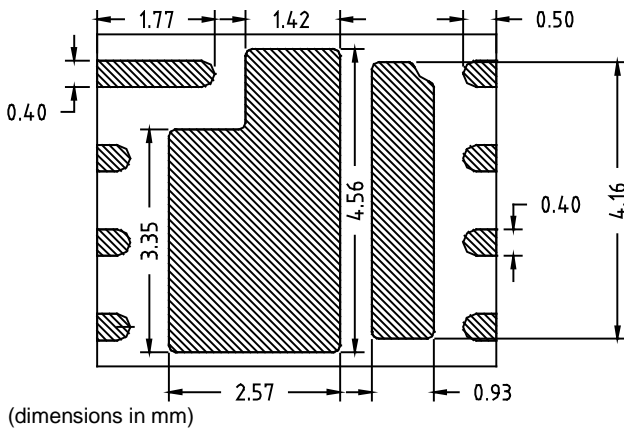


Figure A.14.1 5x6 H device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.14.2 (a and b).

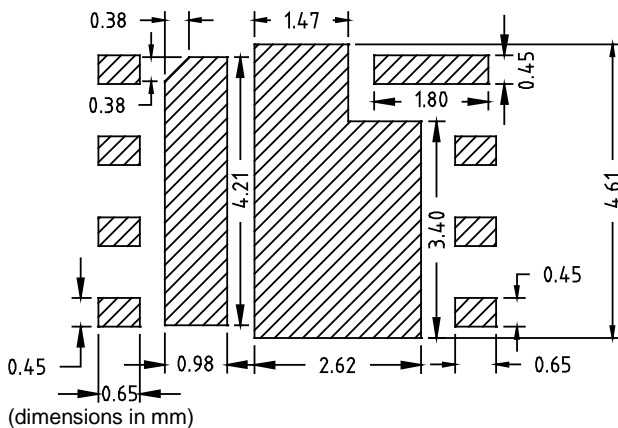
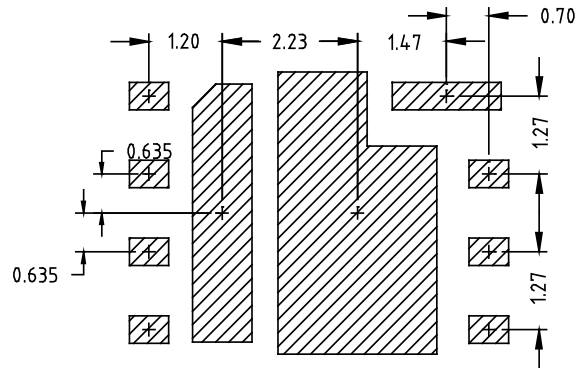


Figure A.14.2(a) 5x6 H substrate/PCB layout



(dimensions in mm)

Figure A.14.2(b) 5x6 H substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.14.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

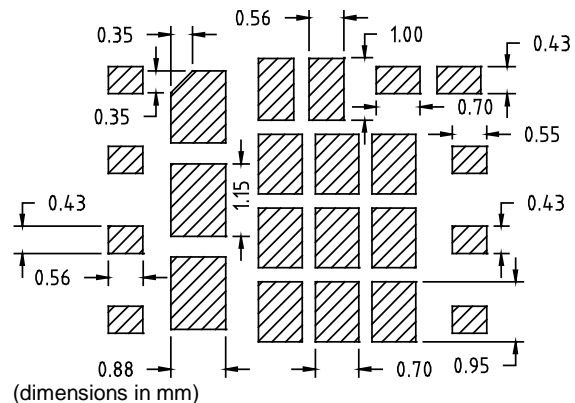


Figure A.14.3(a) 5x6 H stencil design

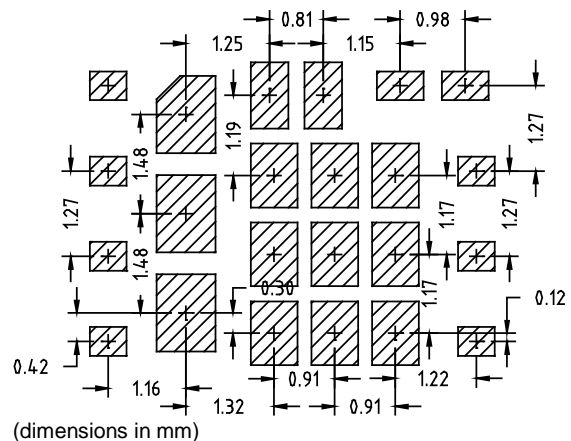
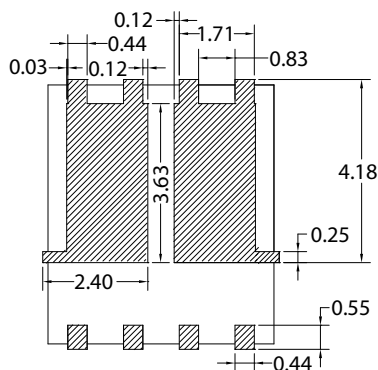


Figure A.14.3(b) 5x6 H stencil design

Appendix A.15 5x6 Dual devices

Device outline

Figure A.15.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

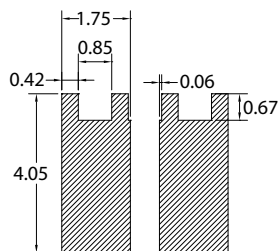


(dimensions in mm)

Figure A.15.1 5x6 Dual device outline

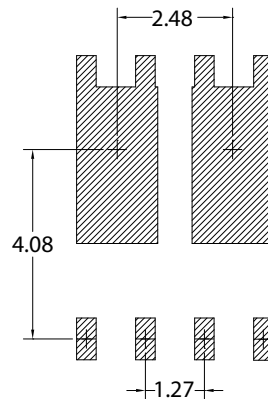
Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.15.2 (a and b).



(dimensions in mm)

Figure A.15.2(a) 5x6 Dual substrate/PCB layout



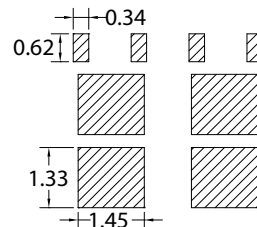
(dimensions in mm)

Figure A.15.2(b) 5x6 Dual substrate/PCB layout

Stencil design

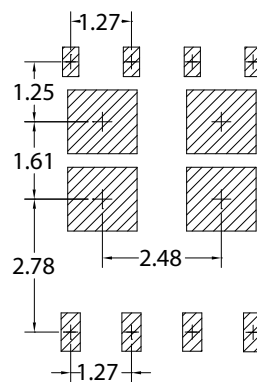
Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.15.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



(dimensions in mm)

Figure A.15.3(a) 5x6 Dual stencil design



(dimensions in mm)

Figure A.15.3(b) 5x6 Dual stencil design

Appendix A.16 6x6 devices

Device outline

Figure A.16.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

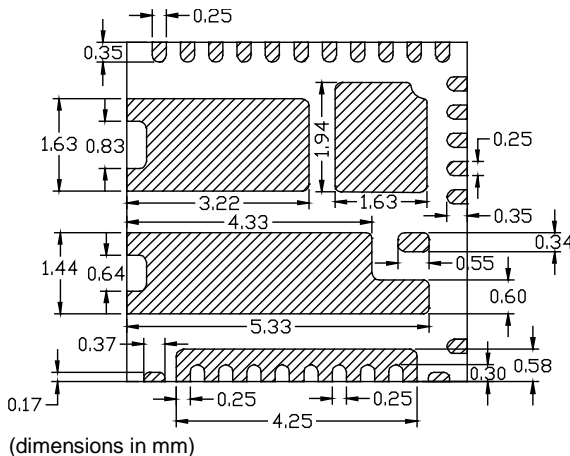


Figure A.16.1 6x6 device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.16.2 (a and b).

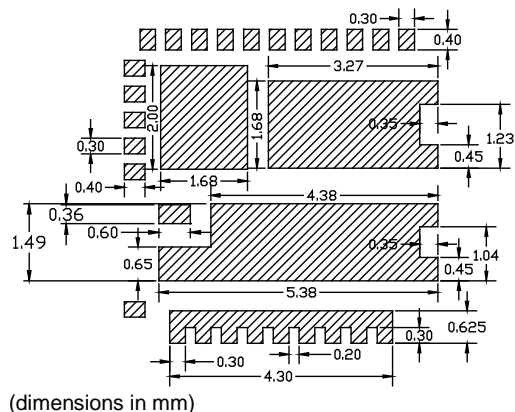


Figure A.16.2(a) 6x6 substrate/PCB layout

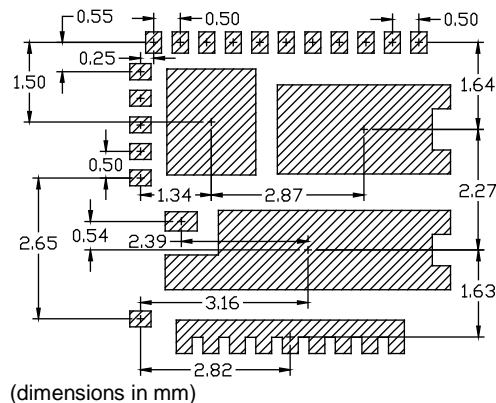


Figure A.16.2(b) 6x6 substrate/PCB layout

Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.16.3 (a and b).

Note: This design is for a stencil thickness of 0.127mm ($0.005''$). The reduction should be adjusted for stencils of other thicknesses.

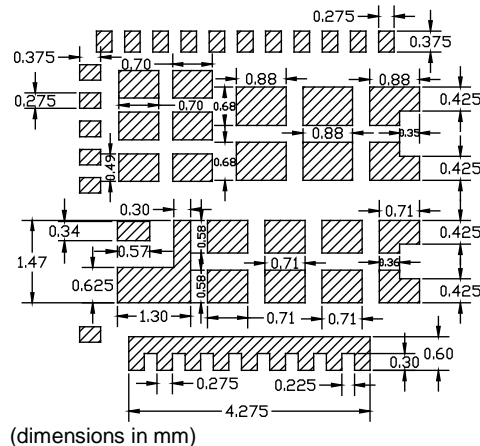


Figure A.16.3(a) 6x6 stencil design

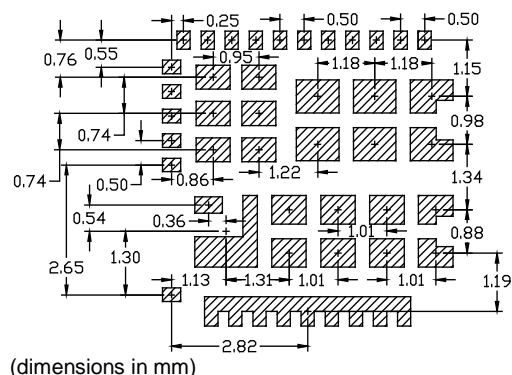


Figure A.16.3(b) 6x6 stencil design