

# AIROC™ Bluetooth® LE system on chip

The AIROC™ CYW20835 Bluetooth® LE SoC is a Bluetooth® 5.2 core spec compliant device for IoT applications. Manufactured using the industry's advanced 40-nm CMOS low-power process, the CYW20835 employs high levels of integration to minimize external components, reducing the device footprint and the costs associated with implementing Bluetooth® Low Energy solutions.

The AIROC™ CYW20835 Bluetooth® LE SoC is designed to support the wide spectrum of Bluetooth® Low Energy use cases for home automation, accessory, sensors (medical, home, security, and industrial), lighting, Bluetooth® Mesh, wireless input devices, and remote controls, or any Bluetooth® LE connected IoT application.

## Features

- Bluetooth® subsystem
  - Complies with Bluetooth® core specification v5.2 with LE 2-Mbps support
  - Bluetooth® Low Energy
  - Supports adaptive frequency hopping (AFH)
  - Programmable TX power up to 12 dBm
  - Rx sensitivity -94.5 dBm (Bluetooth® LE)
  - Ultra-low-power radio
    - RX current 8 mA
    - TX current 18 mA @ 12 dBm
- Coexistence support
  - Support for global coexistence interface for easy coexistence implementation with select Infineon AIROC™ Wi-Fi devices
- MCU subsystem
  - 96-MHz Arm® Cortex®-M4 microcontroller unit MCU with floating point unit (FPU)
  - Supports Serial Wire Debug (SWD)
  - Runs Bluetooth® stack and application
- Memory subsystem
  - 384-KB RAM
  - 2-MB ROM
- Audio features and interfaces
  - 1x I2S with master and slave modes
  - 1x PCM
  - PDM
  - Analog front end for analog microphone
- Clocks
  - On chip 32-kHz oscillator
  - On chip 128-kHz oscillator
  - 32-kHz crystal oscillator
  - 24-MHz crystal oscillator
  - 32-bit real time clock (RTC)

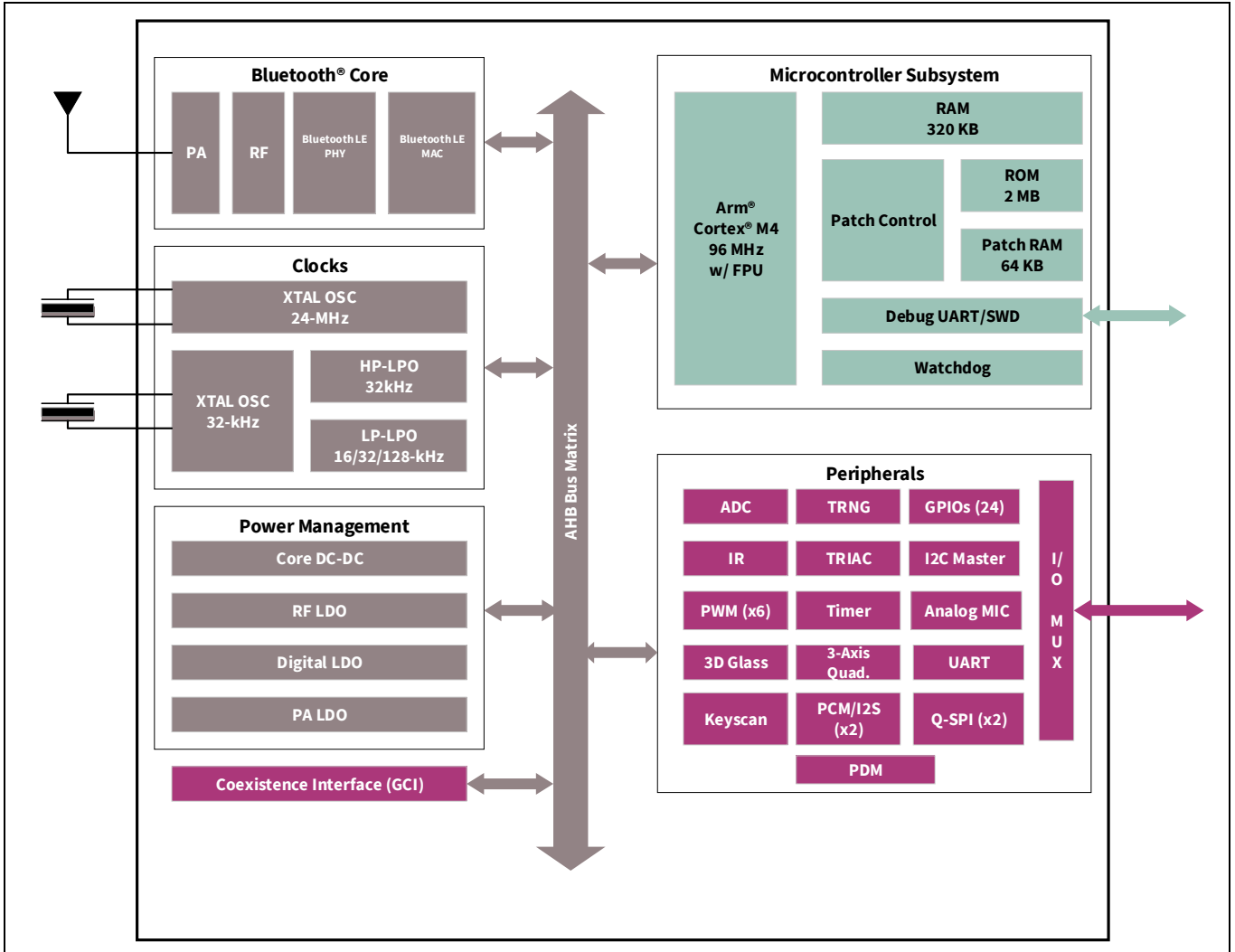
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## Features

- Peripherals and communication
  - 6x 16-bit PWMs
  - Programmable key-scan matrix interface, up to 8x20 key-scanning matrix
  - Quadrature decoder
  - Watchdog timer
  - 1x peripheral UART, 1x UART for programming and HCI
  - 1x SPI (master or slave mode)
  - 1x I2C master
  - One ADC (10-ENoB for DC measurement and 12-ENOB for audio measurement)
  - Hardware security engine
- General-purpose input output (GPIO)
  - 24 GPIOs
  - 2 dedicated pins for analog microphone
  - Support 1.7 V to 3.63 V operation
  - Four GPIOs support 16 mA and 8 mA source at 3.3 V and 1.8 V respectively
- Operating voltage and low-power support
  - Wide operating voltage range - 1.625 V to 3.63V
  - 4 power modes to implement ultra-low power application - managed by real time operating system
  - 1  $\mu$ A current in HID-Off mode
- Packages
  - 7 mm x 7 mm 60-pin quad flat no-lead (QFN)
- Software support
  - ModusToolbox™ software: Features are subject to support in the Bluetooth® SDK
  - Check the latest version of the Bluetooth® SDK technical brief for supported features
- Applications
  - Bluetooth® Mesh
  - Wireless pointing devices (mice)
  - Remote controls
  - Joysticks
  - Home automation
  - Point-of-sale input devices
  - Blood pressure monitors
  - Find-me devices
  - Heart-rate monitors
  - Proximity sensors
  - Thermometers

Functional block diagram

**Functional block diagram**



**Table of contents**

**Features .....1**

**Functional block diagram.....3**

**Table of contents .....4**

**1 Bluetooth® Baseband Core (BBC).....6**

1.1 Link control layer .....6

1.2 Test mode support.....7

1.3 Frequency hopping generator .....7

1.4 Microprocessor unit .....7

1.4.1 Floating point unit .....7

1.4.2 OTP memory .....7

1.4.3 NVRAM configuration data and storage.....7

1.4.4 Power-on reset (POR) .....8

1.4.5 External reset .....8

1.4.6 Brownout detection (BOD) .....8

1.5 Power management unit (PMU).....9

1.6 Integrated radio transceiver.....9

1.6.1 Transmit path.....9

1.6.2 Digital modulator .....9

1.6.3 Power amplifier.....9

1.6.4 Receiver path .....9

1.6.5 Digital demodulator and bit synchronizer.....9

1.6.6 Receiver signal strength indicator .....10

1.6.7 Local oscillator .....10

1.6.8 Calibration.....10

1.7 Peripheral transport unit.....10

1.7.1 I2C compatible master .....10

1.7.2 HCI UART interface.....10

1.8 Peripheral UART interface .....11

1.9 Clock frequencies.....11

1.9.1 Crystal oscillator .....11

1.9.2 HID peripheral block.....12

1.9.3 32-kHz crystal oscillator .....12

1.10 GPIO ports .....13

1.11 Keyboard scanner .....13

1.11.1 Theory of operation .....14

1.11.2 Idle .....14

1.11.3 Scan .....14

1.11.4 Scan end .....14

1.12 Mouse quadrature signal decoder .....14

1.12.1 Theory of operation .....14

1.13 ADC port .....15

1.14 PWM .....15

1.15 Triac control .....15

1.16 Serial peripheral interface (SPI) .....16

1.17 Infrared modulator .....16

1.18 PDM microphone .....16

1.19 Security engine .....17

1.20 Power management unit.....17

1.20.1 RF power management .....17

1.20.2 Host controller power management .....17

1.20.3 BBC power management.....17

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Table of contents

<b>2 Pin assignments and GPIOs.....</b>	<b>18</b>
2.1 Pin assignments.....	18
2.2 GPIO pin descriptions.....	19
2.3 Pinouts.....	22
2.3.1 60-pin QFN package.....	22
<b>3 Electrical specifications.....</b>	<b>23</b>
3.1 Electrical characteristics.....	23
3.1.1 Core buck regulator.....	24
3.1.2 Digital LDO.....	25
3.1.3 PA LDO.....	26
3.1.4 RF LDO.....	27
3.1.5 Digital I/O characteristics.....	28
3.1.6 Current consumption.....	28
3.2 ADC electrical characteristics.....	29
3.3 RF specifications.....	30
3.4 Timing and AC characteristics.....	32
3.4.1 UART timing.....	32
3.4.2 SPI timing.....	33
3.4.3 I2C interface timing.....	35
<b>4 Package diagram.....</b>	<b>38</b>
4.1 Tray packaging specifications.....	39
<b>5 Ordering information.....</b>	<b>40</b>
<b>6 Additional information.....</b>	<b>41</b>
6.1 IoT resources.....	41
<b>7 Acronyms.....</b>	<b>42</b>
<b>Revision history.....</b>	<b>43</b>

# 1 Bluetooth® Baseband Core (BBC)

The BBC implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL and TX/RX transactions, monitors Bluetooth® slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types. **Table 1** lists the major Bluetooth® SIG specification features supported by the CYW20835.

**Table 1 Bluetooth® features**

<b>Bluetooth® 4.0</b>	<b>Bluetooth® 4.1</b>	<b>Bluetooth® 4.2</b>
Bluetooth® Low Energy	Low duty cycle advertising	Data packet length extension
–	LE link layer topology	LE secure connection
–	–	LE privacy 1.2
<b>Bluetooth® 5.0</b>		
Bluetooth® LE 2-Mbps		
Slot availability mask (SAM)		
LE channel selection		
High duty cycle non-connectable advertisement		

## 1.1 Link control layer

The link control layer is part of the Bluetooth® link control functions that are implemented in dedicated logic in the link control unit (LCU).

This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state or substate in the Bluetooth® link controller.

- Bluetooth® LE states
  - Advertising
  - Scanning
  - Connection
- Major states
  - Standby
  - Connection
- Substates
  - Page
  - Page scan
  - Inquiry
  - Inquiry scan
  - Sniff

## 1.2 Test mode support

The CYW20835 fully supports Bluetooth® test mode as described in Part I:1 of the specification of the Bluetooth® system version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth® test mode, the CYW20835 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

## 1.3 Frequency hopping generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth® clock, and device address.

## 1.4 Microprocessor unit

The CYW20835 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is a Cortex®-M4 32-bit RISC processor with embedded ICE-RT debug and Serial Wire Debug (SWD) interface units. The microprocessor also includes 2 MB of ROM memory for Bluetooth® stack and drivers for on-chip peripherals and 384 KB of RAM for data scratch-pad.

The internal ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device also supports the integration of user applications and profiles.

### 1.4.1 Floating point unit

CYW20835 includes the CM4 single precision IEEE-754 compliant floating point unit. For details see the Cortex®-M4 manual.

### 1.4.2 OTP memory

The CYW20835 includes 2 KB of one-time programmable memory that can be used by the factory to store product-specific information.

**Note:** Use of OTP requires that a 3 V supply be present at all times.

### 1.4.3 NVRAM configuration data and storage

NVRAM contains configuration information about the customer application, including the following:

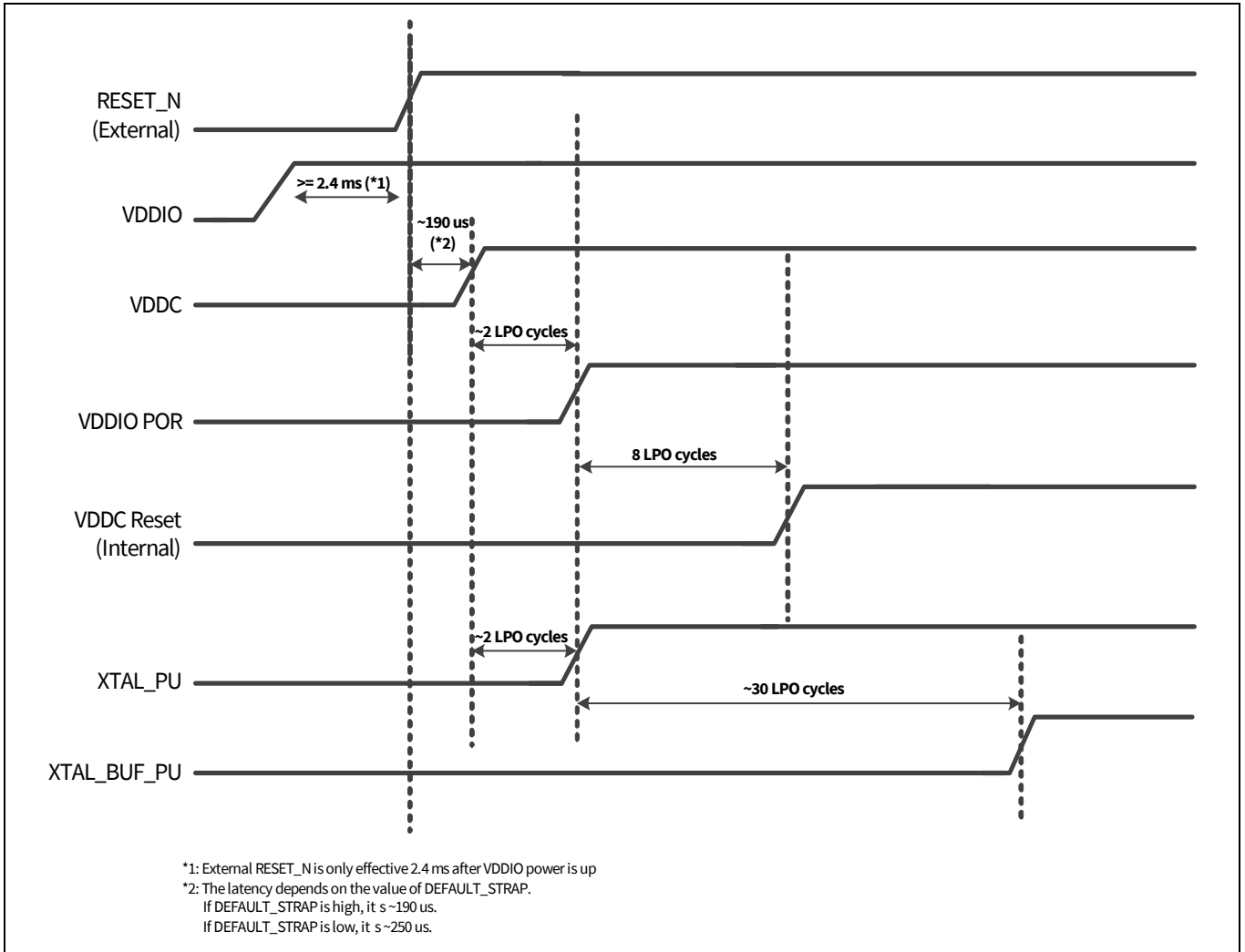
- Fractional-N information
- BD\_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYW20835 uses SPI flash for NVRAM storage.

**1.4.4 Power-on reset (POR)**

The CYW20835 includes POR logic to allow the part to initialize correctly when power is applied. **Figure 2** shows the sequence used by the CYW20835 during initialization. An small external cap may be used on RESET\_N to add delay as VDDIO ramps up.

**1.4.5 External reset**

An external active-low reset signal, RESET\_N, can be used to put the CYW20835 in the reset state.



**Figure 2 Power-on reset timing**

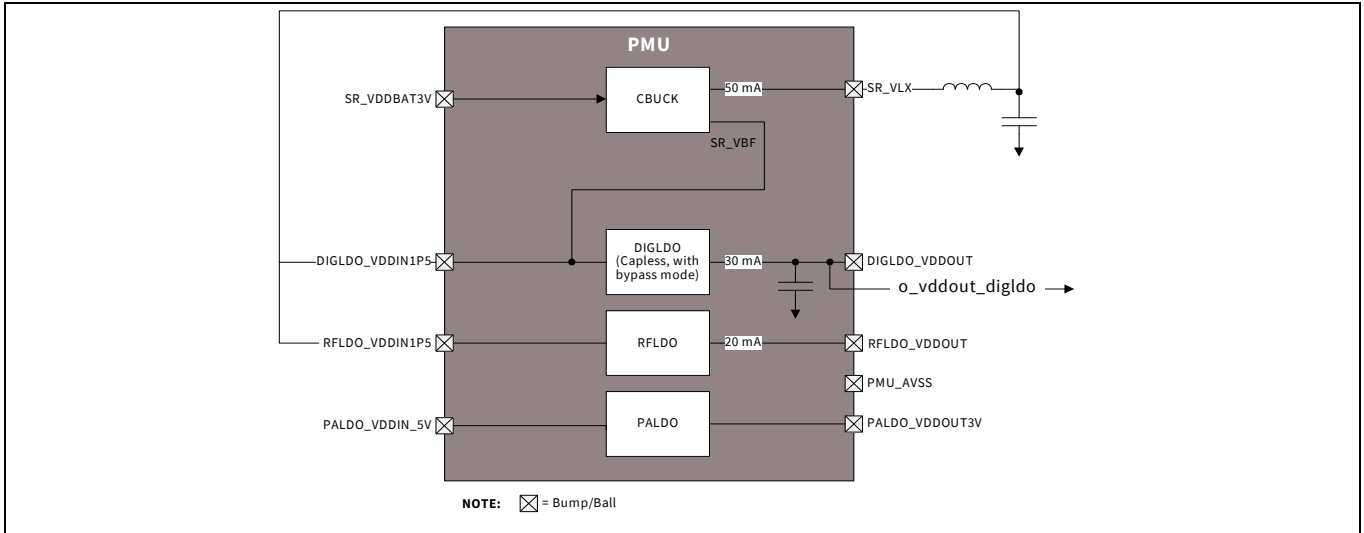
**1.4.6 Brownout detection (BOD)**

An external voltage detector reset IC may be used if brownout detection is required. The reset IC should release RESET\_N only after the VDDO supply voltage level has been at or above a minimum operating voltage for 50 ms or longer.



## 1.5 Power management unit (PMU)

**Figure 3** shows the CYW20835 power management unit (PMU) block diagram. The CYW20835 includes an integrated buck regulator, a capless LDO, PALDO and an additional 1.2 V LDO for RF.



**Figure 3 Power management unit**

## 1.6 Integrated radio transceiver

The CYW20835 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth® wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20835 is fully compliant with the Bluetooth® radio specification and meets or exceeds the requirements to provide the highest communication link quality of service.

### 1.6.1 Transmit path

The CYW20835 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

### 1.6.2 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

### 1.6.3 Power amplifier

The CYW20835 has an integrated power amplifier (PA) that can transmit up to +12 dBm for class 1 operations.

### 1.6.4 Receiver path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYW20835 to be used in most applications with minimal off-chip filtering.

### 1.6.5 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer takes the low-IF received signal and performs an optimal frequency tracking and bit-synchronization algorithm.

### 1.6.6 Receiver signal strength indicator

The radio portion of the CYW20835 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

### 1.6.7 Local oscillator

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 40 maximum available channels. The CYW20835 uses an internal loop filter.

### 1.6.8 Calibration

The CYW20835 radio transceiver features a self-contained automated calibration scheme. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration compensates for filter, matching network, and amplifier gain and phase characteristics to yield radio performance within 2% of what is optimal. Calibration takes process and temperature variations into account, and it occurs transparently during normal operation and hop setting times.

## 1.7 Peripheral transport unit

### 1.7.1 I<sup>2</sup>C compatible master

The CYW20835 provides a 2-pin I<sup>2</sup>C compatible master interface to communicate with I<sup>2</sup>C compatible peripherals. I<sup>2</sup>C does not support multi-master capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by I<sup>2</sup>C:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I<sup>2</sup>C-compatible speed.)
- 1 MHz (Compatibility with high-speed I<sup>2</sup>C-compatible devices is not guaranteed).

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20835 are required on both the SCL and SDA pins for proper operation.

### 1.7.2 HCI UART interface

The CYW20835 includes a UART interface for factory programming and when operating as a Bluetooth® HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 57600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYW20835 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the CYW20835 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

**Table 2** contains example values to generate common baud rates with a 24 MHz UART clock.

**Table 2 Common baud rate examples, 24 MHz clock**

Baud rate (bps)	Baud rate adjustment		Mode	Error (%)
	High nibble	Low nibble		
3M	0xFF	0xF8	High rate	0.00
2M	0xFF	0xF4	High rate	0.00
1M	0x44	0xFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16

**Table 3** contains example values to generate common baud rates with a 48 MHz UART clock.

**Table 3 Common baud rate examples, 48 MHz clock**

Baud rate (bps)	High rate	Low rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	-0.08
57600	0x1	0xCC	Normal	0.04

Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW20835 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

## 1.8 Peripheral UART interface

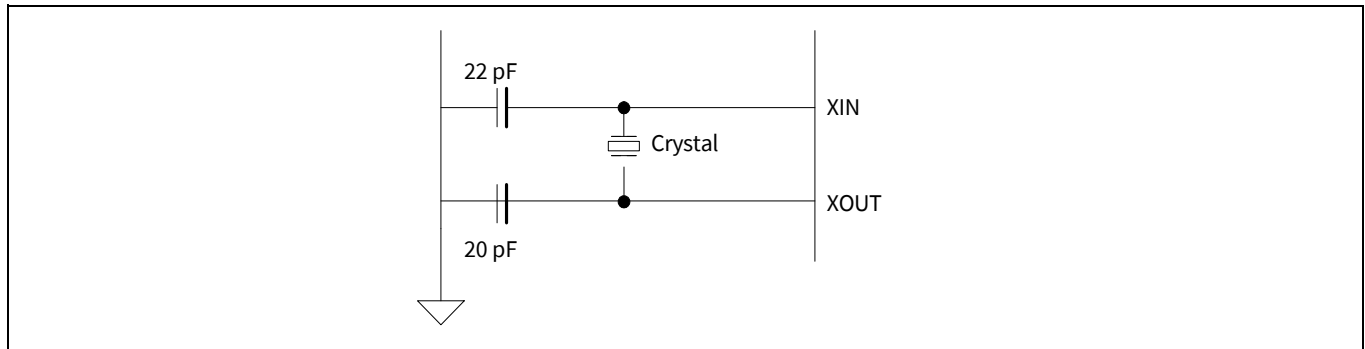
The CYW20835 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYW20835 can map the peripheral UART to any LHL GPIO. The peripheral UART clock is fixed at 24 MHz. Both TX and RX have a 256-byte FIFO (see [Table 2](#)).

## 1.9 Clock frequencies

The CYW20835 uses a 24 MHz crystal oscillator (XTAL).

### 1.9.1 Crystal oscillator

The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth® specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see [Figure 4](#)).



**Figure 4 Recommended oscillator configuration – 12 pF load crystal**

**Table 4** shows the recommended crystal specifications.

**Table 4 Reference crystal electrical specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	20	24	40	MHz
Oscillation mode	–	Fundamental			–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	60	Ω
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	μW
Aging	–	–	±3	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

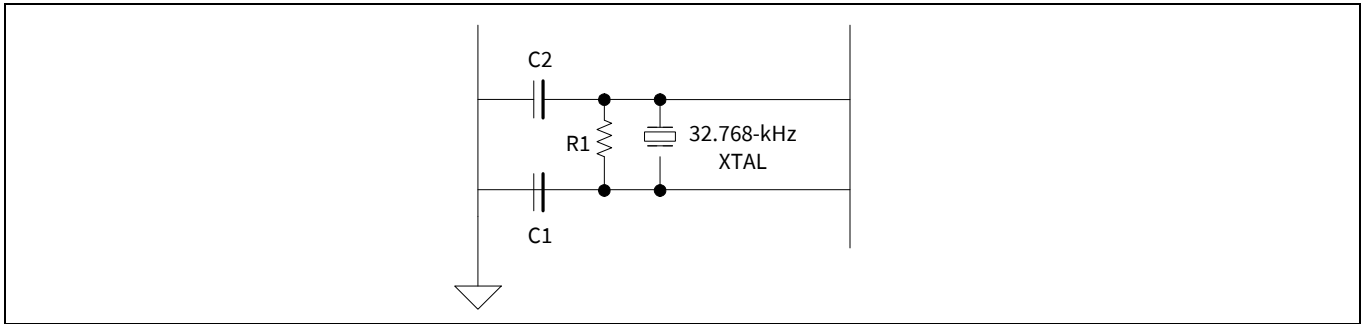
### 1.9.2 HID peripheral block

The peripheral blocks of the CYW20835 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

### 1.9.3 32-kHz crystal oscillator

**Figure 5** shows the 32-kHz XTAL oscillator with external components and **Table 5** lists the oscillator’s characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32-kHz or 32.768-kHz crystal oscillator or be driven with a clock input at a similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.



**Figure 5 32-kHz oscillator block diagram**

**Table 5 XTAL oscillator characteristics**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	$F_{\text{oscout}}$	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{\text{startup}}$	–	–	–	500	ms
XTAL drive level	$P_{\text{drv}}$	For crystal selection	0.5	–	–	$\mu\text{W}$
XTAL series resistance	$R_{\text{series}}$	For crystal selection	–	–	70	$\text{k}\Omega$
XTAL shunt capacitance	$C_{\text{shunt}}$	For crystal selection	–	–	1.3	pF

### 1.10 GPIO ports

GPIO ports for this device is shown in [Table 7](#).

The CYW20835 uses 40 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3 V or 4 mA at 1.8 V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3 V or 8 mA at 1.8 V.

**P0, P1, P8-P18, P21-23, P28-P38:** All of these pins can be programmed as ADC inputs.

**Port 26–Port 29:** all four of these pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

### 1.11 Keyboard scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys are pressed.
- Sequential scanning of up to 160 keys in an 8 × 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key code buffer (can be augmented by firmware).
- 128 kHz clock that allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.
- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit  $\mu\text{A}$ -level sleep current.

### 1.11.1 Theory of operation

The key scan block is controlled by a state machine with the following states:

#### 1.11.2 Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to 0.

#### 1.11.3 Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter value is compared to the modifier key codes stored in RAM, or in the key code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the  $n$ th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

#### 1.11.4 Scan end

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

**Note:** The microcontroller can poll the key status register.

## 1.12 Mouse quadrature signal decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.
- Control of up to four external high-current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active high or active low.
  - Control signal can be tristated for off condition or driven high or low, as appropriate.

### 1.12.1 Theory of operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

**1.13 ADC port**

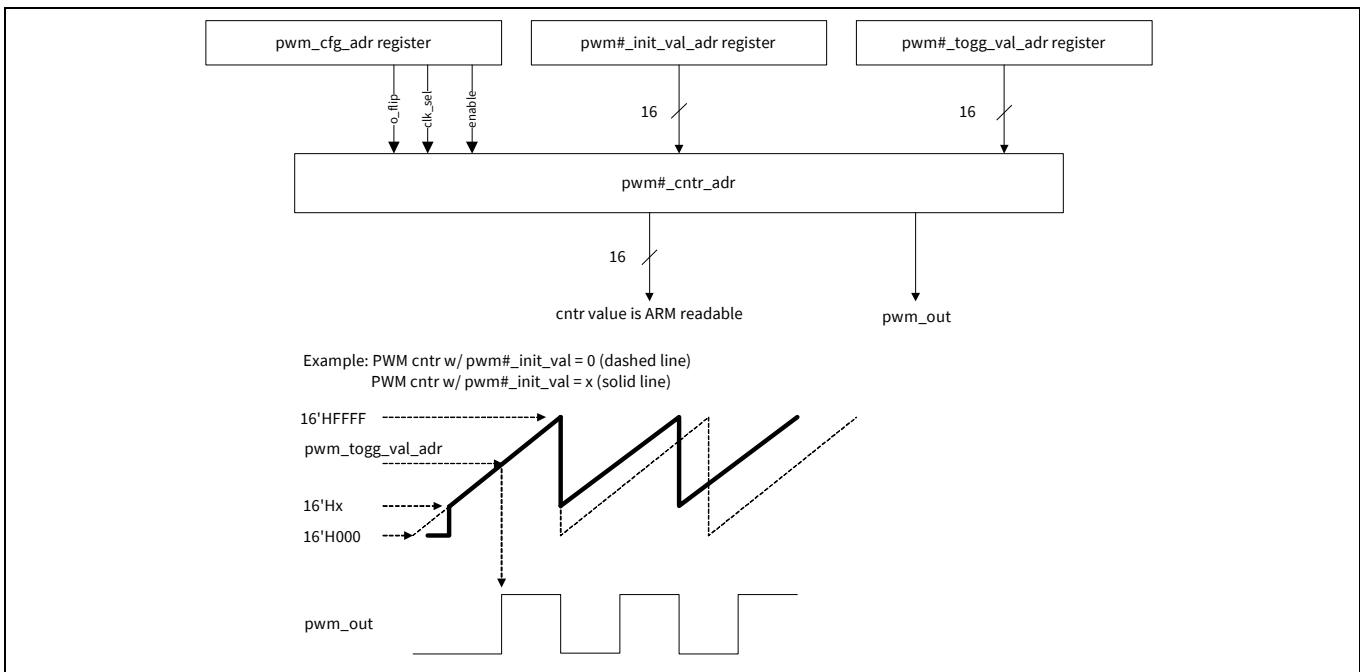
The ADC block is a single switched-cap  $\Sigma$ - $\Delta$  ADC core for audio and DC measurement. It operates at the 12 MHz clock rate and has 32 DC input channels, including 28 GPIO inputs. The internal bandgap reference has  $\pm 5\%$  accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

**1.14 PWM**

The CYW20835 has six internal PWMs. The PWM module consists of the following:

- PWM0–5. Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 6 shows the structure of one PWM.



**Figure 6 PWM block diagram**

**1.15 Triac control**

The CYW20835 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYW20835 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYW20835 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

### 1.16 Serial peripheral interface (SPI)

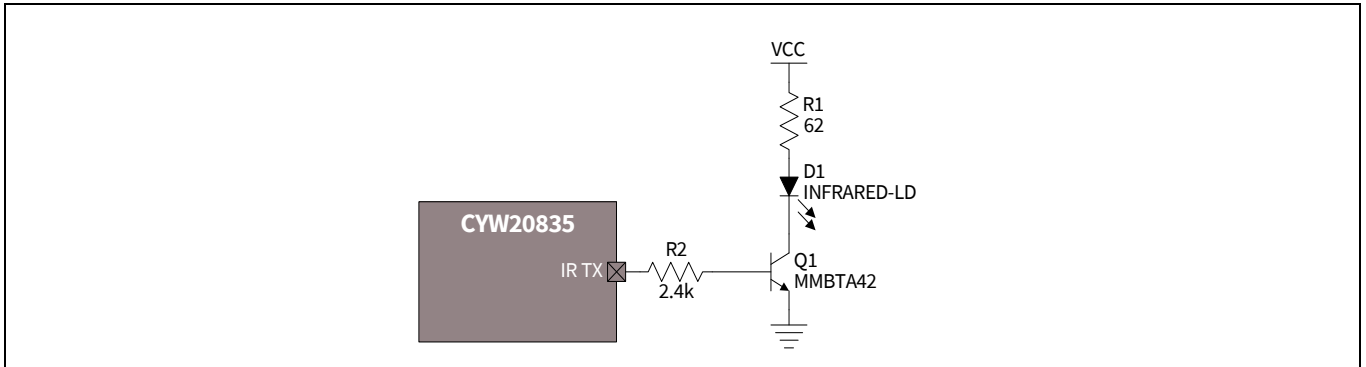
The CYW20835 has two independent SPI interfaces, both of which support single, dual, and quad mode SPI operations. Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20835 has optional I/O ports that can be configured individually and separately for each functional pin. The CYW20835 acts as an SPI master device that supports 1.8 V or 3.3 V SPI slaves. The CYW20835 can also act as an SPI slave device that supports a 1.8 V or 3.3 V SPI master.

**Note:** SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

### 1.17 Infrared modulator

The CYW20835 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767  $\mu$ sec. The CYW20835 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to under run (see [Figure 7](#)).



**Figure 7 Infrared TX**

### 1.18 PDM microphone

The CYW20835 accepts a  $\Sigma\Delta$ -based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The digital signal passes through the chip IO and MUX inputs using an auxADC signal. The PDM shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone accepts a 2.4 MHz clock generated by the CYW20835 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.



## 1.19 Security engine

The CYW20835 includes a hardware security accelerator that greatly decreases the time required to perform typical security operations. These functions include:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)

**Note:** Security engine is used only by Bluetooth® stack to reduce CPU overhead. It is not available for application use.

## 1.20 Power management unit

The PMU provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

### 1.20.1 RF power management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

### 1.20.2 Host controller power management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDEOFF (deep sleep) mode.

### 1.20.3 BBC power management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth®-specified low-power connection mode. While in these low-power connection modes, the CYW20835 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYW20835 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDEOFF (Deep Sleep) mode

The CYW20835 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the CYW20835 immediately enters Active mode.

In HIDEOFF mode, the CYW20835 baseband and core are powered off by disabling power to VDDC\_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is used for longer periods of inactivity.

Pin assignments and GPIOs

## 2 Pin assignments and GPIOs

### 2.1 Pin assignments

**Table 6 Pin assignments**

Pin name	QFN pin	I/O	Power domain	Description
<b>Microphone</b>				
MIC_AVDD	48	I	MIC_AVDD	Microphone supply
MICBIAS	45	I	MIC_AVDD	Microphone bias supply
MICN	47	I	MIC_AVDD	Microphone negative input
MICP	46	I	MIC_AVDD	Microphone positive input
<b>Baseband supply</b>				
BT_VDDO	36	I	VDDO	I/O pad power supply
BT_VDDC	37	I	VDDC	Baseband core power supply
LHL_VDDO	60	I	VDDO	LHL PAD power supply: can be tied to BT_VDDO
<b>RF power supply</b>				
BT_PAVDD2P5	26	I	PAVDD2P5	PA supply
BT_PLLVDD1P2	31	I	PLLVDD1P2	RFPLL and crystal oscillator supply
BT_VCOVDD1P2	29	I	VCOVDD1P2	VCO supply
BT_IFVDD1P2	28	I	IFVDD1P2	IFPLL power supply
<b>Onboard LDOs</b>				
DIGLDO_VDDIN1P5	25	I	–	Internal digital LDO input and feedback pin of switching regulator (CBIUCK).
RFLDO_VDDIN1P5	24	I	–	RF LDO input
RFLDO_VDDOUT	23	O	–	RF LDO output
PALDO_VDDIN_5V	19	I	–	PA LDO input
PALDO_VDDOUT3V	20	O	–	PA LDO output
SR_VDDBAT3V	22	I	–	Core buck input
SR_VLX	21	O	–	Core buck output
<b>Ground pins</b>				
HS-VSS	H	I	VSS	Digital ground
<b>UART</b>				
UART_CTS_N	44	I, PU	VDDO	CTS for HCI UART interface: NC if unused.
UART_RTS_N	43	O, PU	VDDO	RTS for HCI UART interface. NC if unused.
UART_RXD	41	I	VDDO	UART serial input. Serial data input for the HCI UART interface.
UART_TXD	42	O, PU	VDDO	UART serial input. Serial data input for the HCI UART interface.
<b>Serial peripheral interface</b>				
SPI_MISO	40	I	VDDO	SPI master in slave out
SPI_MOSI	39	O	VDDO	SPI master out slave in
SPI_CSN	38	O	VDDO	SPI chip select
SPI_CLK	35	O	VDDO	SPI clock

## Pin assignments and GPIOs

**Table 6 Pin assignments** (continued)

Pin name	QFN pin	I/O	Power domain	Description
<b>Crystal</b>				
BT_XTALI	32	I	PLLVD1P2	Crystal oscillator input: see <b>“Crystal oscillator”</b> on page 11 for options
BT_XTALO	33	O	PLLVD1P2	Crystal oscillator output
XTALI_32K	50	I	VDDO	Low-power oscillator input
XTALO_32K	49	O	VDDO	Low-power oscillator output
<b>Others</b>				
DEFAULT_STRAP	18	I	VDDO	Connect to VDDO
BT_HOST_WAKE	34	O	VDDO	Host wake-up. This is a signal from the Bluetooth® device to the host indicating that the Bluetooth® device requires attention. <ul style="list-style-type: none"> <li>• Asserted: Host device must wake up or remain awake.</li> <li>• Deasserted: Host device may sleep when sleep criteria is met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low.
BT_RF	27	I/O	PAVDD2P5	RF antenna port
JTAG_SEL	17	–	–	ARM JTAG debug mode control: Connect to GND for all applications
RST_N	16	I	VDDO	Active-low system reset with open-drain output and internal pull-up resistor
NC	30	–	–	Leave floating

## 2.2 GPIO pin descriptions

**Table 7 GPIO pin descriptions** <sup>[1, 2]</sup>

QFN pin number	Pin name	Default direction	POR state	Power domain	Default alternate function description
8	P0	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P0</li> <li>• A/D converter input 29</li> <li>• Not available during TM1 = 1.</li> </ul>
9	P1	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P1</li> <li>• A/D converter input 28</li> </ul>
52	P2	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P2</li> </ul>
53	P3	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P3</li> </ul>
54	P4	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P4</li> </ul>
55	P5	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P5</li> </ul>

**Notes**

1. All GPIOs are supermux. All GPIOs can be programmed for any alternative functions. For example, key scan, SPI, I<sup>2</sup>C, IR\_TX, quadrature, peripheral UART, ADC, etc.
2. During power-on reset, all inputs are disabled.

## Pin assignments and GPIOs

**Table 7** GPIO pin descriptions <sup>[1, 2]</sup> (continued)

QFN pin number	Pin name	Default direction	POR state	Power domain	Default alternate function description
56	P6	Input	Floating	VDDO	• GPIO: P6
57	P7	Input	Floating	VDDO	• GPIO: P7
58	P8	Input	Floating	VDDO	• GPIO: P8 • A/D converter input 27
1	P9	Input	Floating	VDDO	• GPIO: P9 • A/D converter input 26
2	P10	Input	Floating	VDDO	• GPIO: P10 • A/D converter input 25
3	P11	Input	Floating	VDDO	• GPIO: P11 • A/D converter input 24
4	P12	Input	Floating	VDDO	• GPIO: P12 • A/D converter input 23
5	P13	Input	Floating	VDDO	• GPIO: P13 • A/D converter input 22
59	P14	Input	Floating	VDDO	• GPIO: P14 • A/D converter input 21
50	P15	Input	Floating	VDDO	• GPIO: P15 • A/D converter input 20
51	P16	Input	Floating	VDDO	• GPIO: P16 • A/D converter input 19
13	P26 PWM0	Input	Floating	VDDO	• GPIO: P26 • Current: 16 mA sink
14	P27 PWM1	Input	Floating	VDDO	• GPIO: P27 • Current: 16 mA sink
6	P28 PWM2	Input	Floating	VDDO	• GPIO: P28 • A/D converter input 11 • Current: 16 mA sink
7	P29 PWM3	Input	Floating	VDDO	• GPIO: P29 • A/D converter input 10 • Current: 16 mA sink
15	P32	Input	Floating	VDDO	• GPIO: P32 • A/D converter input 7

**Notes**

1. All GPIOs are supermux. All GPIOs can be programmed for any alternative functions. For example, key scan, SPI, I<sup>2</sup>C, IR\_TX, quadrature, peripheral UART, ADC, etc.
2. During power-on reset, all inputs are disabled.

## Pin assignments and GPIOs

**Table 7** GPIO pin descriptions <sup>[1, 2]</sup> (continued)

QFN pin number	Pin name	Default direction	POR state	Power domain	Default alternate function description
10	P34	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P34</li> <li>A/D converter input 5</li> </ul>
11	P38	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P38</li> <li>A/D converter input 1</li> </ul>
12	P39	Input	Floating	VDDO	Reserved for system use. Leave this GPIO unconnected

**Notes**

- All GPIOs are supermux. All GPIOs can be programmed for any alternative functions. For example, key scan, SPI, I<sup>2</sup>C, IR\_TX, quadrature, peripheral UART, ADC, etc.
- During power-on reset, all inputs are disabled.

**Table 8** GPIO supermux input/output function list

Function	Function	Function	Function
SPI_1: CLK	SPI_1: CS	SPI_1: MOSI	SPI_1: MISO
SPI_1: INT	SPI_2: CLK	SPI_2: CS	SPI_2: MOSI
SPI_2: MISO	SPI_2: INT	SPI_3: CLK	SPI_3: CS
SPI_3: MOSI	SPI_3: MISO	SPI_3: INT	UART_RX
UART_CTS	UART_TX	UART_RTS	PUART_RX
PUART_CTS	PUART_TX	PUART_RTS	SCL
SDA	SCL2	SDA2	PCM_IN
PCM_OUT	PCM_CLK	PCM_SYNC	I2S_DO
I2S_DI	I2S_WS	I2S_CLK	IR_TX
kso0	kso1	kso2	kso3
kso4	kso5	kso6	kso7
kso8	kso9	kso10	kso11
kso12	kso13	kso14	kso15
kso16	kso17	kso18	kso19
PWM0	PWM1	PWM2	PWM3
PWM4	PWM5	aclk0	aclk1
pa_ramp	tx_pd	~tx_pd	-

Pin assignments and GPIOs

## 2.3 Pinouts

### 2.3.1 60-pin QFN package

The 60-pin QFN package is shown in **Figure 8**.

		60	59	58	57	56	55	54	53	52	51	50	49	48	47	46		
		LHL_VDDO	P14	P8	P7	P6	P5	P4	P3	P2	P16	P15/XTALI_32K	XTALO_32K	MIC_AVDD	MICN	MICP		
1	P9	<div style="border: 1px solid black; width: 100%; height: 100%; display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>H</p> <p>HS-VSS</p> </div> </div>														45	MICBIAS	
2	P10															44	UART_CTS_N	
3	P11															43	UART_RTS_N	
4	P12															42	UART_TXD	
5	P13															41	UART_RXD	
6	P28															40	SPL_MISO	
7	P29															39	SPL_MOSI	
8	P0															38	SPL_CSN	
9	P1															37	BT_VDDC	
10	P34															36	BT_VDDO	
11	P38															35	SPI_CLK	
12	P39															34	BT_HOST_WAKE	
13	P26															33	BT_XTALO	
14	P27															32	BT_XTALI	
15	P32															31	BT_PLLVDD1P2	
		RST_N	JTAG_SEL	DEFAULT_STRAP	PALDO_VDDIN_5V	PALDO_VDDOUT3V	SR_VLX	SR_VDDBAT3V	RFLDO_VDDOUT	RFLDO_VDDIN1P5	DIGLDO_VDDIN1P5	BT_PAVDD2P5	BT_RF	BT_IFVDD1P2	BT_VCOVDD1P2	---		
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30		

**Figure 8** CYW20835 60-pin QFN package

**Note:** Pin H is a ground pin that is used for the signal name HS-VSS.

### 3 Electrical specifications

#### 3.1 Electrical characteristics

The absolute maximum ratings in the following table indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 9 Absolute maximum ratings**

Requirement parameter	Specification			Unit
	Min	Nom	Max	
Maximum junction temperature	–	–	125	°C
VDD IO	–0.5	–	3.795	V
VDD RF	–0.5	–	1.38	V
VDDBAT3V	–0.5	–	3.795	V
DIGLDO_VDDIN1P5	–0.5	–	1.65	V
RFLDO_VDDIN1P5	–0.5	–	1.65	V
PALDO_VDDIN_5V	–0.5	–	3.795	V
MIC_AVDD	–0.5	–	3.795	V
OTP_3P3V	–0.5	–	3.795	V

**Table 10 ESD/latchup**

Requirement parameter	Specification			Unit
	Min	Nom	Max	
ESD tolerance HBM	–2000	–	2000	V
ESD tolerance CDM	–500	–	500	V
Latch-up	–	200	–	mA

**Table 11 Environmental ratings**

Characteristic	Value	Unit
Operating temperature	–30 to +85	°C
Storage temperature	–40 to +150	°C

**Table 12 Recommended operating conditions**

Parameter	Specification			Unit
	Min	Typ	Max	
VDD IO <sup>[3]</sup>	V <sub>SHUT</sub> <sup>[4]</sup>	3.0	3.63	V
VDDRF	1.14	1.2	1.26	V
VDDBAT3V <sup>a</sup>	V <sub>SHUT</sub> <sup>[4]</sup>	3.0	3.63	V
PALDO_VDDIN_5V	2.5	3.3	3.63	
DIGLDO_VDDIN1P5	1.3	1.35	1.5	V

**Notes**

3. V<sub>BAT</sub> must be greater or equal to VDDIO.

4. See [Table 13](#).

## Electrical specifications

**Table 12 Recommended operating conditions (continued)**

Parameter	Specification			Unit
	Min	Typ	Max	
RFLDO_VDDIN1P5	1.3	1.35	1.5	V
MIC_AVDD	$V_{SHUT}^{[4]}$	3.0	3.63	V
OTP_3P3V	3.0	3.3	3.63	V

**Notes**

 3.  $V_{BAT}$  must be greater or equal to VDDIO.

 4. See [Table 13](#).

The CYW20835 uses an onboard low voltage detector to shut down the part when supply voltage (VDDBAT3V) drops below operating range.

**Table 13 Shutdown voltage**

Parameter	Specification			Unit
	Min	Typ	Max	
$V_{SHUT}$	1.625	1.7	1.775	V

**3.1.1 Core buck regulator**
**Table 14 Core buck regulator**

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage DC, VBAT	DC voltage range	1.62	3.0	3.63	V
CBUCK output current	–	–	–	65	mA
Output voltage range	Programmable, 30 mV/step Default = 1.35 V (bits = 0000)	1.2	1.35	1.5	V
Output voltage DC accuracy	Includes load and line regulation	–4	–	+4	%
LPOM ripple voltage, static	Measured with 20 MHz bandwidth limit, static load. Max ripple based on VBAT = 3V, Vout = 1.35 V Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 $\mu$ H $\pm$ 25%, DCR = 114 m $\Omega$ $\pm$ 20%, ACR < 1 $\Omega$ (for frequency < 1 MHz) Capacitor: 1 $\mu$ F $\pm$ 10%, 6.3 V, 0603 inch, X5R, MLCC capacitor + board total-ESR < 20 m $\Omega$	–	–	30	mVpp
Efficiency (high load)	10–50 mA load current, Vout = 1.35 V, Vbat = 3 V @25°C Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 $\mu$ H $\pm$ 25%, DCR = 114 m $\Omega$ $\pm$ 20%, ACR < 1 $\Omega$ (for frequency < 1 MHz) Capacitor: 1 $\mu$ F $\pm$ 10%, 6.3 V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 m $\Omega$	–	85	–	%



## Electrical specifications

**Table 14 Core buck regulator** (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Efficiency (low load)	1–5 mA load current, $V_{out} = 1.35\text{ V}$ , $V_{bat} = 3\text{ V}$ @25°C Inductor: 0806 inch-size, $T_{max} = 1\text{ mm}$ , $2.2\ \mu\text{H} \pm 25\%$ , $\text{DCR} = 114\ \text{m}\Omega \pm 20\%$ , $\text{ACR} < 1\ \Omega$ (for frequency $< 1\ \text{MHz}$ ) Capacitor: $1\ \mu\text{F} \pm 10\%$ , 6.3 V, 0603 inch, X5R, MLCC capacitor +board total-ESR $< 20\ \text{m}\Omega$	–	80	–	%
Startup time	See <a href="#">Table 15</a> .	–	–	–	–
External inductor L	$2.2\ \mu\text{H} \pm 25\%$ , $\text{DCR} = 114\ \text{m}\Omega \pm 20\%$ , $\text{ACR} < 1\ \Omega$ (for frequency $< 1\ \text{MHz}$ )	–	2.2	–	$\mu\text{H}$
External output capacitor, $C_{out}$	$1\ \mu\text{F} \pm 10\%$ , 6.3 V, 0603 inch, X5R, MLCC capacitor +board total-ESR $< 20\ \text{m}\Omega$	0.7	1	1.1	$\mu\text{F}$
External input capacitor, $C_{in}$	For SR_VDDBAT 3 V pin Ceramic, X5R, 0402, ESR $< 30\ \text{m}\Omega$ at 4 MHz, +/-20%, 6.3 V, 4.7 $\mu\text{F}$	0.7	4.7	5.64	$\mu\text{F}$
Input supply voltage ramp-up time	0 to 3.3V	40	–	–	$\mu\text{s}$

- Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.
- Maximum capacitor value refers to the total capacitance seen at a node where the capacitor is connected. This also includes any decoupling capacitors connected at the load side, if any.

### 3.1.2 Digital LDO

**Table 15 Digital LDO**

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, $V_{in}$	Minimum $V_{in} = V_o + 0.12\text{V}$ requirement must be met under maximum load.	1.3	1.35	1.5	V
Nominal output voltage, $V_o$	Internal default bit setting	–	1.2	–	V
Output voltage programmability	Range Step size Accuracy at any step (including line/load regulation)	0.9 – –4	– 10 –	1.25 – +4	V mV %
Dropout voltage	At maximum load	–	–	120	mV
Output current	DC load	0.2 <sup>[5]</sup>	–	40	mA
Output loading capacitor	Internal, including the decoupling capacitor to be placed next to the load and the equivalent loading capacitor by the core.	4	–	10	nF

**Note**

- By default, an internal loading of ~0.2 mA resides inside the LDO. This is to ensure the LDO is stable with zero loading from the core. After the core is up, digital logic can disable this internal loading by setting `i_ldo_cntl<8:7>` to 00.

## Electrical specifications

**Table 15 Digital LDO** (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Quiescent current	At no load, excluding main bandgap I <sub>q</sub>	–	90	120	μA
Line regulation	V <sub>in</sub> from (V <sub>o</sub> +0.12 V) to 1.5 V; 40 mA load	–	–	5	mV/V
Load regulation	Load from 1 mA to 25 mA; V <sub>in</sub> (V <sub>o</sub> +0.12 V)	–	0.025	0.045	mV/mA
Leakage current	In full power-down mode or bypass mode: Junction temperature: 25°C Junction temperature: 125°C	–	0.05	0.2	μA
		–	1.1	5.0	μA
PSRR	@1 kHz, V <sub>in</sub> , V <sub>o</sub> +0.12 V Output cap of 4 nF~10 nF	40	–	–	dB
LDO turn-on time	LDO turn-on time when balance of chip is up	–	–	22	μs
External input capacitor	Only use an external input capacitor at VDD_DIGLDO1P5 pin if it is not supplied from CBUCK output.	–	1	2.2	μF

**Note**

5. By default, an internal loading of ~0.2 mA resides inside the LDO. This is to ensure the LDO is stable with zero loading from the core. After the core is up, digital logic can disable this internal loading by setting `i_ldo_cntl<8:7>` to 00.

**3.1.3 PA LDO**
**Table 16 PA LDO**

Specification	Notes	Min	Typ	Max	Units
Input supply voltage	Min = 3.0 + 0.1 V = 3.1 V Dropout voltage requirement must be met under max load for performance specs	1.8 <sup>[6]</sup>	3.3	3.63	V
Output current	Junction temperature 125°C	–	–	50	mA
Output voltage (V <sub>o</sub> )	Default = 3.0 V	2.4	3.0	3.4	V
Dropout voltage	At max. load	–	–	100	mV
Output voltage DC accuracy	Include line/load regulation	–5		+5	%
Quiescent current	No load	–	8	–	μA
Line regulation	V <sub>in</sub> from (V <sub>o</sub> + 0.1 V) to 4.8 V, max load	–0.2		+0.2	%V <sub>o</sub> /V
Load regulation	Load from 1 mA to 50 mA		0.02	0.05	%V <sub>o</sub> /mA
Leakage current	In power-down mode at 25°C junction temp	–	0.3	–	μA
PSRR	V <sub>bat</sub> 3.6V, V <sub>o</sub> = 2.5V, C <sub>o</sub> = 1 μF, max load, 100 Hz to 100 kHz	20	–		dB
LDO turn-on time	LDO turn-on time when the rest of the chip is up	–	–	100	μs

**Note**

6. Guaranteed TX power is 4 dBm when PALDO input supply voltage is 1.8 V.

## Electrical specifications

**Table 16 PA LDO (continued)**

Specification	Notes	Min	Typ	Max	Units
In-rush current during turn-on	From its output cap in the fully-discharged state	–	–	70	mA
External output capacitor (Co)	Ceramic, X5R, 0402, (ESR: 30 m–200 mΩ), ±10%, 6.3 V	0.44	1	–	μF
External input capacitor	For PALDO_VDDIN_5V pin Ceramic, X5R, 0402, (ESR: 30 m–200 mΩ), ±10%, 6.3 V	–	1	–	μF

**Note**

6. Guaranteed TX power is 4 dBm when PALDO input supply voltage is 1.8 V.

**3.1.4 RF LDO**
**Table 17 RF LDO**

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Min Vin = Vo + 0.15 V = 1.35 V (for Vo = 1.2 V) Dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Nominal output voltage, Vo	Internal default bit setting 000	–	1.2	–	V
Output voltage programmability	Range	1.1	–	1.275	V
	Step size	–	25	–	mV
	Accuracy at any step (including line/load regulation)	–4	–	+4	%
Dropout voltage	At maximum load	–	–	150	mV
Output current	Operating voltage range	0.1	–	25	mA
Quiescent current	No load	–	44	–	μA
Line regulation	Vin from (Vo + 0.15 V) to 1.5 V; 25 mA load	–	–	5.5	mV/V
Load regulation	Load from 1 mA to 25 mA; Vin ≥ (Vo + 0.15 V)	–	0.025	0.045	mV/ mA
Load step error	Load step from 1 mA–25 mA in 1 μs and 25 mA–1 mA in 1 μs; Vin(Vo + 0.15 V); Co = 2.2 μF	–	–	35	mV
Leakage current	Power-down junction temperature: 85°C	–	–	10	μA
Output noise	@30 kHz, 25 mA load, Co = 2.2 μF	–	–	60	nV/ √Hz
	@100 kHz, 25 mA load, Co = 2.2 μF	–	–	35	nV/ √Hz
PSRR	@1 kHz, Input > 1.35 V, Co = 2.2 μF, Vo = 1.2 V	20	–	–	dB
LDO turn-on time	LDO turn-on time when balance of chip is up	–	140	180	μs
In-rush current	Vin = Vo+0.15 V to 1.5 V, Co = 2.2 μF, no load	–	–	100	mA

## Electrical specifications

**Table 17** RF LDO (continued)

Parameter	Conditions	Min	Typ	Max	Unit
External output capacitor, Co	Total ESR (trace/cap): 5 m–240 mΩ	0.5	2.2	4.7	μF
External input capacitor	Only use an external input capacitor at RFLDO_VDDIN1P5 pin if it is not supplied from CBUCK output.	–	1	2.2	μF

**Note:** Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

### 3.1.5 Digital I/O characteristics

**Table 18** Digital I/O characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage (VDDO = 3.3 V)	V <sub>IL</sub>	–	–	0.8	V
Input high voltage (VDDO = 3.3 V)	V <sub>IH</sub>	2.0	–	–	V
Input low voltage (VDDO = 1.8 V)	V <sub>IL</sub>	–	–	0.6	V
Input high voltage (VDDO = 1.8 V)	V <sub>IH</sub>	1.1	–	–	V
Output low voltage	V <sub>OL</sub>	–	–	0.4	V
Output high voltage	V <sub>OH</sub>	VDDO – 0.4V	–	–	V
Input low current	I <sub>IL</sub>	–	–	1.0	μA
Input high current	I <sub>IH</sub>	–	–	1.0	μA
Output low current (VDDO = 3.3 V, V <sub>OL</sub> = 0.4 V)	I <sub>OL</sub>	–	–	2.0	mA
Output high current (VDDO = 3.3 V, V <sub>OH</sub> = 2.9 V)	I <sub>OH</sub>	–	–	4.0	mA
Output high current (VDDO = 1.8 V, V <sub>OH</sub> = 1.4 V)	I <sub>OH</sub>	–	–	2.0	mA
Input capacitance	C <sub>IN</sub>	–	–	0.4	pF

### 3.1.6 Current consumption

In [Table 19](#), current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN.

**Table 19** Bluetooth® LE current consumption

Operational mode	Conditions	Typ	Unit
Receiving	Receiver and baseband are both operating, 100% ON.	8	mA
Transmitting@12 dBm	Transmitter and baseband are both operating, 100% ON.	18	mA
Advertising	1.28s direct advertising in low power idle mode	30	μA
Scanning	1.28s scan interval and 11.25 mS scan window	0.076	mA
Connecting	1-second connection interval in low power idle mode	25	μA
HIDOFF (Deep Sleep)	–	1	μA

## Electrical specifications

**3.2 ADC electrical characteristics**
**Table 20 ADC electrical characteristics**

Parameter	Symbol	Conditions/comments	Min	Typ	Max	Unit
Analog supply voltage	avddBAT	Battery and I/O supply	1.62	–	3.6	V
Analog core supply	AVDDC	±10%	1.08	1.2	1.32	V
Audio supply	Mic_avdd	Only available for audio application	1.8	2.5	3.3	V
Current consumption	I <sub>TOT</sub>	–	–	2	3	mA
Power down current	–	At room temperature	–	1	–	µA
<b>ADC Core Specification</b>						
ADC reference voltage	VREF	From BG with ±3% accuracy	–	0.85	–	V
ADC sampling clock	–	–	–	12	–	MHz
Absolute error	–	Includes gain error, offset and distortion. Without factory calibration.	–	–	5	%
		Includes gain error, offset and distortion. After factory calibration.	–	–	2	%
ENOB	–	For audio application	12	13	–	Bit
		For static measurement	10	–	–	
ADC input full scale	FS	For audio application	–	1.6	–	
		For static measurement	1.8	–	3.6	
Conversion rate	–	For audio application	8	16	–	kHz
		For static measurement	16	20	–	
Signal bandwidth	–	For audio application	20	–	8K	Hz
		For static measurement	–	DC	–	
Input impedance	R <sub>IN</sub>	For audio application	10	–	–	KΩ
		For static measurement	500	–	–	
Startup time	–	For audio application	–	10	–	ms
		For static measurement	–	20	–	
<b>MIC PGA specifications</b>						
MIC PGA gain range	–	–	0	–	42	dB
MIC PGA gain step	–	–	–	1	–	dB
MIC PGA gain error	–	Includes part-to-part gain variation	–1	–	1	dB
PGA input referred noise	–	At 42 dB PGA gain A-weighted	–	–	4	µV
Passband gain flatness	–	PGA and ADC, 100 Hz–4 kHz	–0.5	–	0.5	dB
<b>MIC bias specifications</b>						
MIC bias output voltage	–	At 2.5 V supply	–	2.1	–	V
MIC bias loading current	–	–	–	–	3	mA

**Note**

7. Conditional requirement for the measurement time of 10 µs. Relaxed with longer measurement time for each GPIO input channel.

## Electrical specifications

**Table 20 ADC electrical characteristics (continued)**

Parameter	Symbol	Conditions/comments	Min	Typ	Max	Unit
MIC bias noise	–	Refers to PGA input 20 Hz to 8 kHz, A-weighted	–	–	3	μV
MIC bias PSRR	–	at 1 kHz	40	–	–	dB
ADC SNR	–	A-weighted 0 dB PGA gain	78	–	–	dB
ADC THD + N	–	–3 dBFS input 0 dB PGA gain	74	–	–	dB
GPIO input voltage	–	Always lower than avddBAT	–	–	3.6	V
GPIO source impedance <sup>[7]</sup>	–	Resistance	–	–	1	kΩ
		Capacitance	–	–	10	pF

**Note**

7. Conditional requirement for the measurement time of 10 μs. Relaxed with longer measurement time for each GPIO input channel.

### 3.3 RF specifications

**Note:** Table 21 and Table 22 apply to single-ended industrial temperatures. Unused inputs are left open.

**Table 21 Receiver RF specifications**

Parameter	Conditions	Min	Typ <sup>[8]</sup>	Max	Unit
Out-of-band blocking performance (CW) <sup>[9]</sup>					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Inter-modulation performance <sup>[10]</sup>					
BT, Df = 4 MHz	–	–39.0	–	–	dBm
Spurious emissions <sup>[11]</sup>					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM RX	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

**Notes**

8. Typical operating conditions are 1.22 V operating voltage and 25°C ambient temperature.

9. Meets this specification using front-end band pass filter.

10.  $f_0 = -64$  dBm Bluetooth®-modulated signal,  $f_1 = -39$  dBm sine wave,  $f_2 = -39$  dBm Bluetooth®-modulated signal,  $f_0 = 2f_1 - f_2$ , and  $|f_2 - f_1| = n \cdot 1$  MHz, where  $n$  is 3, 4, or 5. For the typical case,  $n = 4$ .

11. Includes baseband radiated emissions.

Electrical specifications

**Table 22 Transmitter RF specifications**

Parameter	Conditions	Min	Typ	Max	Unit
<b>General</b>					
Frequency range	–	2402	–	2480	MHz
GFSK TX power	–	–	12	–	dBm
Power control step	–	2	4	8	dB
<b>Out-of-band spurious emissions</b>					
30 MHz to 1 GHz	–	–	–	–36.0 <sup>[12]</sup>	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 <sup>[12, 13]</sup>	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

**Notes**

- 12. Maximum value is the value required for Bluetooth® qualification.
- 13. Meets this spec using a front-end band-pass filter.

**Table 23 Bluetooth® LE RF specifications**

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sense <sup>[14]</sup>	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power	N/A	–	12	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max <sup>[15]</sup>	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

**Notes**

- 14. Dirty TX is OFF.
- 15. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

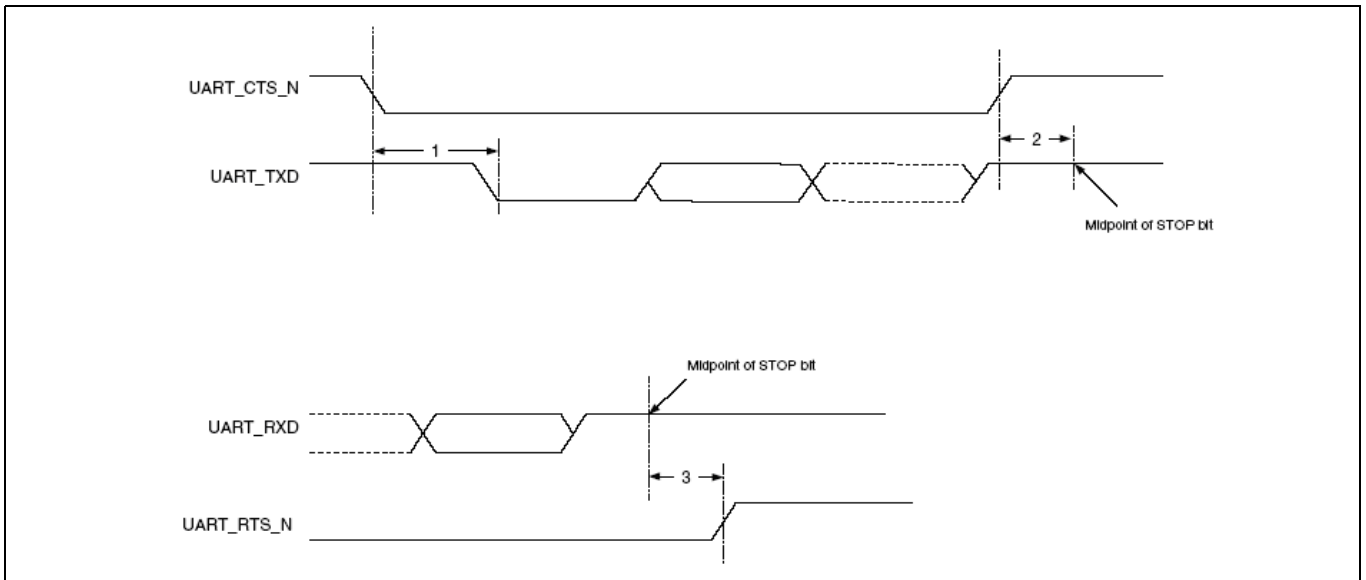
### 3.4 Timing and AC characteristics

In this section, use the numbers listed in the Reference column of each table to interpret the following timing diagrams.

#### 3.4.1 UART timing

**Table 24** UART timing specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	1.50	Baud periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	0.67	Baud periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	1.33	Baud periods



**Figure 9** UART timing



Electrical specifications

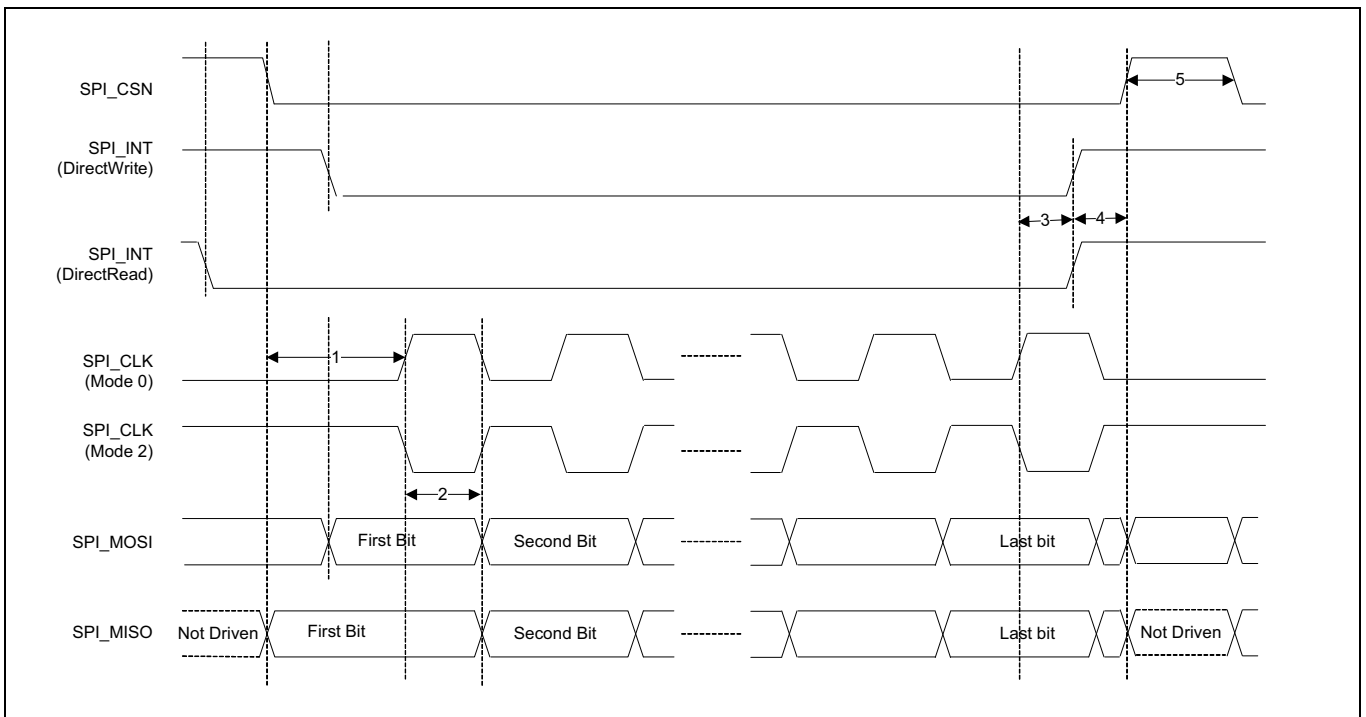
**3.4.2 SPI timing**

The SPI interface can be clocked up to 12 MHz.

**Table 25** and **Figure 10** show the timing requirements when operating in SPI mode 0 and 2.

**Table 25 SPI Mode 0 and 2**

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns



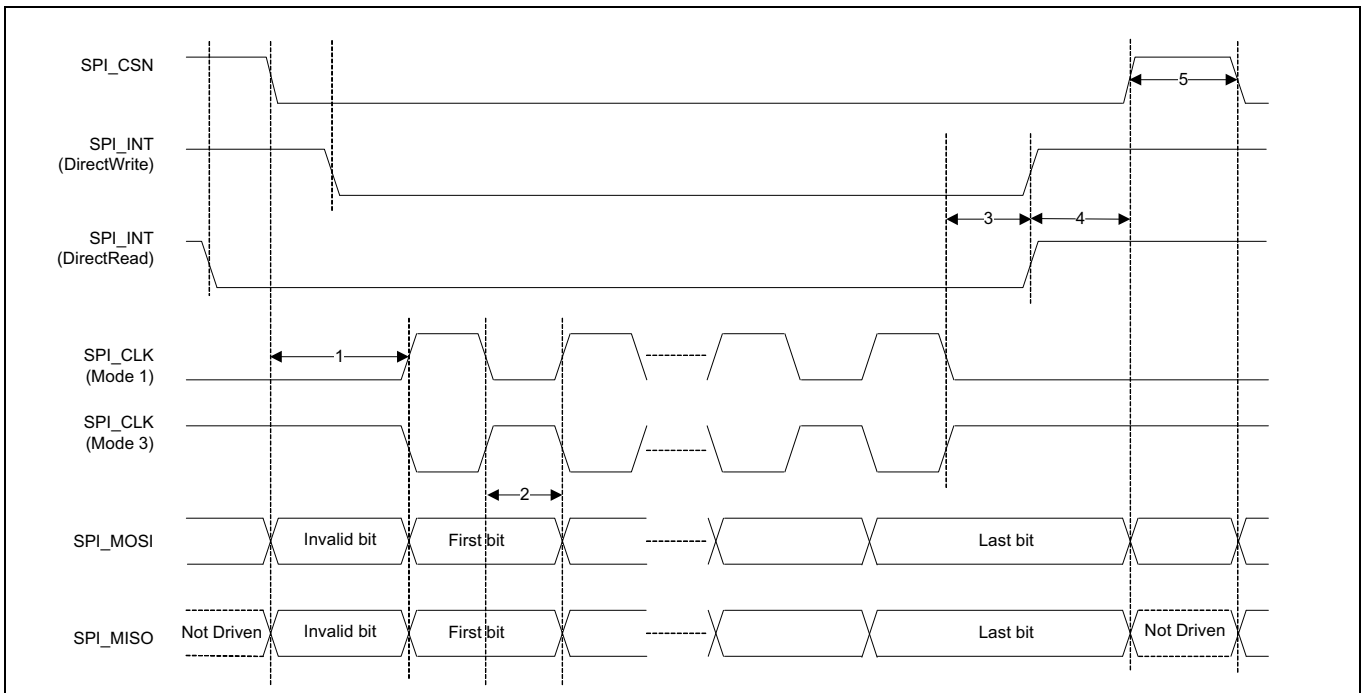
**Figure 10 SPI timing, mode 0 and 2**

Electrical specifications

**Table 26** and **Figure 11** show the timing requirements when operating in SPI mode 1 and 3.

**Table 26 SPI mode 1 and 3**

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns



**Figure 11 SPI timing, mode 1 and 3**

Electrical specifications

**3.4.3 I<sup>2</sup>C interface timing**

The specifications in **Table 27** references **Figure 12**.

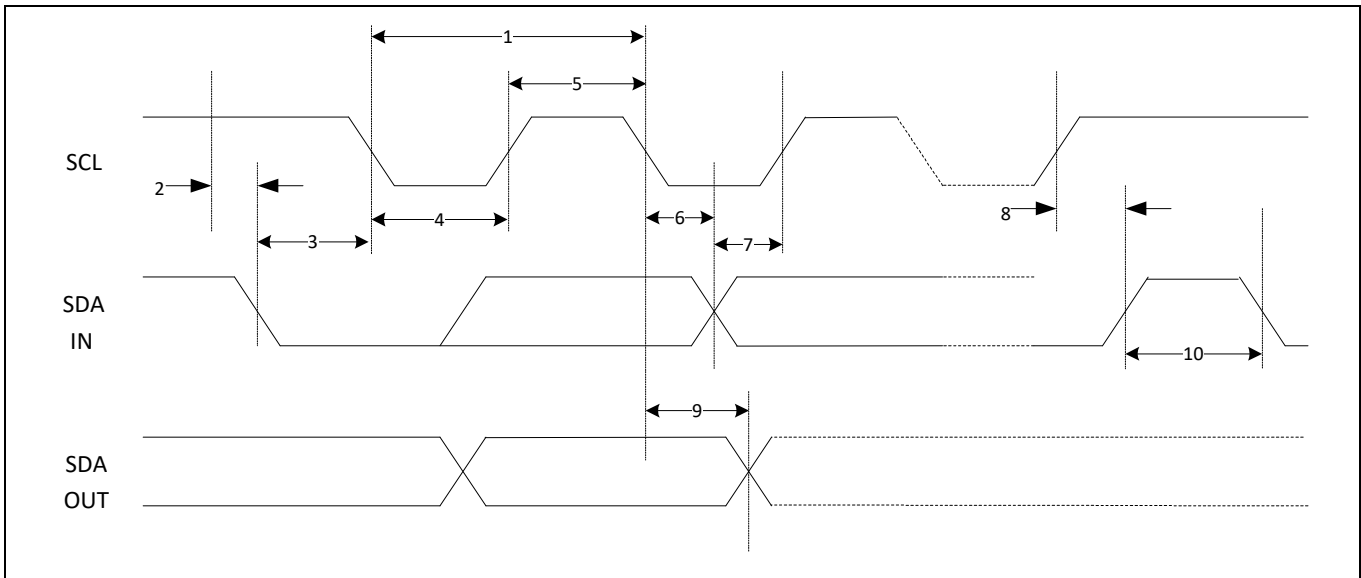
**Table 27 I<sup>2</sup>C interface timing specifications (up to 1 MHz)**

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	-	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	-	ns
3	START condition hold time	280	-	ns
4	Clock low time	650	-	ns
5	Clock high time	280	-	ns
6	Data input hold time <sup>[16]</sup>	0	-	ns
7	Data input setup time	100	-	ns
8	STOP condition setup time	280	-	ns
9	Output valid from clock	-	400	ns
10	Bus free time <sup>[17]</sup>	650	-	ns

**Notes**

16.As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

17.Time that the CBUS must be free before a new transaction can start.



**Figure 12 I<sup>2</sup>C interface timing diagram**

Electrical specifications

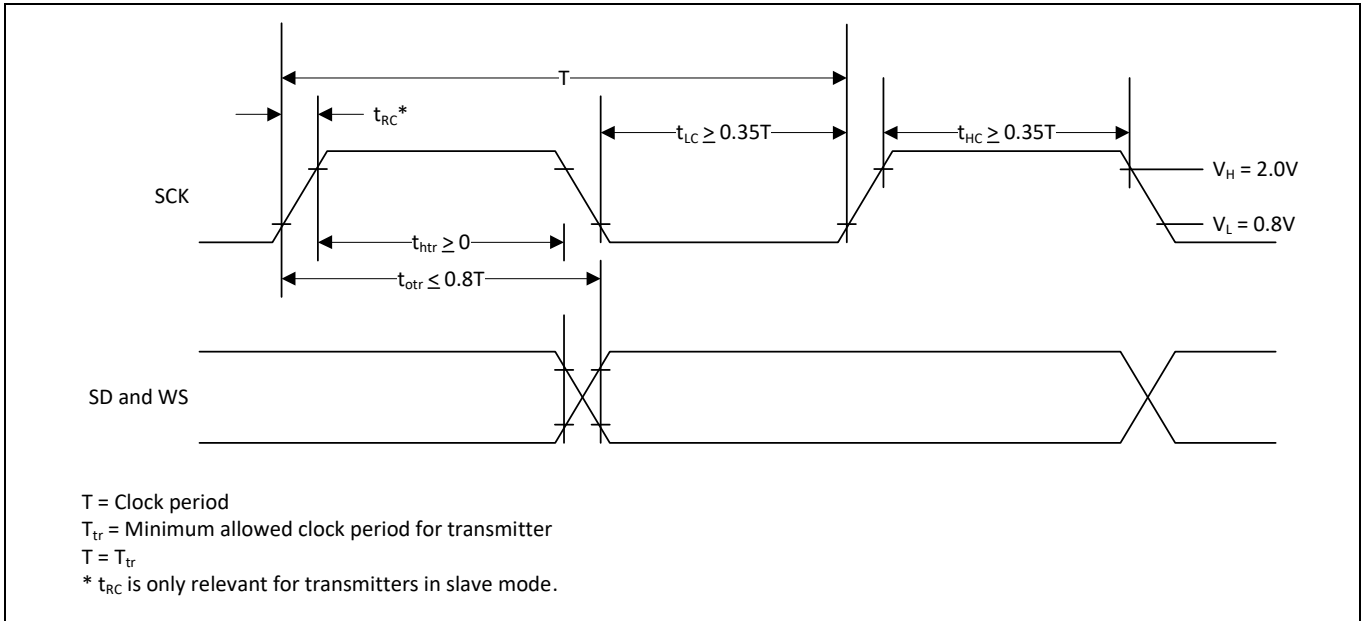
**Table 28 Timing for I<sup>2</sup>S transmitters and receivers**

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period T	T <sub>tr</sub>	-	-	-	T <sub>r</sub>	-	-	-	[18]
<b>Master mode: Clock generated by transmitter or receiver</b>									
HIGH t <sub>HC</sub>	0.35T <sub>tr</sub>	-	-	-	0.35T <sub>tr</sub>	-	-	-	[19]
LOW t <sub>LC</sub>	0.35T <sub>tr</sub>	-	-	-	0.35T <sub>tr</sub>	-	-	-	[19]
<b>Slave mode: Clock accepted by transmitter or receiver</b>									
HIGH t <sub>HC</sub>	-	0.35T <sub>tr</sub>	-	-	-	0.35T <sub>tr</sub>	-	-	[20]
LOW t <sub>LC</sub>	-	0.35T <sub>tr</sub>	-	-	-	0.35T <sub>tr</sub>	-	-	[20]
Rise time t <sub>RC</sub>	-	-	0.15T <sub>tr</sub>	-	-	-	-	-	[21]
<b>Transmitter</b>									
Delay t <sub>dtr</sub>	-	-	-	0.8T	-	-	-	-	[22]
Hold time t <sub>htr</sub>	0	-	-	-	-	-	-	-	[21]
<b>Receiver</b>									
Setup time t <sub>sr</sub>	-	-	-	-	-	0.2T <sub>r</sub>	-	-	[23]
Hold time t <sub>hr</sub>	-	-	-	-	-	0	-	-	[23]

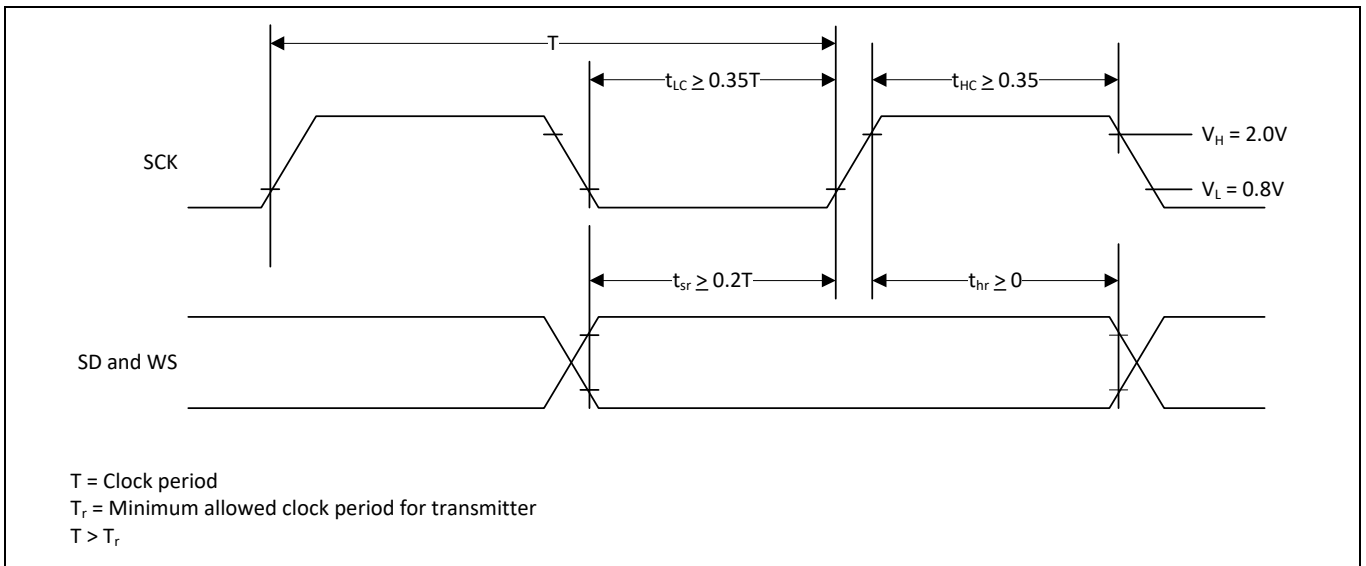
**Notes**

18. The system clock period T must be greater than T<sub>tr</sub> and T<sub>r</sub> because both the transmitter and receiver have to be able to handle the data transfer rate.
19. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t<sub>HC</sub> and t<sub>LC</sub> are specified with respect to T
20. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35T<sub>r</sub>, any clock that meets the requirements can be used.
21. Because the delay (t<sub>dtr</sub>) and the maximum transmitter speed (defined by T<sub>tr</sub>) are related, a fast transmitter driven by a slow clock edge can result in t<sub>dtr</sub> not exceeding t<sub>RC</sub> which means t<sub>htr</sub> becomes zero or negative. Therefore, the transmitter has to guarantee that t<sub>htr</sub> is greater than or equal to zero, so long as the clock rise-time t<sub>RC</sub> is not more than t<sub>RCmax</sub>, where t<sub>RCmax</sub> is not less than 0.15T<sub>tr</sub>
22. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
23. The data setup and hold time must not be less than the specified receiver setup and hold time.

Electrical specifications



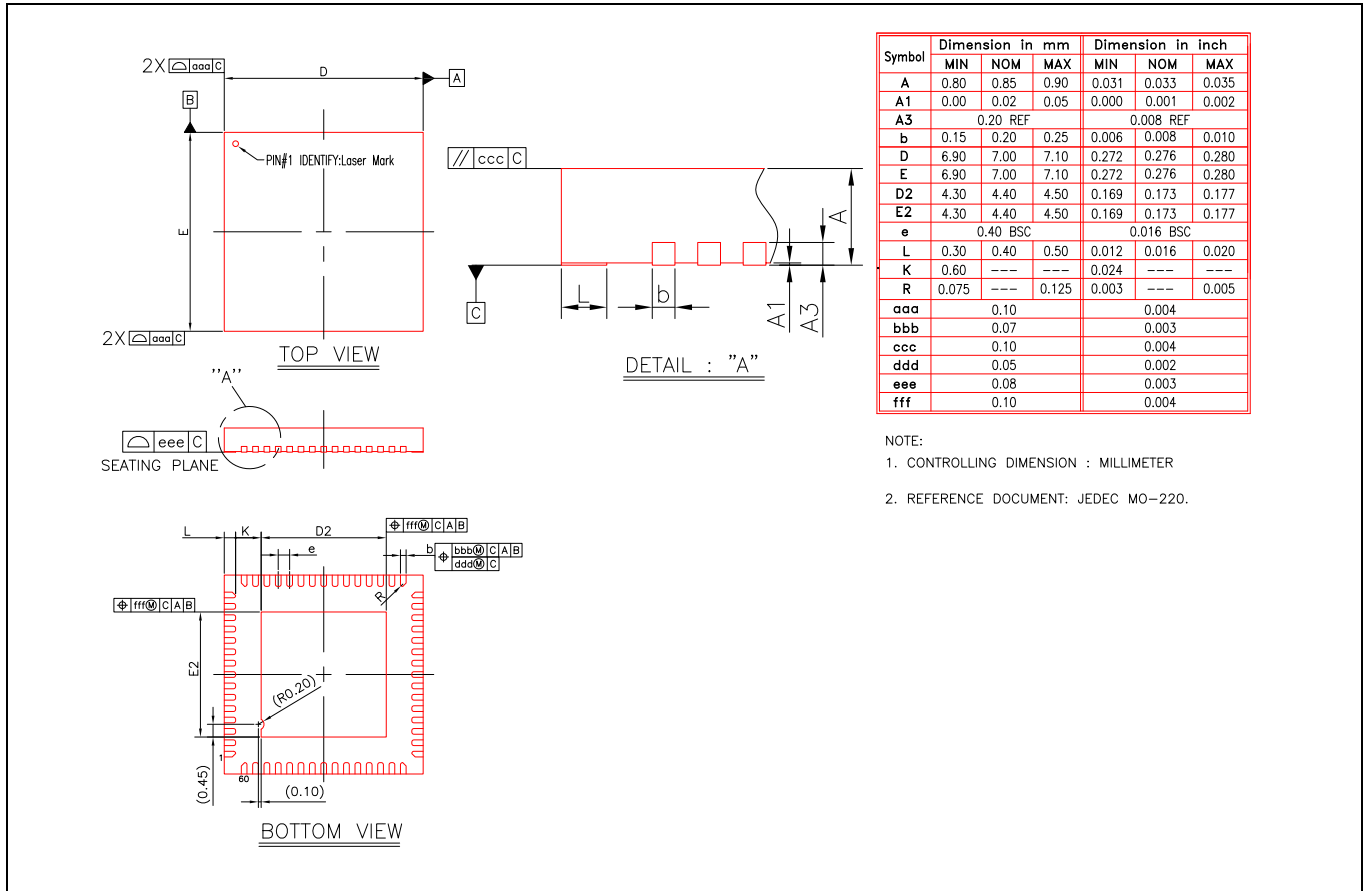
**Figure 13 I<sup>2</sup>S transmitter timing**



**Figure 14 I<sup>2</sup>S receiver timing**

Package diagram

### 4 Package diagram

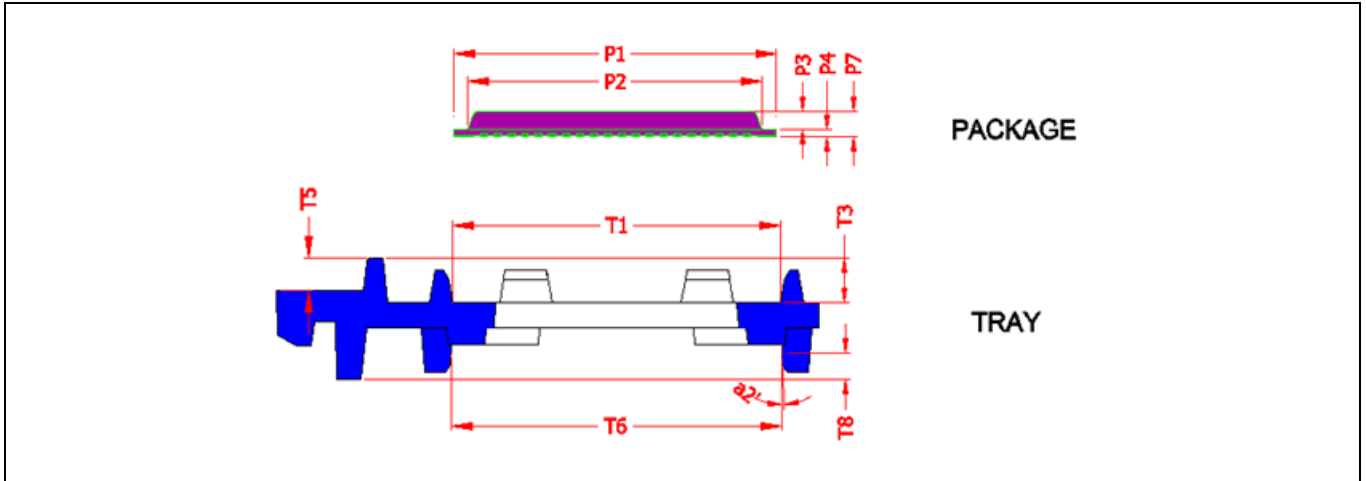


**Figure 15** CYW20835 7 mm × 7 mm 60-pin QFN package

Package diagram

**4.1 Tray packaging specifications**

The CYW20835 QFN package and tray dimensions are annotated in **Figure 16** and defined in **Table 29** and **Table 30**.



**Figure 16** QFN package and tray dimensions

**Table 29** QFN package dimensions and tolerances

Parameter	Description	Nom	Min	Max	± Tol	Unit
P1	Package size	7	6.9	7.1	0.1	mm
P2	Top hat width	0	0	0	-	mm
P3	Top hat height	0	0	0	-	mm
P4	Substrate thickness	0.85	0.8	0.9	0.05	mm
P7	Total thickness (P3 + P4)	0.85	0.8	0.9	0.05	mm

**Table 30** QFN tray dimensions and tolerances

Parameter	Description	Nom	Min	Max	± Tol	Unit
T1	Top pocket size	7.25	7.17	7.33	0.08	mm
T3	Top pocket depth	1.75	1.5	2	0.25	mm
T5	Stacking height	2	1.87	2.13	0.13	mm
T6	Bottom pocket size	7.25	7.17	7.33	0.08	mm
T8	Bottom pocket depth	1.650	1.52	1.78	0.13	mm
a2	Bottom pocket relief wall draft angle	5	5	5	0	°C
T10	Packing value between two stacking trays	0.2	0.07	0.33	0.13	mm

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Ordering information

## 5 Ordering information

**Table 31**      **Ordering information**

<b>Part number</b>	<b>Package</b>	<b>Ambient operating temperature</b>
CYW20835PB1KML1G	60-pin QFN	-30°C to +85°C
CYW20835PB1KML1GT		



## 6 Additional information

### 6.1 IoT resources

Infineon provides a wealth of data at [www.infineon.com/cms/en/discoveries/internet-of-things](http://www.infineon.com/cms/en/discoveries/internet-of-things) to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Infineon provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Infineon community website at [community.infineon.com](http://community.infineon.com).

## 7 Acronyms

**Table 32 Acronyms used in this document**

<b>Acronym</b>	<b>Description</b>
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
AHB	advanced high-performance bus
APB	advanced peripheral bus
BTC	Bluetooth® controller
COEX	coexistence
DFU	device firmware update
DMA	direct memory access
HCI	Host Control Interface
IF	intermediate frequency
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LHL	lean high land
LPO	low power oscillator
PDM	pulse density modulation
PLL	phase locked loop
PMU	power management unit
PWM	pulse width modulation
QD	quadrature decoder
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read-only memory
RX/TX	receive, transmit
SPI	serial peripheral interface
SW	software
SWD	serial wire debug
UART	universal asynchronous receiver/transmitter
UPI	μ-processor interface
WD	watchdog

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Revision history

## Revision history

Document revision	Date	Description of changes
**	2021-08-04	Initial release
*A	2022-07-21	Migrated to Infineon template Added Bluetooth® 5 features in <a href="#">Table 1</a> Updated footnote 3 in <a href="#">Table 12</a> Updated scanning mode in <a href="#">Table 19</a> Added ordering part numbers and updated operating temperature in <a href="#">Table 31</a> Updated maximum channels to 40 in <b>“Local oscillator”</b> on page 10

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