AIMZHN120R080M1T

CoolSiC™ 1200 V SiC Trench MOSFET

Final datasheet

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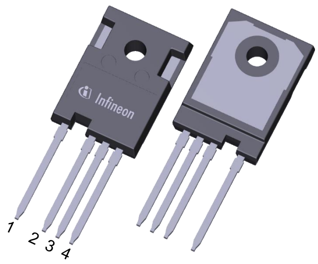


Halogen-free

Green

Lead-free

RoHS

AEC Qualified

Features

- V_{DSS} = 1200 V at T_{vj} = -55...175°C
- I_{DDC} = 31 A at T_C = 25°C
- New performance-optimized chip technology (Gen1p) with improved R_{DSon}* A FOM
- Increased recommended turn-on voltage ($V_{GS(on)}$ = 20 V) for lower $R_{DS(on)}$
- Best-in-class switching energy for lower switching losses and reduced cooling efforts
- Lowest device capacitances for higher switching speeds and higher power density
- A combination of low C_{rss}/C_{iss} ratio and high $V_{GS(th)}$ to avoid parasitic turn-on and enable unipolar gate driving
- Reduced total gate charge Q_{Gtot} for lower driving power and losses
- .XT die attach technology for best-in-class thermal performance
- Sense pin for optimized switching performance
- Minimum creepage distance of 7.07 mm to fit HV requirements

Potential applications

- On-board charger
- DC/DC converter
- Auxiliary drives

Product validation

- Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

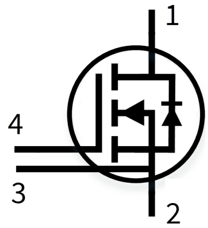
Pin definition:

1 – drain

2 – source

3 – Kelvin sense contact

4 – gate



Type	Package	Marking
AIMZHN120R080M1T	PG-TO247-4-U05	A12M1N080

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}				260	°C
MOSFET/body diode thermal resistance, junction-case[1)]	$R_{th(j-c)}$			0.68	0.89	K/W

1) Not subject to production test. Parameter verified by design / characterization

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage[1)]	V_{DSS}	T_{vj} = -55...175 °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$[2)]	I_{DDC}	V_{GS} = 20 V	T_c = 25 °C	31	A
			T_c = 100 °C	22	
Peak drain current, t_p limited by $T_{vj(max)}$[2)]	I_{DM}	V_{GS} = 20 V		79	A
Gate-source voltage, max. transient voltage[3)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage[3)]	V_{GS}			-5...23	V
Avalanche energy, single pulse	E_{AS}	I_D = 7.6 A, V_{DD} = 50 V, L = 4.76 mH		136	mJ
Power dissipation, limited by $T_{vj(max)}$[2)]	P_{tot}		T_c = 25 °C	169	W
			T_c = 100 °C	84	

1) Tested at Tvj=25°C, verified by design/characterization over full temperature range
2) Not subject to production test. Parameter verified by design / characterization
3) **Important note:**: The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		20	V
Recommended turn-off gate voltage	$V_{GS(off)}$		0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 10 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 20 V		80	100	mΩ
			T_{vj} = 100 °C, $V_{GS(on)}$ = 20 V		112		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 20 V		159		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		84		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 3.3 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.7	4.4	5.1	V
			T_{vj} = 175 °C		3.6		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C		0.2	10	µA
			T_{vj} = 175 °C		50		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 25 V			100	nA
			V_{GS} = -10 V			-100	
Forward transconductance	g_{fs}	I_D = 10 A, V_{DS} = 20 V			6.2		S
Short-circuit withstand time[1]	t_{SC}	V_{DD} ≤ 800 V, $V_{DS,peak}$ < 1200 V, $T_{vj(start)}$=25 °C, $R_{G,ext}$=2 Ω	$V_{GS(on)}$ = 20 V		1.5		µs
			$V_{GS(on)}$ = 18 V		2		
			$V_{GS(on)}$ = 15 V		2.5		
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			3.8		Ω
Input capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			671		pF
Output capacitance	C_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			35		pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			2		pF
C_{oss} stored energy	E_{oss}	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			14		µJ
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, turn-on pulse			24		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, turn-on pulse			7		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, turn-on pulse			4		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		8		ns
			T_{vj} = 175 °C		8		

(table continues...)

Table 4 **(continued) Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		6		ns
			T_{vj} = 175 °C		7		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		13		ns
			T_{vj} = 175 °C		14		
Fall time	t_f	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		13		ns
			T_{vj} = 175 °C		13		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		58		µJ
			T_{vj} = 175 °C		91		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		34		µJ
			T_{vj} = 175 °C		38		
Total switching energy	E_{tot}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 33 nH	T_{vj} = 25 °C		92		µJ
			T_{vj} = 175 °C		129		
Virtual junction temperature	T_{vj}			-55		175	°C

1) verified by the design/characterization

Note: *Dynamic test circuit see Fig. F.*
Characteristics at T_{vj} = 25°C, unless otherwise specified.

3 Body diode (MOSFET)

Table 5 **Maximum rated values**

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage[1)]	V_{DSS}	T_{vj} = -55...175 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$[2)]	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	22.7	A
			T_c = 100 °C	17	

(table continues...)

Table 5 (continued) Maximum rated values

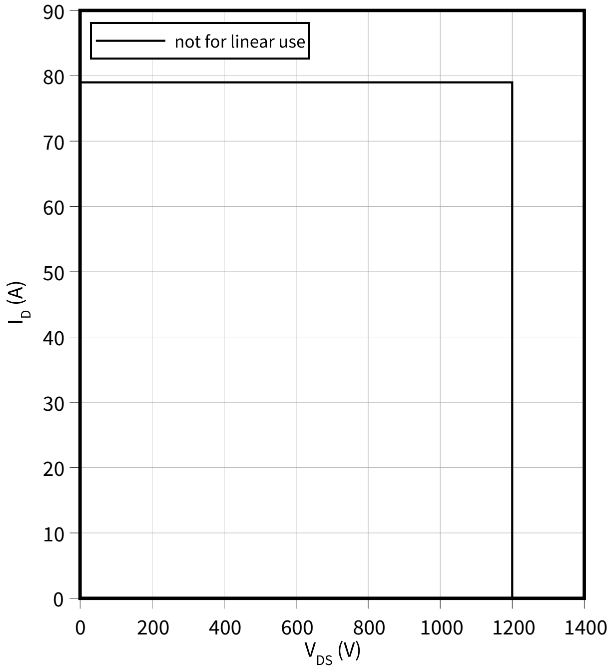
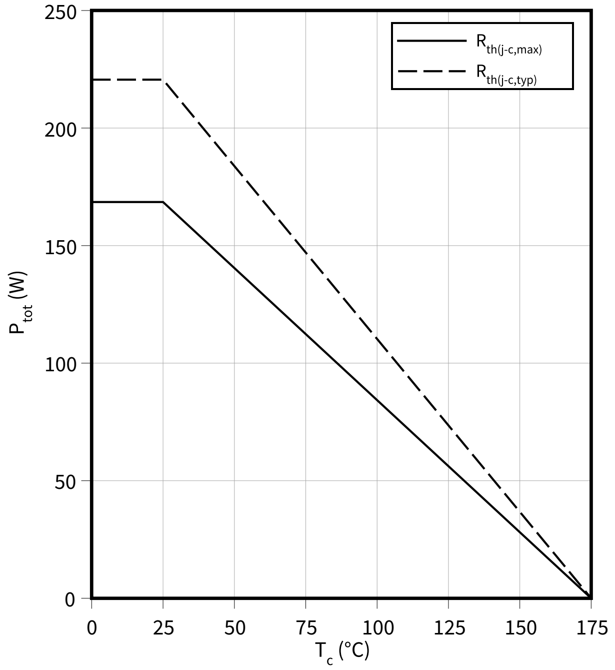
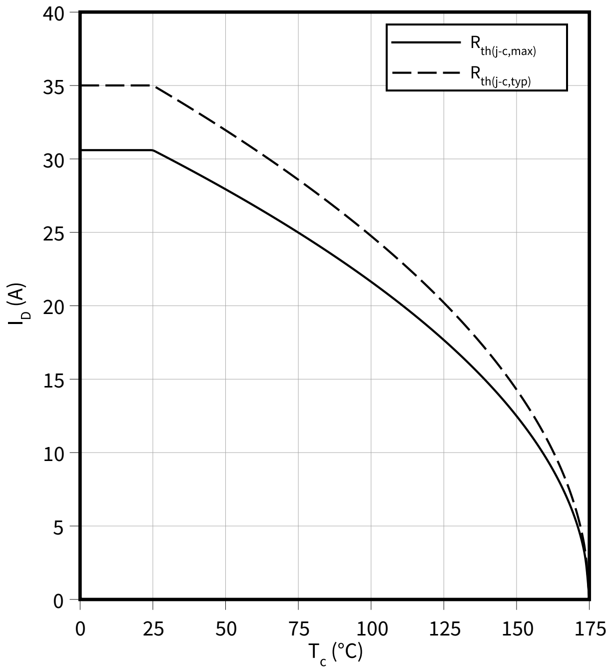
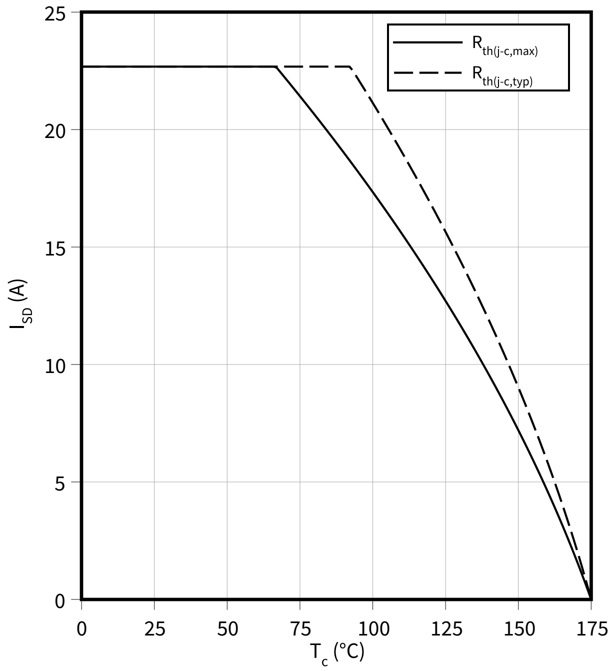
Parameter	Symbol	Note or test condition		Values	Unit
Peak reverse drain current, t_p limited by $T_{vj(max)}$ [2]	I_{SM}	$V_{GS} = 0$ V		22.7	A
			$-5\ V \leq V_{GS} \leq 0$ V, $t_p = 0.3$ µs	30	
			$-5 \leq V_{GS} \leq 0$ V, $T_{vj} \leq 175$°C; $t_p \leq 0.3$ ms for accumulated conduction time < 5 s or $t_p \leq 1$ ms for accumulated conduction time < 2.5 s [3]	78	

1) Tested at Tvj=25°C, verified by design/characterization
2) Not subject to production test. Parameter verified by design / characterization
3) Combination of t_p and Ism should not lead to $T_{vj(max)} > 175$°C

Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	$I_{SD} = 10$ A, $V_{GS} = 0$ V	$T_{vj} = 25$ °C		3.9	5	V
			$T_{vj} = 100$ °C		3.8		
			$T_{vj} = 175$ °C		3.7		
MOSFET forward recovery charge	Q_{fr}	$V_{DD} = 800$ V, $I_{SD} = 10$ A, $V_{GS} = 0$ V, $-di_{SD}/dt = 1000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		143		nC
			$T_{vj} = 175$ °C		270		
MOSFET peak forward recovery current	I_{frm}	$V_{DD} = 800$ V, $I_{SD} = 10$ A, $V_{GS} = 0$ V, $-di_{SD}/dt = 1000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		8		A
			$T_{vj} = 175$ °C		10		
Virtual junction temperature	T_{vj}			-55		175	°C

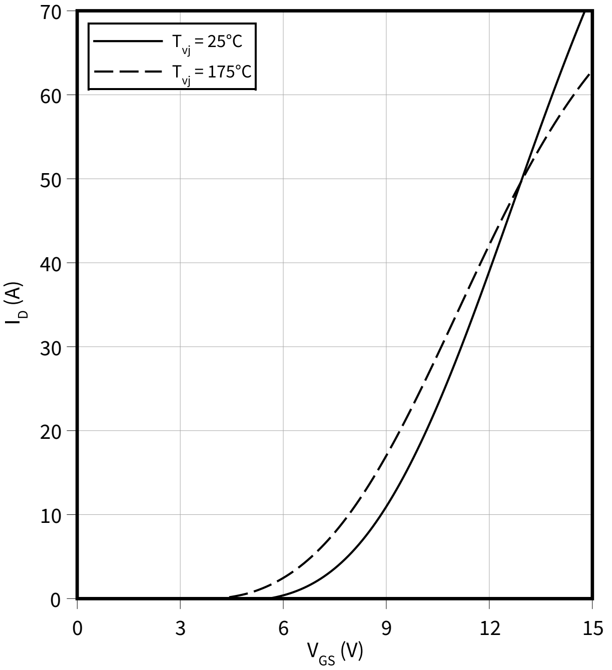
4 Characteristics diagrams

Reverse bias safe operating area (RBSOA) $I_D = f(V_{DS})$ $V_{GS} = 0/20$ V, $T_{vj} \leq 175$ °C, $T_c = 25$ °C	Power dissipation as a function of case temperature $P_{tot} = f(T_c)$
 	
Maximum DC drain to source current as a function of case temperature $I_D = f(T_c)$	**Maximum source to drain current as a function of case temperature** $I_{SD} = f(T_c)$ $V_{GS} = 0$ V
 	

Typical transfer characteristic

$I_D = f(V_{GS})$

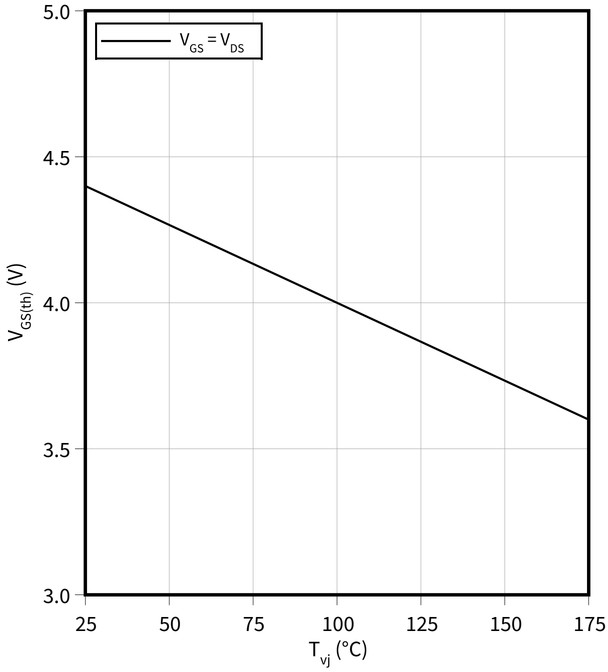
$V_{DS} = 20$ V, $t_p = 20$ µs



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

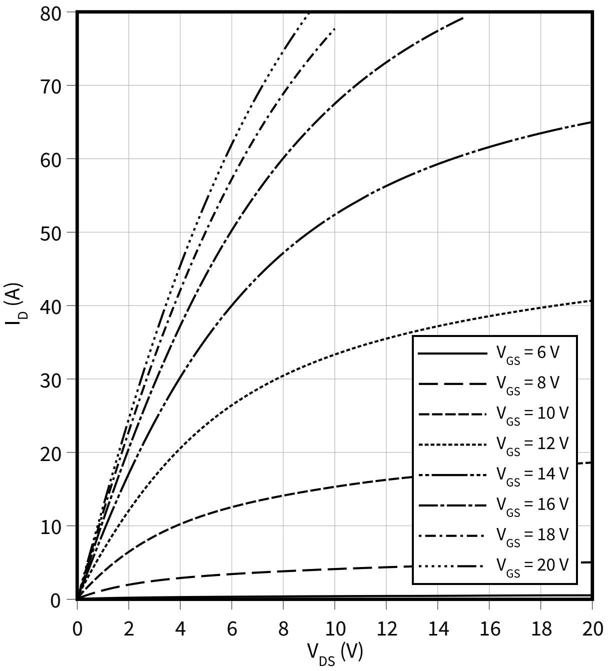
$I_D = 3.3$ mA



Typical output characteristic, V_{GS} as parameter

$I_D = f(V_{DS})$

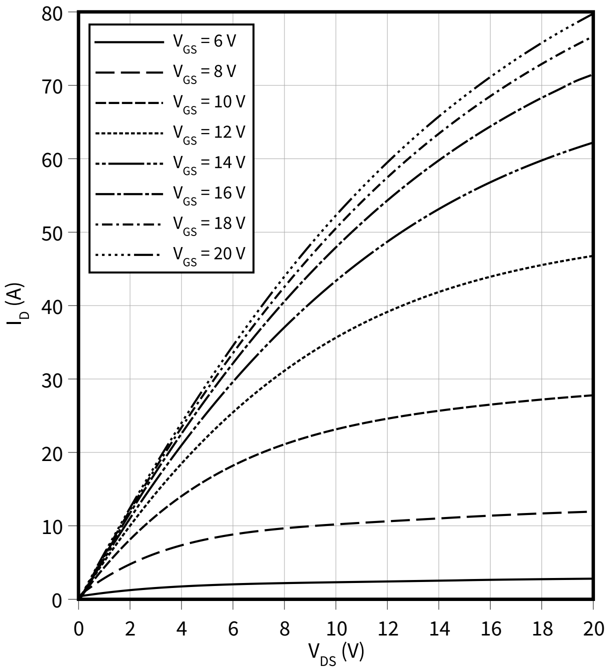
$T_{vj} = 25$ °C, $t_p = 20$ µs



Typical output characteristic, V_{GS} as parameter

$I_D = f(V_{DS})$

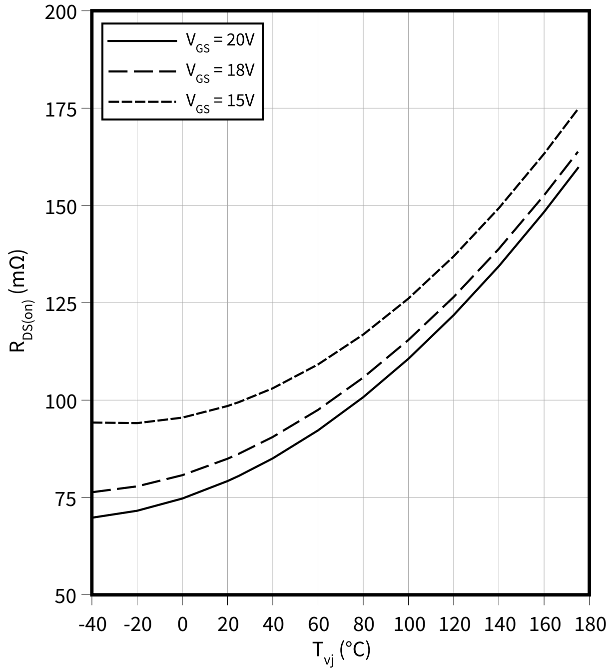
$T_{vj} = 175$ °C, $t_p = 20$ µs



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$

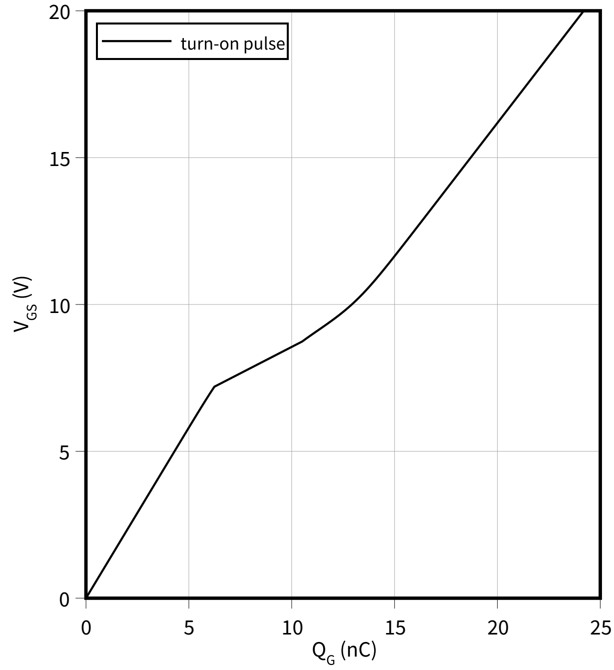
$I_D = 10$ A



Typical gate charge

$V_{GS} = f(Q_G)$

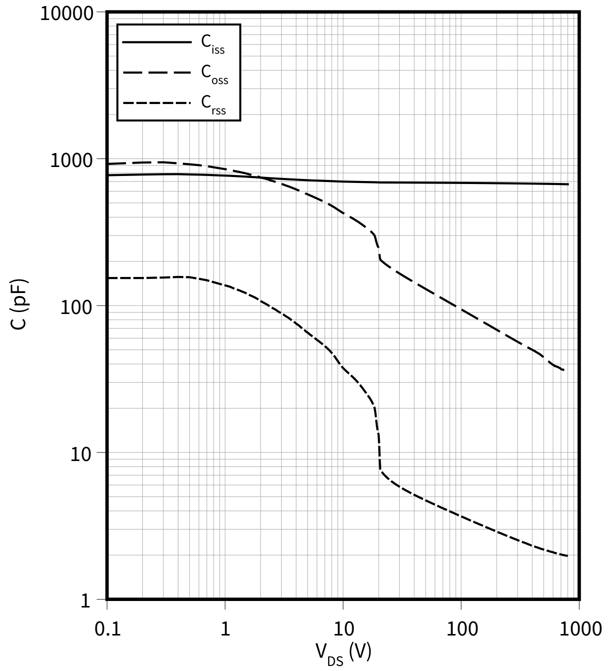
$I_D = 10$ A, $V_{DS} = 800$ V



Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$

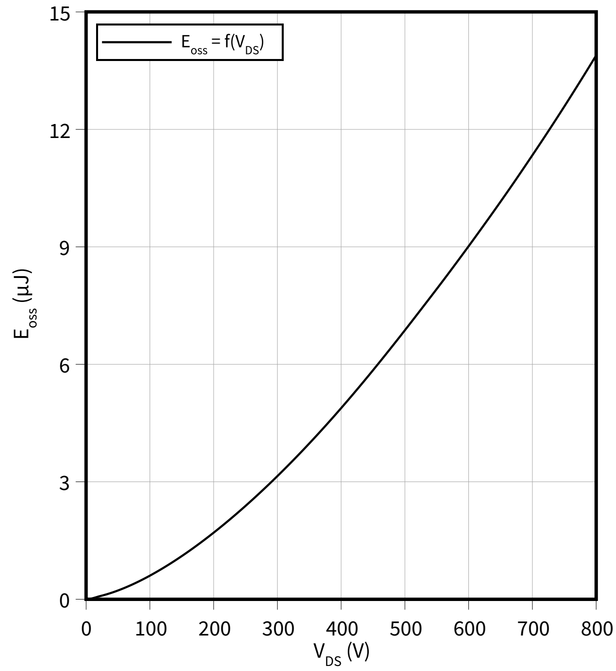
f = 100 kHz, $V_{GS} = 0$ V



Typical C_{oss} stored energy

$E_{oss} = f(V_{DS})$

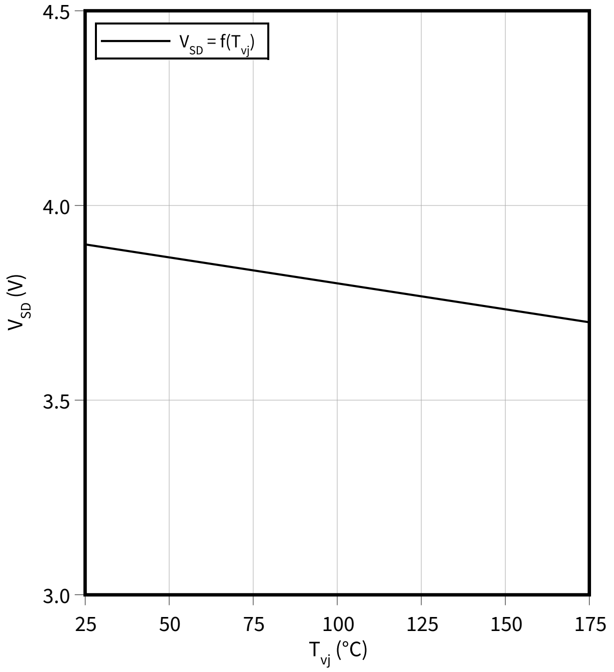
f = 100 kHz, $V_{GS} = 0$ V



Typical reverse drain voltage as function of junction temperature

$V_{SD} = f(T_{vj})$

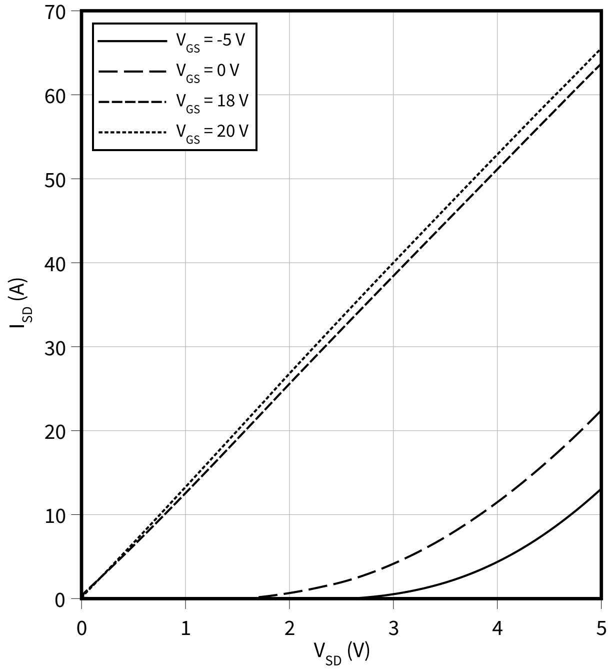
$I_{SD} = 10$ A, $V_{GS} = 0$ V



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

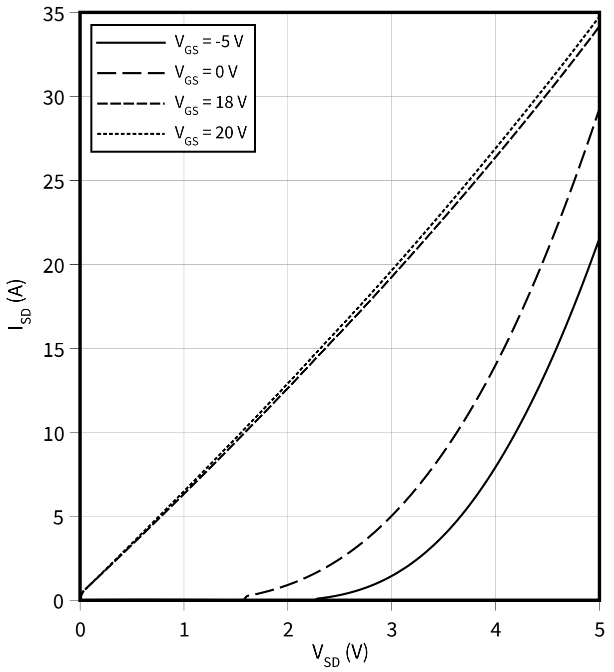
$T_{vj} = 25$ °C, $t_p = 20$ µs



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

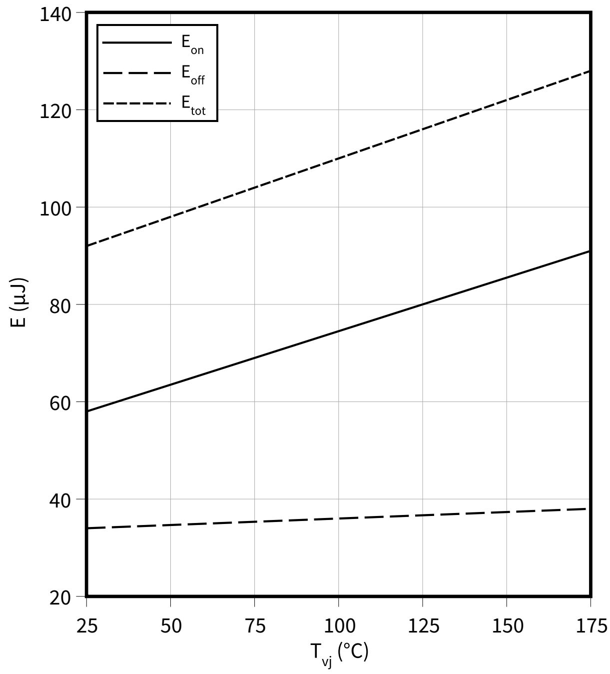
$T_{vj} = 175$ °C, $t_p = 20$ µs



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0$ V

$E = f(T_{vj})$

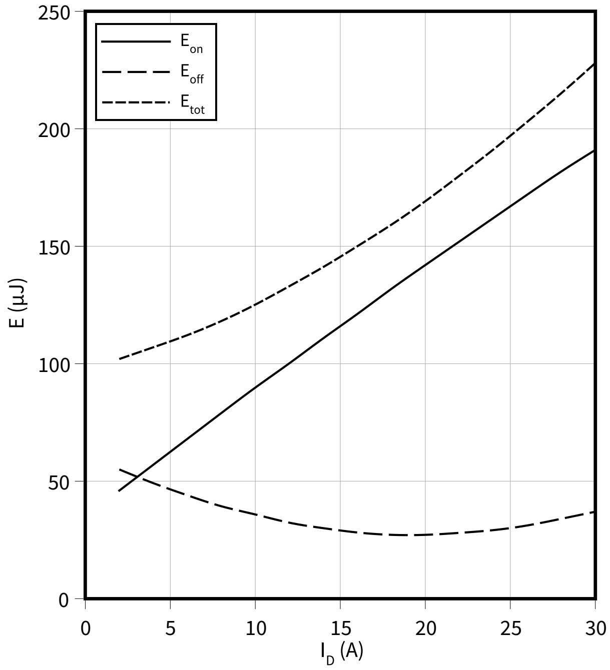
$V_{GS} = 0/20$ V, $I_D = 10$ A, $R_{G,ext} = 2$ Ω, $V_{DD} = 800$ V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(I_D)$

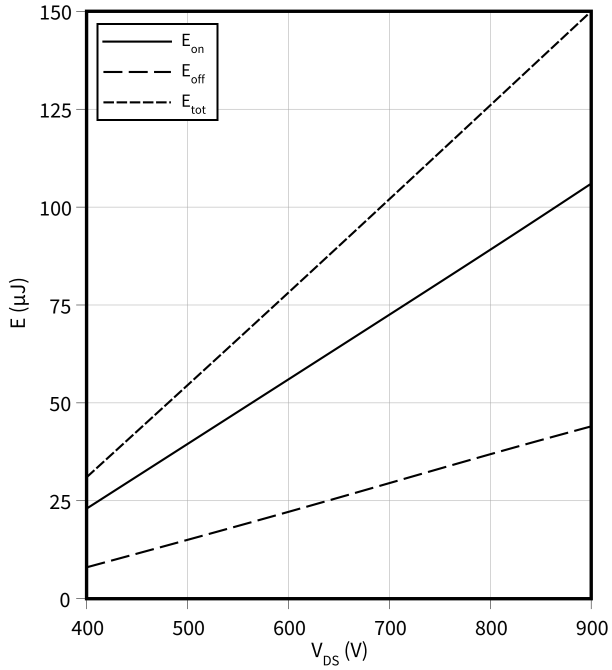
V_{GS} = 0/20 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(V_{DS})$

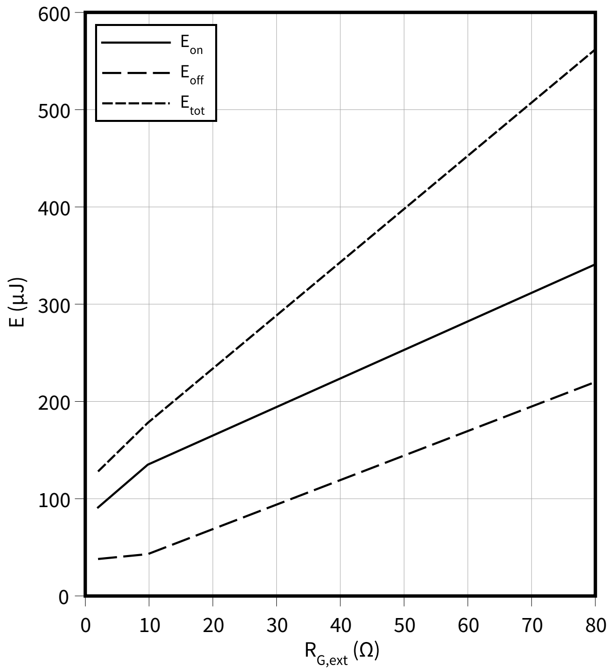
V_{GS} = 0/18 V, I_D = 10 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2 Ω



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

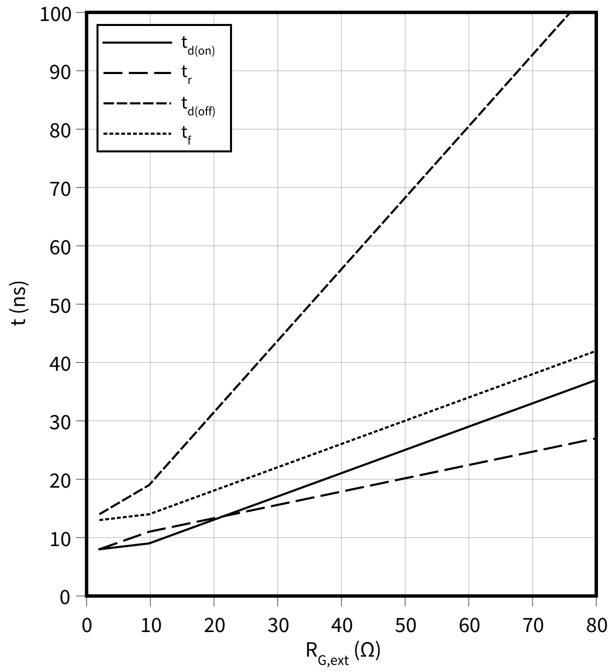
V_{GS} = 0/20 V, I_D = 10 A, T_{vj} = 175 °C, V_{DD} = 800 V

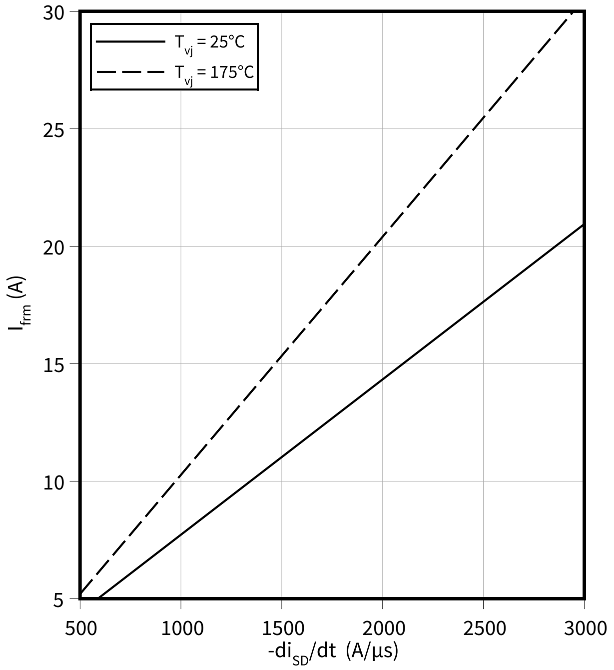
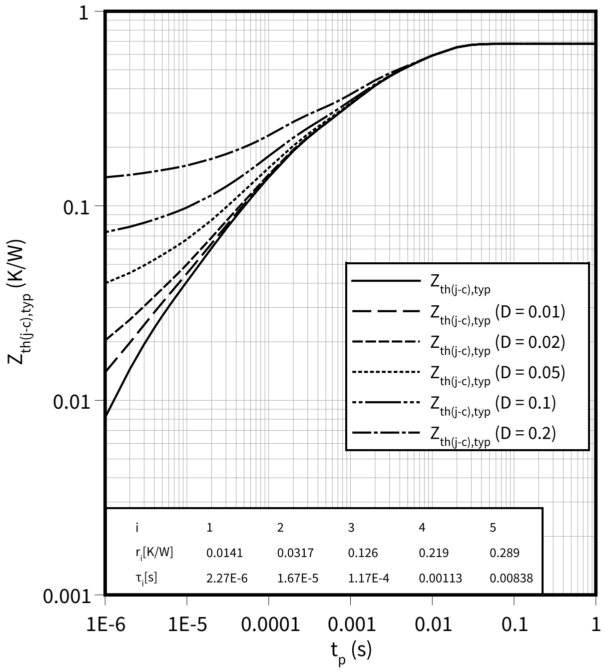


Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

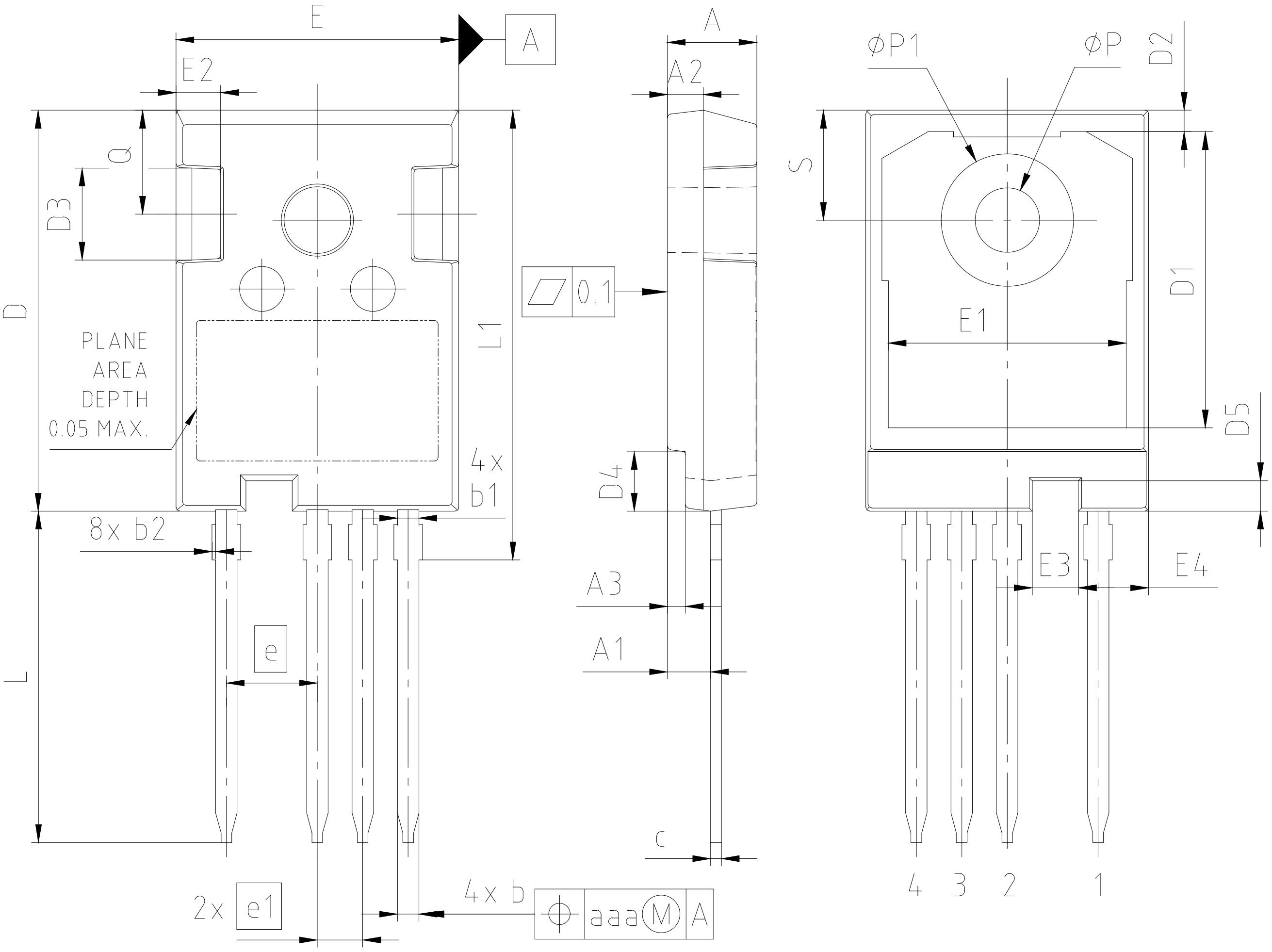
$t = f(R_{G,ext})$

V_{GS} = 0/20 V, I_D = 10 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V $I_{frm} = f(-di_{SD}/dt)$ V_{GS} = 0/18 V, I_{SD} = 10 A, V_{DD} = 800 V	**Typ. transient thermal impedance (MOSFET/diode)** $Z_{th(j-c),typ} = f(t_p)$ $D = t_p/T$
	

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO247-4-U05				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	**E**	15.70	15.90
A1	2.31	2.51	**E1**	13.10	13.50
A2	1.90	2.10	**E2**	2.40	2.60
A3	0.90	1.10	**E3**	2.48	2.68
b	1.16	1.29	**E4**	3.82	4.02
b1	1.16	1.29	**e**	5.08	
b2		0.20	**e1**	2.54	
c	0.59	0.66	**N**	4	
D	22.30	22.50	**L**	18.40	18.70
D1	16.25	16.85	**L1**	24.97	25.27
D2	1.05	1.35	**øP**	3.50	3.70
D3	5.00	5.20	**øP1**		7.40
D4	3.22	3.42	**Q**	5.60	6.00
D5	1.60	1.80	**S**	6.00	6.30
			aaa	0.25	

NOTE: DIMENSIONS DO NOT INCLUDE MOLDFLASH; PROTRUSION OR GARE BURRS

Figure 1

6 Testing conditions

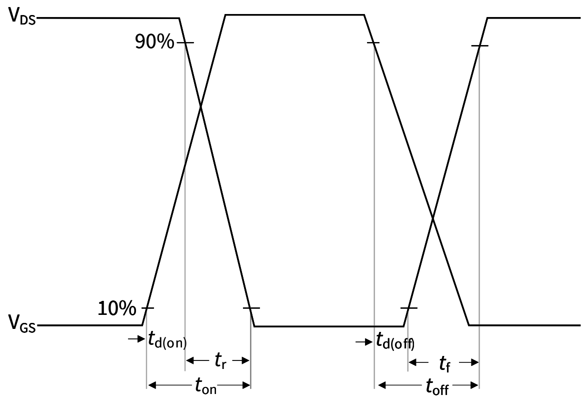


Figure A. **Definition of switching times**

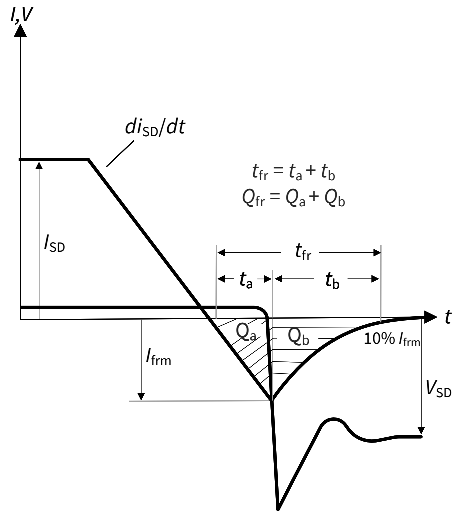


Figure B. **Definition of body diode switching characteristics**

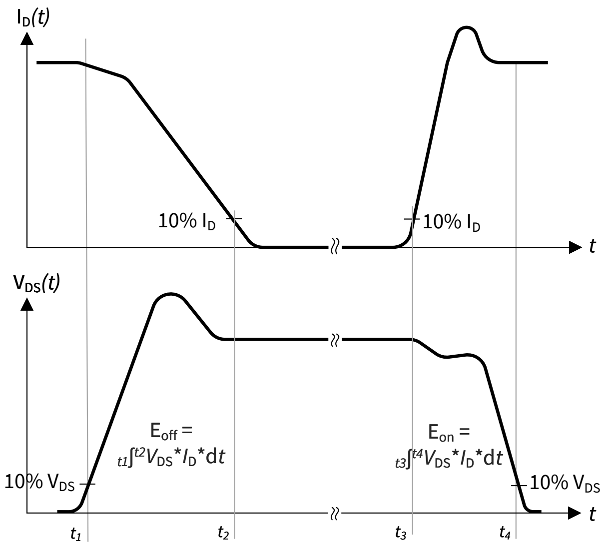


Figure C. **Definition of switching losses**

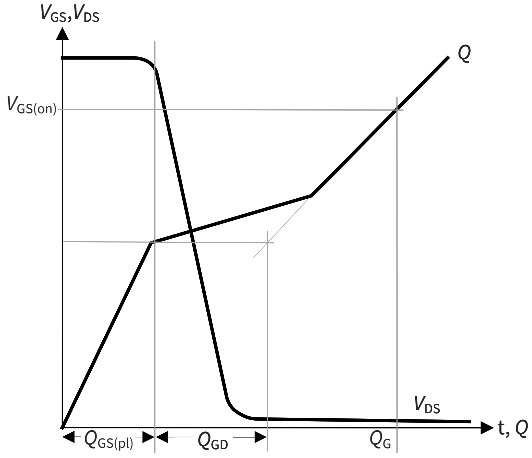


Figure D. **Definition of QGD**

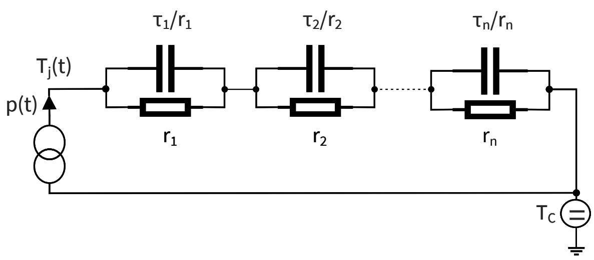


Figure E. **Thermal equivalent circuit**

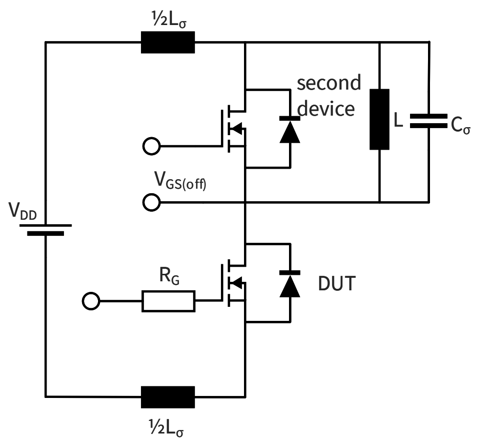


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2022-04-19	Target datasheet
0.20	2023-08-03	Preliminary datasheet
1.00	2023-12-01	Final datasheet
1.10	2025-10-15	Updated table values: g_{fs}, Rg_{int}, L_{σ} for switching parameters, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f, E_{on}, E_{off}, E_{tot}, I_{SDC}, Q_{fr}, I_{frm} condition $d_{isd/dt}$ for Q_{fr} and I_{frm} Added values: creepage distance value on p.1, Ism values for limited t_p Updated graphs: $I_{DS} = f(V_{DS})$, $R_{on}(T_{vj})$, $I_{DS}(V_{GS})$, $I_{SD} = f(V_{SD})$, $E = f(T_{vj})$, $E = f(R_{G,ext})$, $E = f(I_D)$, $t_{sw} = f(R_{G,ext})$, $Z_{th(j\text{-}c)} = f(t_p)$ Added graphs: $E_{sw} = f(V_{DS})$, $I_{frm} = f(di/dt)$ No change to the product, new/added values are based on additional assessments

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