Qualification Report

QTP 96091/96393, Version 2.0

September 1996

Dual Port SRAM - R28 Technology, 6% Shrink	
CY7C0251	8K x 18 Dual Port SRAM
CY7C025	8K x 16 Dual Port SRAM
CY7C0241	4K x 18 Dual Port SRAM
CY7C024	4K x 16 Dual Port SRAM
CY7C145	8K x 9 Dual Port SRAM
CY7C144	8K x 8 Dual Port SRAM
CY7C139	4K x 9 Dual Port SRAM
CY7C138	4K x 8 Dual Port SRAM
CY7C133	2K x 16 Dual Port SRAM
CY7C143	2K x 16 Dual Port SRAM
CY7C016	16 x 9 Dual Port SRAM
CY7C006	16 x 8 Dual Port SRAM

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:			
Marketing Part #:	CY7C025		
Package:	84-Lead Plastic Lead Chip Carrier (CY7C025) 80 -Pin Thin Quad Flat Pack (CY7C016) 100-Pin Thin Quad Flat Pack (CY7C025)		
Device Description:	8K x 16 Dual Port SRAM		
Cypress Division:	Cypress Semiconductor Corporation - DCD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. B	
Die Size (stepping):	311 mils x 201 mils	What ID markings on Die:	CY7C025B

TECHNOLOGY/FAB PROCESS DESCRIPTION - R28			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti/TiW/AL-Si/TiW, 500A/1200A/6000A/1200A Metal 2: TiW/Al-Si/Ti 1200A/10000A/150A
Passivation Type and Materials:	7000A TEOS + 6000A Oxynitride		
Free Phosphorus contents in top glass layer (%):	n/a		
Die Coating(s), if used:	None		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Double Poly, Double Metal /0.65 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 165 A		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor, Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab3/R28		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	84-Lead Plastic Lead Chip Carrier (CY7C025) 80-Pin Thin Quad Flat Pack (CY7C016) 100-Pin Thin Quad Flat Pack (CY7C025)		
Mold Compound Name/Manufacturer:	Sumitomo EME-7320 (TQFP) Sumitomo EME-6300H (PLCC)		
Die Coatings, (if used):	Hitachi PIX-8144 (PLCC)		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Paste	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level:	Level 5		
Name/Location of Assembly (prime) facility:	Anam, Korea		

Note: Please contact a Cypress Representative for other package availability.

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	1951 Devices	0	n/a	n/a	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	180,000 DHRs	0	0.6	82	62 FITs

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] Failure rate was based on Dual Port SRAM, R28 technology qualification (QTP 95226 & 96091).

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating condition, Vcc = 5.75V, 150°C	P
Read & Record Life Test	Dynamic Operating Contidion, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 85% RH, 5.5V Precondition: Dry bake, 3 Cys Solder Reflow	P
High Accelerated Saturation Test (HAST)	140°C, 5.5V Precondition: Dry bake + 72 Hrs 30°C/60%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: Dry Bake, 3 Cys Solder Relfow	P
Temperature Cycle	JEDEC22 CONDITION B, -40°C to 125°C Precondition: Dry Bake, 3 Cys Solder Reflow	P
Pressure Cooker Test	121°C, 100% RH	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	P 2,200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	P 1,000V
Latchup Sensitivity	In accordance with JEDEC 17, Cypress Spec. 01-00081	P
Alpha Particle Sensitivity	Cypress Spec. 25-00055	P
Current Density	Cypress Spec. 22-00029	P

RELIABILITY TEST DATA

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DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C025-AC	KOREA-Q	3604479	349602347	48	434	0	
CY7C025-JC	KOREA-A	3604479	349602348	48	493	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 5.5V), PRECONDITION DRY BAKE + 3 CYS SOLDER REFLOW							
CY7C016-AC	KOREA-Q	3604479	349602669	128	48	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 85%RH, 5.5V), PRECONDITION DRY BAKE + 72 HRS 30C/60%RH							
CY7C025-JC	KOREA-Q	3604479	349602348	128	51	0	
CY7C025-JI	KOREA-A	3623123	349609319	128	48	0	
CY7C025-JC	KOREA-A	3625406	349610027	128	50	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C025-AC	KOREA-Q	3604479	349602347	80	80	0	
CY7C025-AC	KOREA-Q	3604479	349602347	168	55	0	
CY7C025-AC	KOREA-Q	3604479	349602347	168	79	0	1 EOS
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C025-AC	KOREA-Q	3604479	349602347	80	120	0	
CY7C025-AC	KOREA-Q	3604479	349602347	500	120	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C025-AC	KOREA-Q	3604479	349602347	48	10	0	
CY7C025-AC	KOREA-Q	3604479	349602347	80	10	0	
CY7C025-AC	KOREA-Q	3604479	349602347	500	10	0	
STRESS: TEMP CYCLE, COND. C, -65 TO 150C, PRECONDITION DRY-BAKE							
CY7C025-AC	KOREA-Q	3604479	349602347	300	48	0	
CY7C025-AC	KOREA-Q	3604479	349602347	1000	48	0	
STRESS: TEMP CYCLE, JEDEC22 COND. B, -40 TO 125C, PRECONDITION DRY-BAKE							
CY7C025-JC	KOREA-A	3601138	349602143	500	52	0	
CY7C025-JC	KOREA-A	3601138	349602143	1500	50	0	
CY7C025-JC	KOREA-A	3602236	349602349	500	59	0	
CY7C025-JC	KOREA-A	3602236	349602349	1500	59	0	

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 95226**

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C025-JC	KOREA-A	3531005	349522865	48	512	0	
CY7C025-JC	KOREA-A	3543592	349524484	48	512	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 85%RH, 5.5V), PRECONDITION DRY BAKE							
CY7C025-JC	KOREA-A	3531005	349522865	128	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C025-JC	KOREA-A	3531005	349522865	80	76	0	
CY7C025-JC	KOREA-A	3531005	349522865	168	76	0	
CY7C025-JC	KOREA-A	3543592	349524484	80	80	0	
CY7C025-JC	KOREA-A	3543592	349524484	168	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C025-JC	KOREA-A	3531005	349522865	80	120	0	
CY7C025-JC	KOREA-A	3531005	349522865	500	120	0	
CY7C025-JC	KOREA-A	3543592	349524484	80	120	0	
CY7C025-JC	KOREA-A	3543592	349524484	500	120	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C025-JC	KOREA-A	3531005	349522865	168	45	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C025-JC	KOREA-A	3531005	349522865	48	10	0	
CY7C025-JC	KOREA-A	3531005	349522865	80	10	0	
CY7C025-JC	KOREA-A	3531005	349522865	500	10	0	
STRESS: TEMP CYCLE, COND. C, -65 TO 150C, PRECONDITION DRY-BAKE							
CY7C025-JC	KOREA-A	3543592	349524484	300	48	0	
CY7C025-AC	KOREA-Q	3544800	349525183	300	50	0	

Note: QTP 95226, original qualification for Dual Port SRAM, R28 technology.