

Qualification Report

May 1996, QTP# 95226, Version 1.0

Dual Port SRAM - R28 Technology (Thin Quad Flat Pack Package)	
CY7C0251	8K x 18 Dual Port SRAM
CY7C025	8K x 16 Dual Port SRAM
CY7C0241	4K x 18 Dual Port SRAM
CY7C024	4K x 16 Dual Port SRAM
CY7C145	8K x 9 Dual Port SRAM
CY7C144	8K x 8 Dual Port SRAM
CY7C139	4K x 9 Dual Port SRAM
CY7C138	4K x 8 Dual Port SRAM
CY7C133	2K x 16 Dual Port SRAM
CY7C143	2K x 16 Dual Port SRAM
CY7C016	16 x 9 Dual Port SRAM
CY7C006	16 x 8 Dual Port SRAM

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:			
Marketing Part #:	CY7C025		
Package:	84-Lead Plastic Lead Chip Carrier 100-Pin Thin Quad Flat Pack		
Device Description:	8K x 16 Dual Port SRAM		
Cypress Division:	Cypress Semiconductor Corporation - DCD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
Die Size (stepping):	333 mils x 215 mils	What ID markings on Die:	CY7C025A

TECHNOLOGY/FAB PROCESS DESCRIPTION - R28			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti/TiW/AL-Si/TiW, 500A/1200A/6000A/1200A Metal 2: TiW/Al-Si/Ti 1200A/10000A/150A
Passivation Type and Materials:	7000A TEOS + 6000A Oxynitride		
Free Phosphorus contents in top glass layer(%):	n/a		
Die Coating(s), if used:	None		
Generic Process Technology/Design Rule (μ -drawn):	CMOS, Double Poly, Double Metal /0.65 μ m		
Gate Oxide Material/Thickness (MOS):	SiO ₂ / 165 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor, Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab3/R28		



PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:		84-Lead Plastic Lead Chip Carrier 100-Pin Thin Quad Flat Pack	
Mold Compound Name/Manufacturer:		Sumitomo EME-6300H(R)	
Lead Frame material:	Copper		
Lead Finish, composition:		Solder Plated, 85%Sn, 15%Pb	
Die Attach Area Plating:		Silver Spot	
Die Attach Method:	Paste	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level:		Level 5	
Name/Location of Assembly (prime) facility:		Anam, Korea	

Note: Please contact a Cypress Representative for other package availability.

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal ³ A.F	Failure Rate
High Temperature Operating Life Early Failure Rate	1024 Devices	0	n/a	n/a	0 PPM
High Temperature Operating Life ^{1,2} Long Term Failure Rate	120,000 DHRs	0	0.6	82	93 FITs

¹ Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

² Chi-squared 60% estimations used to calculate the failure rate.

³ Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E_A = The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.

T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating condition, Vcc = 5.75V, 150°C	P
Read & Record Life Test	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85% RH, 5.5V Precondition: Dry bake, 3 Cys Solder Reflow	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: Dry Bake, 3 Cys Solder Reflow	P* (See Note)
Pressure Cooker Test	121°C, 100% RH	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	P 2,200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	P 1,000V
Latchup Sensitivity	In accordance with JEDEC 17, Cypress Spec. 01-00081	P
Alpha Particle Sensitivity	Cypress Spec. 25-00055	P
Current Density	Cypress Spec. 22-00029	P

* NOTE: 84-pin PLCC package needs to repeat Temperature Cycle with die coat.



RELIABILITY TEST DATA

QTP#: 95226

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
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STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)

CY7C025-JC	KOREA-A	3531005	349522865	48	512	0	
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CY7C025-JC	KOREA-A	3543592	349524484	48	512	0	
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STRESS: HI-ACCEL SATURATION TEST (140C, 85%RH, 5.5V), PRECONDITION DRY BAKE

CY7C025-JC	KOREA-A	3531005	349522865	128	48	0	
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STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)

CY7C025-JC	KOREA-A	3531005	349522865	80	76	0	
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CY7C025-JC	KOREA-A	3531005	349522865	168	76	0	
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CY7C025-JC	KOREA-A	3543592	349524484	80	80	0	
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CY7C025-JC	KOREA-A	3543592	349524484	168	80	0	
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STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)

CY7C025-JC	KOREA-A	3531005	349522865	80	120	0	
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CY7C025-JC	KOREA-A	3531005	349522865	500	120	0	
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CY7C025-JC	KOREA-A	3543592	349524484	80	120	0	
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CY7C025-JC	KOREA-A	3543592	349524484	500	120	0	
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STRESS: PRESSURE COOKER TEST (121C, 100%RH)

CY7C025-JC	KOREA-A	3531005	349522865	168	45	0	
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STRESS: READ & RECORD LIFE TEST (150C, 5.75V)

CY7C025-JC	KOREA-A	3531005	349522865	48	10	0	
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CY7C025-JC	KOREA-A	3531005	349522865	80	10	0	
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CY7C025-JC	KOREA-A	3531005	349522865	500	10	0	
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STRESS: TEMP CYCLE, COND. C, -65 TO 150C, PRECONDITION DRY-BAKE

CY7C025-JC	KOREA-A	3543592	349524484	300	48	0	
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CY7C025-AC	KOREA-Q	3544800	349525183	300	50	0	
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