Data Sheet, V 1.0D3, Mar. 2001

82C900

Standalone TwinCAN Controller

Microcontrollers

Infineon technologies

Never stop thinking.

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82C900
Preliminary
Revision History: **2001-03** V 1.0D3

Previous Version: -

Page	Subjects (major changes since last revision)

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82C900

Architectural Overview

The Standalone TwinCAN device provides several submodules to control the data flow and to configure the peripheral function:

Features:

- Two interface channels are implemented for the communication with a host device:
  - the Multiplexed Data/Address Bus can be used by an external CPU to read and write the TwinCAN's internal registers for initial configuration and control during normal operation. The standard Infineon Bus Mode and the Motorola Bus Mode can be handled.
  - alternatively, a Synchronous Serial Channel (SSC) may be selected to read out the initial TwinCAN's register configuration from a serial EEPROM. The SSC can be also used by an external control device (microcontroller, CPU, etc.) in order to exchange control and status information.
- Both communication channels are based on byte transfers. In order to minimize the communication overhead, all internal 16 bit and 32 bit wide registers can be accessed in Page Mode requiring only one address byte.
- Powerful initialization mechanism for all registers, the device can be configured via EEPROM, based on CAN messages or by an external host device.
- Additional input/output functionality controlled by CAN messages. The transmission of CAN messages can be triggered by input pins if the SSC is used for communication.
- The clock control unit can be supplied with an external clock. Alternatively, an on-chip oscillator may be used to generate a clock driving also an external device via an output pin.
- Power Saving features have been implemented. A Sleep Mode and a Power-Down Mode can be activated in order to minimize the power consumption. The clock control of the device can be controlled by CAN messages.
- The internal power saving status can be monitored at output pins. This allows flexible and powerful system partitioning.
- The Device Controller unit generates the internal target address by concatenating the contents of the PAGE register with the address delivered by the appropriate host read/write access.
- The Interrupt Control unit passes the interrupt requests generated by the TwinCAN controller to the external host via selectable output pins.
- The Port Control unit can be used to select the required functionality of the port pins operating as communication channel, CAN node function monitor, interrupt request line or general purpose I/O. Furthermore, the slew rate of pins configured for output operation can be adjusted via this module.

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The TwinCAN module permits the connection and autonomous handling of two independent CAN buses.

- Full-CAN module with 32 message objects, which can be independently assigned to one of the two buses.
- The CAN protocol version 2.0B active with standard and extended identifiers can be handled.
- The full CAN baud rate range is supported.
- Scalable FIFO mechanism for reception and transmission in order to improve the real-time behavior of the system.
- Built-in automatic gateway functionality for data exchange between both CAN buses. The gateway feature can also be used for automatic reply to received messages (lifesign: “I got it!”).
- Powerful interrupt structure, permitting application-specific interrupt generation.
- Remote frames can be monitored.
- Enhanced acceptance filtering (an acceptance mask for each message object).
- A 16 bit frame count / timestamp is implemented for each message object.
- Analyzing mode (no dominant level will be sent) supported.

Figure 1 shows a block diagram of the 82C900 device architecture.

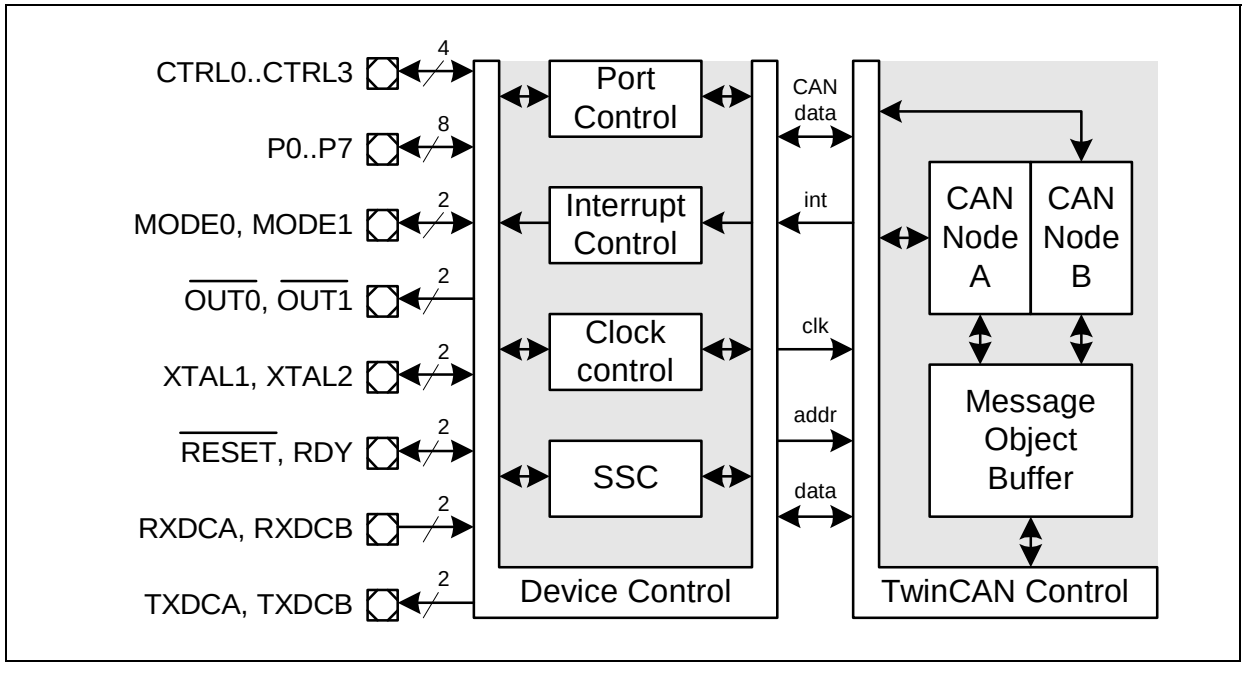

Figure 1 Standalone TwinCAN Architecture

Note: The CAN bus transceivers are not integrated and have to be connected externally.

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Application Fields

The Standalone TwinCAN device 82C900 can be used in application requiring one or two independent CAN nodes. The built-in FIFO and gateway features minimize the CPU load for the message handling and lead to an improved real-time behavior. The access to the internal registers can be handled via a parallel or a serial interface, adapted to a large variety of applications. The interface selection is done via the two MODE pins, which can be directly connected to the supply voltage or via pull-up/down resistors (of about 10-47 kOhm). In all modes, the clock generation can be controlled either by the 82C900 device or by the system it is connected to.

Connection to a Host Device via the Parallel Interface

The 82C900 can be connected to a host device via a parallel 8 bit multiplexed interface. Therefore, pin MODE0 has to be 0, whereas pin MODE1 selects, whether an Infineon- (Intel-) compatible or an Motorola-compatible protocol is handled. In this mode, the device can be easily used to extend the CAN capability of a system. The internal registers can be accessed in pages of 256 bytes per page. An additional RDY output indicates when the device is ready to be accessed. This signal can be used to detect an overload situation of the CAN device (too many host accesses to the TwinCAN module). One interrupt output line ($\overline{OUT1}$) is always available, a second one ($\overline{OUT0}$) can be used as clockout pin or as another interrupt output.

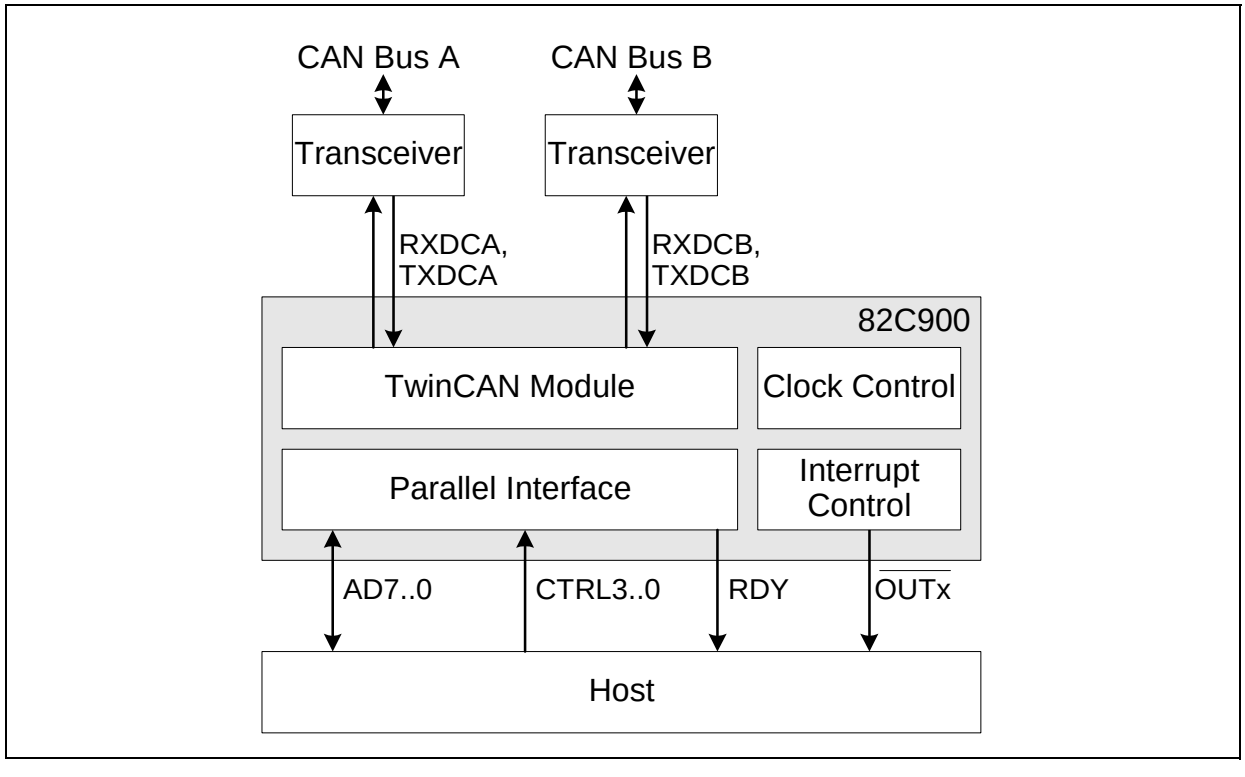

Figure 2 Host Connection via the Parallel Interface

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Connection to a Host Device via the Serial Interface

The second possibility to connect the 82C900 to a host device is via the serial interface. This mode is selected if the pin MODE0=1 and MODE1=0.
The standard four-line SPI-compatible interface has been extended by a RDY signal, which indicates that the serial interface is ready for the next access by the host.
The page size is reduced to 128 bytes per page, because the MSB of the address byte contains a read/write indication. A special incremental access mode has been implemented in order to reduce significantly the number of transferred bytes for consecutive register accesses.
The 8 remaining I/O pins from the unused parallel interface are controlled by a port control logic and can be used as I/O extension. These lines can be read or written by the serial channel or by CAN messages. Furthermore, these lines can be programmed as additional interrupt output lines in order to increase the number of independent interrupts.
The output lines $\overline{\text{OUT0}}$ and $\overline{\text{OUT1}}$ have the same functionality in the case a parallel interface or a serial interface connects the 82C900 to a host device.

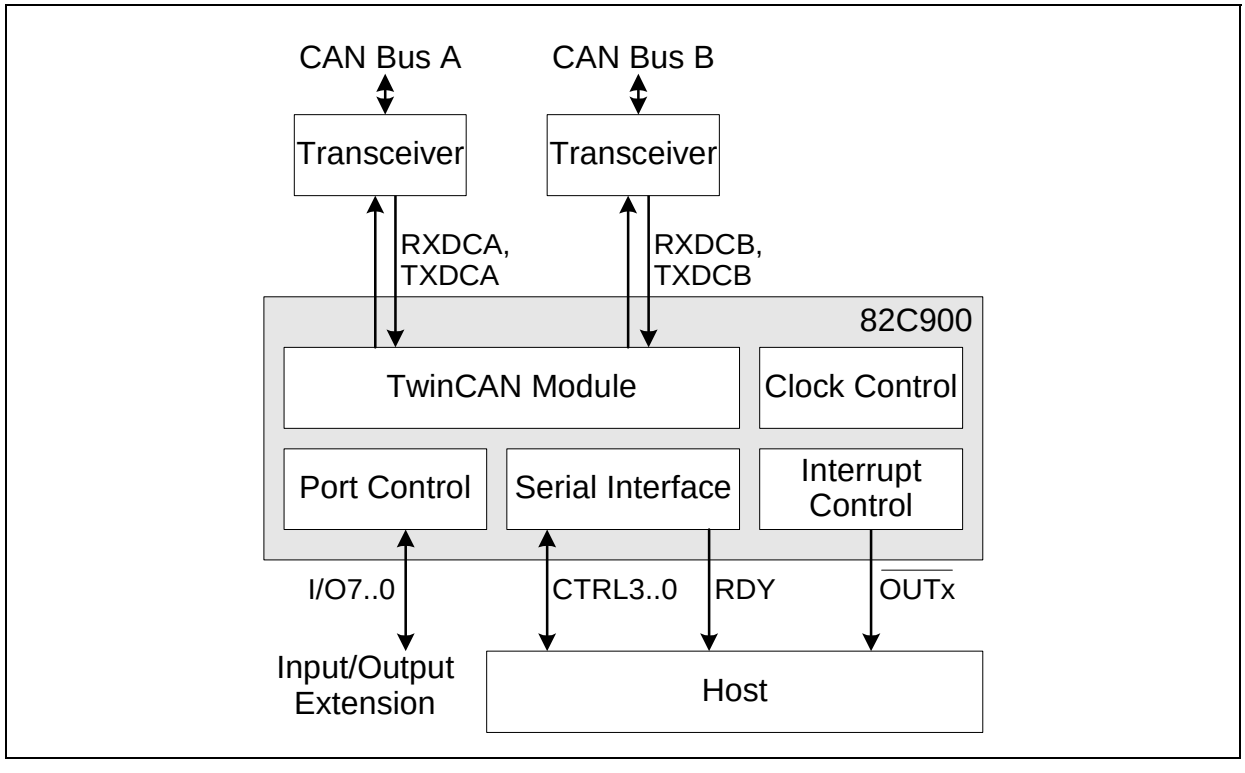

Figure 3 Host Connection via the Serial Interface

Preliminary

Operation without Host Device

The standalone functionality comprises an additional mode, leading to a low-cost system, which does not require any external host device. This mode can be selected by setting the input pins MODE0 and MODE1 to 1. The best solution are pull-up resistors (about 10 to 47 kOhm). After the reset phase, the MODE pins can be enabled to control the power-down functionality of the entire connected system by indicating the internal status of two clock control bits. The power-down functionality can run completely via CAN messages (sleep and wake-up by CAN messages).

The initialization sequence is automatically started from an external non-volatile memory, a serial (SPI-compatible) EEPROM. The data, which is read out from the EEPROM permits the user to initialize the registers with the desired values in a freely programmable order. Changes in the application only lead to modified data stored in the non-volatile memory.

For example, the bit timing, one message object and some control registers are set up via the data read from the EEPROM. Then, the initialization can continue via CAN messages.

The 8 remaining I/O pins from the unused parallel interface are controlled by a port control logic and can be used as I/O extension. These lines can be read or written by CAN messages.

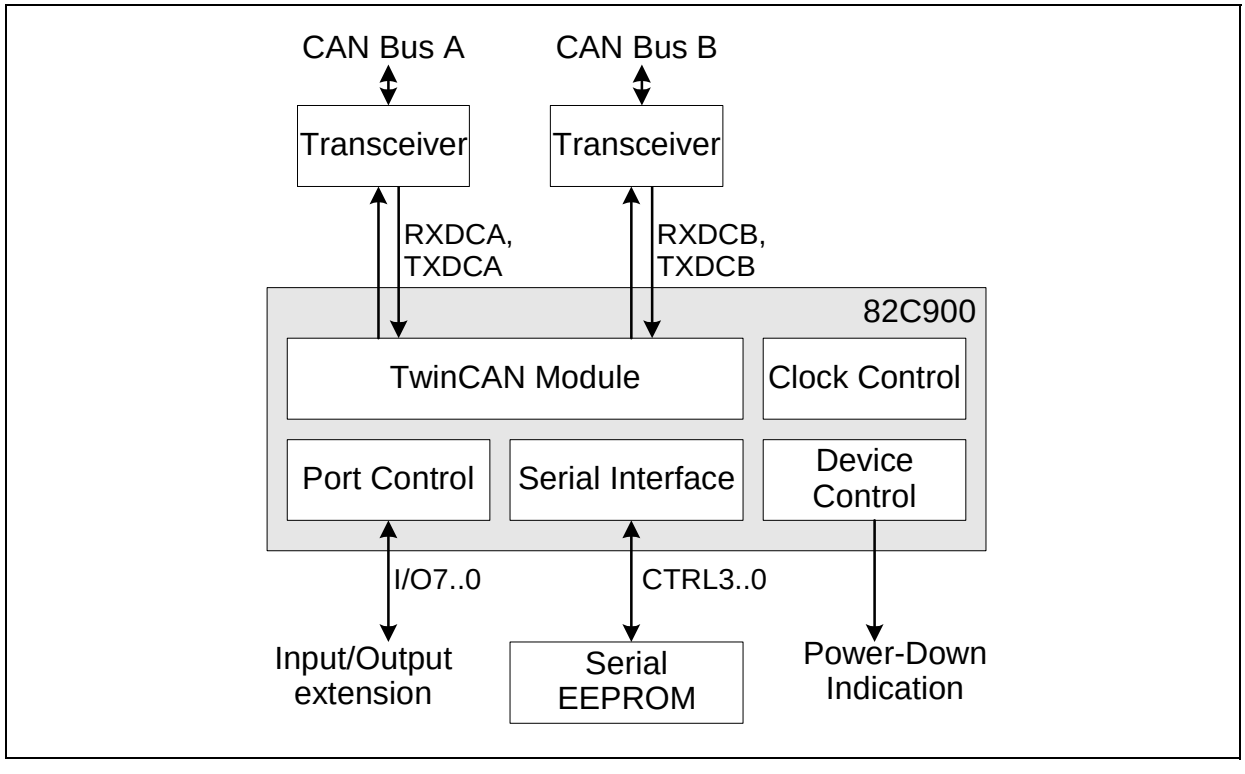

Figure 4 Connection to a Serial EEPROM

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Pin Configuration

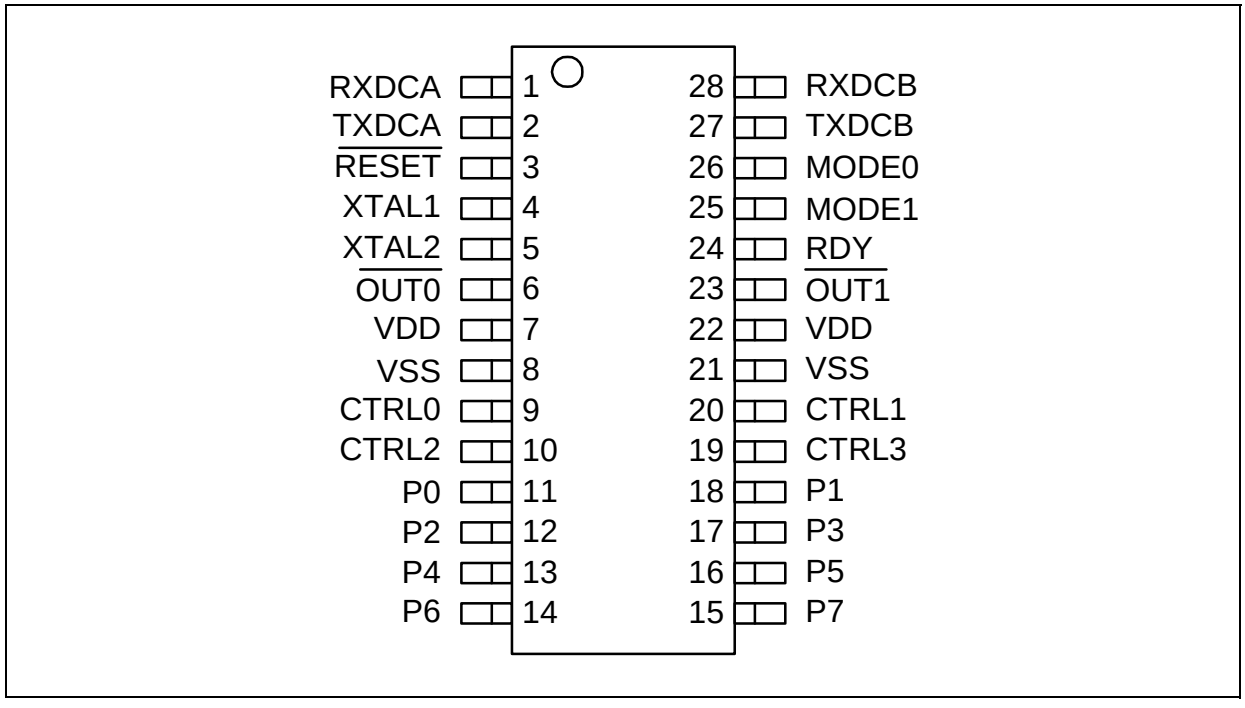

Figure 5 82C900 Pin Configuration

Pin Definition

Table 1 Pin Definitions and Functions

Symbol	Pin Number	I/O [1)]	Function
RXDCA	1	I	**Receiver Input of CAN Node A** Receiver input of CAN node A, connected to the associated CAN bus via a transceiver device.
TXDCA	2	O	**Transmitter Output of CAN Node A** TXDCA delivers the output signal of CAN node A. The signal level has to be adapted to the physical layer of the CAN bus via a transceiver device.
RXDCB	28	I	**Receiver Input of CAN Node B** Receiver input of CAN node B, connected to the associated CAN bus via a transceiver device.

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Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O [1]	Function
TXDCB	27	O	**Transmitter Output of CAN Node B** TXDCB delivers the output signal of CAN node B. The signal level has to be adapted to the physical layer of the CAN bus via a transceiver device.
$\overline{\text{RESET}}$	3	I	**Reset** A low level on this pin resets the device.
RDY	24	O	**Ready Signal** Output signal indicating that the standalone device is ready for data transfer.
CTRL0	9	I/O	**Control 0** MODE0=0: **Chip Select $\overline{\text{CS}}$** Input used as Chip Select for the device. MODE0=1: **Select Slave $\overline{\text{SLS}}$** MODE1=0: Input used to enable SSC action when active. MODE1=1: Output used to select a slave when active.
CTRL1	20	I/O	**Control 1** MODE0=0: **Address Latch Enable or Address Strobe, ALE or AS** Input used for latching the address from the multiplexed address/data bus. MODE0=1: **Serial Channel Clock SCLK** Input/output of the SSC clock. MODE1=0: Clock input MODE1=1: Clock output
CTRL2	10	I/O	**Control 2** MODE0=0: **Write or Read/Write, $\overline{\text{WR}}$ or R/$\overline{\text{W}}$** MODE1=0: Input used as write signal $\overline{\text{WR}}$ MODE1=1: R/$\overline{\text{W}}$=0: Data transfer direction = write MODE1=1: R/$\overline{\text{W}}$=1: Data transfer direction = read MODE0=1: **Master Transmit Slave Receive MTSR** MODE1=0: Serial data input MODE1=1: Serial data output

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Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O [1]	Function
CTRL3	19	I/O	**Control 3** MODE0=0: **Read or Read/Write Enable, $\overline{RD}$ or E** MODE1=0: Input used as read signal $\overline{RD}$ MODE1=0: Read/write enable MODE0=1: **Master Receive Slave Transmit MRST** MODE1=0: Serial data output MODE1=1: Serial data input
P7 **P6** **P5** **P4** **P3** **P2** **P1** **P0**	15 14 16 13 17 12 18 11	I/O	**Parallel Bus** MODE0=0: **8-bit Address/ Data Bus AD[7:0]** Address and data bus AD7..AD0 in 8-bit multiplexed modes. MODE0=1: **8-bit parallel I/O Port IO[7:0]** Programmable 8-bit general purpose I/O-port IO7..IO0.
$\overline{OUT0}$ [2]	6	O	**Output Line 0** The logic 0 level at this pin indicates an interrupt request to the external host device if selected as interrupt output. The interrupt line will be active if there is a new pending interrupt request for interrupt node 0 (according to register GLOBCTR). If selected as clock output, the functionality is defined by register CLKCTR.
$\overline{OUT1}$	23	O, open drain	**Output Line 1** The logic 0 level at this pin indicates an interrupt request to the external host device. The interrupt line will be active if there is a new pending interrupt request for interrupt node 1 (according to register GLOBCTR).
MODE0 [3]	26	I/O, open drain	**Interface Selection** Pin MODE0 selects whether the on-chip SSC or an 8-bit multiplexed bus are used to access the TwinCAN device. MODE0=0: 8-bit multiplexed address/data bus MODE0=1: on-chip SSC After registering the initial state of MODE0 with the rising edge of the reset signal, the respective pin can be used as additional general purpose or special function I/O line according register IOMODE4.

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Table 1 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O [1]	Function
MODE1	25	I/O, open drain	**Interface Mode Selection** Pin MODE1 determines the access mode of the host device. MODE0=0: **8-bit multiplexed bus** MODE1=0: Infineon / Intel mode, ($\overline{RD}$, $\overline{WR}$) MODE1=1: Motorola mode, (R/$\overline{W}$, E) MODE0=1: **On-chip SSC** MODE1=0: SSC is slave, host device is master MODE1=1: SSC is master, external serial EEPROM is slave After registering the initial state of MODE1 with the rising edge of the reset signal, the respective pin can be used as additional general purpose or special function I/O line according register IOMODE4.
XTAL1	4	I	**XTAL1** Input of the inverting oscillator amplifier and input to the internal clock generation circuit. When the 82C900 device is provided with an external clock, XTAL1 should be driven while XTAL2 is left unconnected. Minimum and maximum high and low pulse width as well as rise/fall times specified in the AC characteristics must be respected.
XTAL2	5	O	**XTAL2** Output of the inverting oscillator amplifier.
V_{SS}	21, 8	0V	**Ground**, both pins must be connected.
V_{DD}	22, 7	+5V	**Power Supply**, both pins must be connected.

[1] The slew rate of the output pins $\overline{OUT0}$, $\overline{OUT1}$, CTRL1..3, P0..P7, TXDCA and TXDCB can be defined by the bit fields SLR0..3 in register GLOBCTR.

[2] After reset, this pin is configured as clock output, see register CLKCTR.

[3] The initial logic state on pins MODE0 and MODE1 is registered with the rising edge of the $\overline{RESET}$ input. Afterwards, both pins can be used as additional I/O lines, according to functionality specified in register IOMODE4.

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Register Address Map

All Shell and Kernel registers, implemented for controlling the 82C900 device, are summarized in **Table 0-1**; detailed information about each register is provided in the respective module description chapter.

Note: Accesses to addresses which are not specified as registers in the following register address map are forbidden.

Table 0-1 Summary of Registers

Register Name	Register Symbol	Address	Reset Value [1]
Standalone Shell Registers			
Global Device Control Register	GLOBCTR	0010_H	A0 00_H
Interrupt Control Register	INTCTR	0012_H	00 00_H
CAN Clock Control Register	CLKCTR	0014_H	00 24_H
Input/Output Mode Register 0	IOMODE0	0020_H	00 00_H
Input/Output Mode Register 2	IOMODE2	0022_H	00 00_H
Input/Output Mode Register 4	IOMODE4	0024_H	00 00_H
Input Value Register (8-bit port)	INREG	0026_H	00 00_H
Output Value Register (8-bit port)	OUTREG	0028_H	00 00_H
CAN Power-Down Control Register	CANPWD	0040_H	00 00_H
CAN Input/Output Control Register	CANIO	0042_H	00 00_H
CAN Initialization Control Register	CANINIT	0044_H	00 00_H
Paging Mode Register (accessible in all pages)	PAGE	$XX7C_H$	00 00_H
CAN RAM Address Buffer Register	CAB	$007E_H$	00 00_H
Initialization Control Register	INITCTR	$02F0_H$	0103 0000_H
TwinCAN Kernel, Common Registers			
CAN Receive Interrupt Pending Register	RXIPND	0284_H	0000 0000_H
CAN Transmit Interrupt Pending Register	TXIPND	0288_H	0000 0000_H
TwinCAN Kernel, Node A Registers			
CAN Node A Control Register	ACR	0200_H	0000 0001_H
CAN Node A Status Register	ASR	0204_H	0000 0000_H
CAN Node A Interrupt Pending Register	AIR	0208_H	0000 0000_H
CAN Node A Bit Timing Register	ABTR	$020C_H$	0000 0000_H

Table 0-1 Summary of Registers (cont'd)

Register Name	Register Symbol	Address	Reset Value [1]
CAN Node A Global Int. Node Pointer Reg.	AGINP	0210_H	$0000\ 0000_H$
CAN Node A Frame Counter Register	AFCR	0214_H	$0000\ 0000_H$
CAN Node A INTID Mask Register 0	AIMR0	0218_H	$0000\ 0000_H$
CAN Node A INTID Mask Register 4	AIMR4	$021C_H$	$0000\ 0000_H$
CAN Node A Error Counter Register	AECNT	0220_H	$0060\ 0000_H$
TwinCAN Kernel, Node B Registers			
CAN Node B Control Register	BCR	0240_H	$0000\ 0001_H$
CAN Node B Status Register	BSR	0244_H	$0000\ 0000_H$
CAN Node B Interrupt Pending Register	BIR	0248_H	$0000\ 0000_H$
CAN Node B Bit Timing Register	BBTR	$024C_H$	$0000\ 0000_H$
CAN Node B Global Int. Node Pointer Reg.	BGINP	0250_H	$0000\ 0000_H$
CAN Node B Frame Counter Register	BFCR	0254_H	$0000\ 0000_H$
CAN Node B INTID Mask Register 0	BIMR0	0258_H	$0000\ 0000_H$
CAN Node B INTID Mask Register 4	BIMR4	$025C_H$	$0000\ 0000_H$
CAN Node B Error Counter Register	BECNT	0260_H	$0060\ 0000_H$
TwinCAN Kernel, Message Object Registers			
CAN Message Object n Data Register 0	MSGDRn0	$0300_H + n*20_H$	$0000\ 0000_H$
CAN Message Object n Data Register 4	MSGDRn4	$0304_H + n*20_H$	$0000\ 0000_H$
CAN Message Object n Arbitration Register	MSGARn	$0308_H + n*20_H$	$0000\ 0000_H$
CAN Message Object n Acceptance Mask Register	MSGAMRn	$030C_H + n*20_H$	$FFFF\ FFFF_H$
CAN Message Object n Message Control Register	MSGCTRn	$0310_H + n*20_H$	$0000\ 5555_H$
CAN Message Object n Message Configuration Register	MSGCFGn	$0314_H + n*20_H$	$0000\ 0000_H$
CAN Message Object n Gateway / FIFO Control Register	MSGFGCRn	$0318_H + n*20_H$	$0000\ 0000_H$

[1] Registers with 32-bit reset values are located in the CAN RAM and have to be accessed accordingly. The other registers are standard SFRs, which have 16-bit reset values.

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Absolute Maximum Ratings

Table 2 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD}+0.5	V	
Input current on any pin during overload condition		-10	10	mA	
Absolute sum of all input currents during overload condition			|100|	mA	
Power dissipation	P_{DISS}		480	mW	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

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Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the device. All parameters, specified in the following sections, refer to the normal operating conditions, unless otherwise noticed. The timings refer to the fast edge mode.

Table 3 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Standard digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{max} = 25 MHz
		2.5 [1]	5.5	V	Power-Down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-	±5	mA	Per pin [2] [3]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	-	50	mA	[4]
External Load Capacitance	C_L	-	|100|	pF	
Ambient temperature	T_A	-40	125	°C	SAK 82C900

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode. The clock frequency has to be reduced to operate with a voltage supply below 4.5V.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < V_{SS}$-0.5V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

3) Not 100% tested, guaranteed by design characterization

4) Not 100% tested, guaranteed by design characterization.

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DC Characteristics

Operating Conditions apply.

Table 4 DC Characteristics under Normal Operation Conditions

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (XTAL1)	V_{IL}	– 0.5	0.3 V_{DD}	V	–
Input high voltage (XTAL1)	V_{IH}	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input low voltage (other pins)	V_{IL}	– 0.5	0.2 V_{DD} – 0.1	V	–
Input high voltage (other pins)	V_{IH}	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Output low voltage [1] (P0..P7)	V_{OLP}	–	0.45	V	I_{OLP} = 5 mA
Output high voltage [1] (P0..P7)	V_{OHP}	2.4	–	V	I_{OHP} = -5 mA
		0.9 V_{DD}	–	V	I_{OHP} = -0.5 mA
Output low voltage (other pins)	V_{OL}	–	0.45	V	I_{OL} = 2.4 mA
Output high voltage [2] (other pins)	V_{OH}	2.4	–	V	I_{OH} = -2.4 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Input leakage current	I_{OZ}	–	±500	nA	0.45V < V_{IN} < V_{DD}
$\overline{\text{RESET}}$ inactive current [3]	I_{RSTH} [4]	–	-10	µA	V_{IN} = V_{IH}
$\overline{\text{RESET}}$ active current	I_{RSTL} [5]	-100	–	µA	V_{IN} = V_{IL}
XTAL1 input current	I_{IL}	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [6] (digital inputs/outputs)	C_{IO}	–	10	pF	f = 1 MHz T_A = 25 °C

1) The sum of | I_{OHP} |, I_{OLP} must not exceed 20mA.

2) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

3) These parameters describe the $\overline{\text{RESET}}$ pull-up, which equals a resistance of ca. 50 to 250 KΩ.

4) The maximum current may be drawn while the respective signal line remains inactive.

5) The minimum current must be drawn in order to drive the respective signal line active.

6) Not 100% tested, guaranteed by design characterization.

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Power Consumption

Operating Conditions apply.

Table 5 Power Consumption

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (5V active) with all elements active	I_{DD5}	–	80	mA	$\overline{\text{RESET}} = V_{IH}$ f_{CAN} = 25 MHz [1]
Sleep mode supply current (5V) (oscillator running, clock gated off)	I_{IDX5} [2]	–	1.5	mA	$\overline{\text{RESET}} = V_{IH}$ f_{CAN} = 25 MHz
Power-down mode supply current (5V) (oscillator stopped)	I_{IDO5}	–	10	µA	$\overline{\text{RESET}} = V_{IH}$

[1] The supply current is a function of the operating frequency. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.
The oscillator also contributes to the total supply current. The given values refer to the worst case. For lower oscillator frequencies the respective supply current can be reduced accordingly.

[2] This parameter is determined mainly by the current consumed by the oscillator. This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

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AC Characteristics

Operating Conditions apply.

Table 6 External Clock Drive XTAL1

Parameter	Symbol	Direct Drive (1:1)		Unit
		min.	max.	
Oscillator period [1]	T_{CAN}	40	–	ns
High time		10	–	ns
Low time		15	–	ns

[1] The clock input signal must reach the defined levels V_{IL} and V_{IH}.

Assuming a maximum access rate from an external host to the CAN RAM via the communication interface (worst case, parallel interface), the CAN protocol can still be handled on both nodes with 1 Mbps if the clock frequency f_{CAN} is 24 MHz. For additional data handling features (FIFO, gateway, etc.), a higher frequency should be used, the access rate to the device has to be reduced or a lower baud rate has to be selected. Under worst case access conditions and CAN traffic, a baud rate of 500 kbps for each node can be achieved with full data handling functionality with f_{CAN}=24 MHz.

CAN input delay, output delay: typ. 15 ns

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8-Bit Multiplexed Bus
Infineon/ Intel Compatibility Mode

The bus access is internally fully synchronized, asynchronous accesses are supported.

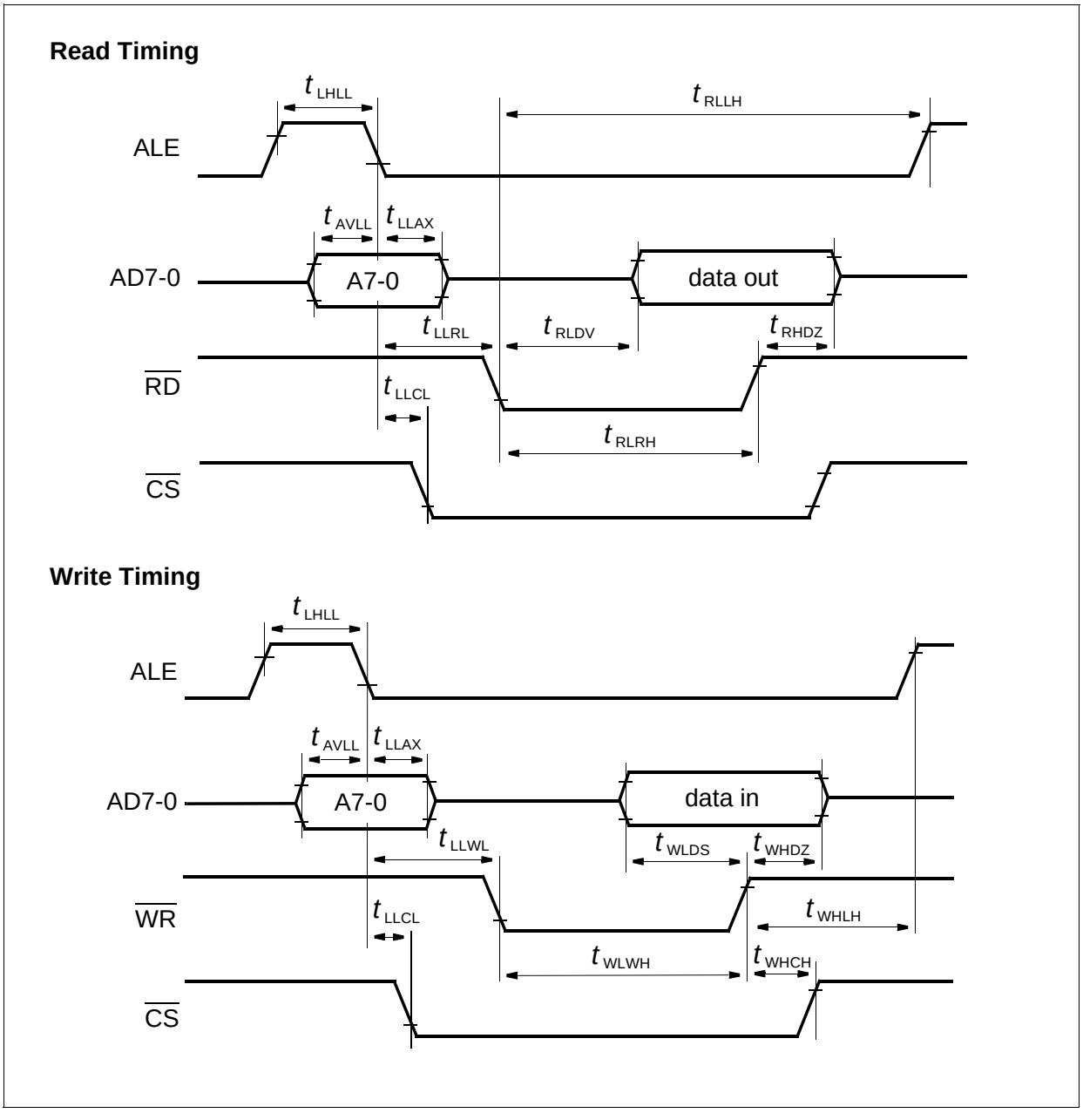

Figure 6 Timing of Multiplexed Address/Data bus with MODE1 = 0

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Operating Conditions apply.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address valid to ALE low	t_{AVLL}	5	–	ns
Address hold after ALE low	t_{LLAX}	10	–	ns
ALE high time	t_{LHLL}	10	–	ns
ALE low to $\overline{RD}$ low	t_{LLRL}	10	–	ns
ALE low to $\overline{WR}$ low	t_{LLWL}	10	–	ns
ALE low to $\overline{CS}$ low	t_{LLCL}	10	–	ns
Data setup to $\overline{WR}$ high	t_{WLDS}	10	–	ns
Input data hold after $\overline{WR}$ high	t_{WHDZ}	10	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	1.5 T_{CAN}	–	ns
$\overline{WR}$ high to next ALE high (if the next access targets the device)	t_{WHLH}	10 T_{CAN}	–	ns
$\overline{WR}$ high to next ALE high (if the next access doesn't target the device)	t_{WHLH}	4 T_{CAN} +15	–	ns
$\overline{WR}$ high to $\overline{CS}$ high	t_{WHCH}	0	–	ns
$\overline{RD}$ pulse width (short read)	t_{RLRH}	1.5 T_{CAN}	–	ns
$\overline{RD}$ pulse width (long read)	t_{RLRH}	8 T_{CAN} + 25	–	ns
$\overline{RD}$ low to data valid (short read)	t_{RLDV}	–	25	ns
$\overline{RD}$ low to data valid (long read)	t_{RLDV}	–	25 + 8 T_{CAN}	ns
$\overline{RD}$ low to next ALE high (short read)	t_{RLLH}	8 T_{CAN}	–	ns
$\overline{RD}$ low to next ALE high (long read)	t_{RLLH}	25	–	ns
Data float after $\overline{RD}$ high	t_{RHDZ}	–	25	ns

Preliminary

8-Bit Multiplexed Bus
Motorola Compatibility Mode

The bus access is internally fully synchronized, asynchronous accesses are supported.

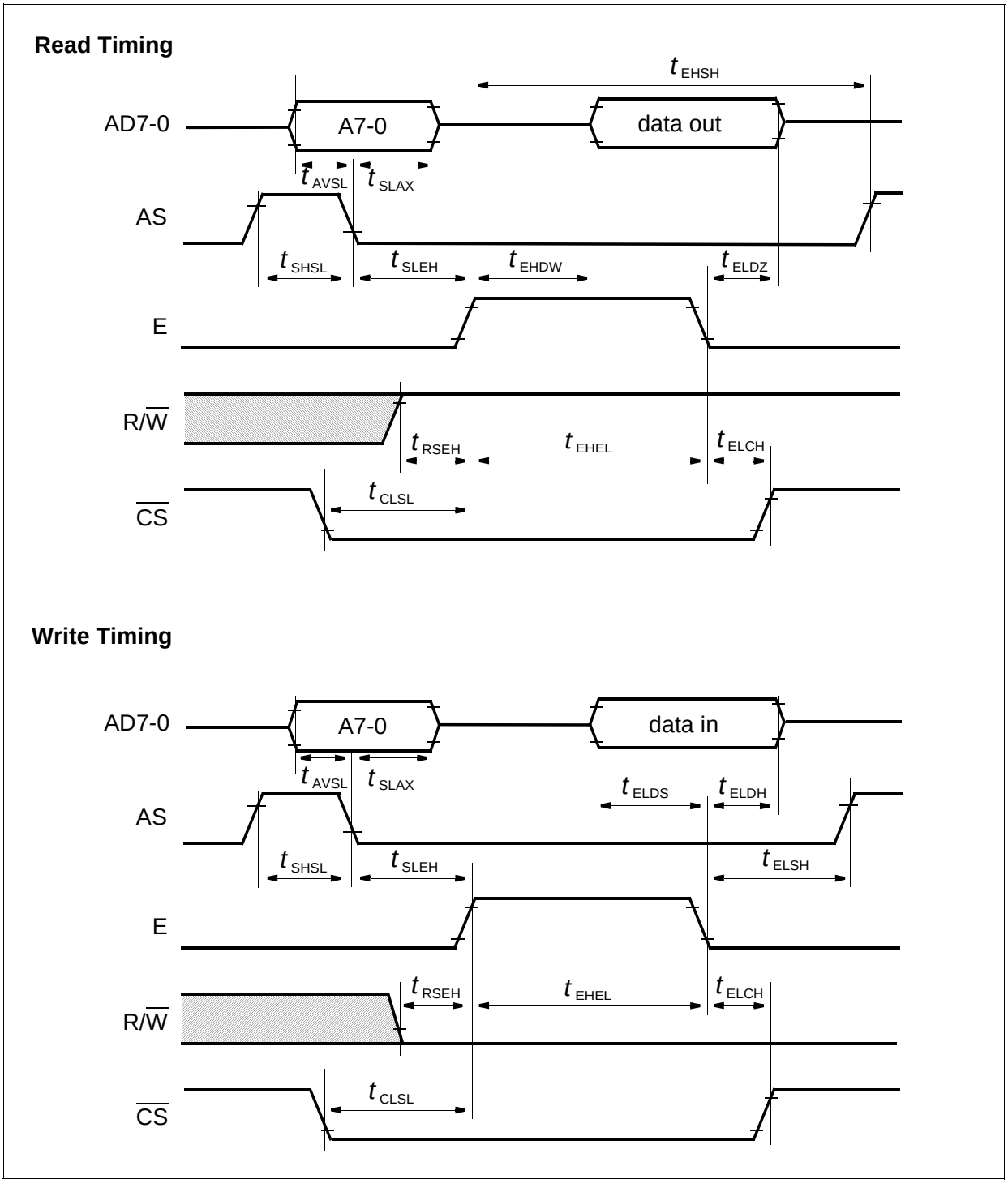


Figure 7 Timing of Multiplexed Address/Data bus with MODE1 = 1

Preliminary

Operating Conditions apply.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address valid to AS low	t_{AVSL}	5	–	ns
Address hold after AS low	t_{SLAX}	10	–	ns
Data float after E low	t_{ELDZ}	–	25	ns
E high to data valid output	t_{EHDV}	–	25	ns
Input data setup to E low	t_{ELDS}	10	–	ns
Input data hold after E low	t_{ELDH}	10	–	ns
E high time	t_{EHEL}	1.5 T_{CAN}	–	ns
AS high time	t_{SHSL}	10	–	ns
Setup time of R/$\overline{W}$ to E high	t_{RSEH}	0	–	ns
AS low to E high	t_{SLEH}	10	–	ns
$\overline{CS}$ low to E high	t_{CLSL}	0	–	ns
E low to $\overline{CS}$ high	t_{ELCH}	0	–	ns
E low to next AS high (for write) (if the next access targets the device)	t_{ELSH}	10 T_{CAN}	–	ns
E low to next AS high (for write) (if the next access doesn't target the device)	t_{ELSH}	4 T_{CAN} + 15	–	ns
E high to next AS high (for read)	t_{EHSH}	8 T_{CAN}	–	ns

Preliminary

Timings of the SSC

In the case that the SSC is used in slave mode without the RDY signal, the following timings have to be respected:

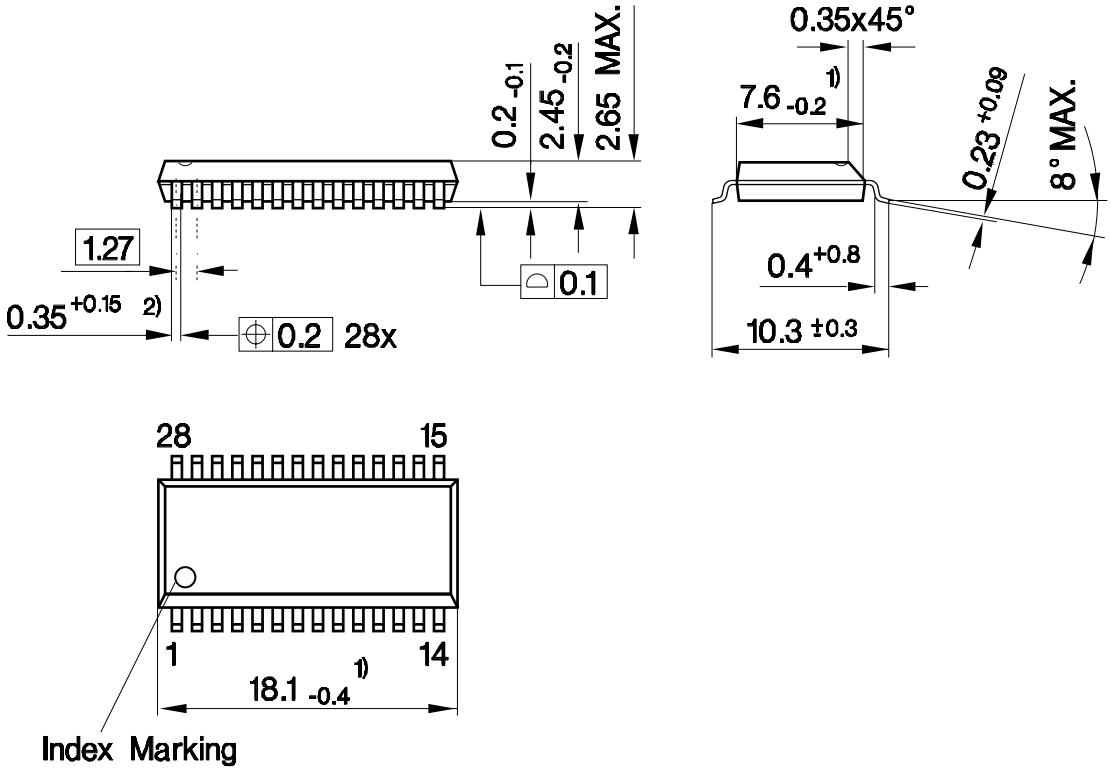
Parameter	Min. Time (access to TwinCAN registers)	Min. Time (access to standalone registers)	Units
First activation of $\overline{SLS}$ after end of reset	1100	1100	T_{CAN}
$\overline{SLS}$ active after $\overline{SLS}$ inactive (to start a new communication cycle)	4	4	T_{CAN}
$\overline{SLS}$ active before SCLK active in order to transfer the address byte	2	2	T_{CAN}
$\overline{SLS}$ inactive after $\overline{SLS}$ active without transfer of data	2	2	T_{CAN}
Time after the address transfer to the first data byte transfer	5 (write) 14 (read)	5 (write) 11 (read)	T_{CAN}
Time between two byte transfers (SCLK active to SCLK active)	5 (write) 14 (read)	5 (write) 11 (read)	T_{CAN}
Time to $\overline{SLS}$ inactive after last byte transfer	11 (write) 1 (read)	6 (write) 1 (read)	T_{CAN}

Note: The RDY signal can be used for a handshake to access to the device. Furthermore, this signal indicates SSC error conditions (see baud rate error detection). Accesses to the device during an SSC error condition can not be correctly taken into account and might lead to errors.

Preliminary

Package

The 82C900 device is available in a 28-pin P-DSO package. **Table 1** contains a functional description of each pin.



1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion of 0.05 max. per side

Figure 8 P-DSO-28-1 Package

Preliminary

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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