



---

The following document contains information on Cypress products. Although the document is marked with the name "Spansion" and "Fujitsu", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

**Continuity of Specifications**

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

**Continuity of Ordering Part Numbers**

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

**For More Information**

Please contact your local sales office for additional information about Cypress products and solutions.

**About Cypress**

Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

# 8-bit Microcontroller

CMOS

## F<sup>2</sup>MC-8FX MB95150M Series

### MB95156M/F156M/F156N/F156J/FV100D-103

#### ■ DESCRIPTION

The MB95150M series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

#### ■ FEATURE

- F<sup>2</sup>MC-8FX CPU core
  - Instruction set optimized for controllers
    - Multiplication and division instructions
    - 16-bit arithmetic operations
    - Bit test branch instruction
    - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock
  - Sub PLL clock

(Continued)

For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevic.fujitsu.com/micom/en-support/>

# MB95150M Series

(Continued)

- Timer
  - 8/16-bit compound timer × 2 channels  
Can be used to interval timer, PWC timer, PWM timer and input capture.
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 1 channel
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel
- LIN-UART × 1 channel
  - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- UART/SIO × 1 channel
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- External interrupt × 8 channels
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels  
8-bit or 10-bit resolution can be selected.
- LCD controller (LCDC)
  - 16 SEG × 4 COM (Max 64 pixels)
  - With blinking function
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode
- I/O port: Max 39
  - General-purpose I/O ports (CMOS) : 39 ports
- Programmable input voltage levels of port  
Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function  
Protects the content of Flash memory (Flash memory device only)

## ■ PRODUCT LINEUP

| Part number           |                                     | MB95156M  | MB95F156M            | MB95F156N | MB95F156J |
|-----------------------|-------------------------------------|---|----------------------|-----------|-----------|
| Parameter             |                                     |   |                      |           |           |
| Type                  |                                     | MASK ROM product  | Flash memory product |           |           |
| ROM capacity          |                                     | 32 Kbytes   |                      |           |           |
| RAM capacity          |                                     | 1 Kbyte   |                      |           |           |
| Reset output          |                                     | Yes/No  | Yes                  |           | No        |
| Option*               | Clock system                        | Dual clock  |                      |           |           |
|                       | Low voltage detection reset         | Yes/No  | No                   | Yes       |           |
|                       | Clock supervisor                    | Yes/No  | No                   |           | Yes       |
| CPU functions         |                                     | Number of basic instructions : 136<br>Instruction bit length : 8 bits<br>Instruction length : 1 to 3 bytes<br>Data bit length : 1, 8, and 16 bits<br>Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz)<br>Interrupt processing time : 0.6 μs (at machine clock frequency 16.25 MHz) |                      |           |           |
| Peripheral functions  | Ports (Max 39 ports)                | General-purpose I/O port (CMOS) : 39 ports<br>Programmable input voltage levels of port :<br>Automotive input level / CMOS input level / hysteresis input level   |                      |           |           |
|                       | Time-base timer (1 channel)         | Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)   |                      |           |           |
|                       | Watchdog timer                      | Reset generated cycle<br>At main oscillation clock 10 MHz : Min 105 ms<br>At sub oscillation clock 32.768 kHz : Min 250 ms  |                      |           |           |
|                       | Wild register                       | Capable of replacing 3 bytes of ROM data  |                      |           |           |
|                       | UART/SIO (1 channel)                | Data transfer capable in UART/SIO<br>Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator<br>NRZ type transfer format, error detected function<br>LSB-first or MSB-first can be selected.<br>Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable |                      |           |           |
|                       | LIN-UART (1 channel)                | Dedicated reload timer allowing a wide range of communication speeds to be set.<br>Full duplex double buffer<br>Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable<br>LIN functions available as the LIN master or LIN slave.  |                      |           |           |
|                       | 8/10-bit A/D converter (8 channels) | 8-bit or 10-bit resolution can be selected.   |                      |           |           |
| LCD controller (LCDC) |                                     | COM output : 4 (Max)<br>SEG output : 16 (Max)<br>LCD drive power supply (bias) pin : 4<br>16 SEG × 4 COM : 64 pixels can be displayed.<br>Duty LCD mode<br>Operable in LCD standby mode<br>With blinking function<br>Built-in division resistance for LCD drive   |                      |           |           |

(Continued)

# MB95150M Series

(Continued)

| Part number          |                                      | MB95156M   | MB95F156M | MB95F156N | MB95F156J |
|----------------------|--------------------------------------|--|-----------|-----------|-----------|
| Parameter            |                                      |  |           |           |           |
| Peripheral functions | 8/16-bit compound timer (2 channels) | Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”.<br>Built-in timer function, PWC function, PWM function, capture function, and square waveform output<br>Count clock : 7 internal clocks and external clock can be selected.   |           |           |           |
|                      | 16-bit PPG (1 channel)               | PWM mode or one-shot mode can be selected.<br>Counter operating clock : Eight selectable clock sources<br>Support for external trigger start   |           |           |           |
|                      | 8/16-bit PPG (2 channels)            | Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”.<br>Counter operating clock : Eight selectable clock sources   |           |           |           |
|                      | Watch counter                        | Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s)<br>Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)   |           |           |           |
|                      | Watch prescaler (1 channel)          | 4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)   |           |           |           |
|                      | External interrupt (8 channels)      | Interrupt by edge detection (rising, falling, or both edges can be selected.)<br>Can be used to recover from standby modes.  |           |           |           |
| Flash memory         |                                      | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of write/erase cycles (Minimum) : 10000 times<br>Data retention time : 20 years<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash |           |           |           |
| Standby mode         |                                      | Sleep, stop, watch, and time-base timer  |           |           |           |

\* : For details of option, refer to “■ MASK OPTION”.

Note : Part number of evaluation products in MB95150M series is MB95FV100D-103. When using it, the MCU board (MB2146-303A-E) is required.

## ■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

| Oscillation stabilization wait time | Remarks   |
|-------------------------------------|---|
| $(2^{14}-2) / F_{CH}$               | Approx. 4.10 ms (at main oscillation clock 4 MHz) |

## ■ PACKAGES AND CORRESPONDING PRODUCTS

| Package \ Part number | MB95156M | MB95F156M/F156N/F156J | MB95FV100D-103 |
|-----------------------|----------|-----------------------|----------------|
| FPT-48P-M26           | ○        | ○                     | ×              |
| FPT-52P-M01           | ○        | ○                     | ×              |
| BGA-224P-M08          | ×        | ×                     | ○              |

○ : Available  
 × : Unavailable

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

### • Notes on Using Evaluation Products

The Evaluation product has not only the functions of the MB95150M series but also those of other products to support software development for multiple series and models of the F<sup>2</sup>MC-8FX family. The I/O addresses for peripheral resources not used by the MB95150M series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the Flash memory and MASK ROM products, do not use these values in the program.

The functions corresponding to certain bits in single-byte registers may not be supported on some mask ROM and Flash memory products. However, reading or writing to these bits will not cause malfunction of the hardware. Also, as the evaluation, Flash memory, and mask ROM products are designed to have identical software operation, no particular precautions are required.

### • Difference of Memory Spaces

If the amount of memory on the Evaluation product is different from that of the Flash memory product or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

### • Current Consumption

- The current consumption of Flash memory product is typically greater than for MASK ROM product.
- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

### • Package

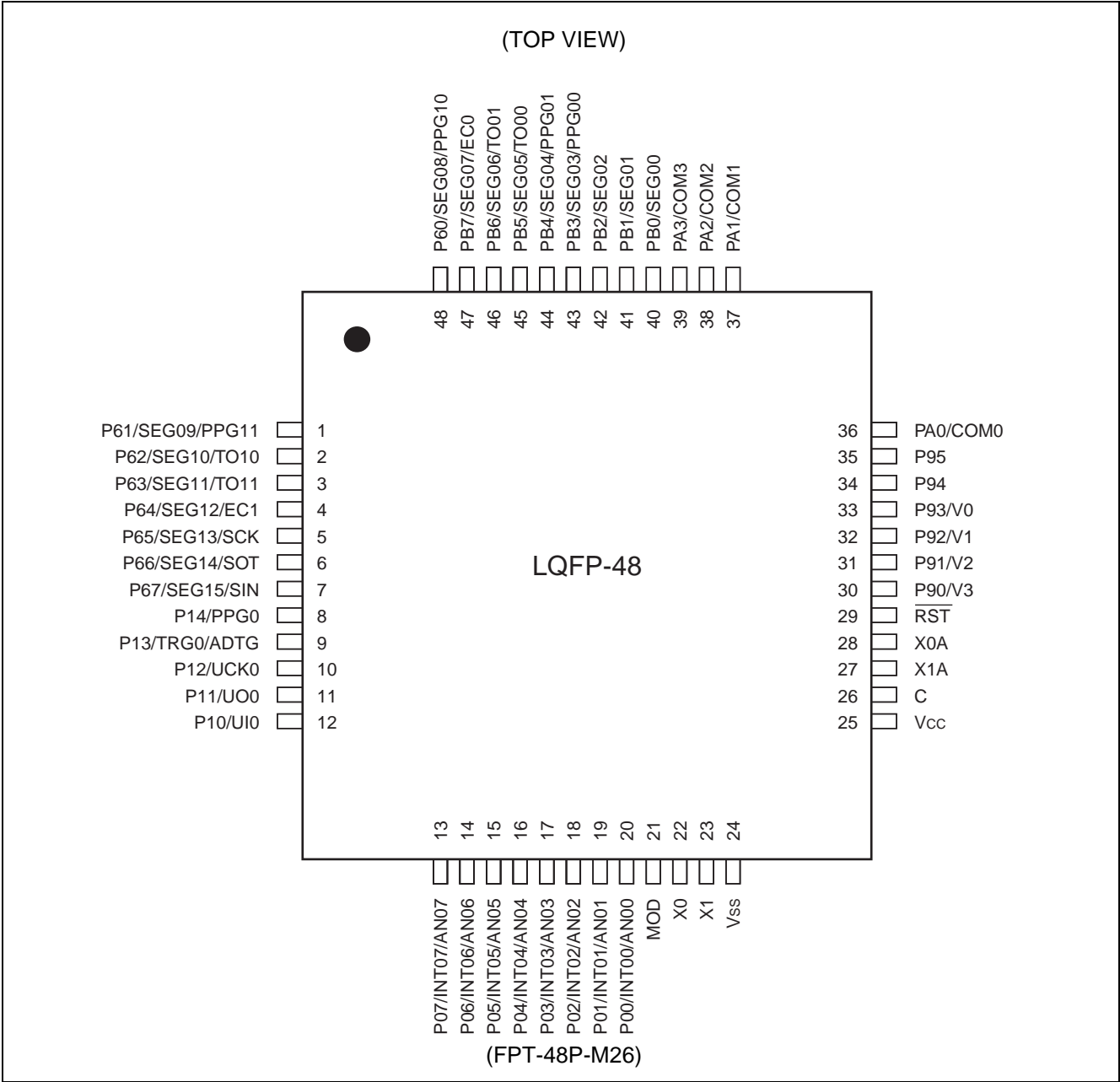
For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

### • Operating voltage

The operating voltage are different between the Evaluation, Flash memory products, and MASK ROM product.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

PIN ASSIGNMENT

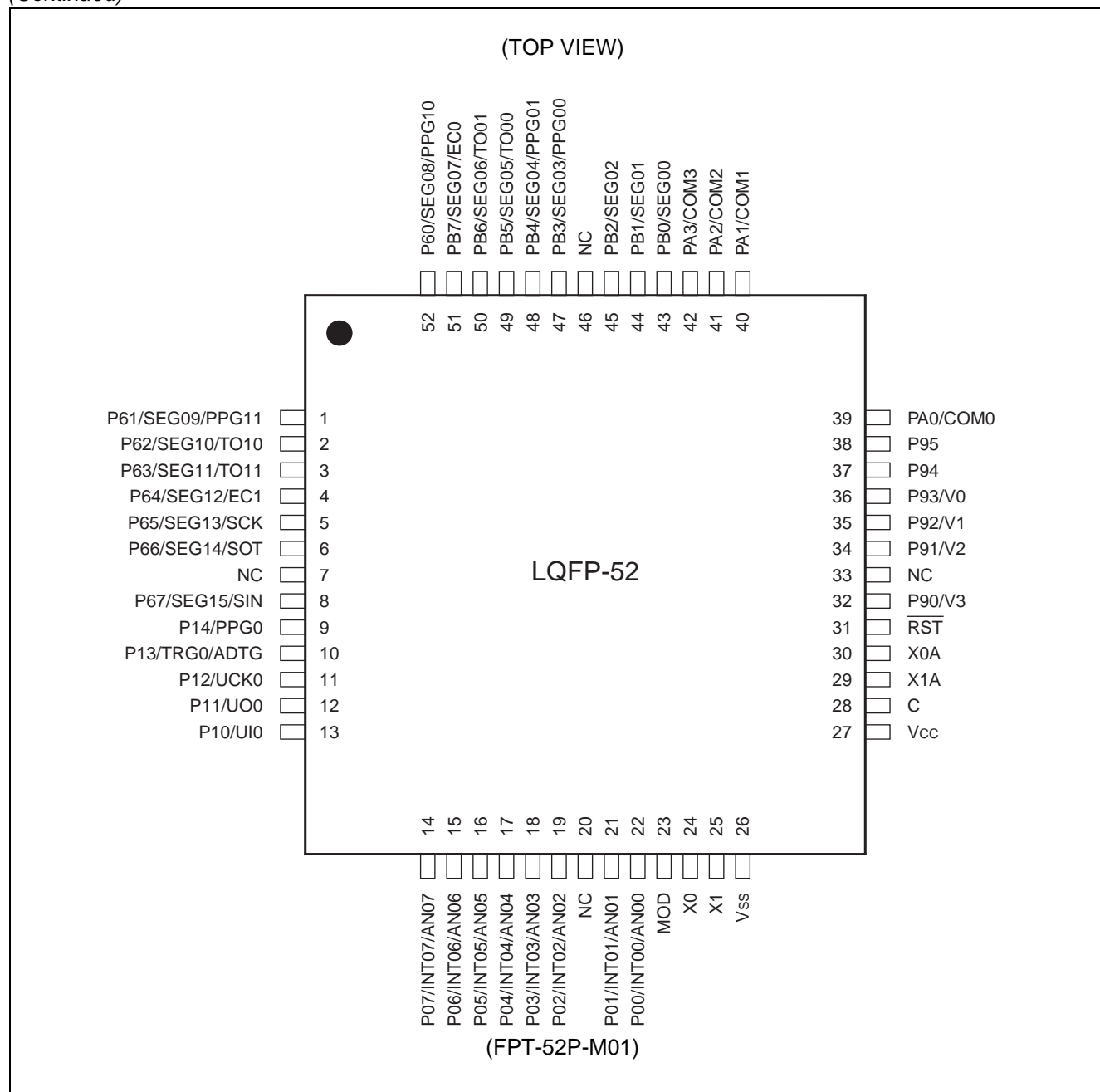


(Continued)



# MB95150M Series

(Continued)



## ■ PIN DESCRIPTION

| Pin no. |        | Pin name        | I/O circuit type*3 | Function   |
|---------|--------|-----------------|--------------------|--|
| LQFP*1  | LQFP*2 |                 |                    |  |
| 1       | 1      | P61/SEG09/PPG11 | M                  | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG09) and 8/16-bit PPG ch.1 output (PPG11).                              |
| 2       | 2      | P62/SEG10/TO10  |                    | General-purpose I/O port.<br>The pins are shared with LCDC SEG output (SEG10, SEG11) and 8/16-bit compound timer ch.1 output (TO10, TO11) .    |
| 3       | 3      | P63/SEG11/TO11  |                    | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG12) and 8/16-bit compound timer ch.1 clock input (EC1).                |
| 4       | 4      | P64/SEG12/EC1   |                    | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG13) and LIN-UART clock I/O (SCK) .                                     |
| 5       | 5      | P65/SEG13/SCK   |                    | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG14) and LIN-UART data output (SOT) .                                   |
| 6       | 6      | P66/SEG14/SOT   |                    | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG15) and LIN-UART data input (SIN) .                                    |
| 7       | 8      | P67/SEG15/SIN   | N                  | General-purpose I/O port.<br>The pin is shared with 16-bit PPG ch.0 output (PPG0) .  |
| 8       | 9      | P14/PPG0        | H                  | General-purpose I/O port.<br>The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG) .              |
| 9       | 10     | P13/TRG0/ADTG   |                    | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 clock I/O (UCK0) .   |
| 10      | 11     | P12/UCK0        |                    | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 data output (UO0) .  |
| 11      | 12     | P11/UO0         |                    | General-purpose I/O port.<br>The pin is shared with UART/SIO ch.0 data input (UI0) .   |
| 12      | 13     | P10/UI0         | G                  | General-purpose I/O port.<br>The pin is shared with external interrupt input (INT00 to INT07) and A/D converter analog input (AN00 to AN07).   |
| 13      | 14     | P07/INT07/AN07  | D                  | General-purpose I/O port.<br>The pins are shared with external interrupt input (INT00 to INT07) and A/D converter analog input (AN00 to AN07). |
| 14      | 15     | P06/INT06/AN06  |                    |  |
| 15      | 16     | P05/INT05/AN05  |                    |  |
| 16      | 17     | P04/INT04/AN04  |                    |  |
| 17      | 18     | P03/INT03/AN03  |                    |  |
| 18      | 19     | P02/INT02/AN02  |                    |  |
| 19      | 21     | P01/INT01/AN01  |                    |  |
| 20      | 22     | P00/INT00/AN00  |                    |  |
| 21      | 23     | MOD             | B                  | The operating mode designation pin   |

(Continued)

# MB95150M Series

(Continued)

| Pin no. |                  | Pin name            | I/O circuit type*3 | Function   |
|---------|------------------|---------------------|--------------------|--|
| LQFP*1  | LQFP*2           |                     |                    |  |
| 22      | 24               | X0                  | A                  | Main clock oscillation pins  |
| 23      | 25               | X1                  |                    |  |
| 24      | 26               | V <sub>SS</sub>     | —                  | Power supply pin (GND)   |
| 25      | 27               | V <sub>CC</sub>     | —                  | Power supply pin   |
| 26      | 28               | C                   | —                  | Capacitor connection pin   |
| 27      | 29               | X1A                 | A                  | Sub clock oscillation pins (32 kHz)  |
| 28      | 30               | X0A                 |                    |  |
| 29      | 31               | R <sub>ST</sub>     | B'                 | Reset pin  |
| 30      | 32               | P90/V3              | R                  | General-purpose I/O port.<br>The pins are shared with power supply pin for LCDC drive (V0 to V3) .   |
| 31      | 34               | P91/V2              |                    |  |
| 32      | 35               | P92/V1              |                    |  |
| 33      | 36               | P93/V0              |                    |  |
| 34      | 37               | P94                 | S                  | General-purpose I/O port   |
| 35      | 38               | P95                 |                    |  |
| 36      | 39               | PA0/COM0            | M                  | General-purpose I/O port.<br>The pins are shared with LCDC COM output (COM0 to COM3) .   |
| 37      | 40               | PA1/COM1            |                    |  |
| 38      | 41               | PA2/COM2            |                    |  |
| 39      | 42               | PA3/COM3            |                    |  |
| 40      | 43               | PB0/SEG00           | M                  | General-purpose I/O port.<br>The pins are shared with LCDC SEG output (SEG00 to SEG02) .   |
| 41      | 44               | PB1/SEG01           |                    |  |
| 42      | 45               | PB2/SEG02           |                    | General-purpose I/O port.<br>The pins are shared with LCDC SEG output (SEG03, SEG04) and 8/16-bit PPG ch.0 output (PPG00, PPG01).          |
| 43      | 47               | PB3/SEG03/<br>PPG00 |                    |  |
| 44      | 48               | PB4/SEG04/<br>PPG01 |                    | General-purpose I/O port.<br>The pins are shared with LCDC SEG output (SEG05, SEG06) and 8/16-bit compound timer ch.0 output (TO00, TO01). |
| 45      | 49               | PB5/SEG05/TO00      |                    |  |
| 46      | 50               | PB6/SEG06/TO01      |                    | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG07) and 8/16-bit compound timer ch.0 clock input (EC0).            |
| 47      | 51               | PB7/SEG07/EC0       |                    |  |
| 48      | 52               | P60/SEG08/<br>PPG10 | M                  | General-purpose I/O port.<br>The pin is shared with LCDC SEG output (SEG08) and 8/16-bit PPG ch.1 output (PPG10) .                         |
| —       | 7, 20,<br>33, 46 | NC                  | —                  | Internal connect pins.<br>Be sure this pin is left open.   |

\*1 : FPT-48P-M26

\*2 : FPT-52P-M01

\*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

## ■ I/O CIRCUIT TYPE

| Type | Circuit  | Remarks   |
|------|--|---|
| A    | <p>Standby control</p>   | <ul style="list-style-type: none"> <li>• Oscillation circuit</li> <li>• High-speed side<br/>Feedback resistance : approx. 1 MΩ</li> <li>• Low-speed side<br/>Feedback resistance : approx. 10 MΩ</li> </ul> |
| B    | <p>Mode input</p>  | <ul style="list-style-type: none"> <li>• Only for input</li> <li>• Hysteresis input</li> </ul>  |
| B'   | <p>Reset input<br/>Reset output</p>  | <ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Reset output</li> </ul>  |
| D    | <p>Pull-up control<br/>Digital output<br/>Digital output<br/>Analog input<br/>Automotive input<br/>Hysteresis input<br/>A/D control<br/>Standby control<br/>External interrupt control</p> | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog input</li> <li>• With pull-up control</li> <li>• Automotive input</li> </ul>                             |
| G    | <p>Pull-up control<br/>Digital output<br/>Digital output<br/>CMOS input<br/>Hysteresis input<br/>Automotive input<br/>Standby control</p>  | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> <li>• Automotive input</li> </ul>                               |
| H    | <p>Pull-up control<br/>Digital output<br/>Digital output<br/>Hysteresis input<br/>Automotive input<br/>Standby control</p>   | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> <li>• Automotive input</li> </ul>   |

(Continued)

# MB95150M Series

(Continued)

| Type | Circuit   | Remarks   |
|------|---|---|
| M    | <p>P-ch Digital output</p> <p>N-ch Digital output</p> <p>LCD output</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>LCD control</p> <p>Standby control</p>                           | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD output</li> <li>• Hysteresis input</li> <li>• Automotive input</li> </ul>                       |
| N    | <p>P-ch Digital output</p> <p>N-ch Digital output</p> <p>LCD output</p> <p>CMOS input</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>LCD control</p> <p>Standby control</p>         | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> <li>• Automotive input</li> </ul> |
| R    | <p>P-ch Digital output</p> <p>N-ch Digital output</p> <p>LCD built-in division resistance I/O</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>LCD control</p> <p>Standby control</p> | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• LCD power supply</li> <li>• Hysteresis input</li> <li>• Automotive input</li> </ul>                 |
| S    | <p>P-ch Digital output</p> <p>N-ch Digital output</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>Standby control</p>  | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Automotive input</li> </ul>   |

## ■ HANDLING DEVICES

- Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between  $V_{CC}$  pin and  $V_{SS}$  pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

- Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the  $V_{CC}$  power-supply voltage.

For stabilization, in principle, keep the variation in  $V_{CC}$  ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard  $V_{CC}$  value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

- Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

## ■ PIN CONNECTION

- Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 k $\Omega$ . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

- Power Supply Pins

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1  $\mu$ F between  $V_{CC}$  and  $V_{SS}$  pins near this device.

# MB95150M Series

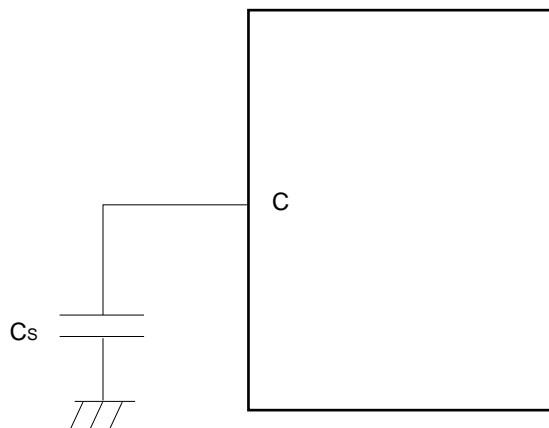
- Mode Pin (MOD)

Connect the MOD pin directly to  $V_{CC}$  or  $V_{SS}$ .

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of  $V_{CC}$  pin must have a capacitance value higher than  $C_s$ . For connection of smoothing capacitor  $C_s$ , refer to the diagram below.

- C pin connection diagram



- NC Pins

Any pins marked "NC" (not connected) must be left open.

## ■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

### • Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

| Package     | Applicable adapter model | Parallel programmers   |
|-------------|--------------------------|--|
| FPT-48P-M26 | TEF110-95F156HPFV        | AF9708 (Ver 02.35G or more)<br>AF9709/B (Ver 02.35G or more)<br>AF9723+AF9834 (Ver 02.08E or more) |
| FPT-52P-M01 | TEF110-95F156HPMC        |  |

Note : For information on applicable adapter models and parallel programmers, contact the following:  
Flash Support Group, Inc. TEL: +81-53-428-8380

### • Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

#### • MB95F156M/F156N/F156J

| Flash memory | CPU address       | Programmer address* |
|--------------|-------------------|---------------------|
| 32 Kbytes    | 8000 <sub>H</sub> | 18000 <sub>H</sub>  |
|              | FFFF <sub>H</sub> | 1FFFF <sub>H</sub>  |

\*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.  
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

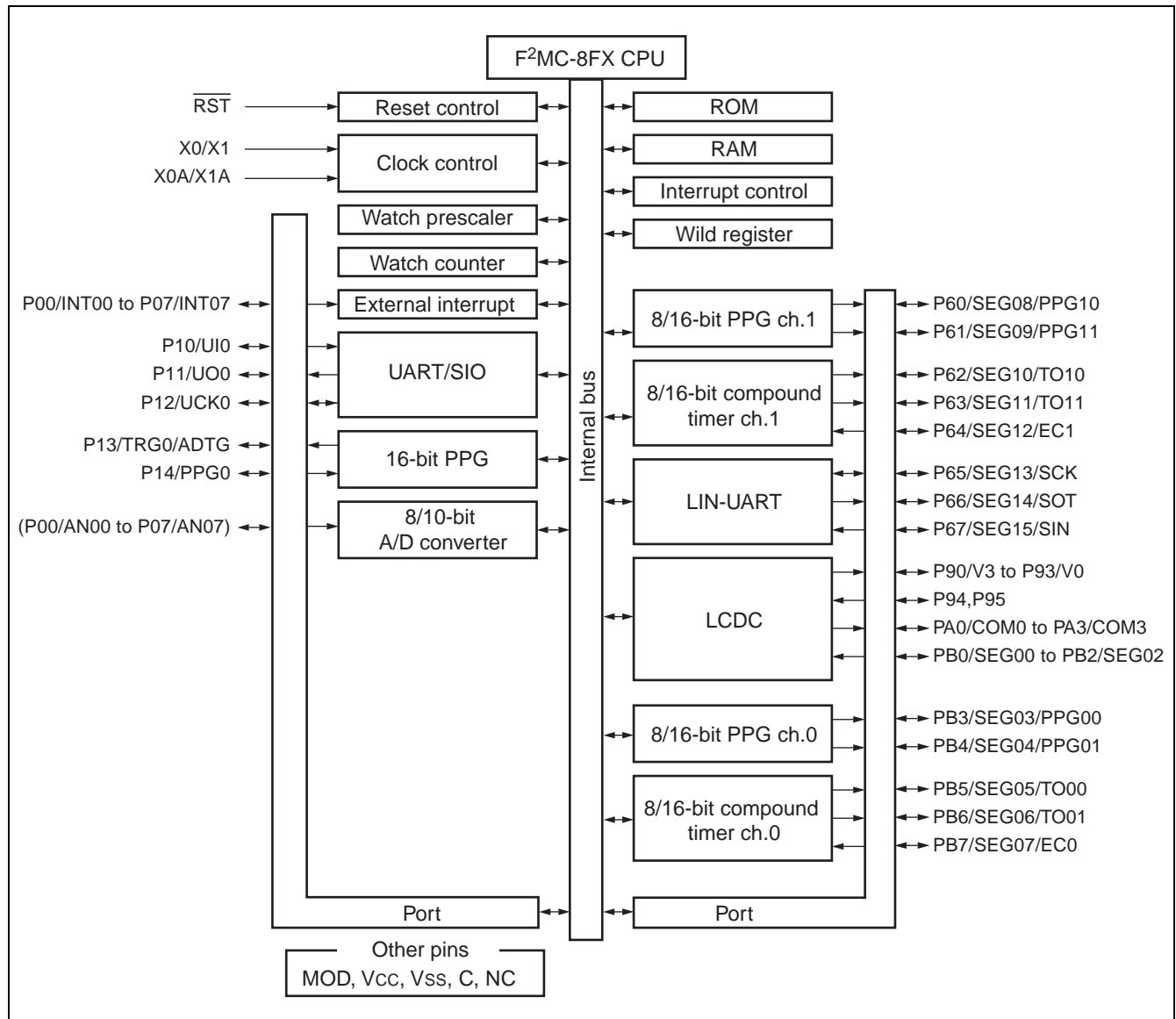
### • Programming Method

- 1) Set the type code of the parallel programmer to 17222.
- 2) Load program data to programmer addresses 18000<sub>H</sub> to 1FFFF<sub>H</sub>.
- 3) Programmed by parallel programmer.



# MB95150M Series

## ■ BLOCK DIAGRAM

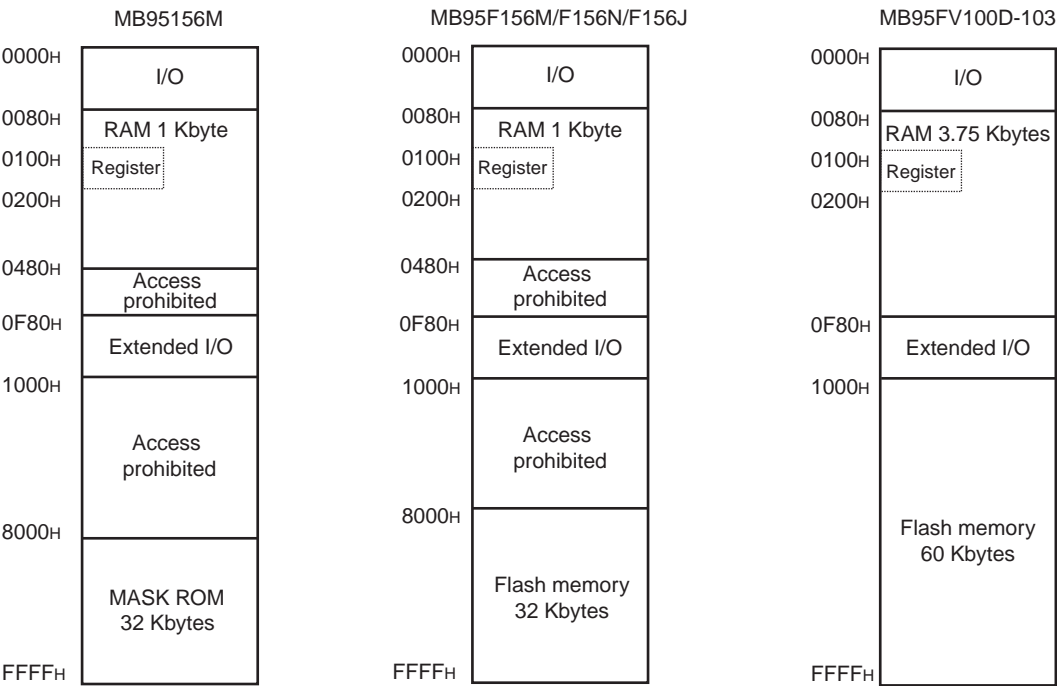


CPU CORE

1. Memory space

Memory space of the MB95150M series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95150M series is shown below.

• Memory Map



# MB95150M Series

## 2. Register

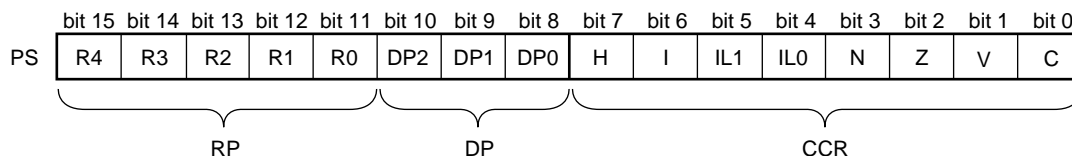
The MB95150M series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

|                           |   |
|---------------------------|---|
| Program counter (PC)      | : A 16-bit register to indicate locations where instructions are stored.  |
| Accumulator (A)           | : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.            |
| Temporary accumulator (T) | : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used. |
| Index register (IX)       | : A 16-bit register for index modification.   |
| Extra pointer (EP)        | : A 16-bit pointer to point to a memory address.  |
| Stack pointer (SP)        | : A 16-bit register to indicate a stack area.   |
| Program status (PS)       | : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register.  |

|  | 16-bit  |                         | Initial Value     |
|--|---------|-------------------------|-------------------|
|  | PC      | : Program counter       | FFFD <sub>H</sub> |
|  | AH   AL | : Accumulator           | 0000 <sub>H</sub> |
|  | TH   TL | : Temporary accumulator | 0000 <sub>H</sub> |
|  | IX      | : Index register        | 0000 <sub>H</sub> |
|  | EP      | : Extra pointer         | 0000 <sub>H</sub> |
|  | SP      | : Stack pointer         | 0000 <sub>H</sub> |
|  | PS      | : Program status        | 0030 <sub>H</sub> |

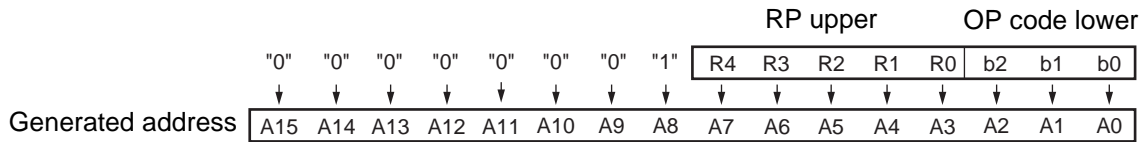
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) . (Refer to the diagram below.)

### • Structure of the Program Status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

• Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080<sub>H</sub> to 00FF<sub>H</sub>.

| Direct bank pointer (DP2 to DP0)        | Specified address area                 | Mapping area   |
|---|--|--|
| XXX <sub>B</sub> (no effect to mapping) | 0000 <sub>H</sub> to 007F <sub>H</sub> | 0000 <sub>H</sub> to 007F <sub>H</sub> (without mapping) |
| 000 <sub>B</sub> (initial value)        | 0080 <sub>H</sub> to 00FF <sub>H</sub> | 0080 <sub>H</sub> to 00FF <sub>H</sub> (without mapping) |
| 001 <sub>B</sub>                        |  | 0100 <sub>H</sub> to 017F <sub>H</sub>                   |
| 010 <sub>B</sub>                        |  | 0180 <sub>H</sub> to 01FF <sub>H</sub>                   |
| 011 <sub>B</sub>                        |  | 0200 <sub>H</sub> to 027F <sub>H</sub>                   |
| 100 <sub>B</sub>                        |  | 0280 <sub>H</sub> to 02FF <sub>H</sub>                   |
| 101 <sub>B</sub>                        |  | 0300 <sub>H</sub> to 037F <sub>H</sub>                   |
| 110 <sub>B</sub>                        |  | 0380 <sub>H</sub> to 03FF <sub>H</sub>                   |
| 111 <sub>B</sub>                        |  | 0400 <sub>H</sub> to 047F <sub>H</sub>                   |

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is set to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

| IL1 | IL0 | Interrupt level | Priority   |
|-----|-----|-----------------|--|
| 0   | 0   | 0               | <div style="text-align: center;"> High<br/> ↑↓<br/> Low (no interruption) </div> |
| 0   | 1   | 1               |  |
| 1   | 0   | 2               |  |
| 1   | 1   | 3               |  |

- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in "0". Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

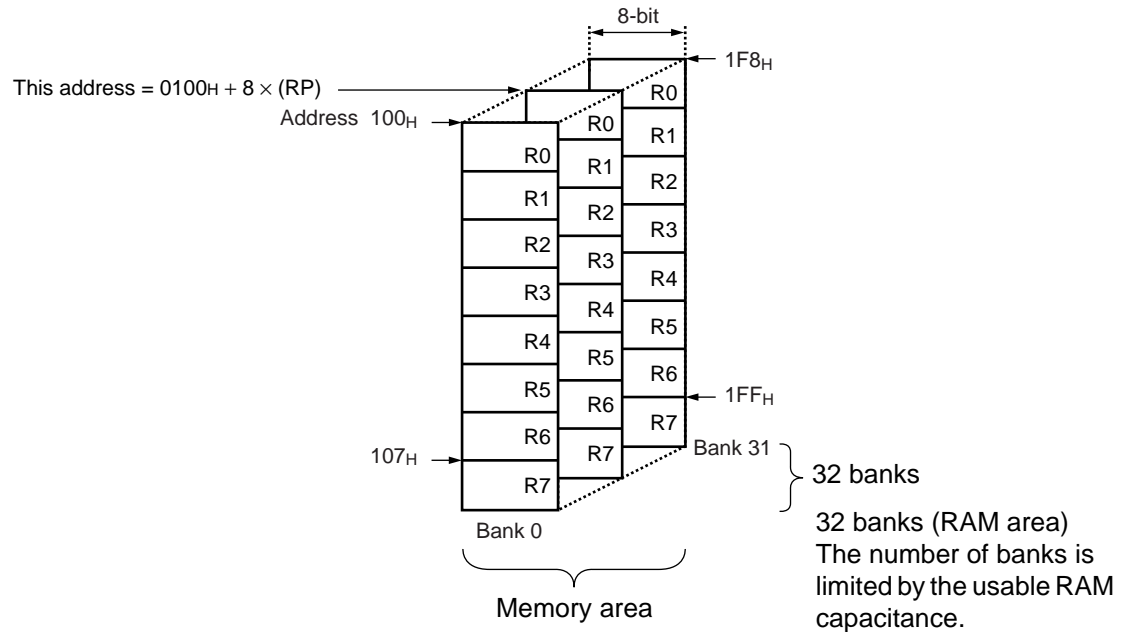
# MB95150M Series

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-register. Up to a total of 32 banks can be used on the MB95150M series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



## ■ I/O MAP

| Address                                      | Register abbreviation | Register name  | R/W | Initial value         |
|--|-----------------------|--|-----|-----------------------|
| 0000 <sub>H</sub>                            | PDR0                  | Port 0 data register                                 | R/W | 00000000 <sub>B</sub> |
| 0001 <sub>H</sub>                            | DDR0                  | Port 0 direction register                            | R/W | 00000000 <sub>B</sub> |
| 0002 <sub>H</sub>                            | PDR1                  | Port 1 data register                                 | R/W | 00000000 <sub>B</sub> |
| 0003 <sub>H</sub>                            | DDR1                  | Port 1 direction register                            | R/W | 00000000 <sub>B</sub> |
| 0004 <sub>H</sub>                            | —                     | (Disabled)   | —   | —                     |
| 0005 <sub>H</sub>                            | WATR                  | Oscillation stabilization wait time setting register | R/W | 11111111 <sub>B</sub> |
| 0006 <sub>H</sub>                            | PLLC                  | PLL control register                                 | R/W | 00000000 <sub>B</sub> |
| 0007 <sub>H</sub>                            | SYCC                  | System clock control register                        | R/W | 1010X011 <sub>B</sub> |
| 0008 <sub>H</sub>                            | STBC                  | Standby control register                             | R/W | 00000000 <sub>B</sub> |
| 0009 <sub>H</sub>                            | RSRR                  | Reset source register                                | R/W | XXXXXXXX <sub>B</sub> |
| 000A <sub>H</sub>                            | TBTC                  | Time-base timer control register                     | R/W | 00000000 <sub>B</sub> |
| 000B <sub>H</sub>                            | WPCR                  | Watch prescaler control register                     | R/W | 00000000 <sub>B</sub> |
| 000C <sub>H</sub>                            | WDTC                  | Watchdog timer control register                      | R/W | 00000000 <sub>B</sub> |
| 000D <sub>H</sub><br>to<br>0015 <sub>H</sub> | —                     | (Disabled)   | —   | —                     |
| 0016 <sub>H</sub>                            | PDR6                  | Port 6 data register                                 | R/W | 00000000 <sub>B</sub> |
| 0017 <sub>H</sub>                            | DDR6                  | Port 6 direction register                            | R/W | 00000000 <sub>B</sub> |
| 0018 <sub>H</sub><br>to<br>001B <sub>H</sub> | —                     | (Disabled)   | —   | —                     |
| 001C <sub>H</sub>                            | PDR9                  | Port 9 data register                                 | R/W | 00000000 <sub>B</sub> |
| 001D <sub>H</sub>                            | DDR9                  | Port 9 direction register                            | R/W | 00000000 <sub>B</sub> |
| 001E <sub>H</sub>                            | PDRA                  | Port A data register                                 | R/W | 00000000 <sub>B</sub> |
| 001F <sub>H</sub>                            | DDRA                  | Port A direction register                            | R/W | 00000000 <sub>B</sub> |
| 0020 <sub>H</sub>                            | PDRB                  | Port B data register                                 | R/W | 00000000 <sub>B</sub> |
| 0021 <sub>H</sub>                            | DDRB                  | Port B direction register                            | R/W | 00000000 <sub>B</sub> |
| 0022 <sub>H</sub><br>to<br>002B <sub>H</sub> | —                     | (Disabled)   | —   | —                     |
| 002C <sub>H</sub>                            | PUL0                  | Port 0 pull-up register                              | R/W | 00000000 <sub>B</sub> |
| 002D <sub>H</sub>                            | PUL1                  | Port 1 pull-up register                              | R/W | 00000000 <sub>B</sub> |
| 002E <sub>H</sub><br>to<br>0035 <sub>H</sub> | —                     | (Disabled)   | —   | —                     |

(Continued)

# MB95150M Series

| Address                                      | Register abbreviation | Register name   | R/W | Initial value         |
|--|-----------------------|---|-----|-----------------------|
| 0036 <sub>H</sub>                            | T01CR1                | 8/16-bit compound timer 01 control status register 1 ch.0 | R/W | 00000000 <sub>B</sub> |
| 0037 <sub>H</sub>                            | T00CR1                | 8/16-bit compound timer 00 control status register 1 ch.0 | R/W | 00000000 <sub>B</sub> |
| 0038 <sub>H</sub>                            | T11CR1                | 8/16-bit compound timer 11 control status register 1 ch.1 | R/W | 00000000 <sub>B</sub> |
| 0039 <sub>H</sub>                            | T10CR1                | 8/16-bit compound timer 10 control status register 1 ch.1 | R/W | 00000000 <sub>B</sub> |
| 003A <sub>H</sub>                            | PC01                  | 8/16-bit PPG1 control register ch.0                       | R/W | 00000000 <sub>B</sub> |
| 003B <sub>H</sub>                            | PC00                  | 8/16-bit PPG0 control register ch.0                       | R/W | 00000000 <sub>B</sub> |
| 003C <sub>H</sub>                            | PC11                  | 8/16-bit PPG1 control register ch.1                       | R/W | 00000000 <sub>B</sub> |
| 003D <sub>H</sub>                            | PC10                  | 8/16-bit PPG0 control register ch.1                       | R/W | 00000000 <sub>B</sub> |
| 003E <sub>H</sub><br>to<br>0041 <sub>H</sub> | —                     | (Disabled)  | —   | —                     |
| 0042 <sub>H</sub>                            | PCNTH0                | 16-bit PPG status control register (upper byte) ch.0      | R/W | 00000000 <sub>B</sub> |
| 0043 <sub>H</sub>                            | PCNTL0                | 16-bit PPG status control register (lower byte) ch.0      | R/W | 00000000 <sub>B</sub> |
| 0044 <sub>H</sub><br>to<br>0047 <sub>H</sub> | —                     | (Disabled)  | —   | —                     |
| 0048 <sub>H</sub>                            | EIC00                 | External interrupt circuit control register ch.0/ch.1     | R/W | 00000000 <sub>B</sub> |
| 0049 <sub>H</sub>                            | EIC10                 | External interrupt circuit control register ch.2/ch.3     | R/W | 00000000 <sub>B</sub> |
| 004A <sub>H</sub>                            | EIC20                 | External interrupt circuit control register ch.4/ch.5     | R/W | 00000000 <sub>B</sub> |
| 004B <sub>H</sub>                            | EIC30                 | External interrupt circuit control register ch.6/ch.7     | R/W | 00000000 <sub>B</sub> |
| 004C <sub>H</sub><br>to<br>004F <sub>H</sub> | —                     | (Disabled)  | —   | —                     |
| 0050 <sub>H</sub>                            | SCR                   | LIN-UART serial control register                          | R/W | 00000000 <sub>B</sub> |
| 0051 <sub>H</sub>                            | SMR                   | LIN-UART serial mode register                             | R/W | 00000000 <sub>B</sub> |
| 0052 <sub>H</sub>                            | SSR                   | LIN-UART serial status register                           | R/W | 00001000 <sub>B</sub> |
| 0053 <sub>H</sub>                            | RDR/TDR               | LIN-UART reception/transmission data register             | R/W | 00000000 <sub>B</sub> |
| 0054 <sub>H</sub>                            | ESCR                  | LIN-UART extended status control register                 | R/W | 00000100 <sub>B</sub> |
| 0055 <sub>H</sub>                            | ECCR                  | LIN-UART extended communication control register          | R/W | 000000XX <sub>B</sub> |
| 0056 <sub>H</sub>                            | SMC10                 | UART/SIO serial mode control register 1 ch.0              | R/W | 00000000 <sub>B</sub> |
| 0057 <sub>H</sub>                            | SMC20                 | UART/SIO serial mode control register 2 ch.0              | R/W | 00100000 <sub>B</sub> |
| 0058 <sub>H</sub>                            | SSR0                  | UART/SIO serial status register ch.0                      | R/W | 00000001 <sub>B</sub> |
| 0059 <sub>H</sub>                            | TDR0                  | UART/SIO serial output data register ch.0                 | R/W | 00000000 <sub>B</sub> |
| 005A <sub>H</sub>                            | RDR0                  | UART/SIO serial input data register ch.0                  | R   | 00000000 <sub>B</sub> |
| 005B <sub>H</sub><br>to<br>006B <sub>H</sub> | —                     | (Disabled)  | —   | —                     |

(Continued)

| Address                                      | Register abbreviation | Register name  | R/W | Initial value         |
|--|-----------------------|--|-----|-----------------------|
| 006C <sub>H</sub>                            | ADC1                  | 8/10-bit A/D converter control register 1                      | R/W | 00000000 <sub>B</sub> |
| 006D <sub>H</sub>                            | ADC2                  | 8/10-bit A/D converter control register 2                      | R/W | 00000000 <sub>B</sub> |
| 006E <sub>H</sub>                            | ADDH                  | 8/10-bit A/D converter data register (Upper byte)              | R/W | 00000000 <sub>B</sub> |
| 006F <sub>H</sub>                            | ADDL                  | 8/10-bit A/D converter data register (Lower byte)              | R/W | 00000000 <sub>B</sub> |
| 0070 <sub>H</sub>                            | WCSR                  | Watch counter status register                                  | R/W | 00000000 <sub>B</sub> |
| 0071 <sub>H</sub>                            | —                     | (Disabled)   | —   | —                     |
| 0072 <sub>H</sub>                            | FSR                   | Flash memory status register                                   | R/W | 000X0000 <sub>B</sub> |
| 0073 <sub>H</sub>                            | SWRE0                 | Flash memory sector writing control register 0                 | R/W | 00000000 <sub>B</sub> |
| 0074 <sub>H</sub>                            | SWRE1                 | Flash memory sector writing control register 1                 | R/W | 00000000 <sub>B</sub> |
| 0075 <sub>H</sub>                            | —                     | (Disabled)   | —   | —                     |
| 0076 <sub>H</sub>                            | WREN                  | Wild register address compare enable register                  | R/W | 00000000 <sub>B</sub> |
| 0077 <sub>H</sub>                            | WROR                  | Wild register data test setting register                       | R/W | 00000000 <sub>B</sub> |
| 0078 <sub>H</sub>                            | —                     | Register bank pointer (RP) , Mirror of direct bank pointer (P) | —   | —                     |
| 0079 <sub>H</sub>                            | ILR0                  | Interrupt level setting register 0                             | R/W | 11111111 <sub>B</sub> |
| 007A <sub>H</sub>                            | ILR1                  | Interrupt level setting register 1                             | R/W | 11111111 <sub>B</sub> |
| 007B <sub>H</sub>                            | ILR2                  | Interrupt level setting register 2                             | R/W | 11111111 <sub>B</sub> |
| 007C <sub>H</sub>                            | ILR3                  | Interrupt level setting register 3                             | R/W | 11111111 <sub>B</sub> |
| 007D <sub>H</sub>                            | ILR4                  | Interrupt level setting register 4                             | R/W | 11111111 <sub>B</sub> |
| 007E <sub>H</sub>                            | ILR5                  | Interrupt level setting register 5                             | R/W | 11111111 <sub>B</sub> |
| 007F <sub>H</sub>                            | —                     | (Disabled)   | —   | —                     |
| 0F80 <sub>H</sub>                            | WRARH0                | Wild register address setting register (upper byte) ch.0       | R/W | 00000000 <sub>B</sub> |
| 0F81 <sub>H</sub>                            | WRARL0                | Wild register address setting register (lower byte) ch.0       | R/W | 00000000 <sub>B</sub> |
| 0F82 <sub>H</sub>                            | WRDR0                 | Wild register data setting register ch.0                       | R/W | 00000000 <sub>B</sub> |
| 0F83 <sub>H</sub>                            | WRARH1                | Wild register address setting register (upper byte) ch.1       | R/W | 00000000 <sub>B</sub> |
| 0F84 <sub>H</sub>                            | WRARL1                | Wild register address setting register (lower byte) ch.1       | R/W | 00000000 <sub>B</sub> |
| 0F85 <sub>H</sub>                            | WRDR1                 | Wild register data setting register ch.1                       | R/W | 00000000 <sub>B</sub> |
| 0F86 <sub>H</sub>                            | WRARH2                | Wild register address setting register (upper byte) ch.2       | R/W | 00000000 <sub>B</sub> |
| 0F87 <sub>H</sub>                            | WRARL2                | Wild register address setting register (lower byte) ch.2       | R/W | 00000000 <sub>B</sub> |
| 0F88 <sub>H</sub>                            | WRDR2                 | Wild register data setting register ch.2                       | R/W | 00000000 <sub>B</sub> |
| 0F89 <sub>H</sub><br>to<br>0F91 <sub>H</sub> | —                     | (Disabled)   | —   | —                     |
| 0F92 <sub>H</sub>                            | T01CR0                | 8/16-bit compound timer 01 control status register 0 ch.0      | R/W | 00000000 <sub>B</sub> |
| 0F93 <sub>H</sub>                            | T00CR0                | 8/16-bit compound timer 00 control status register 0 ch.0      | R/W | 00000000 <sub>B</sub> |
| 0F94 <sub>H</sub>                            | T01DR                 | 8/16-bit compound timer 01 data register ch.0                  | R/W | 00000000 <sub>B</sub> |

(Continued)



# MB95150M Series

| Address                                      | Register abbreviation | Register name  | R/W | Initial value         |
|--|-----------------------|--|-----|-----------------------|
| 0F95 <sub>H</sub>                            | T00DR                 | 8/16-bit compound timer 00 data register ch.0                            | R/W | 00000000 <sub>B</sub> |
| 0F96 <sub>H</sub>                            | TMCR0                 | 8/16-bit compound timer 00/01 timer mode control register ch.0           | R/W | 00000000 <sub>B</sub> |
| 0F97 <sub>H</sub>                            | T11CR0                | 8/16-bit compound timer 11 control status register 0 ch.1                | R/W | 00000000 <sub>B</sub> |
| 0F98 <sub>H</sub>                            | T10CR0                | 8/16-bit compound timer 10 control status register 0 ch.1                | R/W | 00000000 <sub>B</sub> |
| 0F99 <sub>H</sub>                            | T11DR                 | 8/16-bit compound timer 11 data register ch.1                            | R/W | 00000000 <sub>B</sub> |
| 0F9A <sub>H</sub>                            | T10DR                 | 8/16-bit compound timer 10 data register ch.1                            | R/W | 00000000 <sub>B</sub> |
| 0F9B <sub>H</sub>                            | TMCR1                 | 8/16-bit compound timer 10/11 timer mode control register ch.1           | R/W | 00000000 <sub>B</sub> |
| 0F9C <sub>H</sub>                            | PPS01                 | 8/16-bit PPG1 cycle setting buffer register ch.0                         | R/W | 11111111 <sub>B</sub> |
| 0F9D <sub>H</sub>                            | PPS00                 | 8/16-bit PPG0 cycle setting buffer register ch.0                         | R/W | 11111111 <sub>B</sub> |
| 0F9E <sub>H</sub>                            | PDS01                 | 8/16-bit PPG1 duty setting buffer register ch.0                          | R/W | 11111111 <sub>B</sub> |
| 0F9F <sub>H</sub>                            | PDS00                 | 8/16-bit PPG0 duty setting buffer register ch.0                          | R/W | 11111111 <sub>B</sub> |
| 0FA0 <sub>H</sub>                            | PPS11                 | 8/16-bit PPG1 cycle setting buffer register ch.1                         | R/W | 11111111 <sub>B</sub> |
| 0FA1 <sub>H</sub>                            | PPS10                 | 8/16-bit PPG0 cycle setting buffer register ch.1                         | R/W | 11111111 <sub>B</sub> |
| 0FA2 <sub>H</sub>                            | PDS11                 | 8/16-bit PPG1 duty setting buffer register ch.1                          | R/W | 11111111 <sub>B</sub> |
| 0FA3 <sub>H</sub>                            | PDS10                 | 8/16-bit PPG0 duty setting buffer register ch.1                          | R/W | 11111111 <sub>B</sub> |
| 0FA4 <sub>H</sub>                            | PPGS                  | 8/16-bit PPG start register  | R/W | 00000000 <sub>B</sub> |
| 0FA5 <sub>H</sub>                            | REVC                  | 8/16-bit PPG output inversion register                                   | R/W | 00000000 <sub>B</sub> |
| 0FA6 <sub>H</sub><br>to<br>0FA9 <sub>H</sub> | —                     | (Disabled)   | —   | —                     |
| 0FAA <sub>H</sub>                            | PDCRH0                | 16-bit PPG down counter register (upper byte) ch.0                       | R   | 00000000 <sub>B</sub> |
| 0FAB <sub>H</sub>                            | PDCRL0                | 16-bit PPG down counter register (lower byte) ch.0                       | R   | 00000000 <sub>B</sub> |
| 0FAC <sub>H</sub>                            | PCSRH0                | 16-bit PPG cycle setting buffer register (upper byte) ch.0               | R/W | 11111111 <sub>B</sub> |
| 0FAD <sub>H</sub>                            | PCSRL0                | 16-bit PPG cycle setting buffer register (lower byte) ch.0               | R/W | 11111111 <sub>B</sub> |
| 0FAE <sub>H</sub>                            | PDUTH0                | 16-bit PPG duty setting buffer register (upper byte) ch.0                | R/W | 11111111 <sub>B</sub> |
| 0FAF <sub>H</sub>                            | PDUTL0                | 16-bit PPG duty setting buffer register (lower byte) ch.0                | R/W | 11111111 <sub>B</sub> |
| 0FB0 <sub>H</sub><br>to<br>0FBB <sub>H</sub> | —                     | (Disabled)   | —   | —                     |
| 0FBC <sub>H</sub>                            | BGR1                  | LIN-UART baud rate generator register 1                                  | R/W | 00000000 <sub>B</sub> |
| 0FBD <sub>H</sub>                            | BGR0                  | LIN-UART baud rate generator register 0                                  | R/W | 00000000 <sub>B</sub> |
| 0FBE <sub>H</sub>                            | PSSR0                 | UART/SIO dedicated baud rate generator prescaler selection register ch.0 | R/W | 00000000 <sub>B</sub> |
| 0FBF <sub>H</sub>                            | BRSR0                 | UART/SIO dedicated baud rate generator baud rate setting register ch.0   | R/W | 00000000 <sub>B</sub> |
| 0FC0 <sub>H</sub><br>to<br>0FC2 <sub>H</sub> | —                     | (Disabled)   | —   | —                     |

(Continued)

(Continued)

| Address                                      | Register abbreviation | Register name                           | R/W | Initial value         |
|--|-----------------------|---|-----|-----------------------|
| 0FC3 <sub>H</sub>                            | AIDRL                 | A/D input disable register (lower byte) | R/W | 00000000 <sub>B</sub> |
| 0FC4 <sub>H</sub>                            | LCDCC                 | LCDC control register                   | R/W | 00010000 <sub>B</sub> |
| 0FC5 <sub>H</sub>                            | LCDCE1                | LCDC enable register 1                  | R/W | 00110000 <sub>B</sub> |
| 0FC6 <sub>H</sub>                            | LCDCE2                | LCDC enable register 2                  | R/W | 00000000 <sub>B</sub> |
| 0FC7 <sub>H</sub>                            | LCDCE3                | LCDC enable register 3                  | R/W | 00000000 <sub>B</sub> |
| 0FC8 <sub>H</sub><br>to<br>0FCA <sub>H</sub> | —                     | (Disabled)                              | —   | —                     |
| 0FCB <sub>H</sub>                            | LCDCB1                | LCDC blinking setting register 1        | R/W | 00000000 <sub>B</sub> |
| 0FCC <sub>H</sub>                            | LCDCB2                | LCDC blinking setting register 2        | R/W | 00000000 <sub>B</sub> |
| 0FCD <sub>H</sub><br>to<br>0FD4 <sub>H</sub> | LCDRAM                | LCDC display RAM                        | R/W | 00000000 <sub>B</sub> |
| 0FD5 <sub>H</sub><br>to<br>0FE2 <sub>H</sub> | —                     | (Disabled)                              | —   | —                     |
| 0FE3 <sub>H</sub>                            | WCDR                  | Watch counter data register             | R/W | 00111111 <sub>B</sub> |
| 0FE4 <sub>H</sub><br>to<br>0FE6 <sub>H</sub> | —                     | (Disabled)                              | —   | —                     |
| 0FE7 <sub>H</sub>                            | ILSR2                 | Input level select register 2           | R/W | 00000000 <sub>B</sub> |
| 0FE8 <sub>H</sub> ,<br>0FE9 <sub>H</sub>     | —                     | (Disabled)                              | —   | —                     |
| 0FEA <sub>H</sub>                            | CSVCR                 | Clock supervisor control register       | R/W | 00011100 <sub>B</sub> |
| 0FEB <sub>H</sub><br>to<br>0FED <sub>H</sub> | —                     | (Disabled)                              | —   | —                     |
| 0FEE <sub>H</sub>                            | ILSR                  | Input level select register             | R/W | 00000000 <sub>B</sub> |
| 0FEF <sub>H</sub>                            | WICR                  | Interrupt pin control register          | R/W | 01000000 <sub>B</sub> |
| 0FF0 <sub>H</sub><br>to<br>0FFF <sub>H</sub> | —                     | (Disabled)                              | —   | —                     |

- R/W access symbols

R/W : Readable/Writable

R : Read only

W : Write only

- Initial value symbols

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

# MB95150M Series

## ■ INTERRUPT SOURCE TABLE

| Interrupt source                     | Interrupt request number | Vector table address |                   | Bit name of interrupt level setting register | Same level priority order (at simultaneous occurrence)   |
|--------------------------------------|--------------------------|----------------------|-------------------|--|--|
|                                      |                          | Upper                | Lower             |  |  |
| External interrupt ch.0              | IRQ0                     | FFFA <sub>H</sub>    | FFFB <sub>H</sub> | L00 [1 : 0]                                  | <div>High</div> <div>↑</div> <div>↓</div> <div>Low</div> |
| External interrupt ch.4              |                          |                      |                   |  |  |
| External interrupt ch.1              | IRQ1                     | FFF8 <sub>H</sub>    | FFF9 <sub>H</sub> | L01 [1 : 0]                                  |  |
| External interrupt ch.5              |                          |                      |                   |  |  |
| External interrupt ch.2              | IRQ2                     | FFF6 <sub>H</sub>    | FFF7 <sub>H</sub> | L02 [1 : 0]                                  |  |
| External interrupt ch.6              |                          |                      |                   |  |  |
| External interrupt ch.3              | IRQ3                     | FFF4 <sub>H</sub>    | FFF5 <sub>H</sub> | L03 [1 : 0]                                  |  |
| External interrupt ch.7              |                          |                      |                   |  |  |
| UART/SIO ch.0                        | IRQ4                     | FFF2 <sub>H</sub>    | FFF3 <sub>H</sub> | L04 [1 : 0]                                  |  |
| 8/16-bit compound timer ch.0 (Lower) | IRQ5                     | FFF0 <sub>H</sub>    | FFF1 <sub>H</sub> | L05 [1 : 0]                                  |  |
| 8/16-bit compound timer ch.0 (Upper) | IRQ6                     | FFEE <sub>H</sub>    | FFEF <sub>H</sub> | L06 [1 : 0]                                  |  |
| LIN-UART (reception)                 | IRQ7                     | FFEC <sub>H</sub>    | FFED <sub>H</sub> | L07 [1 : 0]                                  |  |
| LIN-UART (transmission)              | IRQ8                     | FFEA <sub>H</sub>    | FFEB <sub>H</sub> | L08 [1 : 0]                                  |  |
| 8/16-bit PPG ch.1 (Lower)            | IRQ9                     | FFE8 <sub>H</sub>    | FFE9 <sub>H</sub> | L09 [1 : 0]                                  |  |
| 8/16-bit PPG ch.1 (Upper)            | IRQ10                    | FFE6 <sub>H</sub>    | FFE7 <sub>H</sub> | L10 [1 : 0]                                  |  |
| (Unused)                             | IRQ11                    | FFE4 <sub>H</sub>    | FFE5 <sub>H</sub> | L11 [1 : 0]                                  |  |
| 8/16-bit PPG ch.0 (Upper)            | IRQ12                    | FFE2 <sub>H</sub>    | FFE3 <sub>H</sub> | L12 [1 : 0]                                  |  |
| 8/16-bit PPG ch.0 (Lower)            | IRQ13                    | FFE0 <sub>H</sub>    | FFE1 <sub>H</sub> | L13 [1 : 0]                                  |  |
| 8/16-bit compound timer ch.1 (Upper) | IRQ14                    | FFDE <sub>H</sub>    | FFDF <sub>H</sub> | L14 [1 : 0]                                  |  |
| 16-bit PPG ch.0                      | IRQ15                    | FFDC <sub>H</sub>    | FFDD <sub>H</sub> | L15 [1 : 0]                                  |  |
| (Unused)                             | IRQ16                    | FFDA <sub>H</sub>    | FFDB <sub>H</sub> | L16 [1 : 0]                                  |  |
| (Unused)                             | IRQ17                    | FFD8 <sub>H</sub>    | FFD9 <sub>H</sub> | L17 [1 : 0]                                  |  |
| 8/10-bit A/D converter               | IRQ18                    | FFD6 <sub>H</sub>    | FFD7 <sub>H</sub> | L18 [1 : 0]                                  |  |
| Time-base timer                      | IRQ19                    | FFD4 <sub>H</sub>    | FFD5 <sub>H</sub> | L19 [1 : 0]                                  |  |
| Watch prescaler/Watch counter        | IRQ20                    | FFD2 <sub>H</sub>    | FFD3 <sub>H</sub> | L20 [1 : 0]                                  |  |
| (Unused)                             | IRQ21                    | FFD0 <sub>H</sub>    | FFD1 <sub>H</sub> | L21 [1 : 0]                                  |  |
| 8/16-bit compound timer ch.1 (Lower) | IRQ22                    | FFCE <sub>H</sub>    | FFCF <sub>H</sub> | L22 [1 : 0]                                  |  |
| Flash memory                         | IRQ23                    | FFCC <sub>H</sub>    | FFCD <sub>H</sub> | L23 [1 : 0]                                  |  |

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter                              | Symbol                           | Rating                |                       | Unit | Remarks  |
|--|----------------------------------|-----------------------|-----------------------|------|--|
|  |                                  | Min                   | Max                   |      |  |
| Power supply voltage*1                 | V <sub>CC</sub>                  | V <sub>SS</sub> – 0.3 | V <sub>SS</sub> + 6.0 | V    |  |
| Power supply voltage for LCD           | V <sub>O</sub> to V <sub>3</sub> | V <sub>SS</sub> – 0.3 | V <sub>SS</sub> + 6.0 | V    | *2   |
| Input voltage*1                        | V <sub>I</sub>                   | V <sub>SS</sub> – 0.3 | V <sub>SS</sub> + 6.0 | V    | *3   |
| Output voltage*1                       | V <sub>O</sub>                   | V <sub>SS</sub> – 0.3 | V <sub>SS</sub> + 6.0 | V    | *3   |
| Maximum clamp current                  | I <sub>CLAMP</sub>               | – 2.0                 | + 2.0                 | mA   | Applicable to pins*4   |
| Total maximum clamp current            | Σ I <sub>CLAMP</sub>             | —                     | 20                    | mA   | Applicable to pins*4   |
| “L” level maximum output current       | I <sub>OL</sub>                  | —                     | 15                    | mA   | Applicable to pins*4   |
| “L” level average current              | I <sub>OLAV</sub>                | —                     | 4                     | mA   | Applicable to pins*4<br>Average output current =<br>operating current × operating ratio<br>(1 pin) |
| “L” level total maximum output current | ΣI <sub>OL</sub>                 | —                     | 100                   | mA   |  |
| “L” level total average output current | ΣI <sub>OLAV</sub>               | —                     | 50                    | mA   | Total average output current =<br>operating current × operating ratio<br>(Total of pins)           |
| “H” level maximum output current       | I <sub>OH</sub>                  | —                     | – 15                  | mA   | Applicable to pins*4   |
| “H” level average current              | I <sub>OHAV</sub>                | —                     | – 4                   | mA   | Applicable to pins*4<br>Average output current =<br>operating current × operating ratio<br>(1 pin) |
| “H” level total maximum output current | ΣI <sub>OH</sub>                 | —                     | – 100                 | mA   |  |
| “H” level total average output current | ΣI <sub>OHAV</sub>               | —                     | – 50                  | mA   | Total average output current =<br>operating current × operating ratio<br>(Total of pins)           |
| Power consumption                      | P <sub>d</sub>                   | —                     | 320                   | mW   |  |
| Operating temperature                  | T <sub>A</sub>                   | – 40                  | + 85                  | °C   |  |
| Storage temperature                    | T <sub>stg</sub>                 | – 55                  | + 150                 | °C   |  |

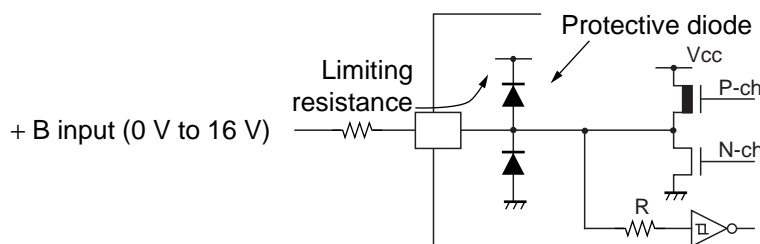
(Continued)

# MB95150M Series

(Continued)

- \*1 : The parameter is based on  $V_{SS} = 0.0 \text{ V}$ .
- \*2 :  $V_0$  to  $V_3$  should not exceed  $V_{CC} + 0.3 \text{ V}$ .
- \*3 :  $V_i$  and  $V_o$  should not exceed  $V_{CC} + 0.3 \text{ V}$ .  $V_i$  must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_i$  rating.
- \*4 : Applicable to pins : P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7
  - Use within recommended operating conditions.
  - Use at DC voltage (current).
  - +B signal is an input signal that exceeds  $V_{CC}$  voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this affects other devices.
  - Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the + B input pin open.
  - Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept + B signal input.
  - Sample recommended circuits :

- Input/Output Equivalent circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

(V<sub>SS</sub> = 0.0 V)

| Parameter                    | Symbol          | Conditions | Value           |                 | Unit | Remarks   |                           |
|------------------------------|-----------------|------------|-----------------|-----------------|------|---|---------------------------|
|                              |                 |            | Min             | Max             |      |   |                           |
| Power supply voltage         | V <sub>CC</sub> | —          | 2.4*1,*2        | 5.5*1           | V    | In normal operating   | Other than MB95FV100D-103 |
|                              |                 |            | 2.3             | 5.5             |      | Hold condition in STOP mode   |                           |
|                              |                 |            | 2.7             | 5.5             |      | In normal operating   | MB95FV100D-103            |
|                              |                 |            | 2.3             | 5.5             |      | Hold condition in STOP mode   |                           |
| Power supply voltage for LCD | V0 to V3        |            | V <sub>SS</sub> | V <sub>CC</sub> | V    | The range of liquid crystal power supply (The optimal value depends on liquid crystal display elements used.) |                           |
| Smoothing capacitor          | C <sub>S</sub>  |            | 0.1             | 1.0             | μF   | *3  |                           |
| Operating temperature        | T <sub>A</sub>  |            | −40             | +85             | °C   | Other than MB95FV100D-103   |                           |
|                              |                 |            | +5              | +35             | °C   | MB95FV100D-103  |                           |

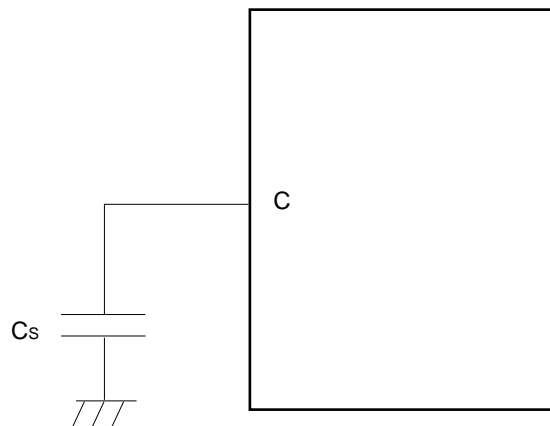
\*1 : The values vary with the operating frequency, machine clock or analog guarantee range.

\*2 : When the low voltage detection reset is used, reset occurs while the low voltage is detected. For details on Low voltage detection, see “(8) Low Voltage Detection” in “4. AC Characteristics”.

\*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V<sub>CC</sub> pin must have a capacitance value higher than C<sub>S</sub>. For connection of smoothing capacitor C<sub>S</sub>, refer to the diagram below.

# MB95150M Series

- C pin connection diagram



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

| Parameter                                     | Symbol     | Pin name   | Conditions                     | Value          |     |                | Unit             | Remarks  |
|---|------------|--|--------------------------------|----------------|-----|----------------|------------------|--|
|   |            |  |                                | Min            | Typ | Max            |                  |  |
| “H” level input voltage                       | $V_{IH1}$  | P10, P67   | *1                             | $0.7 V_{CC}$   | —   | $V_{CC} + 0.3$ | V                | When selecting CMOS input level                    |
|   | $V_{IHA}$  | P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7 | —                              | $0.8 V_{CC}$   | —   | $V_{CC} + 0.3$ | V                | Pin input at selecting of automotive input level   |
|   | $V_{IHS1}$ | P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7 | *1                             | $0.8 V_{CC}$   | —   | $V_{CC} + 0.3$ | V                | Hysteresis input                                   |
|   | $V_{IHM}$  | $\overline{RST}$ , MOD   | —                              | $0.8 V_{CC}$   | —   | $V_{CC} + 0.3$ | V                | Hysteresis input                                   |
| “L” level input voltage                       | $V_{IL}$   | P10, P67   | *1                             | $V_{SS} - 0.3$ | —   | $0.3 V_{CC}$   | V                | When selecting CMOS input level (Hysteresis input) |
|   | $V_{ILA}$  | P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7 | —                              | $V_{SS} - 0.3$ | —   | $0.5 V_{CC}$   | V                | Pin input at selecting of automotive input level   |
|   | $V_{ILS}$  | P00 to P07, P10 to P14, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7 | *1                             | $V_{SS} - 0.3$ | —   | $0.2 V_{CC}$   | V                | Hysteresis input                                   |
|   | $V_{ILM}$  | $\overline{RST}$ , MOD   | —                              | $V_{SS} - 0.3$ | —   | $0.2 V_{CC}$   | V                | Hysteresis input                                   |
| “H” level output voltage                      | $V_{OH}$   | All output pins  | $I_{OH} = -4.0 \text{ mA}$     | $V_{CC} - 0.5$ | —   | —              | V                |  |
| “L” level output voltage                      | $V_{OL}$   | All output pins, $\overline{RST}^{*2}$                                 | $I_{OL} = 4.0 \text{ mA}$      | —              | —   | 0.4            | V                |  |
| Input leak current (Hi-Z output leak current) | $I_{LI}$   | Port other than P00 to P07, P10 to P14                                 | $0.0 \text{ V} < V_i < V_{CC}$ | -5             | —   | +5             | $\mu\text{A}$    | When specifying without pull-up resistance         |
| Pull-up resistance                            | $R_{PULL}$ | P00 to P07, P10 to P14   | $V_i = 0.0 \text{ V}$          | 25             | 50  | 100            | $\text{k}\Omega$ | When specifying with pull-up resistance            |
| Pull-down resistance                          | $R_{MOD}$  | MOD  | $V_1 = V_{CC}$                 | 50             | 100 | 200            | $\text{k}\Omega$ | MASK ROM product only                              |

(Continued)



# MB95150M Series

(V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = - 40 °C to + 85 °C)

| Parameter                 | Sym-<br>bol      | Pin name   | Conditions  | Value |      |      | Unit | Remarks  |
|---------------------------|------------------|--|---|-------|------|------|------|--|
|                           |                  |  |   | Min   | Typ  | Max  |      |  |
| Power supply<br>current*3 | I <sub>CC</sub>  | V <sub>CC</sub><br>(External clock<br>operation)   | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 20 MHz,<br>F <sub>MP</sub> = 10 MHz<br>Main clock mode<br>(divided by 2)  | —     | 9.5  | 12.5 | mA   | Flash memory product<br>(at other than Flash<br>memory writing and<br>erasing) |
|                           |                  |  |   | —     | 30   | 35   | mA   | Flash memory product<br>(at Flash memory<br>writing and erasing)               |
|                           |                  |  |   | —     | 11.9 | 17.2 | mA   | Flash memory product<br>(When A/D conversion)                                  |
|                           |                  |  |   | —     | 7.2  | 9.5  | mA   | MASK ROM product   |
|                           |                  |  |   | —     | 9.6  | 14.2 | mA   | MASK ROM product<br>(When A/D conversion)                                      |
|                           |                  |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 32 MHz,<br>F <sub>MP</sub> = 16 MHz,<br>Main clock mode<br>(divided by 2) | —     | 15.2 | 20.0 | mA   | Flash memory product<br>(at other than Flash<br>memory writing and<br>erasing) |
|                           |                  |  |   | —     | 35.7 | 42.5 | mA   | Flash memory product<br>(at Flash memory<br>writing and erasing)               |
|                           |                  |  |   | —     | 19.0 | 27.5 | mA   | Flash memory product<br>(When A/D conversion)                                  |
|                           |                  |  |   | —     | 11.6 | 15.2 | mA   | MASK ROM product   |
|                           |                  |  |   | —     | 15.4 | 22.7 | mA   | MASK ROM product<br>(When A/D conversion)                                      |
|                           | I <sub>CCS</sub> |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 20 MHz,<br>F <sub>MP</sub> = 10 MHz<br>Main sleep mode<br>(divided by 2)  | —     | 4.5  | 7.5  | mA   |  |
|                           |                  |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 32 MHz,<br>F <sub>MP</sub> = 16 MHz<br>Main sleep mode<br>(divided by 2)  | —     | 7.2  | 12.0 | mA   |  |
|                           | I <sub>CCL</sub> | V <sub>CC</sub> = 5.5 V,<br>F <sub>CL</sub> = 32 kHz,<br>F <sub>MPL</sub> = 16 kHz<br>Sub clock mode<br>(divided by 2) ,<br>T <sub>A</sub> = + 25 °C | —   | 45    | 100  | μA   |      |  |

(Continued)

# MB95150M Series

(V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = - 40 °C to + 85 °C)

| Parameter                          | Sym-<br>bol         | Pin name   | Conditions   | Value |      |      | Unit | Remarks                    |
|------------------------------------|---------------------|--|--|-------|------|------|------|----------------------------|
|                                    |                     |  |  | Min   | Typ  | Max  |      |                            |
| Power supply<br>current*3          | I <sub>CCLS</sub>   | V <sub>CC</sub><br>(External clock<br>operation) | V <sub>CC</sub> = 5.5 V,<br>F <sub>CL</sub> = 32 kHz,<br>F <sub>MPL</sub> = 16 kHz<br>Sub sleep mode<br>(divided by 2) ,<br>T <sub>A</sub> = + 25 °C | —     | 10   | 81   | μA   |                            |
|                                    | I <sub>CCT</sub>    |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CL</sub> = 32 kHz<br>Watch mode,<br>Main stop mode<br>T <sub>A</sub> = + 25 °C                                    | —     | 4.6  | 27.0 | μA   |                            |
|                                    | I <sub>CCMPLL</sub> |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 4 MHz,<br>F <sub>MP</sub> = 10 MHz<br>Main PLL mode<br>(multiplied by 2.5)                             | —     | 9.3  | 12.5 | mA   | Flash<br>memory<br>product |
|                                    |                     |  |  | —     | 7.0  | 9.5  | mA   | MASK<br>ROM<br>product     |
|                                    |                     |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 6.4 MHz,<br>F <sub>MP</sub> = 16 MHz<br>Main PLL mode<br>(multiplied by 2.5)                           | —     | 14.9 | 20.0 | mA   | Flash<br>memory<br>product |
|                                    |                     |  |  | —     | 11.2 | 15.2 | mA   | MASK<br>ROM<br>product     |
|                                    | I <sub>CCSPLL</sub> |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CL</sub> = 32 kHz,<br>F <sub>MPL</sub> = 128 kHz<br>Sub PLL mode<br>(multiplied by 4)<br>T <sub>A</sub> = + 25 °C | —     | 160  | 400  | μA   |                            |
|                                    | I <sub>CTS</sub>    |  | V <sub>CC</sub> = 5.5 V,<br>F <sub>CH</sub> = 10 MHz<br>Time-base timer<br>mode<br>T <sub>A</sub> = + 25 °C  | —     | 0.40 | 1.10 | mA   |                            |
|                                    | I <sub>CCH</sub>    |  | V <sub>CC</sub> = 5.5 V,<br>Sub stop mode<br>T <sub>A</sub> = + 25 °C  | —     | 3.5  | 20   | μA   |                            |
| LCD division<br>resistance         | R <sub>LCD</sub>    | —  | Between V3 and<br>V <sub>SS</sub>  | —     | 300  | —    | kΩ   |                            |
| COM0 to COM3<br>output impedance   | R <sub>VCOM</sub>   | COM0 to COM3                                     | V1 to V3 = 5.0V  | —     | —    | 5    | kΩ   |                            |
| SEG00 to SEG15<br>output impedance | R <sub>VSEG</sub>   | SEG00 to SEG15                                   |  | —     | —    | 7    | kΩ   |                            |

(Continued)

# MB95150M Series

(Continued)

(V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = −40 °C to +85 °C)

| Parameter         | Sym-<br>bol       | Pin name  | Conditions | Value |     |     | Unit | Remarks |
|-------------------|-------------------|---|------------|-------|-----|-----|------|---------|
|                   |                   |   |            | Min   | Typ | Max |      |         |
| LCD leak current  | I <sub>LCDL</sub> | V0 to V3<br>COM0 to COM3<br>SEG00 to SEG15      | —          | −1    | —   | +1  | μA   |         |
| Input capacitance | C <sub>IN</sub>   | Other than V <sub>CC</sub> ,<br>V <sub>SS</sub> | f = 1 MHz  | —     | 5   | 15  | pF   |         |

\*1 : P10 and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”.  
The switching of the input level can be set by the input level selection register (ILSR) .

\*2 : Product without clock supervisor only

\*3 : • The power-supply current is determined by the external clock. When both low voltage detection option and clock supervisor are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I<sub>LVD</sub>) and current consumption of built-in CR oscillator (I<sub>CSV</sub>) to the specified value.

- Refer to “4. AC Characteristics (1) Clock Timing” for F<sub>CH</sub> and F<sub>CL</sub>.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F<sub>MIP</sub> and F<sub>MPL</sub>.

## 4. AC Characteristics

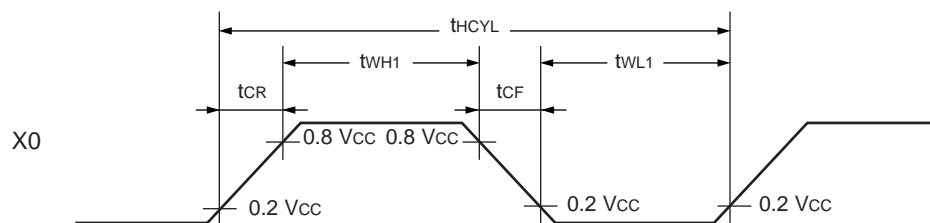
### (1) Clock Timing

(V<sub>CC</sub> = 2.4 V to 5.5 V, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = - 40 °C to + 85 °C)

| Parameter                           | Sym-<br>bol                          | Pin name | Condi-<br>tions | Value |        |       | Unit | Remarks  |
|-------------------------------------|--------------------------------------|----------|-----------------|-------|--------|-------|------|--|
|                                     |                                      |          |                 | Min   | Typ    | Max   |      |  |
| Clock frequency                     | F <sub>CH</sub>                      | X0, X1   | —               | 1.00  | —      | 16.25 | MHz  | When using main oscillation circuit                          |
|                                     |                                      |          |                 | 1.00  | —      | 32.50 | MHz  | When using external clock                                    |
|                                     |                                      |          |                 | 3.00  | —      | 10.00 | MHz  | Main PLL multiplied by 1                                     |
|                                     |                                      |          |                 | 3.00  | —      | 8.13  | MHz  | Main PLL multiplied by 2                                     |
|                                     |                                      |          |                 | 3.00  | —      | 6.50  | MHz  | Main PLL multiplied by 2.5                                   |
|                                     |                                      |          |                 | 3.00  | —      | 4.06  | MHz  | Main PLL multiplied by 4                                     |
|                                     | F <sub>CL</sub>                      | X0A, X1A |                 | —     | 32.768 | —     | kHz  | When using sub oscillation circuit                           |
|                                     |                                      |          |                 | —     | 32.768 | —     | kHz  | When using sub PLL   |
| Clock cycle time                    | t <sub>H CYL</sub>                   | X0, X1   |                 | 61.5  | —      | 1000  | ns   | When using oscillation circuit                               |
|                                     |                                      |          |                 | 30.8  | —      | 1000  | ns   | When using external clock                                    |
|                                     | t <sub>L CYL</sub>                   | X0A, X1A |                 | —     | 30.5   | —     | μs   | When using sub clock   |
| Input clock pulse width             | t <sub>WH1</sub><br>t <sub>WL1</sub> | X0       |                 | 61.5  | —      | —     | ns   | When using external clock<br>Duty ratio is about 30% to 70%. |
|                                     | t <sub>WH2</sub><br>t <sub>WL2</sub> | X0A      |                 | —     | 15.2   | —     | μs   |  |
| Input clock rise time and fall time | t <sub>CR</sub><br>t <sub>CF</sub>   | X0, X0A  |                 | —     | —      | 5     | ns   | When using external clock                                    |

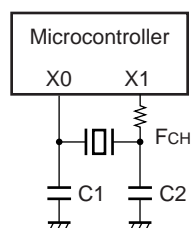
# MB95150M Series

- Input wave form for using external clock (main clock)

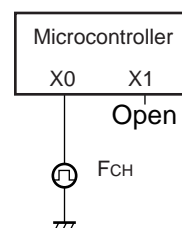


- Figure of main clock input port external connection

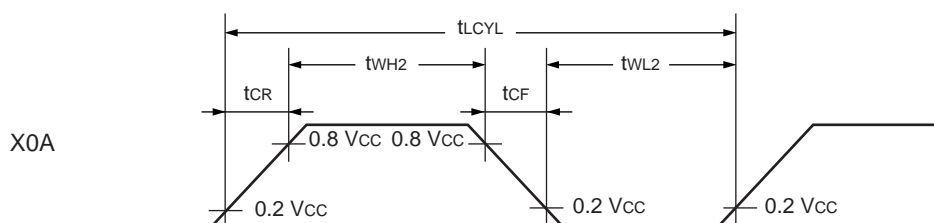
When using a crystal or ceramic oscillator



When using external clock

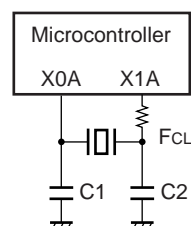


- Input wave form for using external clock (sub clock)

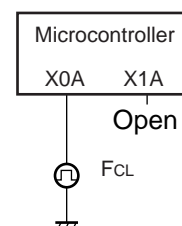


- Figure of sub clock input port external connection

When using a crystal or ceramic oscillator



When using external clock



## (2) Source Clock/Machine Clock

(V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = - 40 °C to + 85 °C)

| Parameter   | Sym-<br>bol       | Pin<br>name | Condi-<br>tions | Value  |     |         | Unit | Remarks  |
|---|-------------------|-------------|-----------------|--------|-----|---------|------|--|
|   |                   |             |                 | Min    | Typ | Max     |      |  |
| Source clock<br>cycle time* <sup>1</sup><br>(Clock before<br>setting division)          | t <sub>SCLK</sub> | —           | —               | 61.5   | —   | 2000    | ns   | When using main clock<br>Min : F <sub>CH</sub> = 8.125 MHz, PLL multiplied by 2<br>Max : F <sub>CH</sub> = 1 MHz, divided by 2 |
|   |                   |             |                 | 7.6    | —   | 61.0    | μs   | When using sub clock<br>Min : F <sub>CL</sub> = 32 kHz, PLL multiplied by 4<br>Max : F <sub>CL</sub> = 32 kHz, divided by 2    |
| Source clock<br>frequency   | F <sub>SP</sub>   | —           | —               | 0.50   | —   | 16.25   | MHz  | When using main clock  |
|   | F <sub>SPL</sub>  | —           |                 | 16.384 | —   | 131.072 | kHz  | When using sub clock   |
| Machine clock<br>cycle time* <sup>2</sup><br>(Minimum<br>instruction<br>execution time) | t <sub>MCLK</sub> | —           | —               | 61.5   | —   | 32000   | ns   | When using main clock<br>Min : F <sub>SP</sub> = 16.25 MHz, no division<br>Max : F <sub>SP</sub> = 0.5 MHz, divided by 16      |
|   |                   |             |                 | 7.6    | —   | 976.5   | μs   | When using sub clock<br>Min : F <sub>SPL</sub> = 131 kHz, no division<br>Max : F <sub>SPL</sub> = 16 kHz, divided by 16        |
| Machine clock<br>frequency  | F <sub>MP</sub>   | —           | —               | 0.031  | —   | 16.250  | MHz  | When using main clock  |
|   | F <sub>MPL</sub>  | —           |                 | 1.024  | —   | 131.072 | kHz  | When using sub clock   |

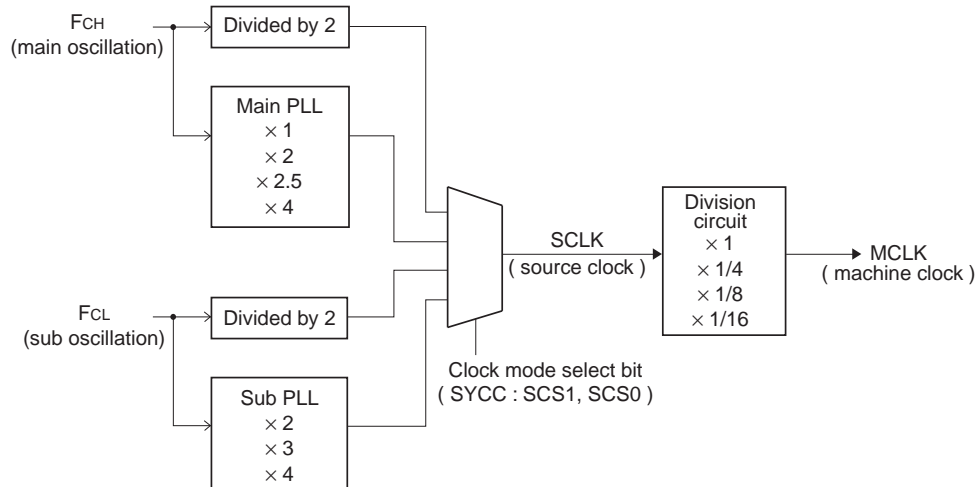
\*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

\*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

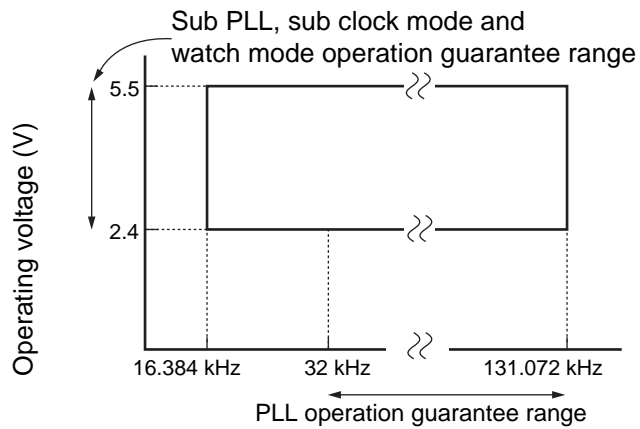
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

### • Outline of clock generation block

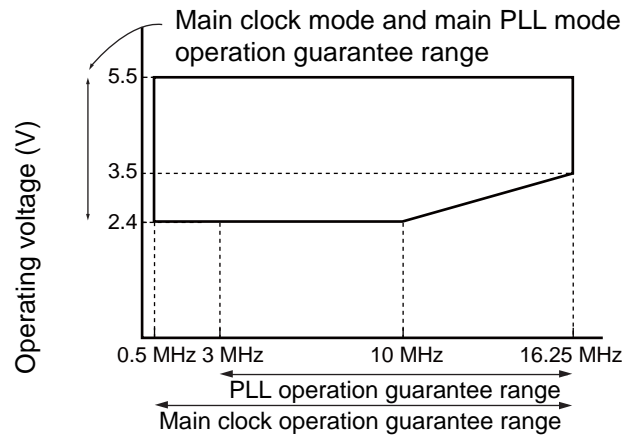


# MB95150M Series

- Operating voltage - Operating frequency (When  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )
  - MB95156M/F156M/F156N/F156J

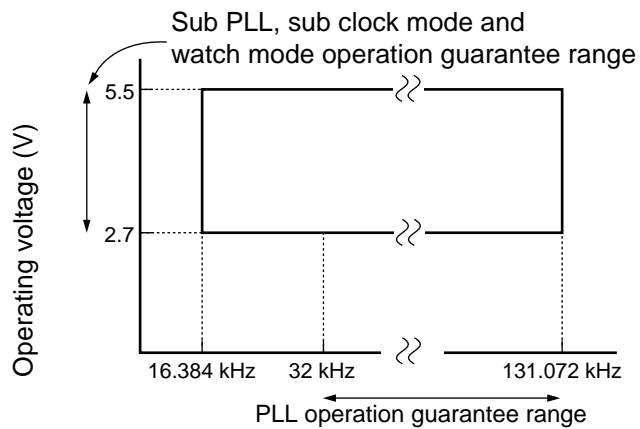


Source clock frequency ( $F_{SPL}$ )

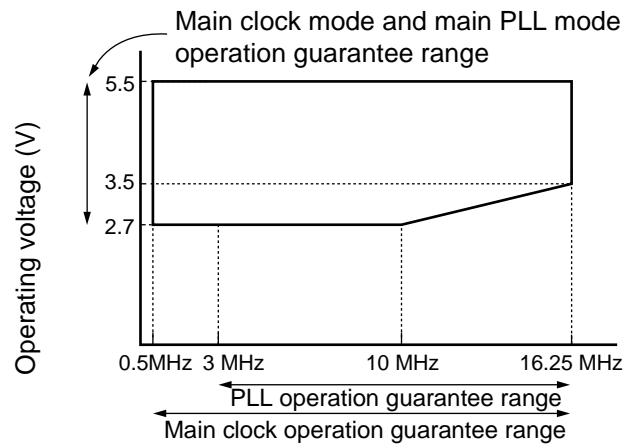


Source clock frequency ( $F_{SP}$ )

- Operating voltage - Operating frequency (When  $T_A = +5\text{ }^{\circ}\text{C}$  to  $+35\text{ }^{\circ}\text{C}$ )
  - MB95FV100D-103

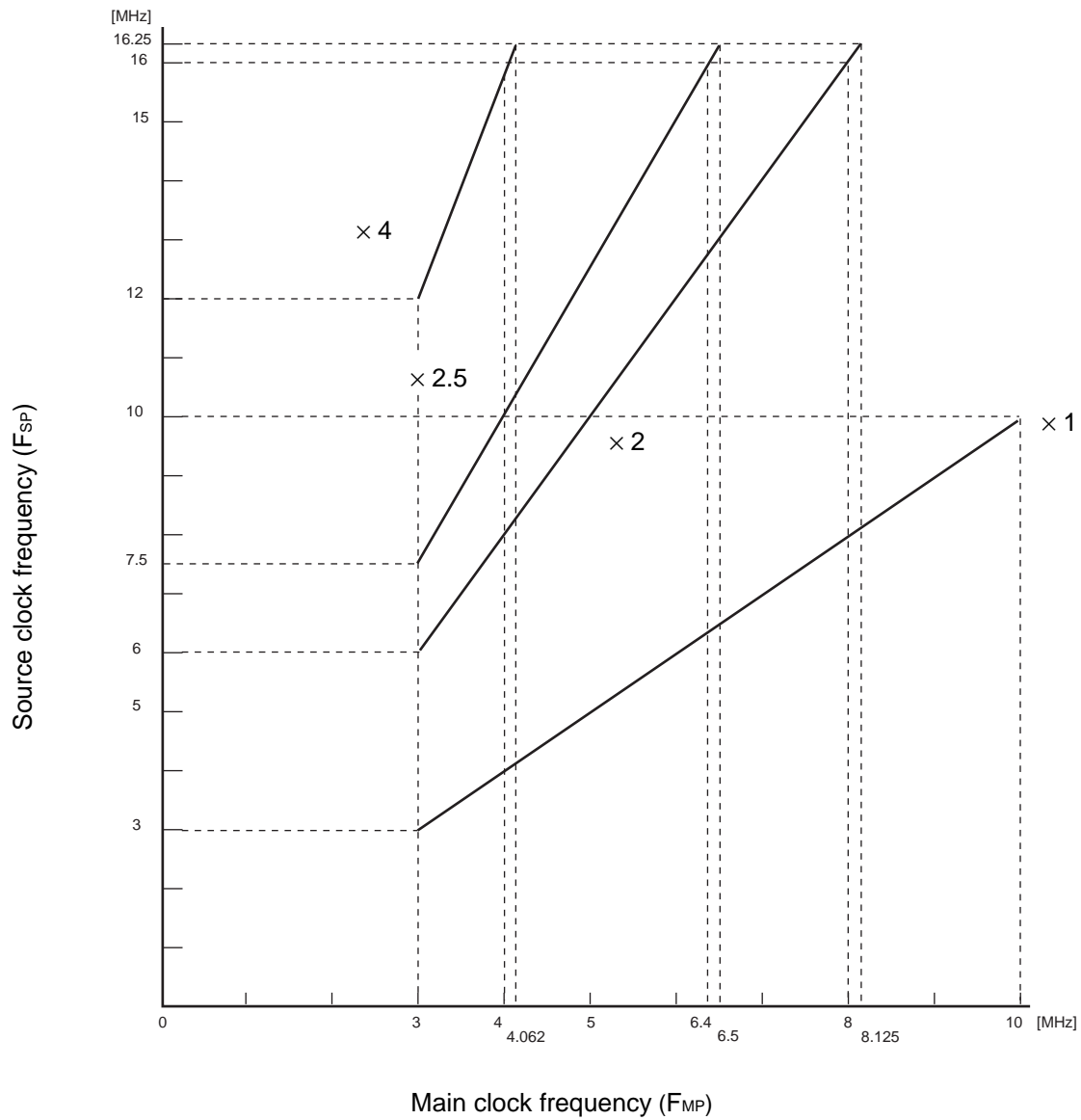


Source clock frequency ( $F_{SPL}$ )



Source clock frequency ( $F_{SP}$ )

• Main PLL operation frequency





# MB95150M Series

## (3) External Reset

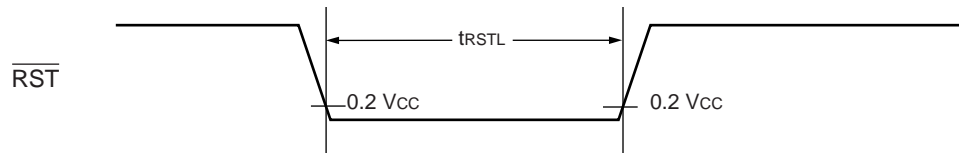
( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

| Parameter                                     | Symbol            | Pin name                | Conditions | Value  |     | Unit          | Remarks  |
|---|-------------------|-------------------------|------------|--|-----|---------------|--|
|   |                   |                         |            | Min  | Max |               |  |
| $\overline{\text{RST}}$ "L" level pulse width | $t_{\text{RSTL}}$ | $\overline{\text{RST}}$ | —          | $2 t_{\text{MCLK}}^{*1}$                           | —   | ns            | At normal operating  |
|   |                   |                         |            | Oscillation time of oscillator <sup>*2</sup> + 100 | —   | $\mu\text{s}$ | At stop mode, sub clock mode, sub sleep mode, and watch mode |
|   |                   |                         |            | 100  | —   | $\mu\text{s}$ | At time-base timer mode                                      |

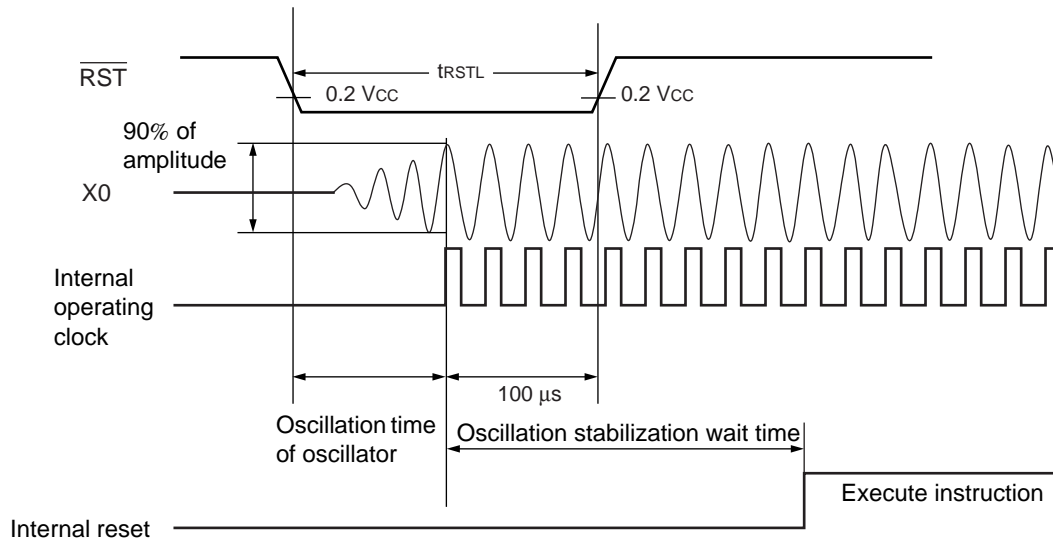
\*1 : Refer to "(2) Source Clock/Machine Clock" for  $t_{\text{MCLK}}$ .

\*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  and several ms. In the external clock, the oscillation time is 0 ms.

- At normal operating



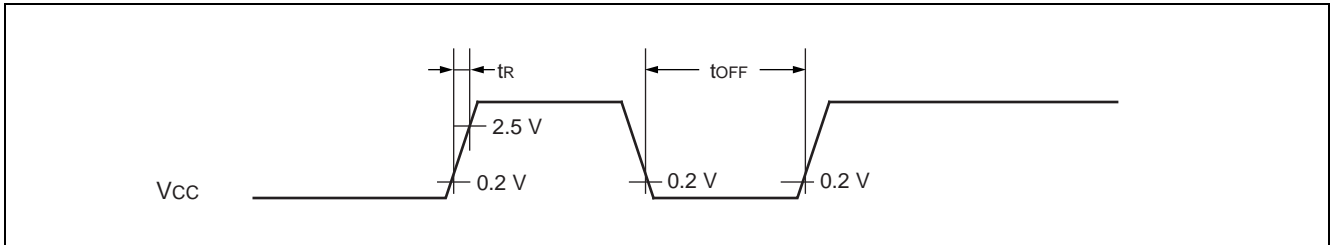
- At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



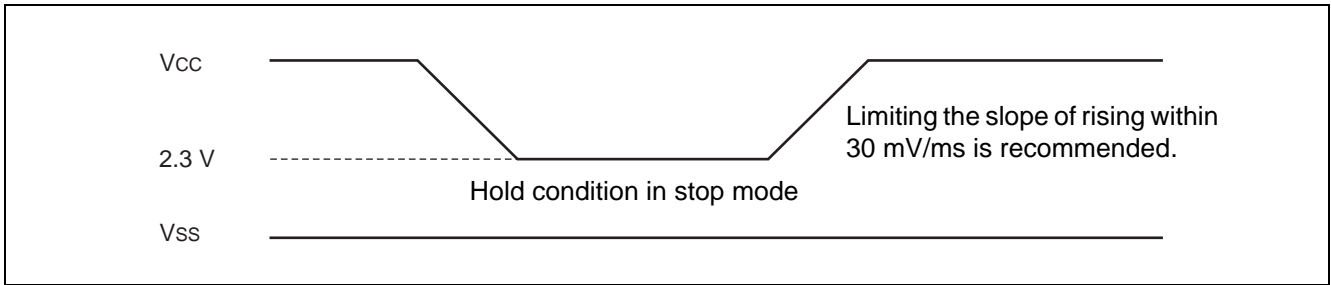
(4) Power-on Reset

(Vss = 0.0 V, TA = - 40 °C to + 85 °C)

| Parameter                | Symbol | Pin name | Conditions | Value |     | Unit | Remarks                     |
|--------------------------|--------|----------|------------|-------|-----|------|-----------------------------|
|                          |        |          |            | Min   | Max |      |                             |
| Power supply rising time | tR     | VCC      | —          | —     | 50  | ms   | Waiting time until power-on |
| Power supply cutoff time | tOFF   |          |            | 1     | —   | ms   |                             |



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.



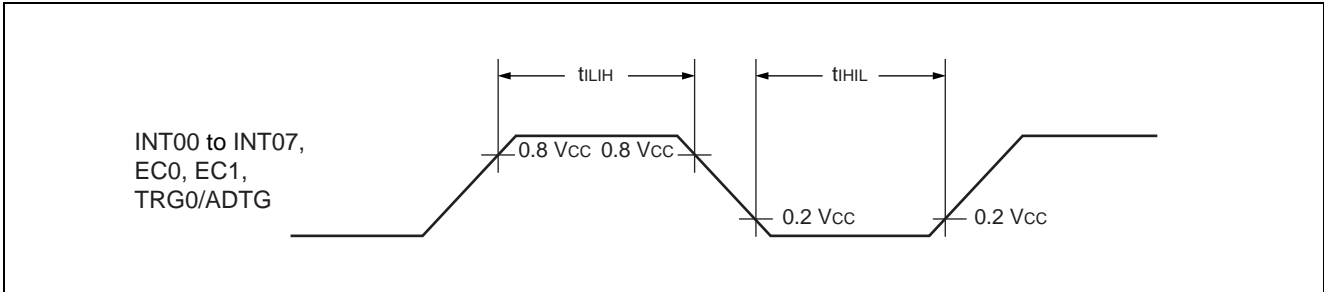
# MB95150M Series

## (5) Peripheral Input Timing

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

| Parameter                        | Symbol           | Pin name                               | Conditions | Value                  |     | Unit |
|----------------------------------|------------------|--|------------|------------------------|-----|------|
|                                  |                  |  |            | Min                    | Max |      |
| Peripheral input "H" pulse width | $t_{\text{LIH}}$ | INT00 to INT07,<br>EC0, EC1, TRG0/ADTG | —          | $2\ t_{\text{MCLK}}^*$ | —   | ns   |
| Peripheral input "L" pulse width | $t_{\text{LIL}}$ |  |            | $2\ t_{\text{MCLK}}^*$ | —   | ns   |

\* : Refer to “ (2) Source Clock/Machine Clock” for  $t_{\text{MCLK}}$ .



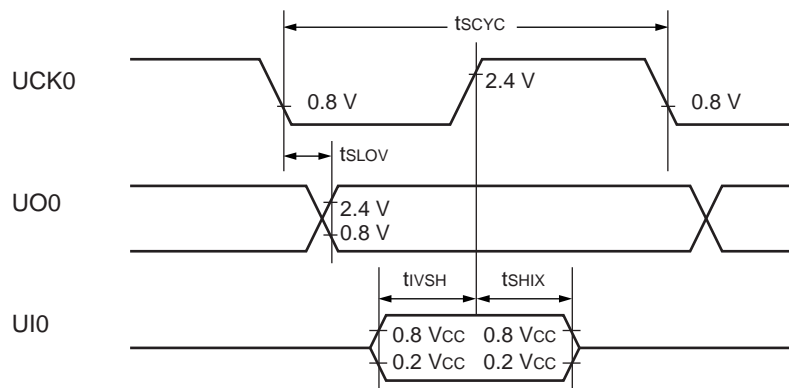
## (6) UART/SIO, Serial I/O Timing

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

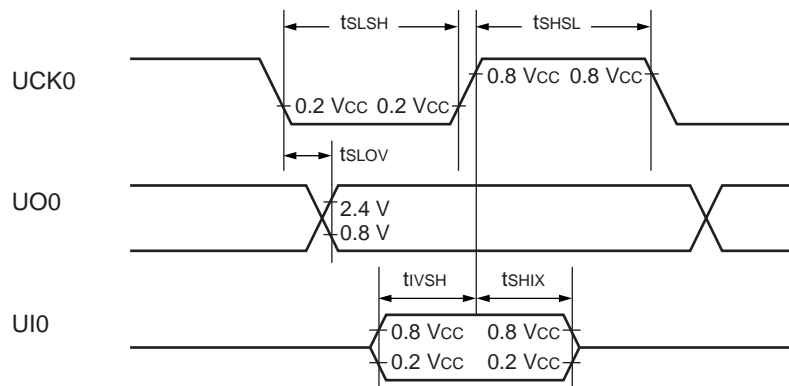
| Parameter                                     | Symbol     | Pin name  | Conditions   | Value          |      | Unit |
|---|------------|-----------|--|----------------|------|------|
|   |            |           |  | Min            | Max  |      |
| Serial clock cycle time                       | $t_{SCYC}$ | UCK0      | Internal clock operation<br>Output pin : $C_L = 80 \text{ pF} + 1\text{TTL}$ . | $4 t_{MCLK}^*$ | —    | ns   |
| UCK $\downarrow \rightarrow$ UO time          | $t_{SLOV}$ | UCK0, UO0 |  | -190           | +190 | ns   |
| Valid UI $\rightarrow$ UCK $\uparrow$         | $t_{IVSH}$ | UCK0, UI0 |  | $2 t_{MCLK}^*$ | —    | ns   |
| UCK $\uparrow \rightarrow$ valid UI hold time | $t_{SHIX}$ | UCK0, UI0 |  | $2 t_{MCLK}^*$ | —    | ns   |
| Serial clock "H" pulse width                  | $t_{SHSL}$ | UCK0      | External clock operation<br>Output pin : $C_L = 80 \text{ pF} + 1\text{TTL}$ . | $4 t_{MCLK}^*$ | —    | ns   |
| Serial clock "L" pulse width                  | $t_{SLSH}$ | UCK0      |  | $4 t_{MCLK}^*$ | —    | ns   |
| UCK $\downarrow \rightarrow$ UO time          | $t_{SLOV}$ | UCK0, UO0 |  | —              | 190  | ns   |
| Valid UI $\rightarrow$ UCK $\uparrow$         | $t_{IVSH}$ | UCK0, UI0 |  | $2 t_{MCLK}^*$ | —    | ns   |
| UCK $\uparrow \rightarrow$ valid UI hold time | $t_{SHIX}$ | UCK0, UI0 |  | $2 t_{MCLK}^*$ | —    | ns   |

\* : Refer to "(2) Source Clock/Machine Clock" for  $t_{MCLK}$ .

### • Internal shift clock mode



### • External shift clock mode



# MB95150M Series

## (7) LIN-UART Timing

Sampling at the rising edge of sampling clock\*1 and prohibited serial clock delay\*2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to + 85 °C)

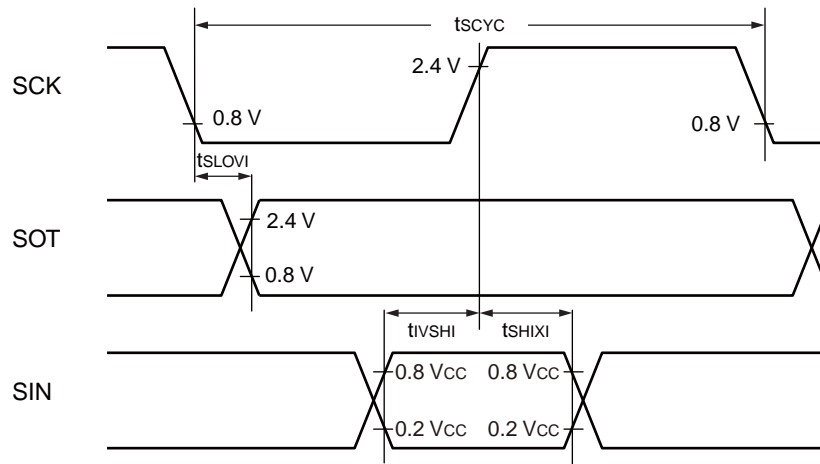
| Parameter                    | Sym-<br>bol        | Pin name | Conditions  | Value                                   |                             | Unit |
|------------------------------|--------------------|----------|---|---|-----------------------------|------|
|                              |                    |          |   | Min                                     | Max                         |      |
| Serial clock cycle time      | t <sub>SCYC</sub>  | SCK      | Internal clock<br>operation output pin :<br>C <sub>L</sub> = 80 pF + 1 TTL. | 5 t <sub>MCLK</sub> *3                  | —                           | ns   |
| SCK ↓ → SOT delay time       | t <sub>SLOVI</sub> | SCK, SOT |   | -95                                     | + 95                        | ns   |
| Valid SIN → SCK ↑            | t <sub>IVSHI</sub> | SCK, SIN |   | t <sub>MCLK</sub> *3 + 190              | —                           | ns   |
| SCK ↑ → valid SIN hold time  | t <sub>SHIXI</sub> | SCK, SIN |   | 0                                       | —                           | ns   |
| Serial clock "L" pulse width | t <sub>SLSH</sub>  | SCK      | External clock<br>operation output pin :<br>C <sub>L</sub> = 80 pF + 1 TTL. | 3 t <sub>MCLK</sub> *3 - t <sub>R</sub> | —                           | ns   |
| Serial clock "H" pulse width | t <sub>SHSL</sub>  | SCK      |   | t <sub>MCLK</sub> *3 + 95               | —                           | ns   |
| SCK ↓ → SOT delay time       | t <sub>SLOVE</sub> | SCK, SOT |   | —                                       | 2 t <sub>MCLK</sub> *3 + 95 | ns   |
| Valid SIN → SCK ↑            | t <sub>IVSHE</sub> | SCK, SIN |   | 190                                     | —                           | ns   |
| SCK ↑ → valid SIN hold time  | t <sub>SHIXE</sub> | SCK, SIN |   | t <sub>MCLK</sub> *3 + 95               | —                           | ns   |
| SCK fall time                | t <sub>F</sub>     | SCK      |   | —                                       | 10                          | ns   |
| SCK rise time                | t <sub>R</sub>     | SCK      |   | —                                       | 10                          | ns   |

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

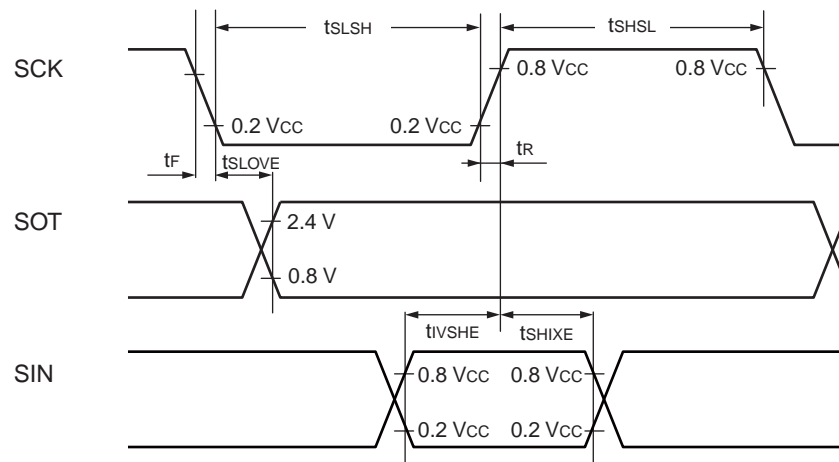
\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to " (2) Source Clock/Machine Clock" for t<sub>MCLK</sub>.

- Internal shift clock mode



- External shift clock mode



# MB95150M Series

**Sampling at the falling edge of sampling clock\*<sup>1</sup> and prohibited serial clock delay\*<sup>2</sup>**  
**(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)**

(V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to + 85 °C)

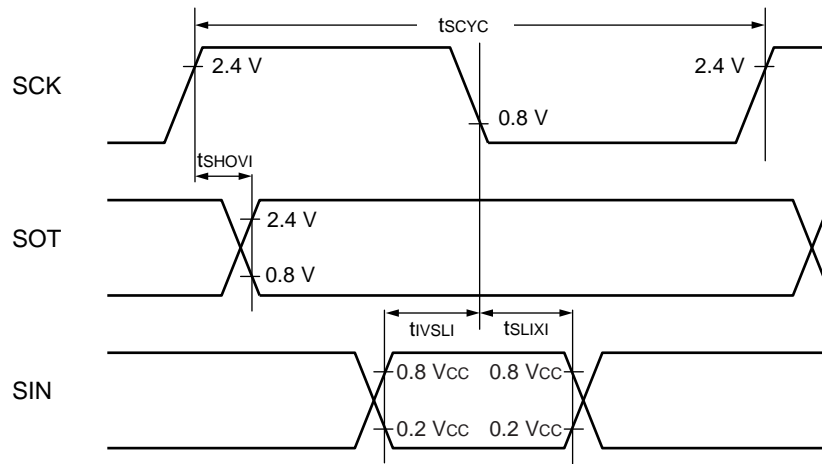
| Parameter                    | Symbol             | Pin name | Conditions  | Value   |   | Unit |
|------------------------------|--------------------|----------|---|---|---|------|
|                              |                    |          |   | Min   | Max                                     |      |
| Serial clock cycle time      | t <sub>SCYC</sub>  | SCK      | Internal clock<br>operation output pin :<br>C <sub>L</sub> = 80 pF + 1 TTL. | 5 t <sub>MCLK</sub> * <sup>3</sup>                  | —                                       | ns   |
| SCK↑→ SOT delay time         | t <sub>SHOVI</sub> | SCK, SOT |   | -95   | + 95                                    | ns   |
| Valid SIN→SCK↓               | t <sub>IVSLI</sub> | SCK, SIN |   | t <sub>MCLK</sub> * <sup>3</sup> + 190              | —                                       | ns   |
| SCK↓→ valid SIN hold time    | t <sub>SLIXI</sub> | SCK, SIN |   | 0   | —                                       | ns   |
| Serial clock "H" pulse width | t <sub>SHSL</sub>  | SCK      | External clock<br>operation output pin :<br>C <sub>L</sub> = 80 pF + 1 TTL. | 3 t <sub>MCLK</sub> * <sup>3</sup> - t <sub>R</sub> | —                                       | ns   |
| Serial clock "L" pulse width | t <sub>SLSH</sub>  | SCK      |   | t <sub>MCLK</sub> * <sup>3</sup> + 95               | —                                       | ns   |
| SCK↑→SOT delay time          | t <sub>SHOVE</sub> | SCK, SOT |   | —   | 2 t <sub>MCLK</sub> * <sup>3</sup> + 95 | ns   |
| Valid SIN→SCK↓               | t <sub>IVSLE</sub> | SCK, SIN |   | 190   | —                                       | ns   |
| SCK↓→ valid SIN hold time    | t <sub>SLIXE</sub> | SCK, SIN |   | t <sub>MCLK</sub> * <sup>3</sup> + 95               | —                                       | ns   |
| SCK fall time                | t <sub>F</sub>     | SCK      |   | —   | 10                                      | ns   |
| SCK rise time                | t <sub>R</sub>     | SCK      |   | —   | 10                                      | ns   |

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

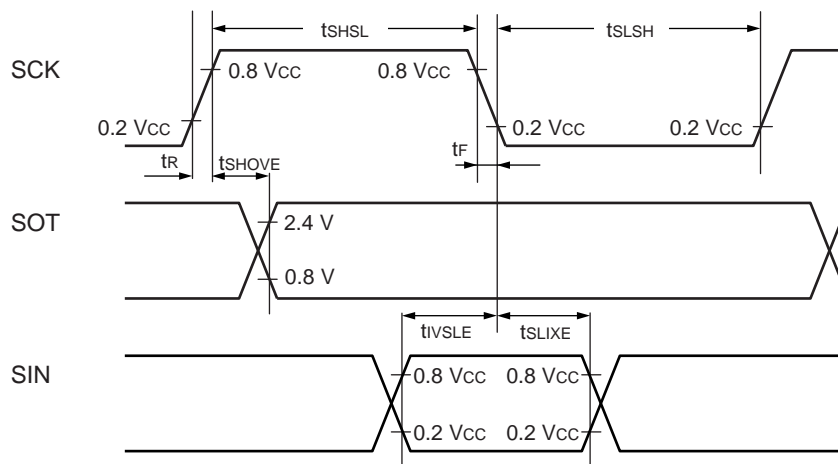
\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to " (2) Source Clock/Machine Clock" for t<sub>MCLK</sub>.

- Internal shift clock mode



- External shift clock mode





# MB95150M Series

Sampling at the rising edge of sampling clock\*<sup>1</sup> and enabled serial clock delay\*<sup>2</sup>  
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

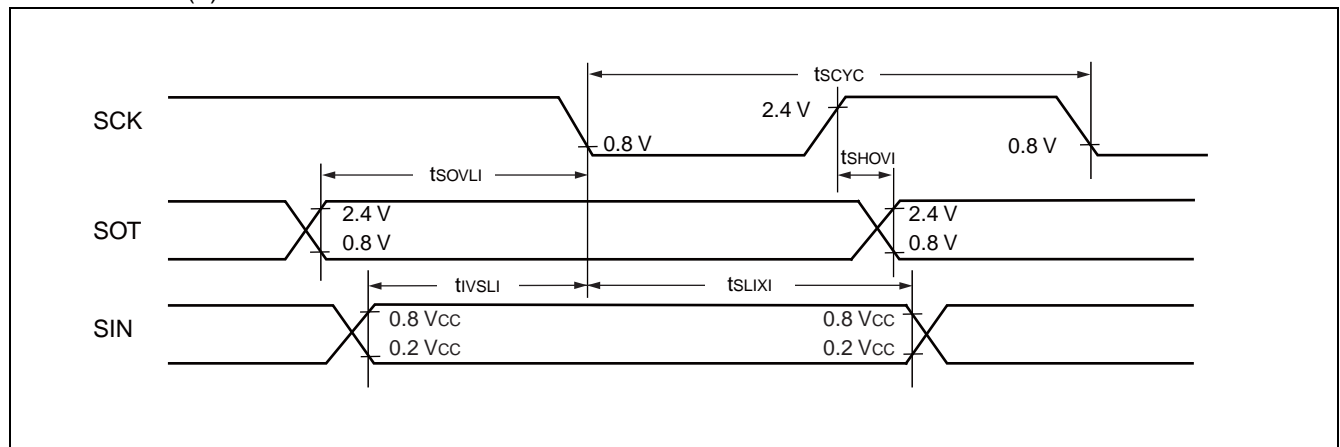
( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

| Parameter                              | Sym-<br>bol | Pin name | Conditions   | Value                 |                   | Unit |
|--|-------------|----------|--|-----------------------|-------------------|------|
|  |             |          |  | Min                   | Max               |      |
| Serial clock cycle time                | $t_{SCYC}$  | SCK      | Internal clock<br>operation output pin :<br>$C_L = 80 \text{ pF} + 1 \text{ TTL.}$ | $5 t_{MCLK}^{*3}$     | —                 | ns   |
| SCK $\uparrow$ → SOT delay time        | $t_{SHOVI}$ | SCK, SOT |  | -95                   | + 95              | ns   |
| Valid SIN→SCK $\downarrow$             | $t_{IVSLI}$ | SCK, SIN |  | $t_{MCLK}^{*3} + 190$ | —                 | ns   |
| SCK $\downarrow$ → valid SIN hold time | $t_{SLIXI}$ | SCK, SIN |  | 0                     | —                 | ns   |
| SOT→SCK $\downarrow$ delay time        | $t_{SOVLI}$ | SCK, SOT |  | —                     | $4 t_{MCLK}^{*3}$ | ns   |

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to “ (2) Source Clock/Machine Clock” for  $t_{MCLK}$ .



**Sampling at the falling edge of sampling clock\*1 and enabled serial clock delay\*2**  
**(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)**

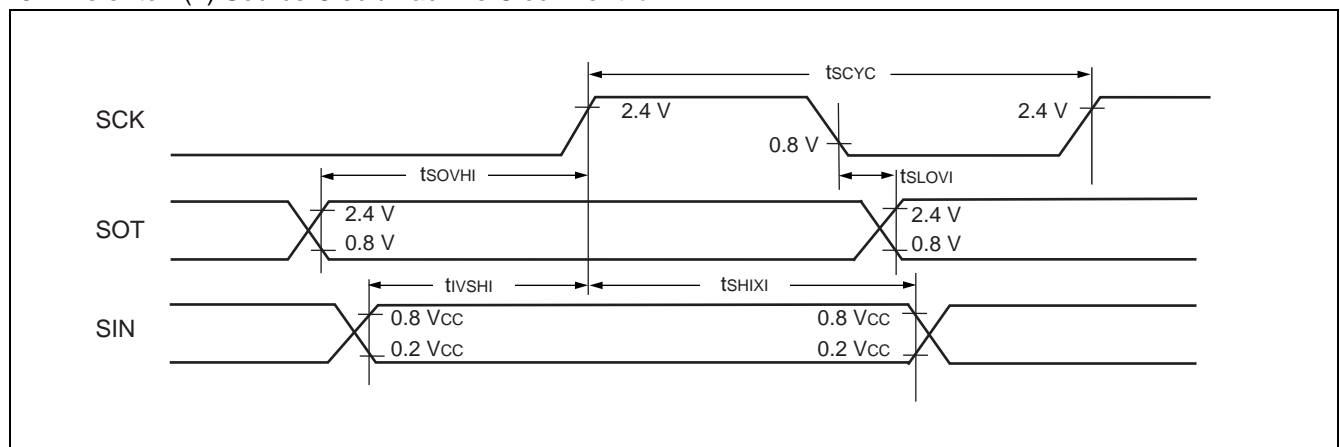
( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

| Parameter                  | Symbol      | Pin name | Conditions   | Value                 |                   | Unit |
|----------------------------|-------------|----------|--|-----------------------|-------------------|------|
|                            |             |          |  | Min                   | Max               |      |
| Serial clock cycle time    | $t_{SCYC}$  | SCK      | Internal clock<br>operation output pin :<br>$C_L = 80 \text{ pF} + 1 \text{ TTL.}$ | $5 t_{MCLK}^{*3}$     | —                 | ns   |
| SCK↓→SOT delay time        | $t_{SLOVI}$ | SCK, SOT |  | −95                   | + 95              | ns   |
| Valid SIN→SCK↑             | $t_{IVSHI}$ | SCK, SIN |  | $t_{MCLK}^{*3} + 190$ | —                 | ns   |
| SCK↑ → valid SIN hold time | $t_{SHIXI}$ | SCK, SIN |  | 0                     | —                 | ns   |
| SOT→SCK↑ delay time        | $t_{SOVHI}$ | SCK, SOT |  | —                     | $4 t_{MCLK}^{*3}$ | ns   |

\*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

\*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

\*3 : Refer to “ (2) Source Clock/Machine Clock” for  $t_{MCLK}$ .

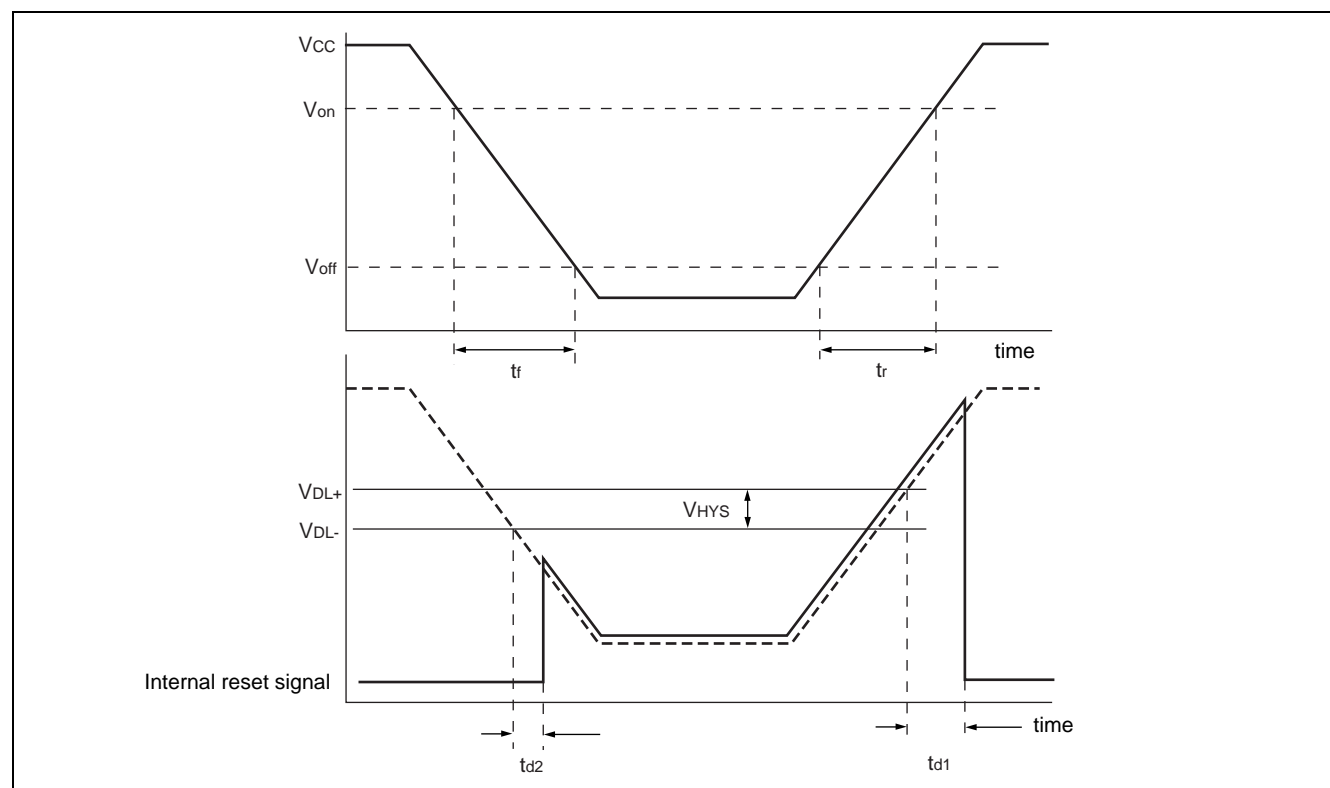


# MB95150M Series

## (8) Low Voltage Detection

(V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

| Parameter   | Symbol           | Condi-<br>tions | Value |      |      | Unit | Remarks   |
|---|------------------|-----------------|-------|------|------|------|---|
|   |                  |                 | Min   | Typ  | Max  |      |   |
| Release voltage   | V <sub>DL+</sub> | —               | 2.52  | 2.70 | 2.88 | V    | At power-supply rise  |
| Detection voltage   | V <sub>DL-</sub> |                 | 2.42  | 2.60 | 2.78 | V    | At power-supply fall  |
| Hysteresis width  | V <sub>HYS</sub> |                 | 70    | 100  | —    | mV   |   |
| Power-supply start voltage                                    | V <sub>off</sub> |                 | —     | —    | 2.3  | V    |   |
| Power-supply end voltage                                      | V <sub>on</sub>  |                 | 4.9   | —    | —    | V    |   |
| Power-supply voltage<br>change time<br>(at power supply rise) | t <sub>r</sub>   |                 | 0.3   | —    | —    | μs   | Slope of power supply that reset<br>release signal generates  |
|   |                  |                 | —     | 3000 | —    | μs   | Slope of power supply that reset<br>release signal generates within<br>rating (V <sub>DL+</sub> )   |
| Power-supply voltage<br>change time<br>(at power supply fall) | t <sub>f</sub>   |                 | 300   | —    | —    | μs   | Slope of power supply that reset<br>detection signal generates                                      |
|   |                  |                 | —     | 300  | —    | μs   | Slope of power supply that reset<br>detection signal generates within<br>rating (V <sub>DL-</sub> ) |
| Reset release delay time                                      | t <sub>d1</sub>  |                 | —     | —    | 400  | μs   |   |
| Reset detection delay time                                    | t <sub>d2</sub>  |                 | —     | —    | 30   | μs   |   |
| Current consumption   | I <sub>LVD</sub> |                 | —     | 38   | 50   | μA   | Current consumption of low<br>voltage detection circuit only  |



## (9) Clock Supervisor Clock

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$ )

| Parameter              | Symbol    | Condi-<br>tions | Value |     |     | Unit          | Remarks   |
|------------------------|-----------|-----------------|-------|-----|-----|---------------|---|
|                        |           |                 | Min   | Typ | Max |               |   |
| Oscillation frequency  | $f_{OUT}$ | —               | 50    | 100 | 200 | kHz           |   |
| Oscillation start time | $t_{wk}$  |                 | —     | —   | 10  | $\mu\text{s}$ |   |
| Current consumption    | $I_{CSV}$ |                 | —     | 20  | 36  | $\mu\text{A}$ | Current consumption of built-in CR oscillator, at 100 kHz oscillation |

# MB95150M Series

## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

( $V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$ )

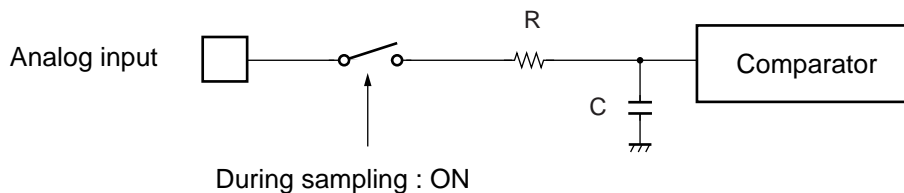
| Parameter                     | Symbol    | Value                      |                            |                            | Unit          | Remarks  |
|-------------------------------|-----------|----------------------------|----------------------------|----------------------------|---------------|--|
|                               |           | Min                        | Typ                        | Max                        |               |  |
| Resolution                    | —         | —                          | —                          | 10                         | bit           |  |
| Total error                   |           | - 3.0                      | —                          | + 3.0                      | LSB           |  |
| Linearity error               |           | - 2.5                      | —                          | + 2.5                      | LSB           |  |
| Differential linear error     |           | - 1.9                      | —                          | + 1.9                      | LSB           |  |
| Zero transition voltage       | $V_{OT}$  | $V_{SS} - 1.5 \text{ LSB}$ | $V_{SS} + 0.5 \text{ LSB}$ | $V_{SS} + 2.5 \text{ LSB}$ | V             |  |
| Full-scale transition voltage | $V_{FST}$ | $V_{CC} - 3.5 \text{ LSB}$ | $V_{CC} - 1.5 \text{ LSB}$ | $V_{CC} + 0.5 \text{ LSB}$ | V             |  |
| Compare time                  | —         | 0.9                        | —                          | 16500                      | $\mu\text{s}$ | $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$   |
|                               |           | 1.8                        | —                          | 16500                      | $\mu\text{s}$ | $4.0 \text{ V} \leq V_{CC} < 4.5 \text{ V}$  |
| Sampling time                 | —         | 0.6                        | —                          | $\infty$                   | $\mu\text{s}$ | $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ ,<br>At external impedance < 5.4 k $\Omega$ |
|                               |           | 1.2                        | —                          | $\infty$                   | $\mu\text{s}$ | $4.0 \text{ V} \leq V_{CC} < 4.5 \text{ V}$ ,<br>At external impedance < 2.4 k $\Omega$    |
| Analog input current          | $I_{AIN}$ | -0.3                       | —                          | + 0.3                      | $\mu\text{A}$ |  |
| Analog input voltage          | $V_{AIN}$ | $V_{SS}$                   | —                          | $V_{CC}$                   | V             |  |

## (2) Notes on Using A/D Converter

### • About the external impedance of analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

#### • Analog input equivalent circuit

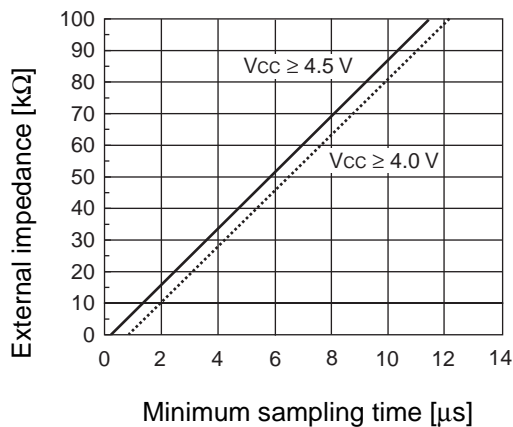


|  | R                    | C           |
|--|----------------------|-------------|
| $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | 2.0 k $\Omega$ (Max) | 16 pF (Max) |
| $4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$    | 8.2 k $\Omega$ (Max) | 16 pF (Max) |

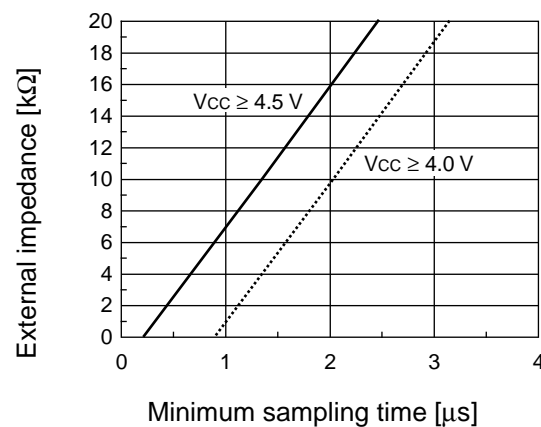
Note : The values are reference values.

#### • The relationship between external impedance and minimum sampling time

(External impedance = 0 k $\Omega$  to 100 k $\Omega$ )



(External impedance = 0 k $\Omega$  to 20 k $\Omega$ )



### • About errors

As  $|V_{CC} - V_{SS}|$  becomes smaller, values of relative errors grow larger.

## (3) Definition of A/D Converter Terms

- Resolution

The level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .

- Linearity error (unit : LSB)

The deviation between the value along a straight line connecting the zero transition point

("00 0000 0000"  $\leftarrow$  "00 0000 0001") of a device and the full-scale transition point

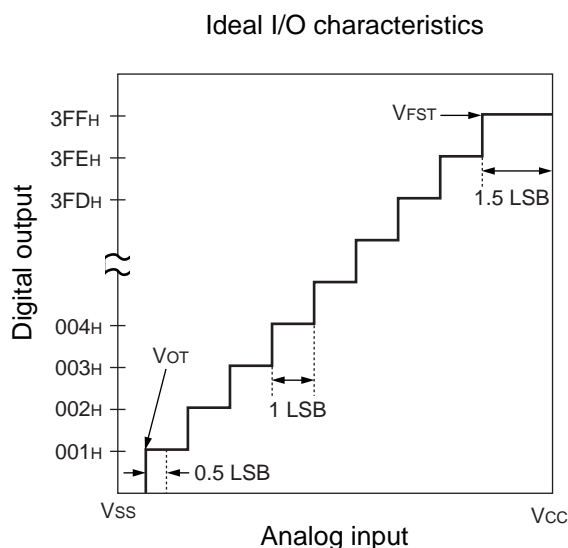
("11 1111 1111"  $\leftarrow$  "11 1111 1110") compared with the actual conversion values obtained.

- Differential linear error (Unit : LSB)

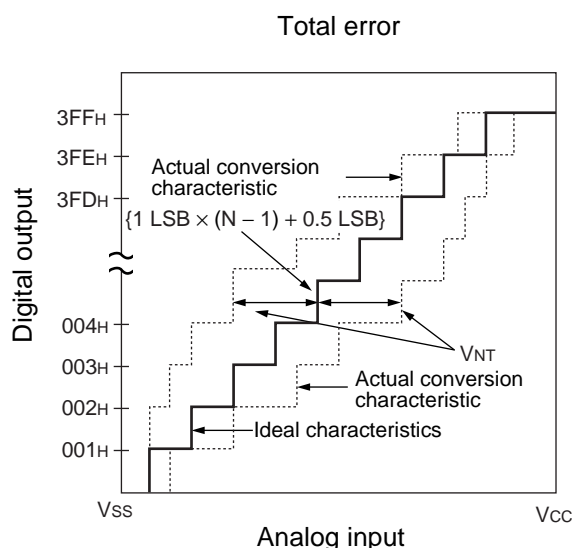
Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

- Total error (unit: LSB)

Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.



$$1 \text{ LSB} = \frac{V_{CC} - V_{SS}}{1024} \text{ (V)}$$



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

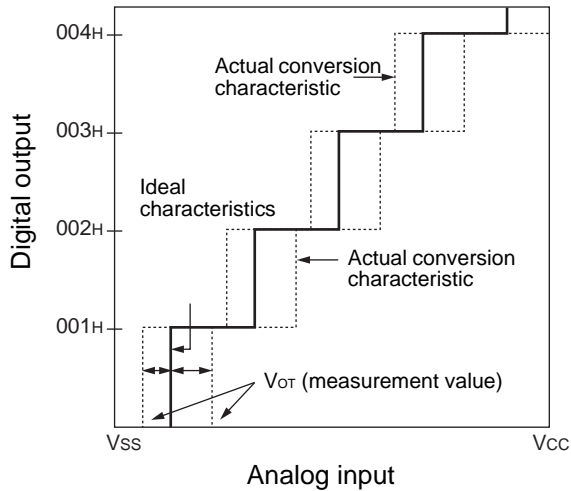
N : A/D converter digital output value

$V_{NT}$  : A voltage at which digital output transits from  $(N - 1)_H$  to  $N_H$

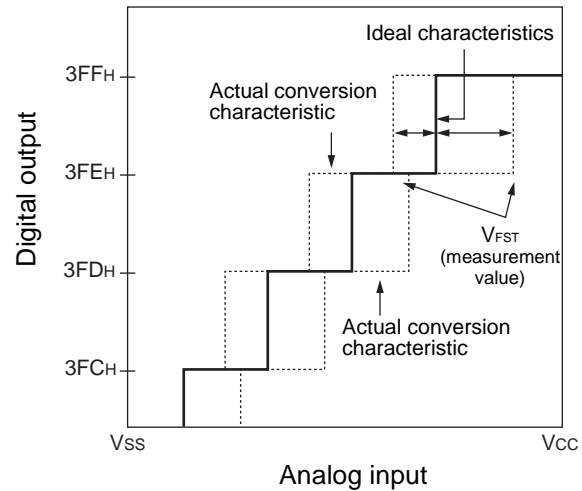
(Continued)

(Continued)

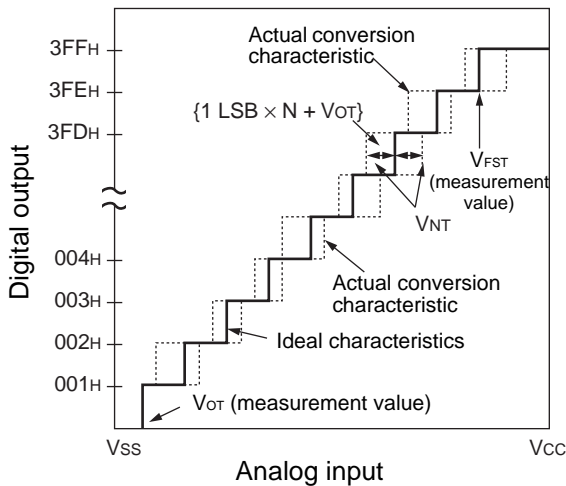
Zero transition error



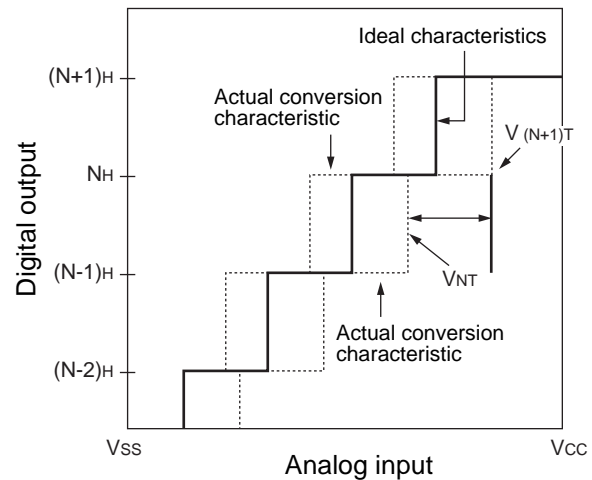
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linearity error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

V<sub>NT</sub> : A voltage at which digital output transits from (N - 1)<sub>H</sub> to N<sub>H</sub>

V<sub>OT</sub> (Ideal value) = V<sub>SS</sub> + 0.5 LSB [V]

V<sub>FST</sub> (Ideal value) = V<sub>CC</sub> - 1.5 LSB [V]



# MB95150M Series

## 6. Flash Memory Program/Erase Characteristics

| Parameter                             | Value            |                   |                    | Unit  | Remarks   |
|---------------------------------------|------------------|-------------------|--------------------|-------|---|
|                                       | Min              | Typ               | Max                |       |   |
| Chip erase time                       | —                | 1.0 <sup>*1</sup> | 15.0 <sup>*2</sup> | s     | Excludes 00 <sub>H</sub> programming prior erasure. |
| Byte programming time                 | —                | 32                | 3600               | μs    | Excludes system-level overhead.                     |
| Erase/program cycle                   | 10000            | —                 | —                  | cycle |   |
| Power supply voltage at erase/program | 4.5              | —                 | 5.5                | V     |   |
| Flash memory data retention time      | 20 <sup>*3</sup> | —                 | —                  | year  | Average T <sub>A</sub> = +85 °C                     |

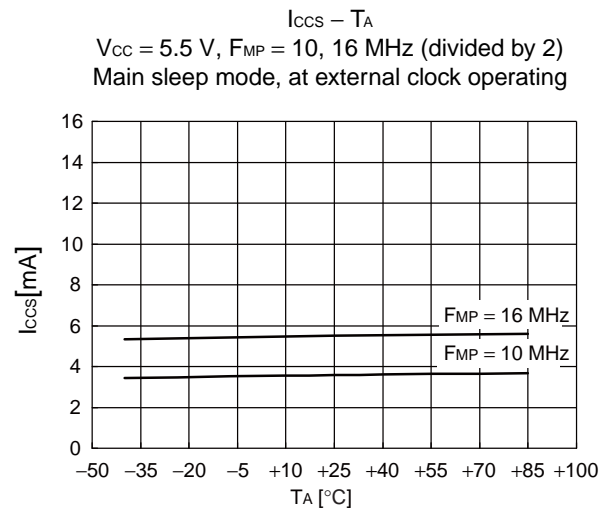
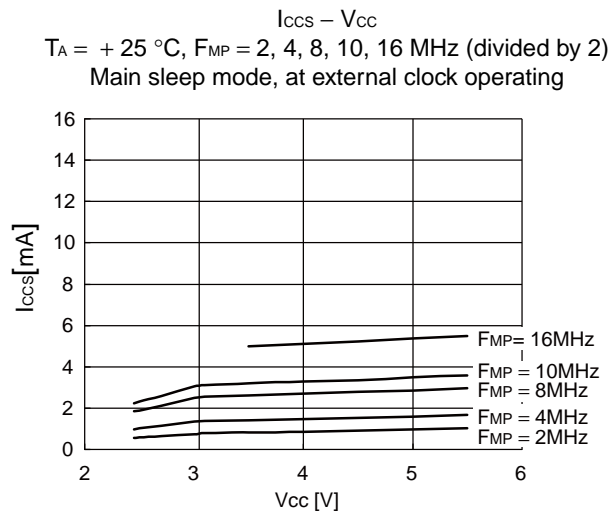
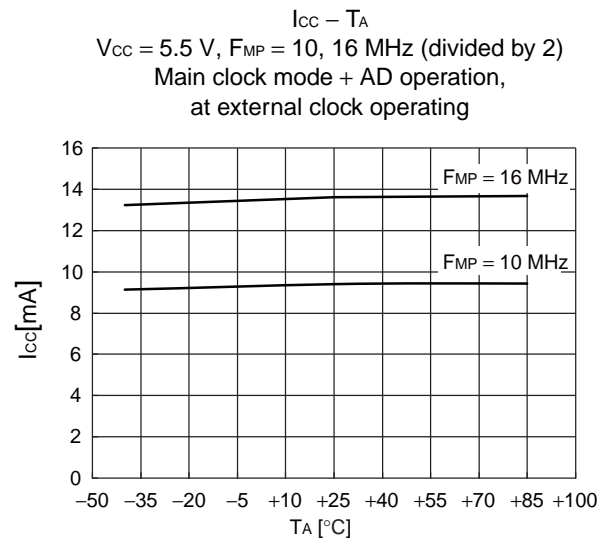
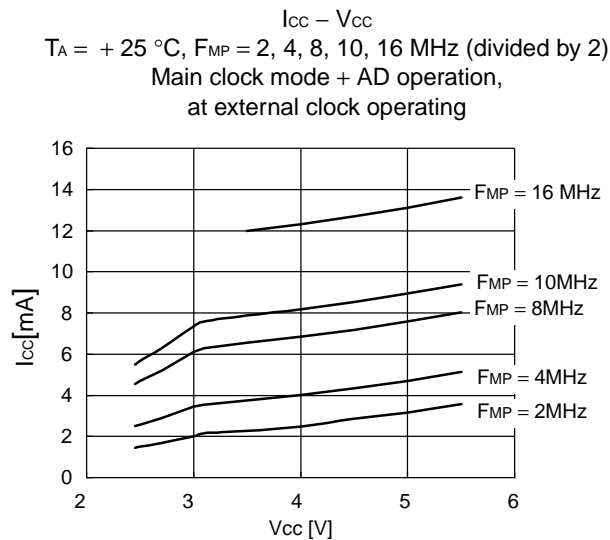
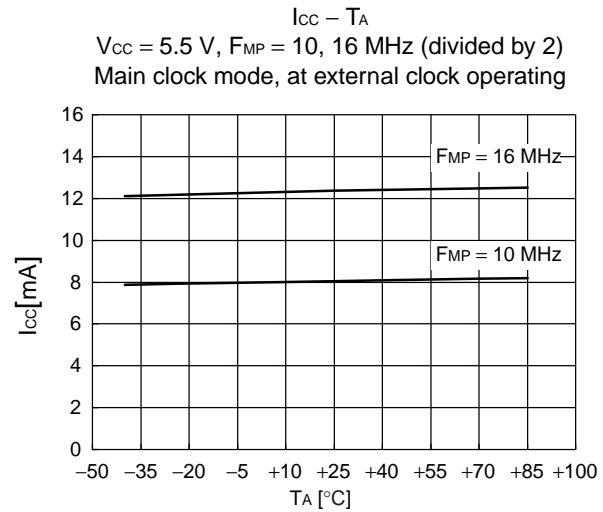
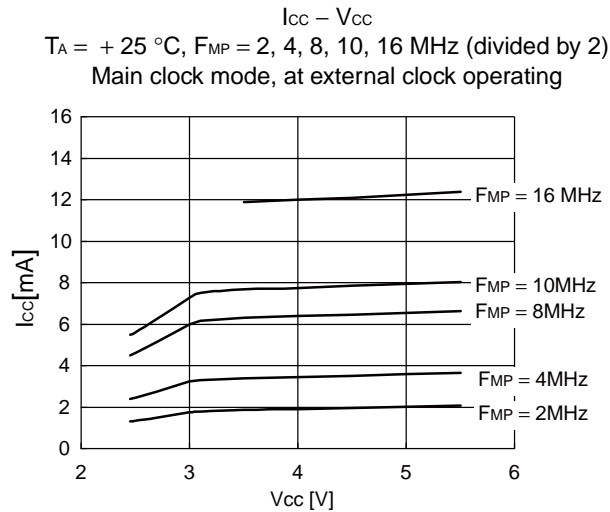
\*1 : T<sub>A</sub> = + 25 °C, V<sub>CC</sub> = 5.0 V, 10000 cycles

\*2 : T<sub>A</sub> = + 85 °C, V<sub>CC</sub> = 4.5 V, 10000 cycles

\*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

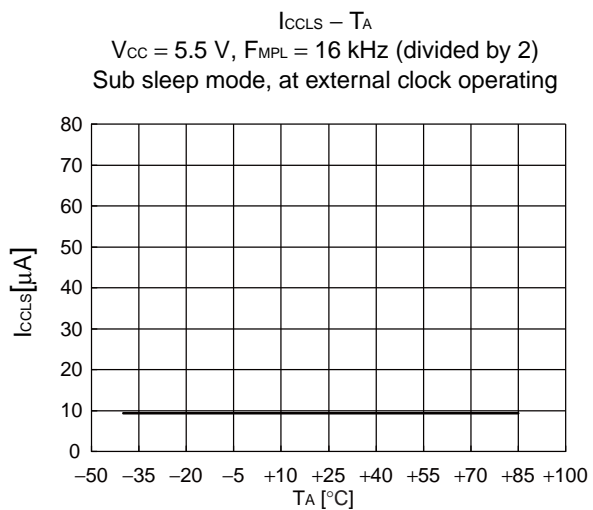
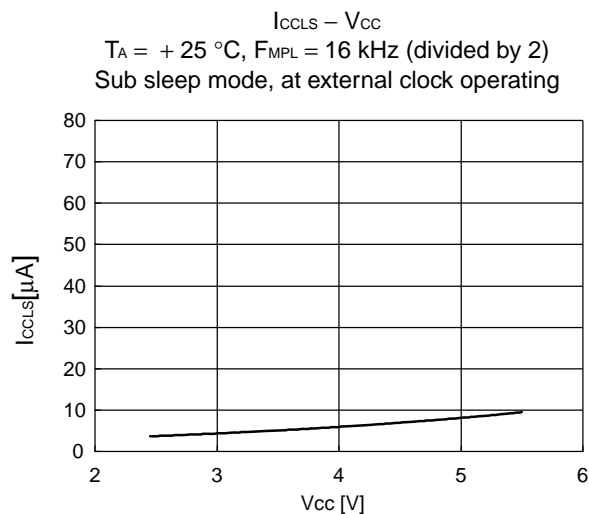
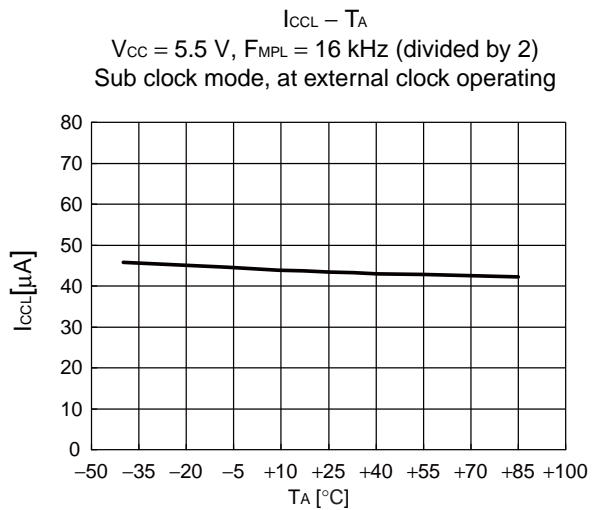
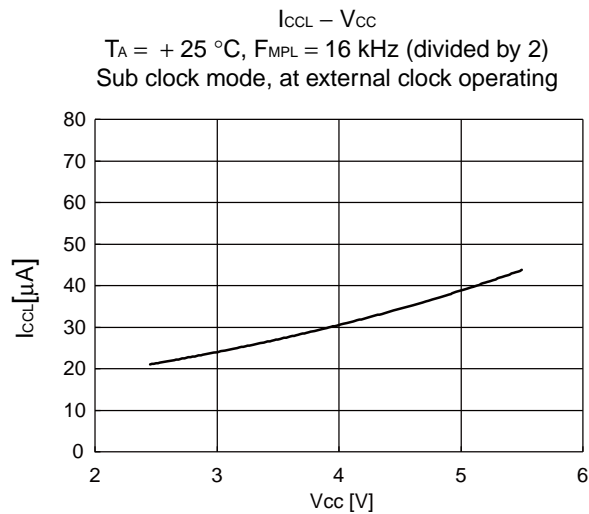
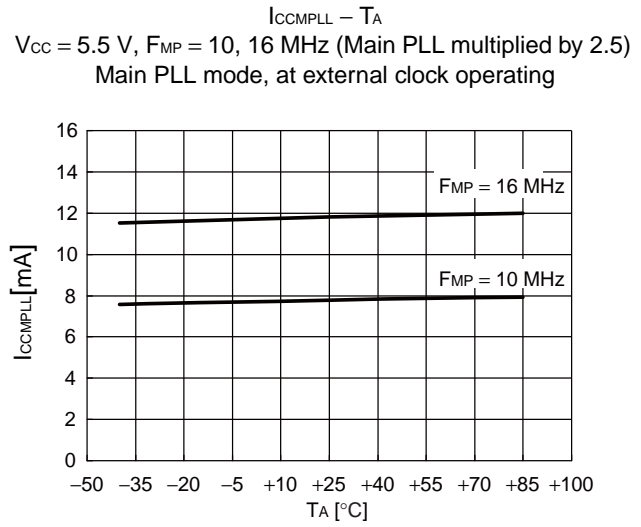
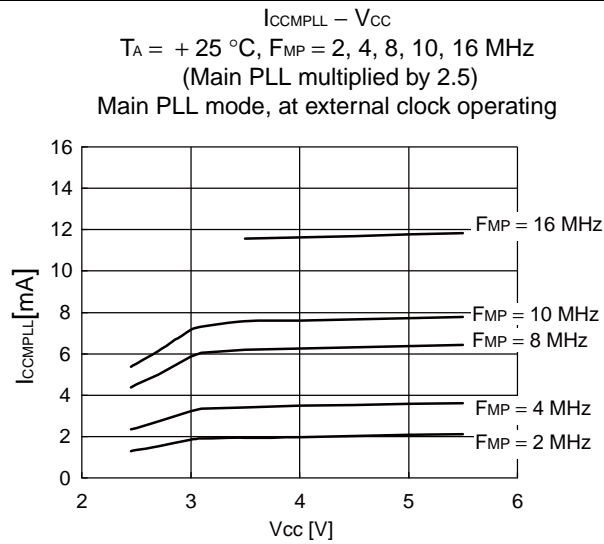
## EXAMPLE CHARACTERISTICS

- Power supply current temperature (Flash memory product)

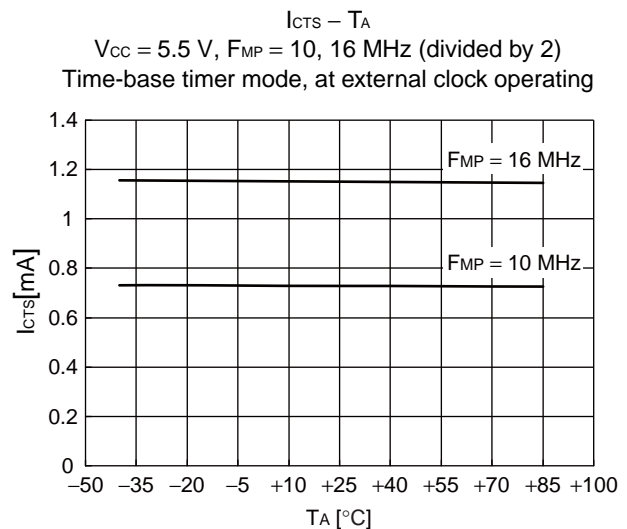
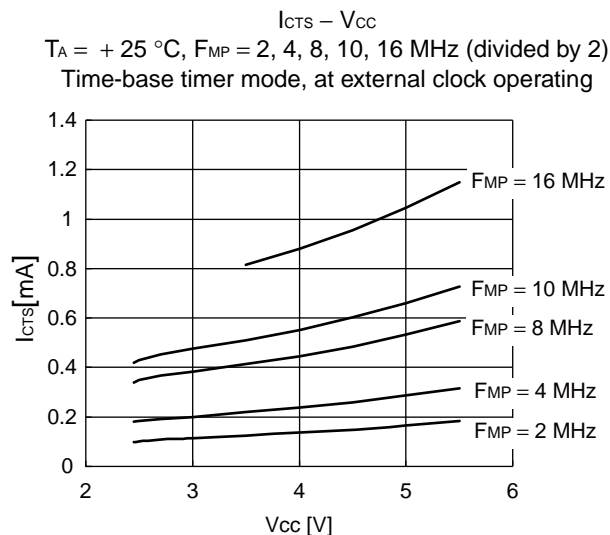
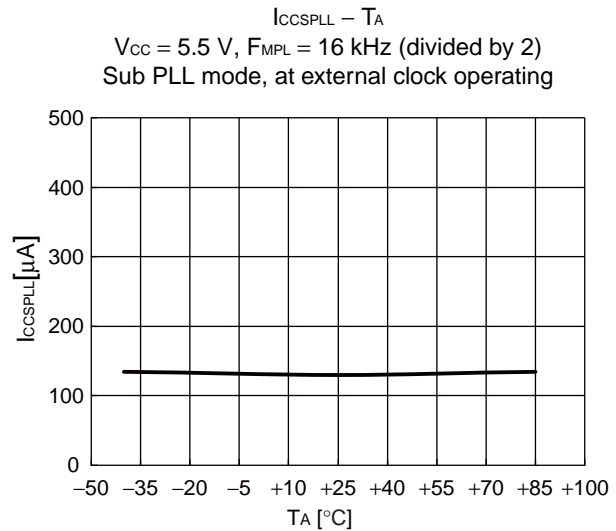
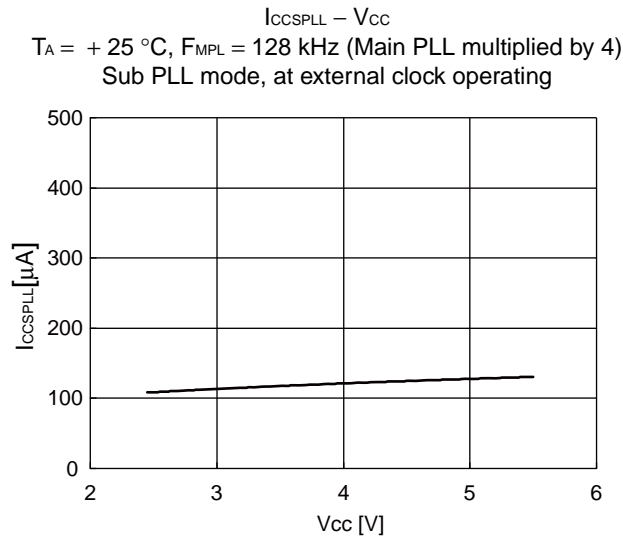
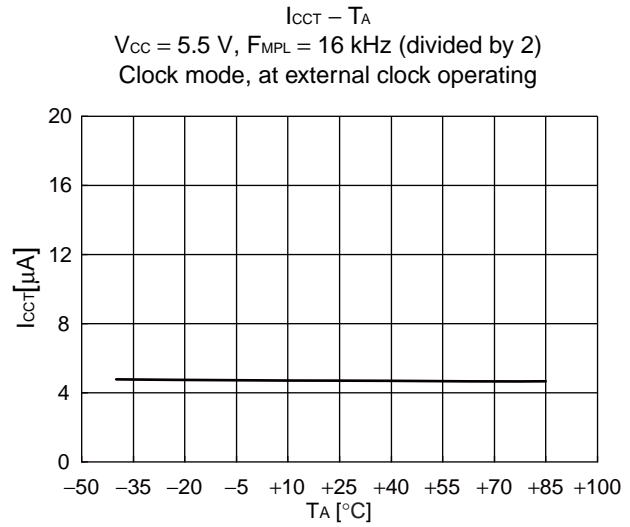
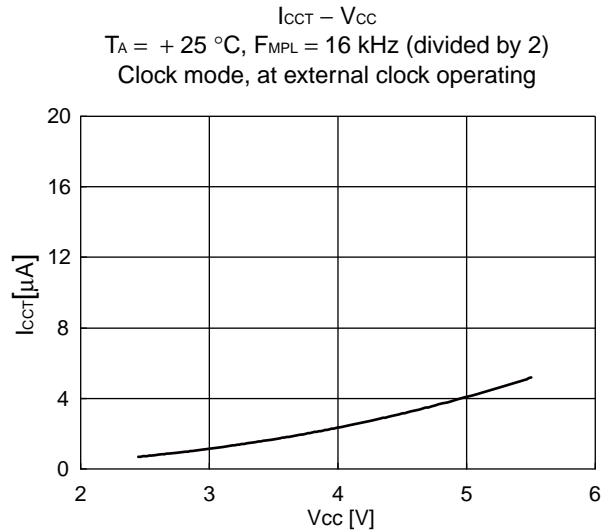


(Continued)

# MB95150M Series

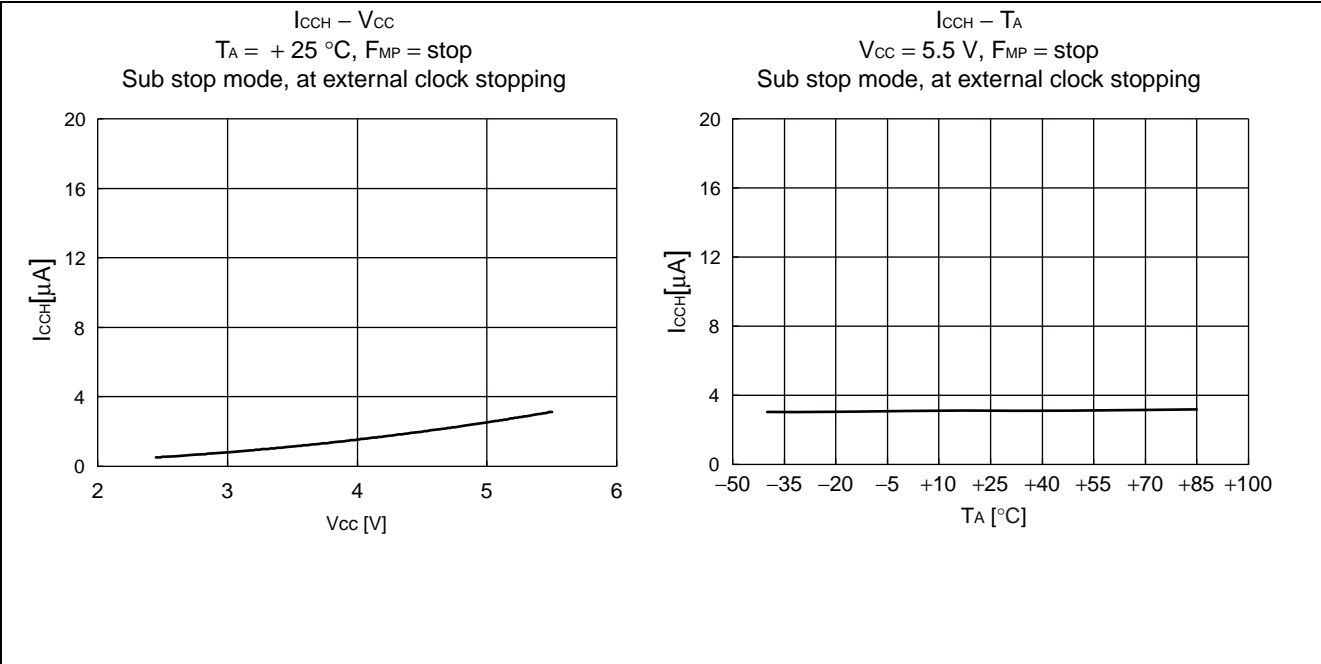


(Continued)



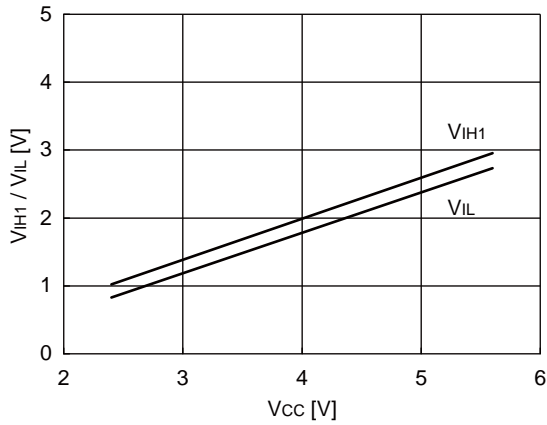
(Continued)

(Continued)

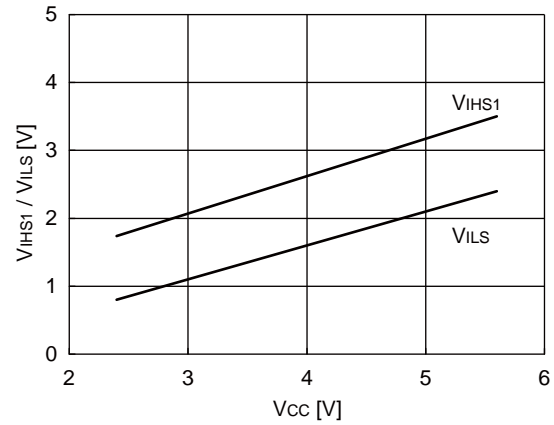


• Input voltage (Flash memory product)

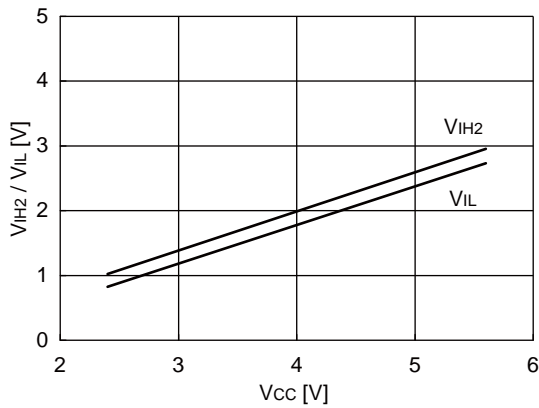
$V_{IH1} - V_{CC}$  and  $V_{IL} - V_{CC}$   
 $T_A = +25^\circ\text{C}$



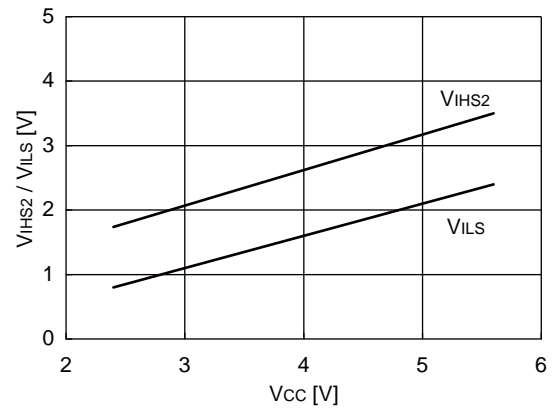
$V_{IHS1} - V_{CC}$  and  $V_{ILS} - V_{CC}$   
 $T_A = +25^\circ\text{C}$



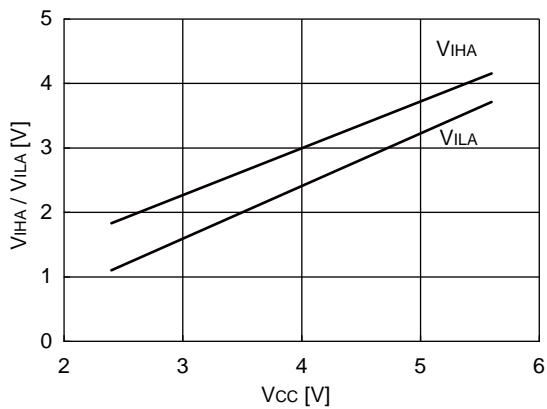
$V_{IH2} - V_{CC}$  and  $V_{IL} - V_{CC}$   
 $T_A = +25^\circ\text{C}$



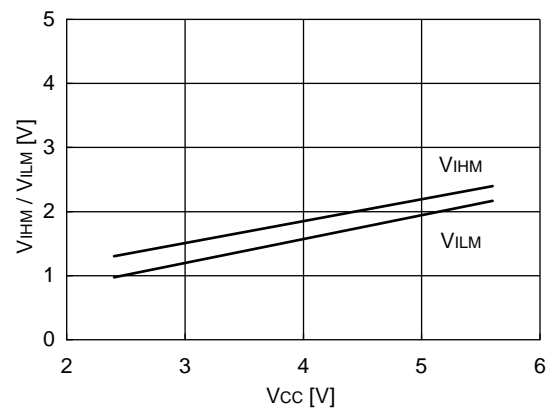
$V_{IHS2} - V_{CC}$  and  $V_{ILS} - V_{CC}$   
 $T_A = +25^\circ\text{C}$



$V_{IHA} - V_{CC}$  and  $V_{ILA} - V_{CC}$   
 $T_A = +25^\circ\text{C}$

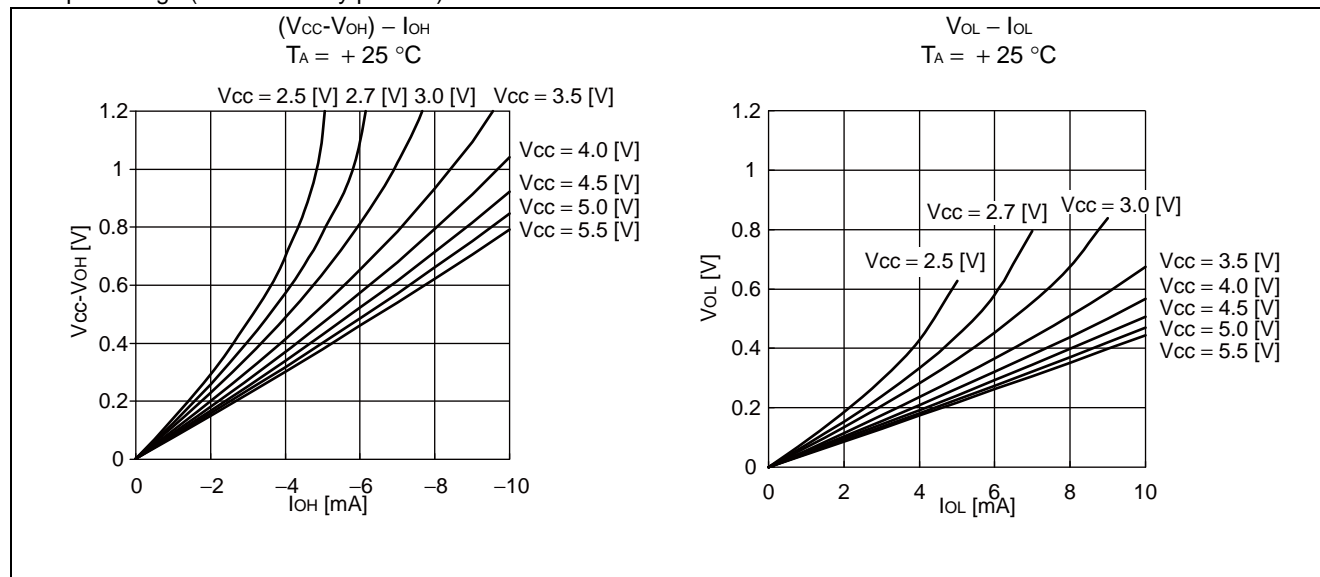


$V_{IHM} - V_{CC}$  and  $V_{ILM} - V_{CC}$   
 $T_A = +25^\circ\text{C}$

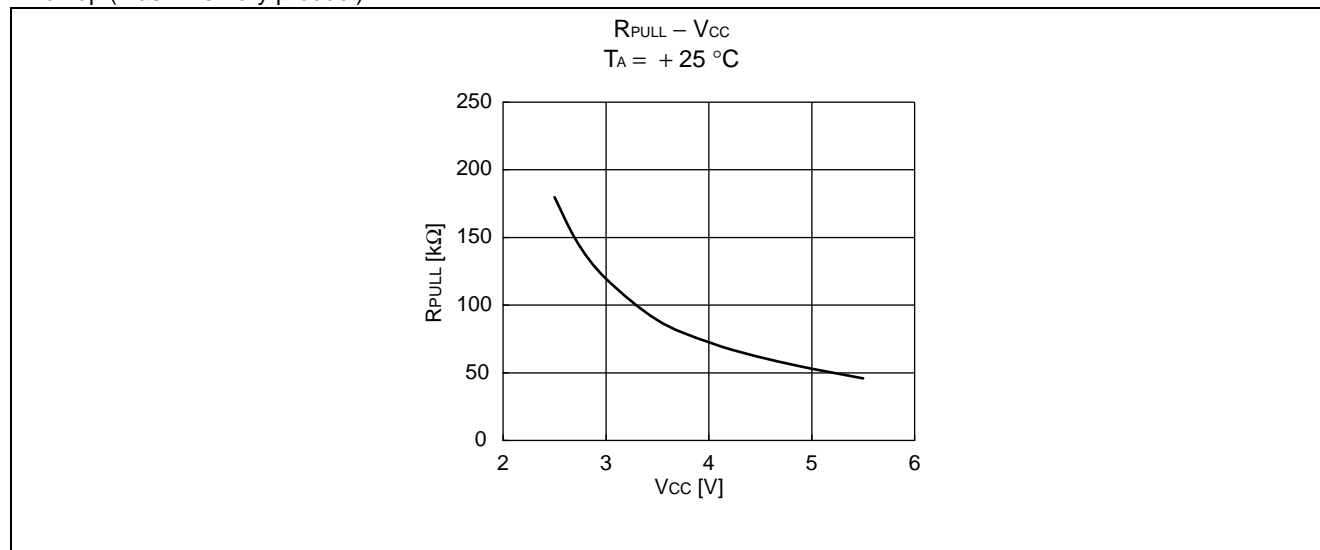


# MB95150M Series

- Output voltage (Flash memory product)



- Pull-up (Flash memory product)



## ■ MASK OPTION

| No. | Part number   | MB95156M  | MB95F156M<br>MB95F156N<br>MB95F156J                                     | MB95FV100D-103   |
|-----|---|---|---|--|
|     | Specifying procedure  | Specify when ordering MASK  | Setting disabled  | Setting disabled   |
| 1   | Clock mode select<br>• Single-system clock mode<br>• Dual-system clock mode                                 | Dual-system clock mode  | Dual-system clock mode  | Changing by the switch on MCU board  |
| 2   | Low voltage detection reset*<br>• With low voltage detection reset<br>• Without low voltage detection reset | Specify when ordering MASK  | Specified by part number  | Changing by the switch on MCU board  |
| 3   | Clock supervisor*<br>• With clock supervisor<br>• Without clock supervisor                                  | Specify when ordering MASK  | Specified by part number  | Changing by the switch on MCU board  |
| 4   | Reset output*<br>• With reset output<br>• Without reset output  | Specify when ordering MASK  | Specified by part number  | MCU board switch sets as follows ;<br>• With clock supervisor : Without reset output<br>• Without clock supervisor : With reset output |
| 5   | Oscillation stabilization wait time   | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$  |

\* : Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

| Part number    | Clock mode select | Low voltage detection reset | Clock supervisor | Reset output |
|----------------|-------------------|-----------------------------|------------------|--------------|
| MB95156M       | Dual-system       | No                          | No               | Yes          |
|                |                   | Yes                         | No               | Yes          |
|                |                   | Yes                         | Yes              | No           |
| MB95F156M      | Dual-system       | No                          | No               | Yes          |
| MB95F156N      |                   | Yes                         | No               | Yes          |
| MB95F156J      |                   | Yes                         | Yes              | No           |
| MB95FV100D-103 | Single-system     | No                          | No               | Yes          |
|                |                   | Yes                         | No               | Yes          |
|                |                   | Yes                         | Yes              | No           |
|                | Dual-system       | No                          | No               | Yes          |
|                |                   | Yes                         | No               | Yes          |
|                |                   | Yes                         | Yes              | No           |

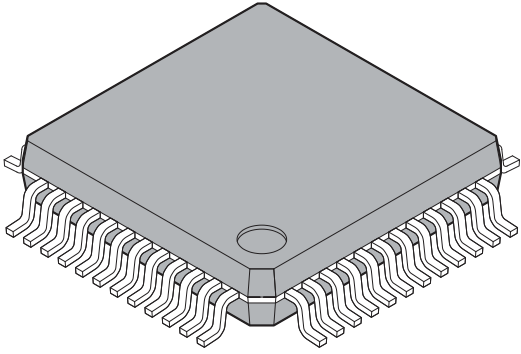


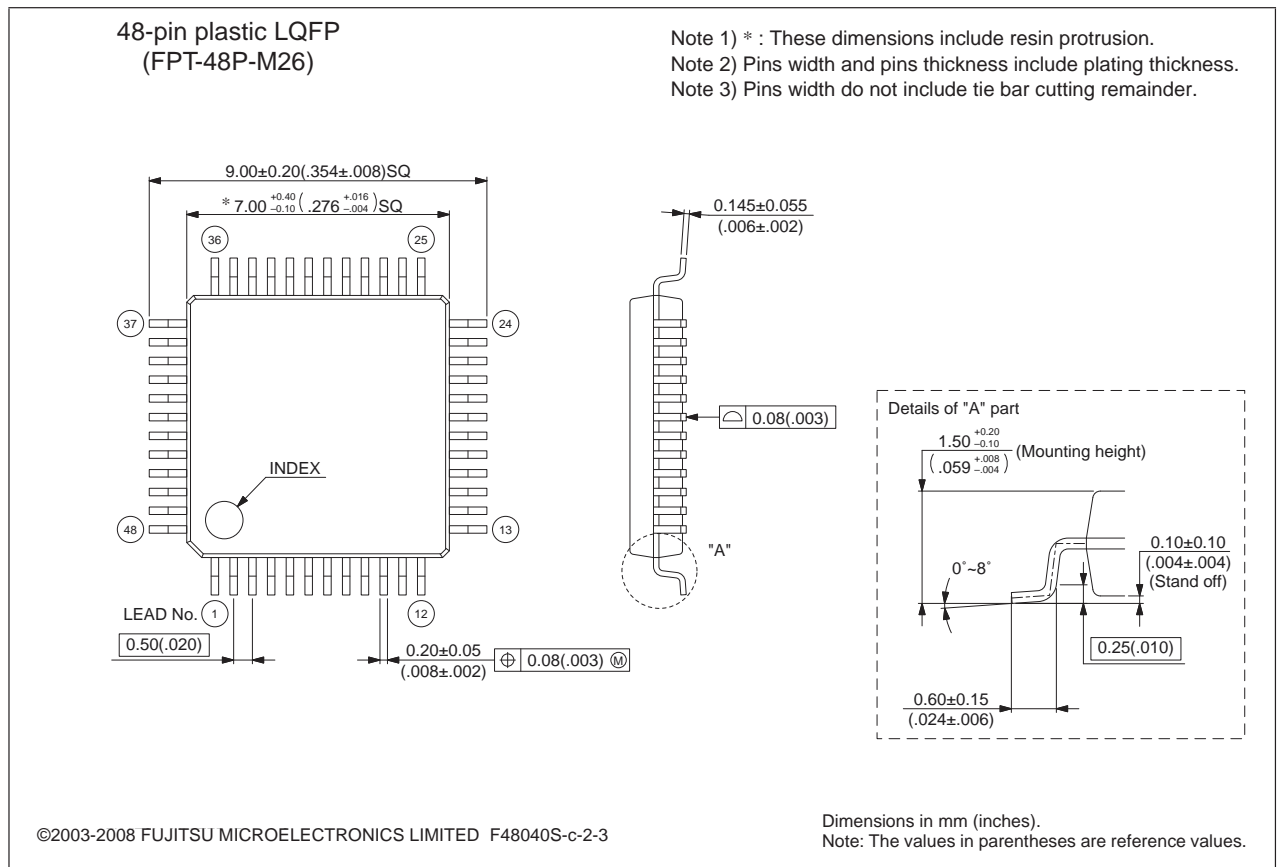
# MB95150M Series

## ■ ORDERING INFORMATION

| Part number   | Package   |
|---|---|
| MB95156MPMT<br>MB95F156MPMT<br>MB95F156NPMT<br>MB95F156JPMT | 48-pin plastic LQFP<br>(FPT-48P-M26)                    |
| MB95156MPMC<br>MB95F156MPMC<br>MB95F156NPMC<br>MB95F156JPMC | 52-pin plastic LQFP<br>(FPT-52P-M01)                    |
| MB2146-303A-E<br>(MB95FV100D-103PBT)                        | MCU board<br>(224-pin plastic PFBGA )<br>(BGA-224P-M08) |

## ■ PACKAGE DIMENSIONS

|   |                                |                    |
|---|--------------------------------|--------------------|
| <p>48-pin plastic LQFP</p>  <p>(FPT-48P-M26)</p> | Lead pitch                     | 0.50 mm            |
|   | Package width × package length | 7 × 7 mm           |
|   | Lead shape                     | Gullwing           |
|   | Sealing method                 | Plastic mold       |
|   | Mounting height                | 1.70 mm MAX        |
|   | Weight                         | 0.17 g             |
|   | Code (Reference)               | P-LFQFP48-7×7-0.50 |

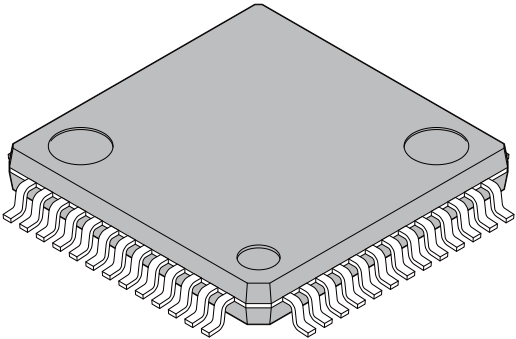


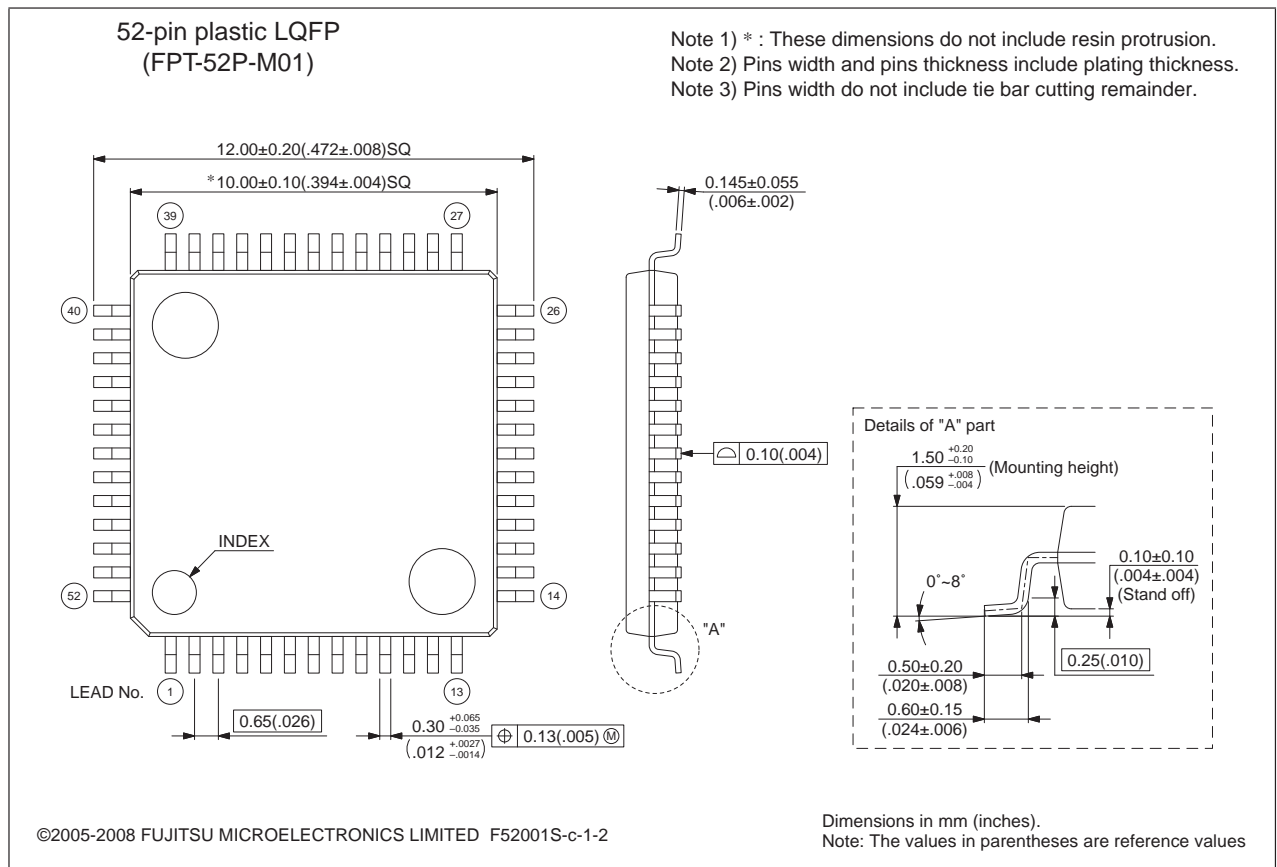
Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

# MB95150M Series

(Continued)

|   |                                |                     |
|---|--------------------------------|---------------------|
| <p>52-pin plastic LQFP</p>  <p>(FPT-52P-M01)</p> | Lead pitch                     | 0.65 mm             |
|   | Package width × package length | 10.0 × 10.0 mm      |
|   | Lead shape                     | Gullwing            |
|   | Sealing method                 | Plastic mold        |
|   | Mounting height                | 1.70 mm Max         |
|   | Code (Reference)               | P-LQFP52-10×10-0.65 |
|   |                                |                     |



Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/package/en-search/>

## ■ MAIN CHANGES IN THIS EDITION

| Page | Section   | Change Results  |
|------|---|---|
| 4    | ■ PRODUCT LINEUP  | Changed the Note.<br>(MB2146-303A → MB2146-303A-E)        |
| 13   | ■ HANDLING DEVICES  | Added the item of “• Serial communication”.               |
| 29   | ■ ELECTRICAL CHARACTERISTICS<br>2. Recommended Operating Conditions | Changed *2 its table footnote.                            |
| 64   | ■ ORDERING INFORMATION  | Changed the part number.<br>(MB2146-303A → MB2146-303A-E) |

The vertical lines marked in the left side of the page show the changes.

# MB95150M Series

## FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,  
Shinjuku-ku, Tokyo 163-0722, Japan  
Tel: +81-3-5322-3347 Fax: +81-3-5322-3387  
<http://jp.fujitsu.com/fml/en/>

*For further information please contact:*

### North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.  
1250 E. Arques Avenue, M/S 333  
Sunnyvale, CA 94085-5401, U.S.A.  
Tel: +1-408-737-5600 Fax: +1-408-737-5999  
<http://www.fma.fujitsu.com/>

### Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.  
151 Lorong Chuan,  
#05-08 New Tech Park 556741 Singapore  
Tel : +65-6281-0770 Fax : +65-6281-0220  
<http://www.fmal.fujitsu.com/>

### Europe

FUJITSU MICROELECTRONICS EUROPE GmbH  
Pittlerstrasse 47, 63225 Langen, Germany  
Tel: +49-6103-690-0 Fax: +49-6103-690-122  
<http://emea.fujitsu.com/microelectronics/>

### FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),  
Shanghai 200002, China  
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605  
<http://cn.fujitsu.com/fmc/>

### Korea

FUJITSU MICROELECTRONICS KOREA LTD.  
206 Kosmo Tower Building, 1002 Daechi-Dong,  
Gangnam-Gu, Seoul 135-280, Republic of Korea  
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111  
<http://kr.fujitsu.com/fmk/>

### FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,  
Tsimshatsui, Kowloon, Hong Kong  
Tel : +852-2377-0226 Fax : +852-2376-3269  
<http://cn.fujitsu.com/fmc/en/>

Specifications are subject to change without notice. For further information please contact each office.

### All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.