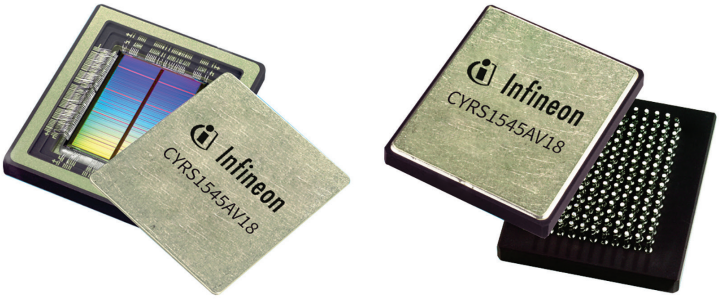
Product brief

72-Mbit QDR® II+ Synchronous SRAM

Infineon's HiRel memories perform in the most extreme environments



Overview

Infineon's 72-Mbit QDR® II+, CYRS154X series, are Synchronous (Sync) SRAMs designed with Infineon's patented RadStop™ Technology that are optimized for space as well as other harsh environment applications. The 72-Mbit QDR® II+ SRAMs are available in x18/x36 and two-word/four-word data bus configurations and designed with a DDR address bus scheme. The QDR™ II+ SRAM architecture provides a low latency and random memory access capability needed for high performance applications such as external cache memories. Infineon's QDR™ II+ Sync SRAM family provides the Random Transaction Rate (RTR) necessary to break system bottlenecks.

Infineon's state-of-the art RadStop™ Technology is radiation hardened through propriety design and process hardening techniques. Our synchronous SRAM devices are of the highest reliability and performance and well suited for applications for payload processing and reconfigurable computing platforms for extreme environments. Well suited for radar implementations and image processing applications due to the low latency and random memory access capability.

Infineon's radiation-hardened memories are QML-V certified, meeting the reliability and lifecycle demands of space applications. Our RadStop™ memory solutions enhance overall system computing limits while providing Size, Weight, and Power (SWaP) benefits and greater design flexibility.

www.infineon.com/cypress

Key benefits

Certified reliability
- DLAM QML-V
- QCI, datapacks
- RHA, WLAT

Ultimate radiation
- >300 Krad TID
- >120 LET SEL immunity
- < $1.34e^{-7}$ Err/bit.day

Product features
- 250 MHz max frequency
- Concurrent R/W
- Throughput up to 36 Gbps
- Low latency (2 cycles)
- HSTL I/O
- SWaP optimized CCGA package with Six Sigma columns

Key applications
- Radar (SAR, LiDAR)
- On-orbit image processing

Differentiated memory portfolio
- Performance
- Density
- Reliability
- Longevity

72-Mbit QDR® II+ Synchronous SRAM

Infineon's HiRel memories perform in the most extreme environments

Key features

- 250 MHz/36 Gbps maximum frequency of operation/throughput
- 4-Mbit x18, 2-Mbit x36 bus-width configurations in two-word or four-word burst mode
- -55 to +125°C military temperature grade
- Two independent unidirectional data ports for concurrent read/write transactions
- Double Data Rate (DDR) address port
- Output impedance matching input (ZQ) matches the device outputs to system data bus impedance
- Memory core bit-interleaving to eliminate multi-bit errors
- 1.5 – 1.8 V (HSTL) I/O signaling standards
- Controller RTL IP cores with embedded EDAC available for Xilinx and Microchip FPGAs
- QML-V qualified

Technical support

Infineon datasheet

72-Mbit 2-Burst SRAMs with RadStop™
72-Mbit 4-Burst SRAMs with RadStop™

DLAM datasheet

5962F11201
5962F11202

EcoSystem support

Mezzanine QDRII+ Board

Parts list

Density	Description	Infineon P/N DLAM P/N	Operating temperature [°C]	Qual Level	TID[1]	SEL[2]	SEU[3]	SEFI[4]	PD[5]
72-Mbit	QDR™ II+ x18 burst of 2	CYRS1542AV18-250GCMB 5962F1120101VXA	-55 to +125	DLAM QML-V	300	>120	<1.34e^{-7}	Immune 120 LET	>2e^{9}
		CYPT1542AV18-250GCMB	-55 to +125	PROTOTYPE	–	–	–	–	–
		CYPT1542AV18-250GLMB	-55 to +125	PROTO LGA	–	–	–	–	–
		CYWT1542AV18-250GCQB	-40 to +105	WIDE TEMP	–	–	–	–	–
	QDR™ II+ x18 burst of 4	CYRS1543AV18-250GCMB 5962F1120102VXA	-55 to +125	DLAM QML-V	300	>120	<1.34e^{-7}	Immune 120 LET	>2e^{9}
		CYPT1543AV18-250GCMB	-55 to +125	PROTOTYPE	–	–	–	–	–
		CYPT1543AV18-250GLMB	-55 to +125	PROTO LGA	–	–	–	–	–
		CYWT1543AV18-250GCQB	-40 to +105	WIDE TEMP	–	–	–	–	–
	QDR™ II+ x36 burst of 4	CYRS1544AV18-250GCMB 5962F1120201VXA	-55 to +125	DLAM QML-V	300	>120	<1.34e^{-7}	Immune 120 LET	>2e^{9}
		CYPT1544AV18-250GCMB	-55 to +125	PROTOTYPE	–	–	–	–	–
		CYPT1544AV18-250GLMB	-55 to +125	PROTO LGA	–	–	–	–	–
		CYWT1544AV18-250GCQB	-40 to +105	WIDE TEMP	–	–	–	–	–
	QDR™ II+ QML-V die	CYRS1543AV18-1X24M	-55 to +125	QML-V	300	>120	<1.34e^{-7}	Immune 120 LET	>2e^{9}
	QDR™ II+ proto die	CYPT1543AV18-1X24M	-55 to +125	PROTOTYPE	–	–	–	–	–

1) Total Ionizing Dose [Krad (Si)]
2) Single Event Latchup [LET] @ 125°C
3) Single Event Upset [err/bit.dy] Geo sync-solar min; Note: SEU is <1e^{-12} with Controller EDAC
4) Single Event Functional Interrupt [err/dev.dy] geo sync-solar min
5) Prompt Dose [rad (Si)/s]

Published by
Infineon Technologies AG
81726 Munich, Germany

Document number:B119-I1140-V1-7600-NA-EC
Date: 2021-08