Quick Presentation:

4Mb Asynchronous SRAM with ECC

ECC = Error-Correcting Code

High-Speed, Low-Power Asynchronous SRAMs
With On-Chip ECC to Improve Reliability 1,000-Fold

Cypress Is the SRAM Market Leader

Cypress is the world's largest and most experienced asynchronous SRAM supplier with:

>40% market share

10 generations of asynchronous SRAMs developed

More in R&D investment than any other competitor

Cypress has the broadest asynchronous SRAM portfolio and offers:

600 asynchronous SRAMs

Fast asynchronous SRAMs from 64Kb to 32Mb

Low-power (MoBL®[1]) SRAMs with densities from 64Kb to 64Mb

Products in industrial[2], automotive[3] and rad-hard grades[4]

Ultra-reliable SRAMs with on-chip ECC[5] for single-bit error detection and correction

Cypress is the most dependable asynchronous SRAM supplier and offers:

Lead times of ≤5 weeks, with ≥99.4% on-time delivery

Multiple qualified fabs, assembly sites and test sites

Legacy product support up to 20 years

Cypress adds three new ultra-reliable 4Mb asynchronous SRAMs with on-chip ECC[1] that are 1,000x more reliable than standard SRAMs without ECC[1]

[1] More Battery Life: Low-power Asynchronous SRAMs with ≤2-µA/Mb standby current
[2] Industrial grade: -40ºC to +85ºC
[3] AEC-Q100: -40ºC to +125ºC
[4] Radiation hardened, military grade: -55ºC to +125ºC
[5] Error-correcting code

Asynchronous SRAM Portfolio

High Density | Wide Voltage Range | Automotive A, E[1,2] | On-chip ECC[3]

	Fast SRAM		Low-Power SRAM (MoBL®: More Battery Life)		PowerSnooze™[4]	Serial SRAM
	Non-ECC	ECC[3]	Non-ECC	ECC[3]	ECC[3]	Quad-SPI, ECC[3]
32Mb-128Mb		**Other Densities NDA Required Contact Sales**	**CY6218x** **64Mb**; 2.5, 3.0 V 55 ns; x8, x16 Ind[5]	**Other Densities NDA Required Contact Sales**	**Other Densities NDA Required Contact Sales**	**Other Densities NDA Required Contact Sales**
	CY7C107x **32Mb**; 3.3 V 12 ns; x8, x16 Ind[5]		**CY6217x** **32Mb**; 2.5, 3.0, 5.0 V 55 ns; x8, x16 Ind[5]			
2Mb-16Mb	**CY7C106x** **16Mb**; 1.8, 3.3 V 10 ns; x8, x16, x32 Ind[5]	**CY7C106x** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind[5], Auto E[2]	**CY6216x** **16Mb**;1.8, 3.0, 5.0 V 45 ns; x8, x16 Ind[5], Auto A[1]	**CY6216x** **16Mb**; 1.8-5.0 V 45 ns; x8, x16, x32 Ind[5], Auto E[2]	**CY7S106x** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind[5], Auto E[2]	
	CY7C105x **8Mb**; 3.3 V 10 ns; x8, x16 Ind[5]	**CY7C1012** **12Mb**; 3.3 V 10 ns; x24 Ind[5]	**CY6215x** **8Mb**; 1.8, 3.0, 2.5-5V 45 ns; x8, x16 Ind[5], Auto A, E[1,2]			
	CY7C104x **4Mb**; 3.3, 5.0 V 10 ns; x4, x8, x16 Ind[5], Auto A, E[1,2], RH[6]	**CY7C1034** **6Mb**; 3.3 V 10 ns; x24 Ind[5]	**CY6214x** **4Mb**; 1.8, 3.0, 2.5-5V 45 ns; x8, x16 Ind[5], Auto A, E[1,2]	**CY6214x** **4Mb**; 1.8-5.0 V 45 ns; x8, x16 Ind[5], Auto E[2]	**CY7S104x** **4Mb**; 3.3 V 10 ns; x8, x16 Ind[5], Auto E[2]	
	CY7C1010/11 **2Mb**; 3.3 V 10 ns; x8, x16 Ind[5], Auto A, E[1,2]	**CY7C1024** **3Mb**; 3.3 V 10 ns; x24 Ind[5]	**CY6213x** **2Mb**; 1.8, 2.5-5.0 V 45 ns; x8, x16 Ind[5], Auto A, E[1,2]			
64Kb-1Mb	**CY7C1020** **512Kb**; 2.6, 3.3, 5.0V 10 ns; x16 Ind[5], Auto E[2]	**CY7C1019/21/100x** **1Mb**; 2.6, 3.3, 5.0 V 10 ns; x4, x8, x16 Ind[5], Auto A, E[1,2]	**CY6212x** **1Mb**; 2.5-5.0 V 45 ns; x8, x16 Ind[5], Auto A, E[1,2]			
	CY7C185 **64Kb**; 5.0 V 15 ns; x8 Ind[5]	**CY7C19x/1399** **256Kb**; 3.3, 5.0 V 10 ns; x4, x8 Ind[5], Auto A[1]	**CY6264** **64Kb**; 5.0 V 55 ns, 70 ns; x8 Ind[5]	**CY62256** **256Kb**; 1.8, 3.0, 5.0V 55 ns; x8 Ind[5], Auto A, E[1,2]		

[1] AEC-Q100 -40ºC to +85ºC
[2] AEC-Q100 -40ºC to +125ºC
[3] Error-correcting code
[4] Fast SRAM with low-power sleep mode
[5] Industrial grade −-40ºC to +85ºC
[6] Radiation hardened, military grade -55ºC to +125ºC

Status: Production | Sampling | Development | Concept
Availability: QQYY | QQYY
● = This presentation

Fast SRAM Family with ECC[1] and PowerSnooze™

Applications

Switches and routers
IP phones
Test equipment
Automotive
Computation servers
Military and aerospace systems

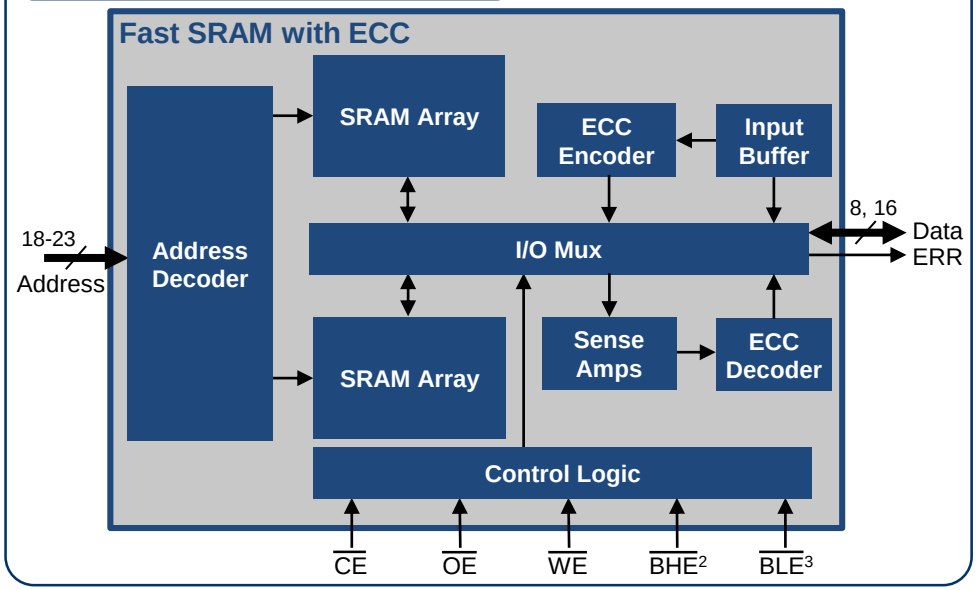
Family Table

Density	MPN	Access Time	Supply Current (Maximum at 85°C)
4Mb	CY7C104x	10 ns	45 mA
16Mb	CY7C106x	10 ns	110 mA

Features

Access time: 10 ns for 4Mb (see Family Table)
Bus-width configurations: x8, x16 for 4Mb
Wide operating voltage range: 1.65-5.5 V
Error-correcting code (ECC) to detect/correct single-bit errors
Bit-interleaving to avoid multi-bit errors
Error-indication (ERR) pin to indicate single-bit errors
Industrial and automotive grades
Industry-standard, RoHS-compliant packages
PowerSnooze: Additional power-saving (deep-sleep) mode with a deep-sleep current of 15 µA for 4Mb

Block Diagram



Collateral

Datasheets: Asynchronous SRAM with ECC

Availability

Sampling: Now
Production: Now

[1] Error-correcting code
[2] Byte high enable
[3] Byte low enable

MoBL®[1] SRAM Family with ECC[2]

Applications

Programmable logic controllers
Handheld devices
Multifunction printers
Automotive
Medical devices
Computation servers

Features

Access time: 45 ns for 4Mb
Standby Current: 8.7 µA for 4Mb
Bus-width configurations: x8, x16 for 4Mb
Wide operating voltage range: 1.65-5.5 V
Error-correcting code (ECC) to detect/correct single-bit errors
Bit-interleaving to avoid multi-bit errors
Error-indication (ERR) pin to indicate single-bit errors
Industrial and automotive grades
Industry-standard, RoHS-compliant packages

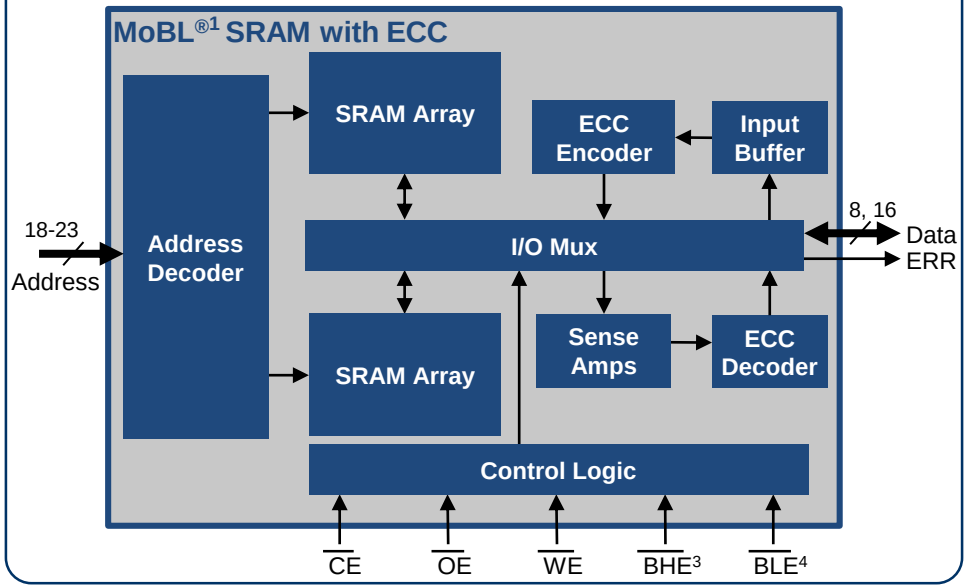
Collateral

Datasheets: Asynchronous SRAM with ECC

Family Table

Density	MPN	Standby Current (Maximum at 85ºC)	Standby Current (Typical at 25ºC)
4Mb	CY6214x	8.7 µA	3.7 µA
16Mb	CY6216x	16 µA	5.3 µA

Block Diagram



Availability

Sampling: Now
Production: Now

[1] More Battery Life
[2] Error-correcting code
[3] Byte high enable
[4] Byte low enable

Here's How to Get Started

1. **Visit the Asynchronous SRAM with ECC Web Page to learn more**
2. **Download the Asynchronous SRAM Roadmap**
3. **Download the Asynchronous SRAM with ECC datasheets**