48 V Regulated Solutions for a Greener Data Center

Dr. Mario Ursino, Dr. Roberto Rizzolatti
Infineon 48 V power architectures for data centers

Infineon portfolio

› ZSC ... Zero voltage switching switched capacitor converter
› HSC... Hybrid switched capacitor converter
› DR-HSC... Dual stage regulated hybrid switched capacitor converter
› RHSC... Regulated hybrid switched capacitor converter

Multiphase buck System

5 V
0.75 V …1.8 V

48 V

conversion ratio >

2:1 ZSC
24 V
12 V

4:1 ZSC
12 V
2:1 ZSC

6:1 HSC
6 V

5:1 HSC
8 V

8:1 HSC
12 V

10:1 RHSC
12 V
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Data center power architectures

48V BUS

48V Server Motherboard

IBC

X:1 ZSC/HSC

[12-6] unregulated

VR

0.5V, 0.8V, 1V

ASIC

GPU

Other System Rails
(FAN, PCIE, Hard Drive, ...)

12V regulated

DC/DC

48V

48V

Regulated IBC

12 regulated

VR

0.5V, 0.8V, 1V

ASIC

GPU

Other System Rails
(FAN, PCIE, Hard Drive, ...)

48V

48V
Conversion ranges unregulated/ regulated/ semi-regulation

\[
\begin{array}{c}
V_{out} \\
15 \text{ V} \\
12 \text{ V} \\
10 \text{ V} \\
8 \text{ V} \\
5.5 \text{ V} \\
40 \text{ V} \\
48 \text{ V} \\
54 \text{ V} \\
60 \text{ V} \\
\end{array}
\]

- RHSC 10:1
  - 750 W
  - 8\text{th} brick

- RHSC 8:1
  - 750 W
  - 40x18 mm
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- 5 V
- 0.75 V …1.8 V
- 12 V
- 24 V
- 9.6 V
- 8 V
- 8:1 HSC
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- 6 V
- 10:1 RHSC
- 8 V
- 4:1 ZSC
- 12 V
- 2:1 ZSC
- 24 V
- 12 V
- 5 V
- 48 V
- conversion ratio >
How is it possible to reduce $F_{sw}$ and output inductance value in a 48 V to 12 V regulated converter?

- $V_{in} = [40 – 60] V$
- $V_{out} = 12 V \pm 2\%$ (full regulation)
  - buck type converter
- $I_{out}$ high current in one phase
  - low inductor value

### Regulation scenarios

<table>
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<tr>
<th>Condition</th>
<th>Diagram</th>
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<tr>
<td>$V_{out} &lt; \frac{V_{in}}{4}$</td>
<td><img src="image" alt="Diagram" /></td>
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How is it possible to reduce $F_{sw}$ and output inductance value in a 48 V to 12 V regulated converter?

### Regulation scenarios

<table>
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<tr>
<th>$V_{out}$ condition</th>
<th>$V_{in}/2$</th>
<th>$V_{in}/4$</th>
<th>$v_{ph}(t)$</th>
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<td>$V_{out} &lt; V_{in}/4$</td>
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- Converter can switch at low frequency, keeping low ripple in the inductor
- In a semi-regulation scenario, the frequency can be further reduced
- High BW performance and reduction of output capacitor
Proposed 48 V to 12 V regulated based on two-stage approach

DR-HSC topology

Unregulated 2:1 ZVS Switched capacitor converter (ZSC)

- High power density
- High $f_{sw}$ (ZVS)
- Low voltage MOSFETs (40 V)

Regulated dual phase 3-level buck converter (DP 3-LBC) with balancing inductor

- Duty cycle modulation
- Highest efficiency at $V_{out} = V_{in}/4$
- Low $f_{sw}$ and small output inductor ($L_{out}$)

$V_{in} = 40 \text{ V} - 60 \text{ V}$

$V_{out} = 12 \text{ V}$ regulated
Main operation ZSC* phases

- Soft charged resonant capacitors over loop parasitic
- Load independent ZVS switching due to $L_{\text{zvs}}$ inductor
Duty-cycle modulation for buck stage:

- Since the dual-phase 3LFC are in phase, it is possible to use two PWMs for multiple multi-level bridges (interleaving the PWMs in a proper way)
- For each dual-phase 3LFC two PWMs are needed
- Additional inductor to balance flying capacitor voltages
  - Balancing inductor is very small:
    - Size depends on voltage and frequency
    - Size does not depend on the converter power level
  - Inductor can be placed between: Q4_D to Q8_D or between Q2_D to Q6_D
How the balancing effect takes place

\[ V_{in} = V_{Cf ly1} + V_{Cf ly2} \]

\[ V_{DQ4} = V_{Cf ly2} \]

\[ V_{DQ8} = 0V \]

› A small DC current appears and ensures this flux balance
How the balancing effect takes place

\[
V_{in} = V_{C\text{fly}1} + V_{C\text{fly}2}
\]

\[
V_{DQ4} = 0\text{V}
\]

\[
V_{DQ8} = V_{C\text{fly}1}
\]

A small DC current appears and ensures this flux balance

\[
\frac{V_{C\text{fly}2}}{L_{bal}} \frac{T_{on\Phi_b}}{L_{bal} T_{on\Phi_a}} = \frac{V_{C\text{fly}1}}{L_{bal}} \frac{T_{on\Phi_a}}{L_{bal} T_{on\Phi_a}}
\]
Balancing inductor for DP 3-LBC

Mathematical model

By considering Q4 controlled by $\Phi_b$, whereas Q8 is controlled by $\Phi_a$, having output inductor valley current always positive, and considering the fux balancing of the balancing inductor $L_{bal}$, the following equation is valid:

\[
\dot{i}_{L_{bal}} = \frac{V_{c\,fly}}{DCR_{L_{bal}}} - DC_{R} \cdot I_{bal,dc}.
\]

Considering balancing inductor parasitic and non-ideal converter behaviour (i.e. in this case drivers missmatch)

\[
\frac{T_{on\Phi_a}}{T_{on\Phi_b}} = \frac{V_{c\,fly2}}{V_{c\,fly1} - DCR_{L_{bal}} \cdot I_{bal,dc}}
\]

$DCR_{L_{bal}}$… DC resistance of the balancing inductor

- A small DC current starts to flow throw $L_{bal}$ in case $T_{on\Phi_a} \neq T_{on\Phi_b}$.
Balancing inductor for DP 3-LBC

Mathematical model

Dual-phase 3-level buck with equivalent balancing model

Main dc current dependency is based on $I_{\text{out}}$ and $V_{\text{in}}$.

$$I_{\text{bal,dc}} = I_{\text{out}} \frac{T_{\text{on,} \Phi_b} - T_{\text{on,} \Phi_a}}{T_{\text{on,} \Phi_b} + T_{\text{on,} \Phi_a}} + 2 \frac{V_{\text{in}} T_{\text{on,} \Phi_b}^2 - V_{\text{fly,} 1} (T_{\text{on,} \Phi_b}^2 + T_{\text{on,} \Phi_a}^2)}{4 L_{\text{out}} (T_{\text{on,} \Phi_b} + T_{\text{on,} \Phi_a})}$$

For the sake of explanation, one leg is considered. Net charges and discharges in the $C_{\text{fly}}$ capacitor (balanced case):

$$Q_{\text{ina}} = Q_{\text{inb}}$$

$$Q_{\text{inb}} = \int_{0}^{T_{\text{on,} \Phi_b}} \left( \frac{V_{\text{in}} - V_{\text{fly,} 1}}{2 L_{\text{out}}} t + \frac{I_{\text{out}}}{2} - \frac{I_{\text{bal,dc}}}{2} \right) dt$$

$$Q_{\text{ina}} = \int_{0}^{T_{\text{on,} \Phi_a}} \left( \frac{V_{\text{fly,} 1}}{2 L_{\text{out}}} t + \frac{I_{\text{out}}}{2} - \frac{I_{\text{bal,dc}}}{2} \right) dt$$

$$\Delta T_{\text{on}} = T_{\text{on,} \Phi_b} - T_{\text{on,} \Phi_a}$$
Balancing inductor for DP 3-LBC

Mathematical model

\[ V_{in} = 30 \text{ V} \quad I_{out} = 50 \text{ A} \]

\[ L_{out} = 250 \text{ nH} \]

\[ F_{sw} = 250 \text{ kHz} \quad I_{out} = 50 \text{ A} \]
Dual-phase 3-level buck converter
- corner case analysis

Assume to have a mismatch between propagation delays at driver level ending in the following situation:

- $\Phi_a$ with $\Phi_a$ has 20 ns dead-time
- $\Phi_b$ with $\Phi_b$ has (20 ns-25 ns-30 ns-35 ns-37.5 ns) dead-time

- $V_{in} = 30 V$, $V_{out} = 12 V$
- $L_{out} = 310 nH$, $f_{sw} = 250 kHz$
Monte Carlo results considering 20 ns deviation in driver propagation mismatch

Flying capacitors

- $\text{max} = 15.65 \text{ V}$
- $\sigma = 74 \text{ mV}$
- $\text{min} = 14.35 \text{ V}$

Output inductor

- $\text{max pk to pk} = 17.2 \text{ A}$
- $\sigma = 487 \text{ mA}$
- $\text{min pk to pk} = 15.21 \text{ A}$

Q1 Vds

Flying capacitor voltage balance achieved under different propagation delays scenario mismatch
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Hardware overview

Q1 to Q8: 8 x BSZ011NE2LS5I
Driver ICs: 8 x 1EDN7550B
C_{r1,2} = 10 \mu F*8 X7R, C_{in} = 10 \mu F*6 X6S
L_{zvs} = 1.45 \mu H custom
E-Fuse controller: LM5060
V_{in} = 22 – 30 V, V_{out} = 12 V
f_{sw} = 250 kHz, I_{out} = 55 A

Q11 to Q41: 4 x IQE013N04LM6
Qh-sw: 1 x IPT012N08N5
Driver ICs: 5 x 1EDN7550B
C_{r1,2} = 10 \mu F*8 X7R, C_{in} = 10 \mu F*6 X6S
L_{zvs} = 1.45 \mu H custom
E-Fuse controller: LM5060
V_{in} = 44 V – 60 V, V_{out} = 22 – 30 V
f_{sw} = 630 kHz

η_{peak_48V} = 99.1%
η_{peak_24V} = 99.38%
η_{sum_peak} = 98.13% (@ V_{in} = 48 V)
Output inductor phase note voltage drift w/wo passive balancing

\[ V_{\text{mid}} = 30 \text{ V} \]

No shift in the phase voltage of the output inductor is present by adding the balancing inductor.

without DT mismatch

with DT mismatch (\(\Delta DT 20 \text{ ns} \))
Balancing inductor current
w/wo passive balancing

Flying capacitors are balanced to half of the input voltage of the DP-3LFC.

\[ V_{\text{fly1,2}} \]

\[ \Delta I_{\text{bal}} = 2 \, A \]

\[ I_{\text{Lbal}} \]

\[ \Delta I_{\text{bal}} = 2 \, A \]

\[ I_{\text{Lbal}} \]

\[ \Delta I_{\text{bal} - \text{dc}} = 300 \, mA \]

\[ V_{\text{mid}} = 30 \, V \]

\[ I_{\text{out}} = 55 \, A \]
Transient response comparison w/wo passive balancing

Without DT mismatch

With DT mismatch ($\Delta T \approx 20$ ns)

During transient event (not anymore a steady state duty-cycle) the current amplitude, inside the equalizing inductance, does not vary.
Efficiency - w/wo passive balancing

Efficiency variation without implementing balancing inductor

Efficiency variation by implementing balancing inductor under extreme corner cases

Power losses spread under applied driver mismatch is almost negligible when balancing inductor is used!

$V_{in} = 60\ V$
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- DR-HSC… Dual-stage regulated hybrid switched capacitor converter
- RHSC… Regulated hybrid switched capacitor converter

Multiphase buck System

REGULATED

- DR-HSC and 4:1 RHSC

UNREGULATED

- 2:1 ZSC
- 4:1 ZSC
- 5:1 HSC
- 6:1 HSC
- 8:1 HSC

Conversion ratio >

- 24 V
- 12 V
- 12 V
- 9.6 V
- 8 V
- 6 V
- 5 V
- 0.75 V … 1.8 V

48 V

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Most of the power is delivered through high-efficiency converter

Regulation is achieved with a fraction of the total power

High efficiency is obtained with auto-transformers and ZVS

Regulation is obtained through an inductor-based converter

\[ \eta = \frac{V_{in1}}{V_{bus}} \cdot \eta_1 + \frac{V_{in2}}{V_{bus}} \cdot \eta_2 \]
RHSC 4:1 topology overview

**Split-boost**

- Hard switching @ low voltage
- Low power delivery

**4:1 HSC**

- High efficiency
- ZVS in high voltage domain
- High power delivery

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**Diagram**

[Diagram of the RHSC 4:1 topology showing components and connections, including symbols for Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, ΦA, and ΦB.]
RHSC 4:1 operation phase 1
RHSC 4:1 operation phase 2
RHSC 4:1 operation phase 3
RHSC 4:1 operation phase 4
RHSC 4:1 operation phase 5
ISOP achieved!
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# RHSC 4:1 – 1.2 kW down-solution

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<tr>
<td><strong>1.2 kW</strong></td>
<td><strong>1 kW / 54 V input – no heat spreader</strong></td>
</tr>
<tr>
<td><strong>1 kW in³</strong></td>
<td></td>
</tr>
<tr>
<td><strong>13 mm profile</strong></td>
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<tbody>
<tr>
<td><strong>Q₁</strong></td>
<td>1×IQE013N04LM6 per side</td>
</tr>
<tr>
<td><strong>Q₂</strong></td>
<td>2×ISZ034N06LM5 per side</td>
</tr>
<tr>
<td><strong>Q₃</strong></td>
<td>4×IQE013N04LM6 per side</td>
</tr>
<tr>
<td><strong>Q₄</strong></td>
<td>1×IQE013N04LM6 per side</td>
</tr>
<tr>
<td><strong>Q₅</strong></td>
<td>2×ISK024NE2L5M</td>
</tr>
<tr>
<td><strong>Q₆</strong></td>
<td>2×BSZ011NE2LS5I</td>
</tr>
<tr>
<td><strong>Q₇</strong></td>
<td>2×BSZ011NE2LS5I</td>
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</table>

| **C_{res}** | 8×GRM21BZ71H475ME15 per side |
| **C_{S}** | 8×GRM21BR61E226ME44 per side |
| **C_{out}** | 14×GRM31CR71E106KA12 |
| **C_{in}** | 4×560 µF electrolytic |
| **V_{in}** | 48 V – 60 V |
| **V_{out}** | 12 V |
| **f_{sw}** | 260 kHz |
| **TX** | 4 µH mag. / 17 nH leak. |
| **L** | XAL7070-551 |
| **Driv** | 4×1EDN7550, 2×2EDN7534G, 3×NCP81155 |

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51 mm

25 mm
1.2 kW down-solution measured efficiency

![Graph showing efficiency and loss vs. output power for different voltages (60 V, 54 V, 48 V).](image)
RHSC 4:1 – Main waveforms

- **ZVS in high voltage domain**
- **Hard switching in low voltage / low power domain**
Infineon 4:1 regulated converter

- DR-HSC converters offer high flexibility and high power density for a fully regulated 48 V to 12 V IBC solution
- Sigma connection allows for IBC regulation with unregulated-like figures of merit
- RHSC 4:1 can replace existing fixed-ratio IBCs with comparable density and efficiency:
  - Down-solution → high flexibility
  - Module → high density
  - Multiphase-ready with active current sharing

Summary
Part of your life. Part of tomorrow.