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32-Bit Microcontroller FM4 Family Peripheral Manual GDC Part

Doc. No. 002-04917 Rev. *D

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Preface

Thank you for your continued use of Cypress products.
Read this manual and the data sheet thoroughly before using products in this family.

Purpose of This Manual / Intended Readers

This manual explains the functions and operations of this family and describes how they are used. The manual is intended for engineers engaged in the actual development of products using this family.
For the descriptions of the Analog macro, Timer, and Communication Macro, see the respective separate peripheral manuals.

Note:

- *This manual explains the configuration and operation of the peripheral functions, but does not cover the specifics of each device in the series.*
  Users should refer to the respective data sheets of devices for device-specific details.
- *Whether a peripheral function is on board or not is dependent on product type. See data sheets for details.*

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Sample Programs and Development Environment

Cypress offers sample programs free of charge for using the peripheral functions of the FM4 family. Cypress also makes available descriptions of the development environment required for this family. Feel free to use them to verify the operational specifications and usage of this Cypress microcontroller.

Microcontroller support information:

https://community.cypress.com/community/MCU

Note:

- *Note that the sample programs are subject to change without notice. Since they are offered as a way to demonstrate standard operations and usage, evaluate them sufficiently before running them on your system.*
  Cypress assumes no responsibility for any damage that may occur as a result of using a sample program.

Overall Organization of This Manual

Peripheral Manual Timer part has 4 chapters and Appendixes as shown below.

CHAPTER 1: Overview
CHAPTER 2: Reference Clock Selector
CHAPTER 3: Subsystem Control
CHAPTER 4: Software Interface
Appendixes

Related Manuals

The manuals related to this family are listed below. See the manual appropriate to the applicable conditions.
The contents of these manuals are subject to change without notice. Contact us to check the latest versions available.

Peripheral Manual

- FM4 Family Peripheral Manual (002-04856)

Called Peripheral Manual hereafter

- FM4 Family Peripheral Manual Timer Part (002-04858)

Called Timer Part hereafter

- FM4 Family Peripheral Manual Analog Macro Part (002-04860)

Called Analog Macro Part hereafter

- FM4 Family Peripheral Manual Communication Macro Part (002-04862)

Called Communication Macro Part hereafter

- FM4 Family Peripheral Manual GDC Part (this manual)

Called GDC Part hereafter

- FM4 Family Peripheral Manual GDC (Subsystem) Part

It is necessary to conclude non-disclosure agreement to obtain this manual. Contact us for more information.

- FM4 Family Peripheral Manual GDC (Core) Part

It is necessary to conclude non-disclosure agreement to obtain this manual. Contact us for more information.

Data Sheet

For details about device-specific, electrical characteristics, package dimensions, ordering information etc., see the following document.

- 32-bit Microcontroller FM4 Family Data Sheet

Note:

- *The data sheets for each series are provided.*
  See the appropriate data sheet for the series that you are using.

CPU Programming Manual

For details about Arm Cortex-M4F core, see the following documents that can be obtained from http://www.arm.com/.

- Cortex-M4 Technical Reference Manual
- Arm v7-M Architecture Application Level Reference Manual

Flash Programming Manual

For details about the functions and operations of the built-in flash memory, see the following document.

- FM4 Family Flash Programming Manual

Note:

- *Flash programming manuals for each series are provided.*
  See the appropriate flash programming manual for the series that you are using.

How to Use This Manual

Finding a Function

The following methods can be used to search for the explanation of a desired function in this manual:

■ Search from the table of the contents

The table of the contents lists the manual contents in the order of description.

■ Search from the register

The address where each register is located is not described in the text. To verify the address of a register, see A. Register Map in Appendixes.

About the Chapters

Basically, this manual explains 1 peripheral function per chapter.

Terminology

This manual uses the following terminology.

Term	Explanation
Word	Indicates access in units of 32 bits.
Half word	Indicates access in units of 16 bits.
Byte	Indicates access in units of 8 bits.

Notations

■ The notations in bit configuration of the register explanation of this manual are written as follows.

□ bit: bit number

□ Field: bit field name

□ Attribute: Attributes for read and write of each bit

・R: Read only

・W: Write only

・R/W: Readable/Writable

・-: Undefined

□ Initial value: Initial value of the register after reset

・0: Initial value is 0

・1: Initial value is 1

・X: Initial value is undefined

■ The multiple bits are written as follows in this manual.

□ Example: bit7:0 indicates the bits from bit7 to bit0

■ The values such as for addresses are written as follows in this manual.

□ Hexadecimal number: 0x is attached in the beginning of a value as a prefix (example: 0xFFFF)

□ Binary number: 0b is attached in the beginning of a value as a prefix (example: 0b1111)

□ Decimal number : Written using numbers only (example: 1000)

The Target Products in This Manual

■ In this manual, the products are classified into the following groups and are described follows.
For the descriptions such as "TYPE1-M4", see the relevant items of the target product in the list below.

Table 1 TYPE4-M4 Product List

Description in this manual	Flash memory size 384 Kbytes	
	VRAM 512 Kbytes	VRAM 512 Kbytes + VFLASH 2 Mbytes
TYPE4-M4	S6E2D35G0 S6E2D35J0	S6E2D35GJ
	S6E2D55G0 S6E2D55J0	S6E2D55GJ
	S6E2DF5G0 S6E2DF5J0	S6E2DF5GJ
	S6E2DH5G0 S6E2DH5J0	S6E2DH5GJ

Contents

CHAPTER 1: Overview

This chapter gives an overview of the GDC subsystem.

---

1. Overview

1.1 Feature Summary

1.1.1 General Features

- Controller for external graphics display.
- Accelerator for 2D block image transfer (blit) operations.
- Embedded SRAM video memory.
- Multilayer GDC bus matrix with master and slave ports.
- Signature computation for display content (use: data integrity/safety requirements)
- Command Sequencer for graphic operations.
- Quad SPI (Serial Peripheral Interface) for external memory extensions.
- SDRAM interface for external memory extensions.
- HBI (Hyper Bus Interface) interface for external memory extensions.
- Two processing pipeline (blit / display).
- Maximum core system clock frequency: Refer to the Data sheet.

Note:

- *User can leverage internal VRAM and external HyperRAM as a graphics memory allowed to be written by GDC.*

1.1.2 Display Controller

1.1.2.1 Display Output Stream

- One display output stream.
- Up to 24-bit color resolution (RGB).
- TTL mode.
- Video modes up to SVGA @ 60 Hz (see Functional Limitations for details).
- Timing controller with up to 12 signal generators.
- Spatial and temporal dithering for low resolution panels.
- Gamma correction.
- Can select on-the-fly between two independent input streams (content and safety stream).
- Can overlay both input streams (e.g. for safety HMI).
- Signature unit (CRC checksum; up to 2 independent windows) for each display.
- 1-bit alpha mask per pixel for one of

- Transparent stream overlay.
- Masked color correction.
- Masked signature computation.

1.1.2.2 2 Background Plane in Total

- 1 x constant color.

1.1.2.3 2 Foreground Planes with 9 Windows in Total

- 1 x integral plane (1 window; optionally compressed).
- 1 x fractional plane (composed from up to 8 windows with independent display buffers).

1.1.2.4 Alpha Blending Stage for Each Plane

- Configurable blending sequence for planes.
- All windows from 1x1 pixel to max supported frame dimension.

1.1.2.5 Display Buffer Formats

- RGBA, Grayscale.
- Source alpha, constant alpha, transparent alpha (any combination).
- Color index (256 x 24 bit palette).
- Compressed (lossless: RL or RLA; lossy: RLAD).
- 1, 2, 4, 8, 16, 18, 24, 32 bits per pixel word (packed in memory).
- All color channels at any bit position in pixel word (configurable).
- Bit width of all color channels between 0 .. 8 bits (configurable).
- Configurable scan direction (90/180/270° rotation; horizontal/vertical flip).

1.1.2.6 Other Features

- All configuration registers shadowed.
- Individual shadow load for each layer (synchronized to display refresh).

1.1.3 Blit Engine

1.1.3.1 Operations

- Fill.
- Copy.
- Blend (compliant to OpenGL, OpenVG and OpenWF).
- Rop2/3 (any logic operation).
- Scale (any factor).
- Rotate (any angle).
- Linear color conversion (a programmable 3x3 matrix).
- Non-linear color conversion (programmable look-up per component).
- Pixel format conversion (from any to any of all supported formats listed below).

1.1.3.2 Source Pixel Formats

- RGBA, Grayscale.
- Source alpha, constant alpha, transparent alpha, mask alpha (any combination).
- Color index (256 x 24 bit palette).
- Compressed (lossless: RL or RLA; lossy: RLAD).
- 1, 2, 4, 8, 16, 18, 24, 32 bits per pixel word (packed in memory).
- All color channels at any bit position in pixel word (configurable).
- Bit width of all color channels between 0 .. 8 bits (configurable).
- Configurable scan direction (90/180/270° rotation; horizontal/vertical flip).

1.1.3.3 Destination Pixel Formats

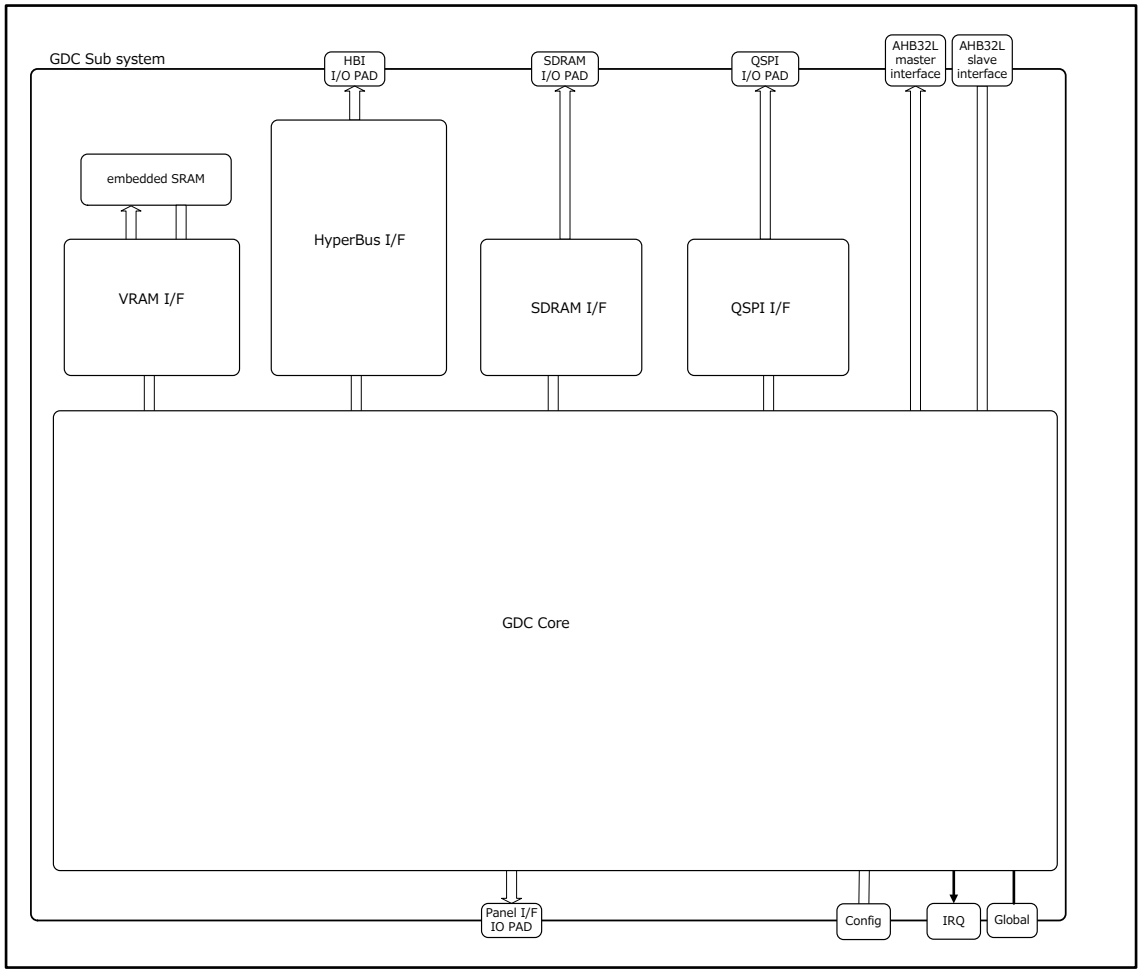
- RGBA, Grayscale.
- Pre-multiplied alpha.
- 1, 2, 4, 8, 16, 18, 24, 32 bits per pixel word (packed in memory).
- All color channels at any bit position in pixel word (configurable).
- Bit width of all color channels between 0 .. 8 bits (configurable).

1.1.3.4 Other Features

- Any image size from 1x1 pixel to max supported dimension (see Functional Limitations).
- All operations with 8-bit precision per color channel.
- Source and destination buffer stride in bytes.
- Source buffer clip window.
- Lot of functions can be combined with single-pass blit (e.g. rotate + blend).
- All configuration registers shadowed (can set up next operation during blit).

2. Block Diagram

Figure 2-1 Block Diagram of the GDC Subsystem



3. Function Summary

3.1 Reference Clock Selector

Reference clock selector selects reference clock for GDC clock and reference clock for peripherals.

3.1.1 Reference Clock for GDC Clock

Clock source can be selected for GDC clock:

- GDC PLL output clock.
- Main PLL output clock.
- HCLK.

3.1.2 Reference Clock for Peripherals

Clock source can be selected for peripherals that are clocks for display controller, HyperBus Interface, SDRAM controller, and QSPI controller:

- GDC PLL output clock.
- HCLK.

3.1.3 Software Reset

Reference clock selector generates software reset signal for the GDC subsystem.

Note:

- *Reference clock for GDC clock and reference clock for peripherals should be stopped as negating software reset.*

3.2 Subsystem Controller (subsysctrl)

Subsystem controller generates clocks from reference clock for GDC clock:

- GDC clock that is used as GDC core clock.
- Configuration clock for control / status register in the GDC core (CFGCLK).

Subsystem controller also generates clocks from reference clock for peripherals.

- Display clock using a fixed point divider.
- HyperBus interface controller clock using an integral divider.
- SDRAM controller clock using an integral divider.
- QSPI controller clock using an integral divider.

3.3 HS-SPI External Memory Interface

Refer to FM4 Family Peripheral Manual Communication Part.

Notes:

- *Both Mode0 and Mode4 are supported in the GDC subsystem. Mode1 ,2, and 3 are not supported in the GDC subsystem.*
- *To set Mode4, set 1 to ACES field of the HSSPIn_PCC0, HSSPIn_PCC1, HSSPIn_PCC2, and HSSPIn_PCC3.*
- *Mode4 can be set in Command Sequencer Mode only.*
- *RTM=1 mode is not supported in the GDC subsystem.*

3.4 SDRAM External Memory Controller

Refer to FM4 Family Peripheral Manual.

3.5 HyperBus Interface

Refer to FM4 Family Peripheral Manual Communication Part.

CHAPTER 2: Reference Clock Selector

This chapter explains the functions and operations of the reference clock selector.

1. Overview

This section describes the overview of the reference clock selector module.

1.1 Feature Summary

Reference clock selector selects reference clocks for the GDC subsystem.

Reference clocks consist of reference clock for GDC clock and reference clock for peripherals.

1.1.1 Reference Clock for GDC Clock

Clock source can be selected for GDC clock:

- GDC PLL output clock
- Main PLL output clock
- HCLK

GDC clock is divided from reference clock for GDC clock, division ratio 1 and 2 to 255, in the GDC subsystem control module.

1.1.2 Reference Clock for Peripherals

Clock source can be selected for peripherals that are clock for display controller, HyperBus Interface, SDRAM controller, and QSPI controller:

- GDC PLL output clock
- HCLK
  - Display clock is divided from Reference Clock for Peripherals, division ratio 2.0 to 255.99609375, in the GDC subsystem control module.
  - Clock for SDRAM interface controller and QSPI interface controller is divided from Reference Clock for Peripherals, division ration 2 to 255, in the GDC subsystem control module.
  - Clock for HyperBus interface is divided from Reference Clock for Peripherals, division ration 4 to 32 in the GDC subsystem control module.

1.1.3 Software Reset

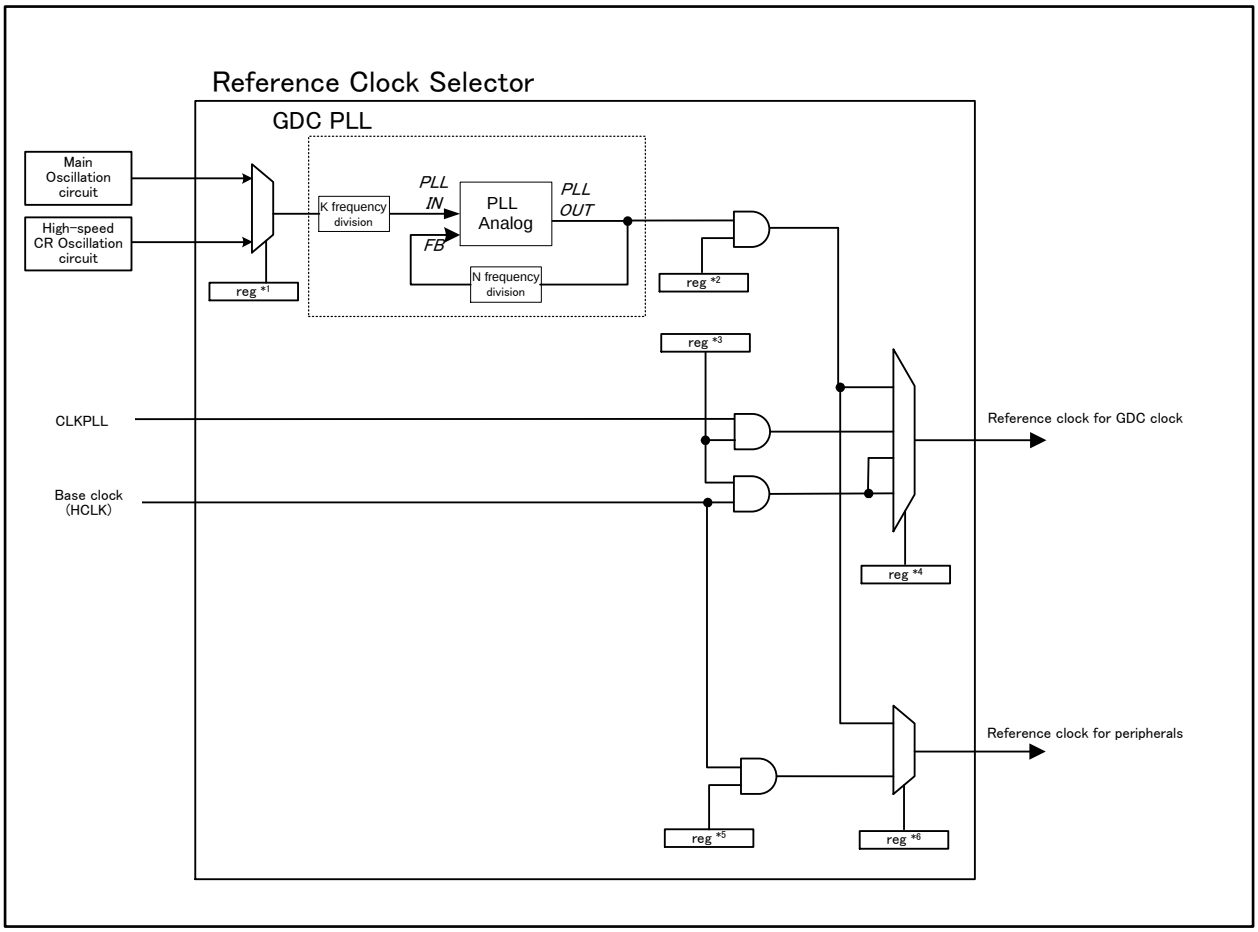
Reference Clock Selector generates software reset signal for the GDC subsystem.

Note:

- *Reference Clock for GDC clock and Reference Clock for Peripherals should stop providing as negating software reset.*

2. Block Diagram

Figure 2-1 Block Diagram of the Reference Clock Selector



*1: GPCR1: GPINC (GDC PLL input clock select bit)
*2: GSSEN: GCCR (GSS clock output enable bit)
*3: GSCR: ACG (Clock gating for Reference clock for GDC clock)
*4: GSCR: ASEL (Reference clock for the GDC clock select bit)
*5: GCSR: PCG (HCLK Clock gating for Reference clock for Peripherals)
*6: GCSR: PSEL (Peripheral clock for the GDC subsystem select bit)
*7: There is no clock coordination requirement between the CPU bus clock and GDC.

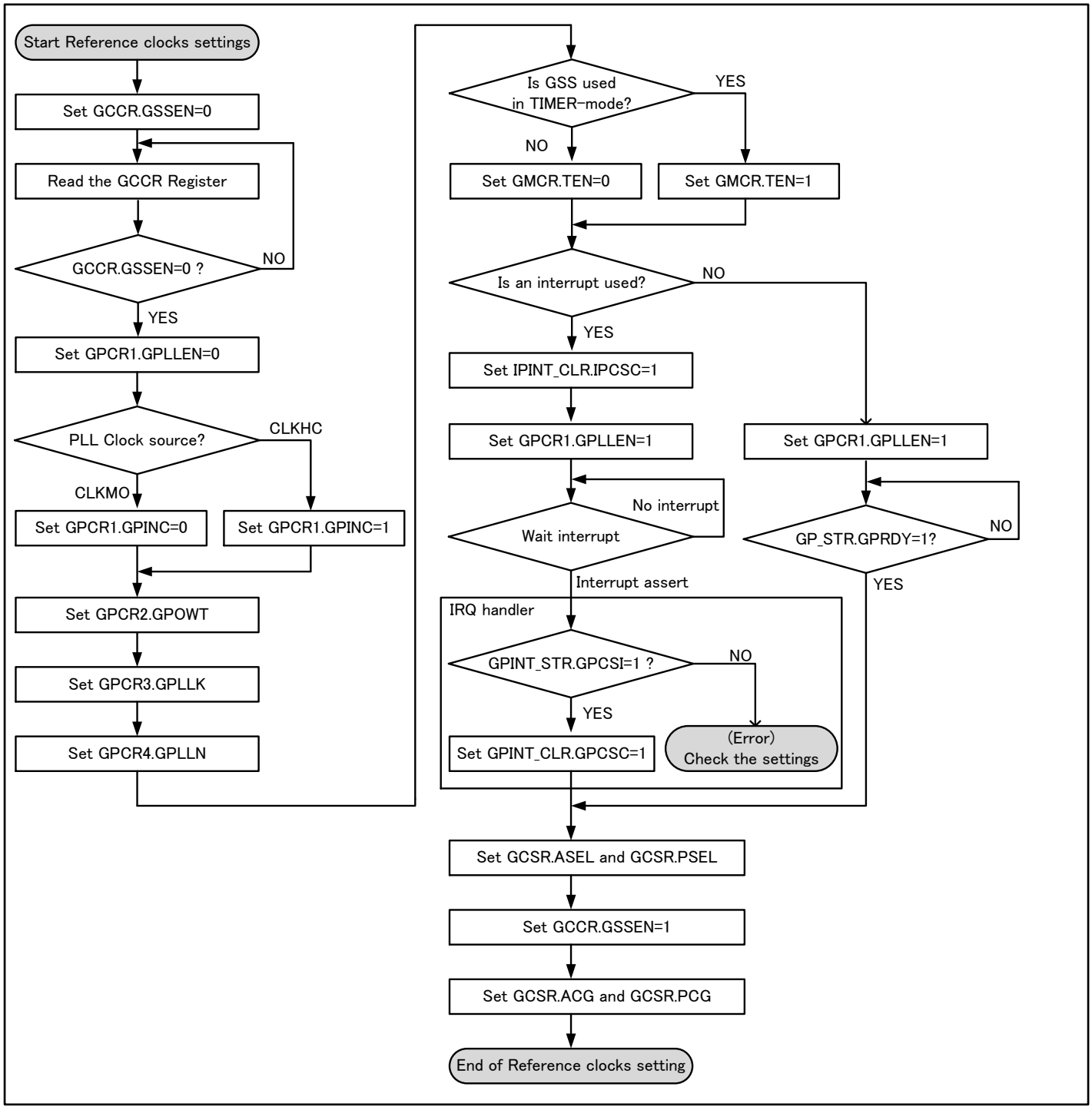
3. Operation

This section describes the operation of the Reference Clock Selector module.

3.1 Clock Setup

Reference clock set up for the GDC subsystem is illustrated in Figure 3-1. Make sure to operate this flow to set GDC and peripheral clock appropriately.

Figure 3-1 Reference Clock Setup Flow



3.2 Setting the Multiplication Ratio to Generate Output Clock of GDC PLL

Each frequency division clock in the PLL Multiplication Circuit must be set using GPCR3 and GPCR4. The Table provides example of frequency setting.

Table 3-1 Example of PLL Multiplication Ratio Setting

Input Clock	K	PLLin	N	PLLOUT_GDC
4 MHz	1	4 MHz	49	200 MHz
4 MHz	1	4 MHz	59	240 MHz
4 MHz	1	4 MHz	69	280 MHz
4 MHz	1	4 MHz	79	320 MHz
4 MHz	1	4 MHz	89	360 MHz
4 MHz	1	4 MHz	99	400 MHz
5 MHz	1	5 MHz	39	200 MHz
5 MHz	1	5 MHz	49	250 MHz
5 MHz	1	5 MHz	59	300 MHz
5 MHz	1	5 MHz	69	350 MHz
5 MHz	1	5 MHz	79	400 MHz
6 MHz	1	6 MHz	39	240 MHz
6 MHz	1	6 MHz	49	300 MHz
6 MHz	1	6 MHz	59	360 MHz
8 MHz	1	8 MHz	24	200 MHz
8 MHz	1	8 MHz	29	240 MHz
8 MHz	1	8 MHz	39	320 MHz
8 MHz	1	8 MHz	49	400 MHz
10 MHz	1	10 MHz	19	200 MHz
10 MHz	1	10 MHz	24	250 MHz
10 MHz	1	10 MHz	29	300 MHz
10 MHz	1	10 MHz	34	350 MHz
10 MHz	1	10 MHz	39	400 MHz
12 MHz	1	12 MHz	19	240 MHz
12 MHz	1	12 MHz	24	300 MHz
12 MHz	1	12 MHz	29	360 MHz
16 MHz	1	16 MHz	14	240 MHz
16 MHz	2	8 MHz	49	400 MHz
19.2 MHz	2	9.6 MHz	29	288 MHz
19.2 MHz	2	9.6 MHz	39	384 MHz
20 MHz	2	10 MHz	39	400 MHz
48 MHz	3	16 MHz	19	320 MHz
48 MHz	4	12 MHz	29	360 MHz
48 MHz	6	8 MHz	39	320 MHz

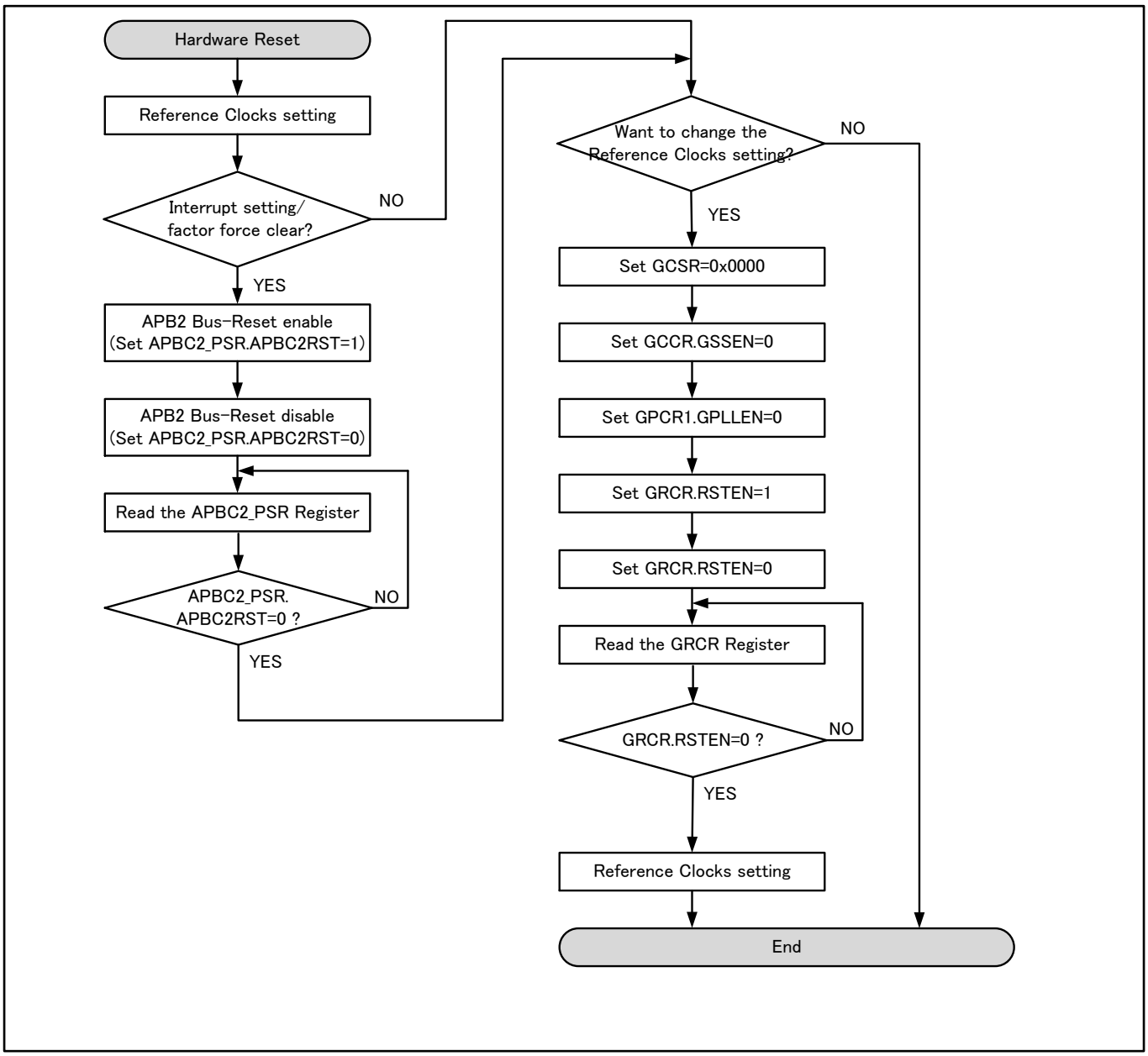
Notes:

- *For PLL characteristics, see the data sheet of the product used.*
- *Set the PLLin within the value PLL input clock frequency: f_{PLLI} shown in the data sheet.*

3.3 Reset Setup

Hardware and software setup for the GDC subsystem is illustrated in Figure 3-2 Hardware and Software Reset Setup.

Figure 3-2 Hardware and Software Reset Setup



4. Registers

This section describes the registers of the reference clock selector in detail.

Registers of the Reference Clock Selector

The following registers are available for each instance of the module.

Abbreviation	Register Name	Reference
GCCR	GDC Clock Control Register	4.1
GPCR1	GDC PLL Control Register 1	4.2
GPCR2	GDC PLL Control Register 2	4.3
GPCR3	GDC PLL Control Register 3	4.4
GPCR4	GDC PLL Control Register 4	4.5
GP_STR	GDC PLL Status Register	4.6
GPINT_ENR	GDC PLL Interrupt Enable Register	4.7
GPINT_CLR	GDC PLL Interrupt Clear Register	4.8
GPINT_STR	GDC PLL Interrupt Status Register	4.9
GCSR	GDC Clock Select Register	4.10
GRCR	GDC Reset Control Register	4.11
GMCR	GDC Mode Control Register	4.12

4.1 GCCR

The GCCR enables/disables output of the GDC PLL.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							GSSEN
Attribute				-				R/W
Initial value				0b0000000				0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b000000 is read from these bits.

Set 0b000000 to these bits when writing.

[bit0] GSSEN: GSS clock output enable/disable setting bit

bit	Description
0	Disables output of the GDC PLL
1	Enables output of the GDC PLL.

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.2 GPCR1

The GPCR1 selects PLL input clock and enables/disables the PLL oscillation.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.						GPINC	GPLLEN
Attribute	-						R/W	R/W
Initial value	0b0000000						0b0	0b0

Register functions

[bit7:2 Reserved: Reserved bits

0b000000 is read from these bits.

Set these bits to 0b000000 when writing.

[bit1] GPINC: GDC PLL input clock selection bit

bit	Description
0	Selects CLKMO (main clock oscillation)
1	Selects CLKHC (high-speed CR clock)

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

[bit0] GPLLEN: GDC PLL enable/disable setting bit

bit	Description
0	Disables oscillation.
1	Enables oscillation.

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.3 GPCR2

The GPCR2 sets the PLL clock stabilization wait time.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.					GPOWT		
Attribute	-					R/W		
Initial value	0b00000					0b000		

Register functions

[bit7:3] Reserved: Reserved bits

0b00000 is read from these bits.

Set these bits to 0b00000 when writing.

[bit2:0] GPOWT: PLL clock stabilization wait time set up bits

bit[2:0]	Description
000	2^9 cycles (Approx. 128 µs, Fin = 4 MHz)
001	2^{10} cycles (Approx. 256 µs, Fin = 4 MHz)
010	2^{11} cycles (Approx. 512 µs, Fin = 4 MHz)
011	2^{12} cycles (Approx. 1024 µs, Fin = 4 MHz)
100	2^{13} cycles (Approx. 2048 µs, Fin = 4 MHz)
101	2^{14} cycles (Approx. 4096 µs, Fin = 4 MHz)
110	2^{15} cycles (Approx. 8192 µs, Fin = 4 MHz)
111	2^{16}cycles (Approx. 16384 µs, Fin = 4 MHz)

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.4 GPCR3

The GPCR3 sets the PLL frequency division ration.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved			GPLLK				
Attribute	-			R/W				
Initial value	0b000			0b00000				

Register functions

[bit7:5] Reserved: Reserved bits

0b000 is read from these bits.

Set these bits to 0b000 when writing.

[bit4:0] GPLLK: PLL input clock frequency division ration setting bits

bit[4:0]	Description
00000	1/1
00001	1/2
00010	1/3
	1/(bit[4:0] + 1)
11111	1/32

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.5 GPCR4

The GPCR4 sets the PLL frequency division ratio.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.	GPLLN						
Attribute	-	R/W						
Initial value	0b0	0b0000000						

Register functions

[bit7] Reserved: Reserved bit

0b0 is read from this bit.

Set this bit to 0b0 when writing.

[bit6:0] GPLLN: PLL feedback frequency division ratio setting bits

bit[6:0]	Description
000000	setting is prohibited
000001	
0001011	
0001100	Division ratio: 1/13 (minimum value)
0001101	Division ratio: 1/14
	Division ratio: 1/(GPLLN[6:0] + 1)
1100011	Division ratio: 1/100 (maximum value)
1100100 to 1111111	setting is prohibited

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.6 GP_STR

The GP_STR indicates status of the PLL.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							GPRDY
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Set 0b000000 to these bits when writing.

[bit0] GPRDY: GDC PLL status bit

This bit indicates status of GDC PLL.

bit	Description
0	No PLL oscillation stabilization wait completion has been asserted
1	A PLL oscillation stabilization wait completion has been asserted

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.7 GPINT_ENR

The GPINT_ENR enables/disables interrupts.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							GPCSE
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Set 0b0000000 to these bits when writing.

[bit0] GPCSE: PLL oscillation stabilization wait completion interrupt enable bit

bit	Description
0	Disables PLL oscillation stabilization wait completion interrupts
1	Enables PLL oscillation stabilization wait completion interrupts

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.8 GPINT_CLR

The GPINT_CLR clears interrupt factor.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							GPCSC
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Set 0b000000 to these bits when writing.

[bit0] GPCSC: GDC PLL oscillation stabilization wait completion interrupt clear bit

bit	Description
0	Not affected
1	Clears GDC PLL oscillation stabilization wait complete interrupt factor.

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.9 GPINT_STR

The GPINT_STR indicates the status of interrupts.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							GPCSI
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Set 0b0000000 to these bits when writing.

[bit0] GPCSI: GDC PLL oscillation stabilization wait completion interrupt status bit

bit	Description
0	No PLL oscillation stabilization wait completion interrupt has been asserted
1	PLL oscillation stabilization wait completion interrupt has been asserted

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.10 GCSR

The GCSR enables/disables output of GDC clock and peripheral clock. The GCSR also selects clock sources for GDC reference clock and peripheral reference clock.

Register configuration

bit	15	14	13	12	11	10	9	8
Field	Reserved.			PCG	Reserved.			PSEL
Attribute		-		R/W		-		R/W
Initial value		0b000		0b0		0b000		0b0

bit	7	6	5	4	3	2	1	0
Field	Reserved.			ACG	Reserved.		ASEL	
Attribute		-		R/W		-	R/W	
Initial value		0b000		0b0		0b00	0b00	

Register functions

[bit15:13] Reserved: Reserved bits

0b000 is read from these bits.

Set 0b000 to these bits when writing.

[bit12] PCG: HCLK Clock gating for Reference clock for Peripherals setting bit

bit	Description
0	Disables output of reference clock for peripherals
1	Enables output of reference clock for peripherals

Notes:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*
- *As operate PSEL field, write '0' to this field to stop providing Reference Clock of peripherals clock to the GDC subsystem.*

[bit11:9] Reserved: Reserved bits

0b000 is read from these bits.

Set 0b000 to these bits when writing.

[bit8] PSEL: Peripheral clock for the GDC subsystem selection bit

bit	Description
0	Selects output of GDC PLL
1	Selects HCLK

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

[bit7:5] Reserved : Reserved bits

0b000 is read from these bits.

Set 0b000 to these bits when writing.

[bit4] ACG: Clock gating for Reference clock for GDC clock setting bit

bit	Description
0	Disables output of reference clock for GDC
1	Enables output of reference clock for GDC

Notes:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*
- *As operate ASEL field or wait for PLL oscillation stabilization, write 0 to this field to stop providing reference clock of GDC clock.*

[bit3:2] Reserved: Reserved bits

“0b00” is read from these bits.

Set “0b00” to these bits when writing.

[bit1:0] ASEL: Reference clock for the GDC clock selection bits

These bits select Reference clock for GDC clock.

bit1:0	Description
00	Selects output clock of GDC PLL
01	Selects HCLK
10	Selects output clock of Main PLL
11	Selects HCLK

Note:

- *These bits initialized by CRGRSTOUT_N, not initialized by PRESETn.*

4.11 GRCR

The GRCR sets software reset for the GDC subsystem control.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							RESETN
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Set 0b0000000 to these bits when writing.

[bit0] RSTEN: Software reset for the GDC subsystem setting bit

bit	Description
0	Releases Software reset
1	Enables software reset

Notes:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*
- *Reference clock for GDC clock and Reference clock for peripherals should be stopped before releasing, writing 0 to the field of RESETN, Software reset.*

4.12 GMCR

The GMCR enables/disables GDC PLL oscillation in case of Timer mode.

Register configuration

bit	7	6	5	4	3	2	1	0
Field	Reserved.							TEN
Attribute				-				R/W
Initial value				0b0000000				0b0

Register functions

[bit7:1] Reserved: Reserved bits

0b0000000 is read from these bits.

Set 0b0000000 to these bits when writing.

[bit0] TEN: PLL oscillation in case of Timer mode control bit

bit	Description
0	Stop oscillation in case of Timer mode
1	Continue PLL status in case of Timer mode

Note:

- *This bit initialized by CRGRSTOUT_N, not initialized by PRESETn.*

CHAPTER 3: Subsystem Control

This chapter explains the functions and operations of the GDC Subsystem control.

---

1. Overview

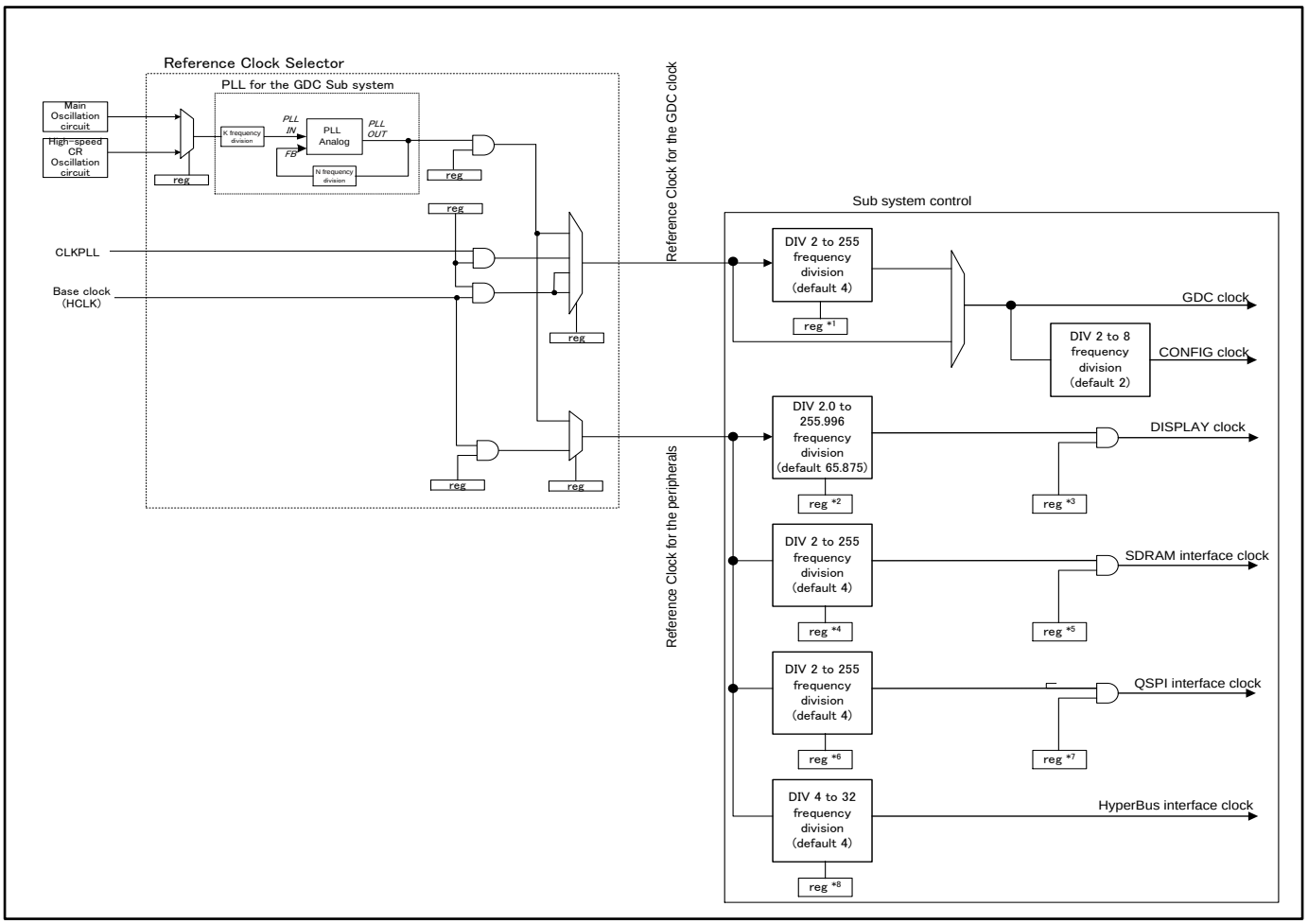
This section describes the overview of the GDC subsystem control.

1.1 Feature Summary

- GDC clock divider
- CONFIG clock divider
- HyperBus interface clock divider
- SDRAM interface clock divider
- QSPI interface clock divider

2. Block Diagram

Figure 2-1 Block Diagram of the Subsystem Control



*1: GDC_ClcokDivider: GDCClockSelect (Division ration of GDC clock generation from the Reference clock for GDC clock)
*2: dsp0_ClockDivider: dsp0ClockDivider (Division ratio from the Reference clock for peripherals)
*3: dsp0_DomaonControl: dsp0_ClockEnable (Display clock output control)
*4: SDRAMC_ClockDivider: SDRAMC_ClockDivider (Division ratio from the Reference clock for peripherals)
*5: SDRAMC_DomainControl: SDRAMC_ClockEnable (SDRAM interface clock output control)
*6: HSSPIC_ClockDivider: HSSPIC_ClockDivider (Division ratio from the Reference clock for peripherals)
*7: HSSPIC_DomainControl: HSSPIC_ClockEnable (Division ratio from the Reference clock for peripherals)
*8: RPCC_ClockDivider: RPCC_ClockDivider (Division ratio from the Reference clock for peripherals)

3. Function and Operation

This section describes function and operation of the GDC subsystem control module.

3.1 Overview

This subsection describes configuration of each clock in the GDC subsystem.

3.1.1 Reference Clocks

■ Reference clock for GDC

GDC clock and CONFIG clock are generated from this reference clock. The source clock for reference clock can be selected from three clock sources. For more information, refer to Chapter 2.

■ Reference clock for peripherals.

Clocks for peripherals are generated from this reference clock. The source clock for reference clock can be selected from two clock sources. For more information, refer to Chapter 2.

3.1.2 GDC Clock

GDC clock is used for GDC core and GDC bus operation mainly.

3.1.3 CONFIG Clock

CONFIG clock is used for configuration register operation in the GDC core.

3.1.4 Peripheral Clocks

Peripheral clocks are generated from the Reference clock for Peripherals.

■ dsp0 clock

dsp0 clock is used for operation of display controller in the GDC core.

■ Dot clock

Dot clock is output for external TFT panel. This clock is divided by 2 automatically at the display controller in the GDC core.

■ SDRAM interface clock

SDRAM interface clock is used for operation of SDRAM controller in the GDC subsystem, and external SDRAM devices.

■ QSPI interface clock

QSPI interface clock is used for operation of QSPI controller in the GDC subsystem, and external QSPI devices.

■ HyperBus interface clock

The HyperBus interface clock is used for operation of the HyperBus controller in the GDC subsystem, and external HyperBus devices.

3.2 GDC Clock Set up

The GDC clock frequency used in the GDC subsystem can be setup using register field GDCClockSelect in the GDC subsystem control module. It specifies the divider used to generate the GDC clock from the reference clock for GDC clock. The reference clock for GDC clock is selected in the Reference Clock Selector module.

Configuration of the GDC clock can be modified during operation.

■ How to set up GDC clock.

1. Select the Reference clock for GDC. For more information, refer to Chapter 2.
2. Set Division ratio to the register field of GDCClockSelect in the register of GDC_ClockDivider.

3.3 CONFIG Clock Set up

The CONFIG clock frequency used in the GDC subsystem can be setup using register field ConfigClockSelect in the GDC subsystem control module. It specifies the divider used to generate the CONFIG clock from GDC clock only. The minimum allowed divider setting can select divided clock from 2 to 8.

The CONFIG clock is generated form GDC clock automatically. There is not a procedure to generate the CONFIG clock.

The CONFIG clock can be changed at any time (even when transfers are in progress), but note that configuration access bandwidth and latency are greatly influenced by this setting.

The CONFIG clock is generated automatically as the GDC clock key in the divider. No other register modifications are needed.

3.4 Display Clock Set up

There is one display clock management unit available in the GDC subsystem Control module of the GDC subsystem. It contains clock generation utility to generate the display clock from the reference clock for peripherals by using a fixed point divider. In addition, the generated display clock can be shifted against the output display data to allow creation of sufficient margin for setup and hold times at the connected external device.

The display clock and clock can be changed at any time (even when transfers are in progress).

3.4.1 Display Clock Generation and Reset Control

The display clock generation can create the display clock from the input reference clock by application of a fixed point divider. The following procedure is how to determine the best possible display clock frequency.

1. Divide the reference clock frequency by a multiple of 2 of the desired display clock frequency.
2. Round this value to a fixed point with 8 decimal places.
3. Program the result to register field of GDCClockSelect in the register dsp0_ClockDivider.
4. Set 1 to the register field dsp0_ClockEnable in the register of dsp0_DomainControl
5. Wait for 0b1 of the register field of DspClockDomainReady in the register of ClockDomainStatus to make sure the display clock domain ready.
6. Set 0b0 to the field of dsp0_Software Reset in the register of the dsp_DomainControl to activate display controller in the GDC core.

At the step 3 above, the field dsp0_ClockSelect can be updated at any point in time (even when dsp0_ClockEnable is set to 1 and the display clock is output). The display clock generation will then update the generated clocks frequency in such a manner that continuity of the generated display clock is guaranteed (for example, no glitches are produced).

Note:

- *Use of the generated display clock for display clock output is only allowed if the GDC core DisEngCfg ClockCtrl setting is set to DIV2. Do not set this to DIV1.*

3.4.2 Display Clock Shift

To allow creating sufficient margin for setup and hold times at the external device the output display clock can be shifted. The dsp0_Clock Offset setting can shift the display clock up to (not including) 180 degrees in reference clock period steps. To achieve shifts larger or equal to 180 degrees the dsp0_ClockInvert setting can be used in addition to add 180 degrees to the shift achieved with dsp0ClockOffset.

It is recommended to verify the achieved margins in setup and hold times by using eg an oscilloscope. Note that the generated display clock periods can jitter from cycle to cycle by the reference clock period due to the way the fixed point clock division works.

The dsp0_ClockOffset and dsp0_ClockInvert settings must not be changed when dsp0_ClockEnable is set to 1. Otherwise corruption of displayed content is possible.

3.4.3 How to Set up Display Clock

Refer to 3.4.1 Display Clock Generation and Reset Control.

3.5 HyperBus Interface Clock Setup

The HyperBus interface clock frequency used in the GDC subsystem can be setup using register field RPCC_ClockDivider in the GDC subsystem control module. It specifies the divider used to generate the clock from reference clock for peripheral only.
After setting the register field RPCC_ClockDiver, to provide the HyperBus interface clock, the register field RPCC_ClockEnable in the RPCC_DomainControl should be set 1.
The HyperBus interface clock cannot be changed in operating the HyperBus Interface.
To change the frequency the HyperBus interface clock:

1. Write 0 to the register field RPCC_ClockEnable in the register of RPCC_DomainControl.
2. Stop providing the reference clock for peripheral.
3. Modify the register field RPCC_ClockDivider in the register of RPCC_ClockDivider.
4. Write 1 to the register field RPCC_ClockEnable in the register of RPCC_DomainControl.

Notes:

- *To make sure maximum frequency of the HyperBus interface clock, refer to related data sheet.*

3.6 SDRAM Interface Clock Setup

The SDRAM interface clock frequency used in the GDC subsystem can be setup using register field SDRAMC_ClockDivider in the register of SDRAMC_ClockDivider in the GDC subsystem control module. It specifies the divider used to generate the clock from reference clock for peripherals only.
After setting the register field of SDRAMC_ClockDivider, to provide the SDRAM interface clock, the register field SDRAMC_ClockEnable in the SDRAMC_DomainControl should be set 1.
After hardware reset or software reset, to activate SDRAM controller, write 0 to register field SDRAMC_SoftwareReset in the SDRAMC_DomainControl.
The SDRAM interface clock can be changed in operating SDRAM interface.

Notes:

- *Decimal part of the SDRAMC_ClockDivider field should be “0x00”.*
- *To shut down the SDRAM controller, setting 1 to the field of SDRAMC_SoftwareReset can be allowed. To re-activate the SDRAM controller, setting 0 again to the field cannot be allowed.*
- *To re-activate the SDRAM controller after the SDRAM controller is shut down by setting 1 to the field of SDRAMC_SoftwareReset, it is required to issue software reset for the GDC subsystem. Refer to Chapter 2 for more information.*
- *To make sure maximum frequency of the SDRAM clock, refer to related data sheet*

3.7 QSPI Interface Clock Setup

The QSPI interface clock frequency used in the GDC subsystem can be setup using register field HSSPIC_ClockDivider in the GDC subsystem control module. It specifies the divider used to generate the clock from reference clock for peripheral only.
The clock frequency generated by this divider has to be two times of the output clock frequency of external QSPI interface.
After setting the register field HSSPIC_ClockDivider, to provide the QSPI interface clock, the register field HSSPIC_ClockEnable in the HSSPIC_DomainControl should be set 1.
After hardware reset or software reset, to activate HSSPI controller, write 0 to register field HSSPIC_SoftwareReset in the HSSPIC_DomainControl.
The QSPI interface clock can be changed in operating QSPI interface.

Notes:

- *Decimal part of the SDRAMC_ClockDivider field should be 0x00.*
- *To shut down the QSPI controller, setting 1 to the field of HSSPIC_SoftwareReset can be allowed. To re-activate the SDRAM controller, setting 0 again to the field cannot be allowed.*
- *To re-activate the QSPI controller after the QSPI controller is shut down by setting 1 to the field of HSSPIC_SoftwareReset, it is required to issue software reset for the GDC subsystem. Refer to Chapter 2 for more information.*
- *To make sure maximum frequency of the QSPI interface clock, refer to related data sheet.*

3.8 Clock Frequency Setup Example

Examples of clock set up are described in this section.

Note:

- *To make sure maximum frequency of each clock, refer to related data sheet.*

3.8.1 Example1

3.8.1.1 Register Field Setting

Register Field	Setting Value	Remarks
GSSEN *1	0b1	Enables output of CLKPLL_GDC
GPINC *1	0b0	Selects external main oscillator for PLL_GDC input clock. In this case, the external main oscillator generates 4 MHz clock for example.
GPLLEN *1	0b0	Enables PLL_GDC
GPOWT *1	0b000	Sets PLL_GDC output clock stabilization time to Approx. 128 µs
GPLLK *1	1	Input clock PLL_GDC sets 4 MHz
GPLLN *1	99	PLL_GDC generates 400 MHz clock
PCG *1	0b0	This field does not need to be set to 1
PSEL *1	0b0	Selects PLL_GDC output for Reference clock for peripherals
ACG *1	0b0	This field does not need to be set to 1.
ASEL *1	0b00	Selects PLL_GDC output for Reference clock for GDC
RESETN *1	0b0	Disables software reset for GDC subsystem.
TEN *1	0b0	Stop oscillation as Timer mode.
GDCClockSelect *2	0x0300	Sets division ratio 3.0 for generating GDC clock
CNFIGClockSelect *2	0b001	Sets division ratio 2 for generation CONFIG clock
dsp0_Clock_Divider *2	0x2150	Sets division ratio 33.3125 for generating dsp0 clock
SDRAMC_ClockDivider *2	0x0500	Sets division ratio 5.0 for generating SDRAM interface clock
RPCC_ClockDivider *2	0b000	Set division ration 4 for generating HyperBus interface clock

*1: Refer to Chapter 2.4 for more information.

*2: Refer to Chapter 3.4 for more information.

3.8.1.2 Output Frequency of Each Clock

Output Clock	Frequency	Remarks
GDC clock	133 MHz	400 MHz divided by 3.0 equals 133 MHz
CONFIG clock	66 MHz	133 MHz divided by 2 equals 66 MHz
dsp0_clock	12.0075 MHz	400 MHz divided by 33.3125 equals 12.0075 MHz
Dot clock for external TFT	6.00375 MHz	Dot clock frequency for external TFT panel is divided by 2 in the GDC Core automatically.
SDRAM interface clock	80 MHz	400 MHz divided by 5.0 equals 80 MHz
HyperBus interface clock	100 MHz	400 MHz divided by 4 equals 100 MHz

3.8.2 Example2

3.8.2.1 Register Field Setting

Register Field	Setting Value	Remarks
GSSEN *1	0b1	Enables output of CLKPLL_GDC
GPINC *1	0b0	Selects external main oscillator for PLL_GDC input clock. In this case, the external main oscillator generates 20 MHz clock for example.
GPLLEN *1	0b1	Enables PLL_GDC
GPOWT *1	0b000	Sets PLL_GDC output clock stabilization time to Approx. 128 µs
GPLLK *1	1	Input clock PLL_GDC sets 10 MHz
GPLLN *1	31	PLL_GDC generates 320 MHz clock
PCG *1	0b0	This field does not need to be set to 1/
PSEL *1	0b0	Selects PLL_GDC output for Reference clock for peripherals
ACG *1	0b0	This field does not need to be set to 1.
ASEL *1	0b00	Selects PLL_GDC output for Reference clock for GDC
RESETN *1	0b0	Disables software reset for GDC subsystem.
TEN *1	0b0	Stop oscillation as Timer mode.
GDCClockSelect *2	0x0200	Sets division ratio 2.0 for generating GDC clock
CNFIGClockSelect *2	0b001	Sets division ratio 2 for generation CONFIG clock
dsp0_Clock_Divider *2	0x1A90	Sets division ratio 26.5625 for generating dsp0 clock
SDRAMC_ClockDivider *2	0x0400	Sets division ratio 4.0 for generating SDRAM interface clock
HSSPIC_ClockDivider *2	0x0200	Set division ration 4 for generating HyperBus interface clock

*1: Refer to Chapter 2.4 for more information.

*2: Refer to Chapter 3.4 for more information.

3.8.2.2 Output Frequency of Each Clock

Output Clock	Frequency	Remarks
CLKPLL_GDC	320 MHz	
GDC clock	160 MHz	320 MHz divided by 2.0 equals 160 MHz
CONFIG clock	80 MHz	160 MHz divided by 2 equals 80 MHz
dsp0_clock	12.0075 MHz	320 MHz divided by 26.5625 equals 12.047
Dot clock for external TFT	6.02352 MHz	Dot clock frequency for external TFT panel is divided by 2 in the GDC Core automatically.
SDRAM interface clock	80 MHz	320 MHz divided by 4.0 equals 80 MHz
QSPI interface clock	160 MHz	320 MHz divided by 2.0 equals 160 MHz. Clock frequency for external QSPI memories is divided by 2 in the QSPI interface controller automatically.

4. Registers

This section describes function and operation of the register for software interface of the GDC subsystem control module.

Notes:

- *The registers in this module can be accessed by word only.*
- *Either byte access or half word access causes a bus error response.*

Registers of the subsystem Control

The following registers are available for each instance of the module.

Abbreviation	Register Name	Reference
LockUnlock	LockUnlock	4.1
LockStatus	LockStatus	4.2
TEST (Reserved)	TEST (Reserved)	4.3
CnfigClockControl	CnfigClockControl	4.4
VRamInterruptEnable	VRamInterruptEnable	4.5
TEST (Reserved)	TEST (Reserved)	4.6
VraminterruptClear	VraminterruptClear	4.7
VramInterruptStatus	VramInterruptStatus	4.8
ExtFlashDevSelect	ExtFlashDevSelect	4.9
VramRemapDisable	VramRemapDisable	4.10
PanicSwitch	PanicSwitch	4.11
GDC_ClockDivider	GDC_ClockDivider	4.12
WkupTriggerMask	WkupTriggerMask	4.13
ClockDomainStatus	ClockDomainStatus	4.14

Abbreviation	Register Name	Reference
dsp0_LockUnlock	dsp0_LockUnlock	4.15
dsp0_LockStatus	dsp0_LockStatus	4.16
dsp0_ClockDivider	dsp0_ClockDivider	4.17
dsp0_DomainControl	dsp0_DomainControl	4.18
dsp0_ClockShift	dsp0_ClockShift	4.19
TEST (Reserved)	TEST (Reserved)	4.20
dsp0_PowerEnControl	dsp0_PowerEnControl	4.21
dsp0_ClockGateModeControl	dsp0_ClockGateModeControl	4.22
dsp0_ClockGateControl	dsp0_ClockGateControl	4.23

Abbreviation	Register Name	Reference
SDRAMC_ClockDivider	SDRAMC_ClockDivider	4.24
SDRAMC_DomainControl	SDRAMC_DomainControl	4.25
HSSPIC_ClockDivider	HSSPIC_ClockDivider	4.26
HSSPIC_DomainControl	HSSPIC_DomainControl	4.27
RPCC_ClockDivider	RPCC_ClockDivider	4.28
RPCC_DomainControl	RPCC_DomainControl	4.29

Abbreviation	Register Name	Reference
vram_LockUnlock	vram_LockUnlock	4.30
vram_LockStatus	vram_LockStatus	4.31
vram_sram_select	vram_sram_select	4.32
TEST (Reserved)	TEST (Reserved)	4.33
TEST (Reserved)	TEST (Reserved)	4.34
TEST (Reserved)	TEST (Reserved)	4.35
TEST (Reserved)	TEST (Reserved)	4.36
TEST (Reserved)	TEST (Reserved)	4.37
TEST (Reserved)	TEST (Reserved)	4.38
TEST (Reserved)	TEST (Reserved)	4.39
TEST (Reserved)	TEST (Reserved)	4.40
vram_aberraddr_s0	vram_aberraddr_s0	4.41
vram_aberraddr_s1	vram_aberraddr_s1	4.42
vram_arbiter_priority	vram_arbiter_priority	4.43

4.1 LockUnlock

The LockUnlock writes key codes of this address block.

The protection status is changed by writing one of the following key values to this field. Writing illegal key code results a bus error response. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

Register functions

[bit31:0] LockUnlock : Protection key of this address block setting bits

The protection status is changed by writing one of the following key values to this field.

When lock protection is active, no write but only read access is possible to all registers of this address block. When privilege protection is active, only privileged read and write access is possible. Both protections can be active at the same time. Reading this register results in an error response.

bit[31:0]	Description
0x5651F763	lock_key: Decrements the unlock counter. When the counter value is null, lock protection is active. Reset counter value is 1.
0x691DB936	unlock_key: Increments the unlock counter. Max allowed value is 15
0xAEE95CDC	privilege_key: Enables privilege protection. Disabled after reset.
0xB5E2466E	unprivilege_key: Disables privilege protection.
0xFBE8B1E6	freeze_key: Freezes current protection status. Writing keys to this register has no more effect until reset.

4.2 LockStatus

The LockStatus indicates protection status of this address block

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							Freeze Status
Attribute	R							R
Initial value	0b0000000							0b0

bit	7	6	5	4	3	2	1	0
Field	Reserved			Privilege Status	Reserved			Lock Status
Attribute	R			R	R			R
Initial value	0b000			0b0	0b000			0b0

Register functions

[bit31:9] Reserved: Reserved bits

[bit8] FreezeStatus: Current status of freeze status

Bit	Description
0	Protection status can be changed
1	Cannot be changed

[bit7:5] Reserved: Reserved for future use

[bit4] PrivilegeStatus: Current status of privilege protection

Bit	Description
0	Current status of privilege protection is inactive.
1	Current status of privilege protection is active.

[bit3:1] Reserved: Reserved bits

[bit0] LockStatus: Current status of lock protection

bit	Description
0	Current status of lock protection is inactive.
1	Current status of lock protection is active.

4.3 TEST (Reserved)

This register is implemented for internal device test purposes. When writing this register, it should be set to the initial value.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved				Reserved			
Attribute	R/W				R/W			
Initial value	0x2				0x2			

bit	23	22	21	20	19	18	17	16
Field	Reserved				Reserved			
Attribute	R/W				R/W			
Initial value	0x4				0x4			

bit	15	14	13	12	11	10	9	8
Field	Reserved				Reserved			
Attribute	R/W				R/W			
Initial value	0x1				0x4			

bit	7	6	5	4	3	2	1	0
Field	Reserved				Reserved			
Attribute	R/W				R/W			
Initial value	0x1				0x0			

4.4 CnfigClockControl

CnfigClockControl sets CONFIG clock generation. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved					ConfigClockSelect		
Attribute	-					R/W		
Initial value	0b00000					0b001		

Register functions

[bit31:8] Reserved: Reserved bits

0x000000 is read from these bits.
Set 0x000000 to these bits when writing.

[bit7:3] Reserved: Reserved bits

0b00000 is read from these bits.
Set 0b00000 to these bits when writing.

[bit2:0] ConfigClockSelect: CONFIG Clock division ratio setting bits

bit[2:0]	Description
000	Reserved. Do not set this value.
001	Division ratio : 2.
010	Division ratio : 3.
011	Division ratio : 4.
100	Division ratio : 5.
101	Division ratio : 6.
110	Division ratio : 7.
111	Division ratio : 8.

4.5 VRamInterruptEnable

The VramInterruptEnable enables/disables interrupt of VRAM ECC error.

Register cofiguration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved						VramInterruptEnableSec1	VramInterruptEnableSec0
Attribute	-						R/W	R/W
Initial value	0b000000						0b1	0b1

Register functions

[bit31:8] Reserved: Reserved bits

0x000000 is read from these bits.
Set 0x000000 to these bits when writing.

[bit7:2] Reserved: Reserved bits

0b000000 is read from these bits.
Set 0b000000 to these bits when writing.

[bit1] VramInterruptEnableSec1: Interrupt control of VRAM ECC error for VRAM port1

bit	Description
0	Disable interrupt
1	Enable interrupt

Note:

- *This field can be programmed only once after reset. A second attempt at programming this will cause an error response and no change to the enable.*

[bit0] VramInterruptEnableSec0: Interrupt control of VRAM ECC error for VRAM port0

bit	Description
0	Disable interrupt
1	Enable interrupt

Note:

- *This field can be programmed only once after reset. A second attempt at programming this will cause an error response and no change to the enable.*

4.6 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved						Reserved	Reserved
Attribute	-						W	W
Initial value	0b000000						0b0	0b0

Register functions

[bit31:2] Reserved: Reserved bits

Do not read these bits.

Set initial value to these bits when writing.

[bit1] Reserved: (for internal device test purposes)

Bit	Description
0	(for internal device test purpose)
1	(for internal device test purpose)

Note:

- *This field can be written as 0b0 only.*

[bit0] Reserved: (for internal device test purposes)

bit	Description
0	(for internal device test purpose)
1	(for internal device test purpose)

Note:

- *This field can be written as 0b0 only.*

4.7 VramInterruptClear

The VramInterruptClear clears interrupt of VRAM ECC error.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	7	6	5	4	3	2	1	0
Field	Reserved						VramInterruptClearSec1	VramInterruptClearSec0
Attribute	-						W	W
Initial value	0b000000						0b0	0b0

Register function

[bit31:2] Reserved: Reserved bits

Do not read these bits.

Set the initial value to these bits when writing.

[bit1] VramInterruptClearSec1: Clear interrupt register

Bit	Description
0	Do not write 0b0 to this field.
1	Clear interrupt field of VramInterruputStatusSec1 in the VramInterrupt status register.

[bit0] VramInterruptClearSec0: Clear interrupt register

bit	Description
0	Do not write 0b0 to this field.
1	Clear interrupt field of VramInterruputStatusSec1 in the VramInterrupt status register.

4.8 VRamInterrunptStatus

VRamInterruptStatus indicates status of VRAM ECC error interrupt.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	7	6	5	4	3	2	1	0
Field	Reserved						VramInterrupt StatusSec1	VramInterrupt StatusSec0
Attribute	-						R	R
Initial value	0b000000						0b0	0b0

Register function

[bit31:2] Reserved: Reserved bits

The initial value if read from these bits.

Do not write to these bits.

[bit1] VramInterruptStatusSec1: Indicator of VRAM Interrupt status

bit	Description
0	No interrupt of VRAM ECC error at VRAM access port1.
1	Caused interrupt of VRAM ECC error at VRAM access port1

[bit0] VramInterruptClearSec0: Indicator of VRAM Interrupt status

bit	Description
0	No interrupt of VRAM ECC error at VRAM access port1 has been asserted.
1	Interrupt of VRAM ECC error at VRAM access port1 has been asserted.

4.9 ExtFlashDevSelect

ExtFlashDevSelect selects either QSPI flash or HyperFlash as external flash memory.

register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	7	6	5	4	3	2	1	0
Field	Reserved							ExtFlashDevSelect
Attribute	-							R/W
Initial value	0b0000000							0b1

Register functions

[bit31:1] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit0] ExtFlashDevSelect: External memory device selection bit

bit	Description
0	Selects HyperFlash as external flash memory.
1	Selects QSPI flash as external flash memory.

4.10 VramRemapDisable

VramRemapDisable sets either VRAM remap mode or VRAM non-remap mode.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	7	6	5	4	3	2	1	0
Field	Reserved							VramRemapDisable
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit31:1] Reserved: Reserved bits

The initial value is read from these bits

Set the initial value to these bits when writing.

[bit0] VramRemapDisable: VRAM address remap or non-remap selection bit

bit	Description
0	Selects remap mode.
1	Selects non-remap mode.

4.11 PanicSwitch

PanicSwitch selects either Panic display mode or normal display mode.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	7	6	5	4	3	2	1	0
Field	Reserved							PanicSwitch
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit31:1] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit0] PanicSwitch: Panic display mode or normal display mode selection bit

bit	Description
0	Disable panic display mode.
1	Enable panic display mode.

Note:

- *For more information, Refer to the Peripheral Manual GDC (Core) part.*

4.12 GDC_ClockDivider

GDC_ClockDivider sets GDC clock generation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	GDCClockSelect(integral part)							
Attribute	R/W							
Initial value	0x04							

bit	15	14	13	12	11	10	9	8
Field	GDCClockSelect(decimal part)							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute	-							
Initial value	0x00							

[bit31:24] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit23:8] GDCClockSelect: Controls GDC clock generation.

bit15:0	Description
0x0200	Division ratio : 2
0x0300	Division ratio : 3
0x0400	Division ratio : 4
0x0500	Division ratio : 5
	(Continued)
0xFF00	Division ratio : 255

Notes:

- *This field must set at least 2.0.*
- *The decimal part of this field can be written 0x00 only.*
- *This field can be written during operation.*

[bit7:0] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

4.13 WkupTriggerMask

Wkup TrigerMask is a register to mask the CPU wake-up trigger, which is used to transfer from timer-mode to run-mode.
For details about Timer-mode, refer to FM4 Family Peripheral Manual.
This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved					WTrigMaskRpc	WtrigMaskSdram	WTrigMaskQspi
Attribute	-					R/W	R/W	R/W
Initial value	0b00000					0b0	0b0	0b0

bit	23	22	21	20	19	18	17	16
Field	Reserved					WTrigMaskGe		
Attribute	-					R/W		
Initial value	0b00000					0b000		

bit	15	14	13	12	11	10	9	8
Field	WTrigMaskGe							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	WTrigMaskGe							
Attribute	R/W							
Initial value	0x00							

Register function

[bit31:27] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit26] WtrigMaskRpc: Wake up trigger mask for HyperBus interface

Wake-up trigger mask setting for CPU- low power consumption mode.
This bit corresponds to IENOn of HyperBus interface.

Bit	Description
0	Disable wake up trigger.
1	Enable wake up trigger.

[bit25] WtrigMaskSdram: Wake up trigger mask for SDRAM interface

Wake-up trigger mask setting for CPU- low power consumption mode.
This bit corresponds to MerrInt of SDRAM interface.

bit	Description
0	Disable wake up trigger.
1	Enable wake up trigger.

[bit24] WtrigMaskQspi: Wake up trigger mask for QSPI interface

Wake-up trigger mask setting for CPU- low power consumption mode.
This bit corresponds to IRQ_FAULT of QSPI interface.

bit	Description
0	Disable wake up trigger.
1	Enable wake up trigger.

[bit23:19] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit18:0] WTrigMaskGe: Wake up trigger mask for GDC Core

Wake-up trigger mask setting for CPU- low power consumption mode.
Each bit corresponds to irq[18:0] of the GDC core interrupts.

bit18:0	Description
0	Disable wake up trigger.
1	Enable wake up trigger.

4.14 ClockDomainStatus

ClockDomainstatus indicates status of each clock domain. Make sure these four bits are set to 1 before accessing the bits' corresponding domains. Accessing domains that are not yet operational causes bus to lock.

Register configration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x0							

bit	7	6	5	4	3	2	1	0
Field	Reserved				Hsspi Clock Domain Ready	Rpc Clock Domain Ready	Sdram Clock Domain Ready	DspClock Domain Ready
Attribute	-				R/W	R/W	R/W	R/W
Initial value	0x0				0b0	0b0	0b0	0b0

Register functions

[bit31:4] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit3] HsspiClockDomainReady: Clock status of QSPI interface clock domain

Bit	Description
0	This clock domain is not ready
1	This clock domain can be operated

[bit2] RpcClockDomainReady: Clock status of HyperBus interface clock domain

bit	Description
0	This clock domain is not ready
1	This clock domain can be operated

[bit1] SdramClockDomainReady: Clock status of SDRAM interface clock domain

Bit	Description
0	This clock domain is not ready
1	This clock domain can be operated

[bit0] DspClockDomainReady: Clock status of Display clock domain

Bit	Description
0	This clock domain is not ready
1	This clock domain can be operated

4.15 dsp_LockUnlock

The dsp_LockUnlock writes key codes of this address block.

The protection status is changed by writing one of the following key values to this field. Writing illegal key code results a bus error response. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	dsp_LockUnlock							
Attribute	W							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	dsp_LockUnlock							
Attribute	W							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	dsp_LockUnlock							
Attribute	W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	dsp_LockUnlock							
Attribute	W							
Initial value	0x00							

Register functions

[bit31:0] dsp_LockUnlock : Protection key of this address block setting bits

The protection status is changed by writing one of the following key values to this field.

When lock protection is active, no write but only read access is possible to all registers of this address block. When privilege protection is active, only privileged read and write access is possible. Both protections can be active at the same time. Reading this register results in an error response.

bit[31:0]	Description
0x5651F763	lock_key: Decrements the unlock counter. When the counter value is null, lock protection is active. Reset counter value is 1.
0x691DB936	unlock_key: Increments the unlock counter. Max allowed value is 15
0xAEE95CDC	privilege_key: Enables privilege protection. Disabled after reset.
0xB5E2466E	unprivilege_key: Disables privilege protection.
0xFBE8B1E6	freeze_key: Freezes current protection status. Writing keys to this register has no more effect until reset.

4.16 dsp_LockStatus

dsp_LockStatus indicates protection status of this address block

Register configuraion

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							dsp_ Freeze Status
Attribute	R							R
Initial value	0b0000000							0b0

bit	7	6	5	4	3	2	1	0
Field	Reserved			dsp_ Privilege Status	Reserved			dsp_ Lock Status
Attribute	R			R	R			R
Initial value	0b000			0b0	0b000			0b0

Register functions

[bit31:9] Reserved: Reserved bits

The initial value is read from these bits.

[bit8] dsp_FreezeStatus: Current status of freeze status

Bit	Description
0	Protection status can be changed
1	Cannot be changed

[bit7:5] Reserved: Reserved bits

The initial value is read from these bits.

[bit4] dsp_PrivilegeStatus: Current status of privilege protection

bit	Description
0	Current status of privilege protection is inactive.
1	Current status of privilege protection is active.

[bit3:1] Reserved: Reserved bits

The initial value is read from these bits.

[bit0] dsp_LockStatus: Current status of lock protection

bit	Description
0	Current status of lock protection is inactive.
1	Current status of lock protection is active.

4.17 dsp0_ClockDivider

dsp0_ClockDivider sets display Clock divider ratio. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	dsp0_ClockDivider (integral part)							
Attribute	R/W							
Initial value	0x41							

bit	15	14	13	12	11	10	9	8
Field	dsp0_ClockDivider (decimal part)							
Attribute	R/W							
Initial value	0xE0							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute	-							
Initial value	0x00							

Register functions

[bit31:24] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit23:8] dsp0_ClockDivider: Division ratio from the Reference clock for peripherals.

bit15:0	Description
0x0200	Division ratio: 2.0
0x0201	Division ratio: $2.0 + 2^{-8}$
0x0202	Division ratio: $2.0 + 2^{-7}$
0x0203	Division ratio: $2.0 + 2^{-7} + 2^{-8}$
	(Continued)
0xFFFF	Division ratio: $255 + 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-6} + 2^{-7} + 2^{-8}$

Notes:

- *This field must set at least 2.0.*
- *To make sure maximum frequency of the display clock, refer to related data sheet.*

[bit7:0] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

4.18 dsp0_DomainControl

dsp0_DomainControl sets display clock domain control operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							dsp0_ Software Reset
Attribute	-							R/W
Initial value	0b0000000							0b1

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							dsp0_ Clock Enable
Attribute	-							R/W
Initial value	0b0000000							0b0

Register function

[bit31:17] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit16] dsp0_SoftwareReset: Display clock domain software reset

bit	Description
0	Display clock domain operational.
1	Display clock domain in reset state.

Note:

- *Setting 0 to this field can be allowed after either hardware reset or software reset only.*

[bit15:1] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit0] dsp0_ClockEnable: Display clock output control

bit	Description
0	Disables display clock generation.
1	Enables display clock generation.

4.19 dsp0_ClockShift

The dsp0_ClockShift is a register for display clock shift. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	dsp0_ClockOffset							
Attribute	R/W							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							dsp0_ Clock Invert
Attribute	-							R/W
Initial value	0b0000000							0x1

Register functions

[bit31:24] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit23:16] dsp0_ClockOffset: Display clock phase setting bits

bit7:0	Description
0x00 to 0xFF	Sets the offset in reference clock cycles for the display clock output with reference to the data output. This has to be smaller than the integer part of dsp0_ClockDivider. This setting shift the data output to forward part of the display clock output.

[bit31:24] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit0] dsp0_ClockInvert: Display clock polarity setting bit

bit	Description
0	Not invert display clock output. At this time, data output is toggled with reference to rise-edge of display clock.
1	Invert display clock output. At this time, data output is toggled with reference to fall-edge of display clock.

4.20 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							Reserved
Attribute	-							R/W
Initial value	0x00							0b0

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved						
Attribute	-	R/W						
Initial value	0b0	0b0000000						

[bit31:27] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit16] Reserved: (for internal device test purposes)

Note:

- *This field can be written as 0b0 only.*

[bit15:7] Reserved: Reserved bit

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit6:0] Reserved: (for internal device test purpose)

Note:

- *This field can be written as 0b0000000 only.*

4.21 dsp0_PowerEnControl

The dsp0_PowerEnControl is a register for display Power Enable Signal Control. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							Power_ Enable
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit31:1] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing

[bit0] Power_Enable: Power control of external TFT panel setting bit

bit	Description
0	PowerEnable signal is held LOW
1	Assert PowerEnable signal HIGH

4.22 dsp0_ClockGateModeLock

The dsp0_ClockGateModeLock is a register to change the protection to change dsp0_ClockGateControl value. Writing illegal key code or byte and half word access results an error response.

This register can be written during operation.

Register configuratiion

bit	31	30	29	28	27	26	25	24
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	LockUnlock							
Attribute	W							
Initial value	0x00							

Register functions

[bit31:0] LockUnlock : Protection of this address block setting bits

bit[31:0]	Description
0x5651F763	lock_key: Decrements the unlock counter. When the counter value is null, lock protection is active. Reset counter value is 1.
0x691DB936	unlock_key: Increments the unlock counter. Max allowed value is 15
0xAEE95CDC	privilege_key: Enables privilege protection. Disabled after reset.
0xB5E2466E	unprivilege_key: Disables privilege protection.
0xFBE8B1E6	freeze_key: Freezes current protection status. Writing keys to this register has no more effect until reset.

4.23 dsp0_ClockGateControl

The dsp0_ClockGateControl is a register for display Clock Gate Control.

This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							ClockGate_Enable
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit31:1] Reserved: Reserved for future use

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit0] ClockGate_Enable: Dot clock for external TFT panel control bit

bit	Description
0	Enables output of Dot clock for external TFT panel.
1	Disables output of Dot clock for external TFT panel.

Note:

- *To use this function, set TCON_CTRL_Bypass register in the GDC core to 0. For more information, refer to Peripheral Manual GDC (Core) part.*

4.24 SDRAMC_ClockDivider

The SDRAMC_ClockDivider sets division ratio of SDRAM interface. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	SDRAMC_ClockDivider (integral part)							
Attribute	R/W							
Initial value	0x04							

bit	15	14	13	12	11	10	9	8
Field	SDRAMC_ClockDivider (decimal part)							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute	-							
Initial value	0x00							

Register function

[bit31:24] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit23:8] SDRAMC_ClockDivider: Division ratio from the Reference clock for peripherals.

bit15:0	Description
0x0000	Do not set this value to this field.
0x0100	Do not set this value to this field.
0x0200	Division ratio : 2
0x0300	Division ratio : 3.
0x0400	Division ratio : 4.
	.(Continued)
0xFE00	Division ratio: 254.
0xFF00	Division ratio: 255

Notes:

- *This field must set at least 2.0.*
- *The decimal part of this field can be written as 0x00 only.*

[bit7:0] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

4.25 SDRAMC_DomainControl

The SDRAMC_DomainControl sets operation of SDRAM interface clock domain.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							SDRAMC_ Software Reset
Attribute	-							R/W
Initial value	0b0000000							0b1

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							SDRAMC_ Clock Enable
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit31:17] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit16] SDRAMC_SoftwareReset: Software for SDRAM interface clock domain

bit	Description
0	SDRAM interface clock domain operational.
1	SDRAM interface clock domain in reset state.

Note:

- *Setting 0 to this field can be allowed after either hardware reset or software reset only.*

[bit15:1] Reserved: Reserved bits

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit0] SDRAMC_ClockEnable: SDRAM interface clock output control

bit	Description
0	Disables SDRAM interface clock generation.
1	Enables SDRAM interface clock generation.

Note:

- *This register can be written during operation.*

4.26 HSSPIC_ClockDivider

The HSSPIC_ClockDivider sets division ratio of QSPI interface. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	HSSPIC_ClockDivider (integral part)							
Attribute	R/W							
Initial value	0x04							

bit	15	14	13	12	11	10	9	8
Field	HSSPIC_ClockDivider (decimal part)							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute	-							
Initial value	0x00							

Register functions

[bit31:24] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit23:8] HSSPIC_ClockDivider: Division ratio from the Reference clock for peripherals.

bit15:0	Description
0x0000	Do not set this value to this field.
0x0100	Do not set this value to this field.
0x0200	Division ratio : 2
0x0300	Division ratio : 3.
0x0400	Division ratio : 4.
	.(Continued)
0xFE00	Division ratio: 254.
0xFF00	Division ratio: 255

Notes:

- *This field must set at least 2.0.*
- *The decimal part of this field can be written as 0x00 only.*

[bit7:0] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

4.27 HSSPIC_DomainControl

The HSSPI_DomainControl sets operation of QSPI interface clock domain.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							HSSPIC_ Software Reset
Attribute	-							R/W
Initial value	0b0000000							0b1

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							HSSPIC_ Clock Enable
Attribute	-							R/W
Initial value	0b0000000							0b0

Register functions

[bit31:17] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit16] HSSPIC_SoftwareReset: QSPI interface clock domain software reset

bit	Description
0	QSPI interface clock domain operational.
1	QSPI interface clock domain in reset state.

Note:

- *Setting 0 to this field can be allowed after either hardware reset or software reset only.*

[bit15:1] Reserved: Reserved bit

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit0] HSSPIC_ClockEnable: QSPI interface clock output control

bit	Description
0	Disables QSPI interface clock generation.
1	Enables QSPI interface clock generation.

Note:

- *This register can be written during operation.*

4.28 RPCC_ClockDivider

The RPCC_ClockDivider sets division ratio of HyperBus interface.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved					RPCC_ClockDivider		
Attribute	-					R/W		
Initial value	0x00					0b000		

Register fuction

[bit31:3] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit2:0] RPCC_ClockDivider: Division ratio from the Reference clock for peripherals.

bit2:0	Description
000	Division ratio: 4
001	Division ratio: 8
010	Division ratio: 12
011	Division ratio: 16
100	Division ratio: 20
101	Division ratio: 24
110	Division ratio: 28
111	Division ratio: 32

Note:

- *This field cannot be written during operation. For modify contents of this field, refer to 3.5 HyperBus Interface Clock Setup.:*

4.29 RPCC_DomainControl

The RPCC_DomainControl sets operation of HyperBus interface clock domain.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							Reserved
Attribute	-							R/W
Initial value	0x00							0x1

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							RPCC_ ClockEnable
Attribute	-							R/W
Initial value	0x00							0x0

Register function

[bit31:17] Reserved: Reserved for future use

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit16] Reserved: (for internal device test purpose)

Note:

- *This field can only be written 0b1 only.*

[bit15:1] Reserved: Reserved for future use

[bit0] RPCC_ClockEnable: HyperBus interface clock output control

bit	Description
0	Disables HyperBus interface clock generation.
1	Enables HyperBus interface clock generation.

Note:

- *This register can be written during operation.*

4.30 vram_LockUnlock

The vram_LockUnlock writes key codes of this address block.

The protection status is changed by writing one of the following key values to this field. Writing illegal key code results a bus error response. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	vram_LockUnlock							
Attribute	W							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	vram_LockUnlock							
Attribute	W							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	vram_LockUnlock							
Attribute	W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	vram_LockUnlock							
Attribute	W							
Initial value	0x00							

Register functions

[bit31:0] vram_LockUnlock: Protection key of this address block setting bit

The protection status is changed by writing one of the following key values to this field.

When lock protection is active, no write but only read access is possible to all registers of this address block. When privilege protection is active, only privileged read and write access is possible. Both protections can be active at the same time. Reading this register results in an error response.

bit[31:0]	Description
0x5651F763	lock_key: Decrements the unlock counter. When the counter value is null, lock protection is active. Reset counter value is 1.
0x691DB936	unlock_key: Increments the unlock counter. Max allowed value is 15
0xAEE95CDC	privilege_key: Enables privilege protection. Disabled after reset.
0xB5E2466E	unprivilege_key: Disables privilege protection.
0xFBE8B1E6	freeze_key: Freezes current protection status. Writing keys to this register has no more effect until reset.

4.31 vram_LockStatus

The vram_LockStatus indicates protection status of this address block.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							vram_ Freeze Status
Attribute	R							R
Initial value	0b0000000							0b0

bit	7	6	5	4	3	2	1	0
Field	Reserved			vram_ Privilege Status	Reserved			vram_ Lock Status
Attribute	R			R	R			R
Initial value	0b000			0b0	0b000			0b0

Register functions

[bit31:9] Reserved: Reserved for future use

The initial value is read from these bits.

[bit8] vram_FreezeStatus: Current status of freeze status

bit	Description
0	Protection status can be changed
1	Cannot be changed

[bit7:5] Reserved: Reserved for future use

The initial value is read from these bits.

[bit4] vram_PrivilegeStatus: Current status of privilege protection

bit	Description
0	Current status of privilege protection is inactive.
1	Current status of privilege protection is active.

[bit3:1] Reserved: Reserved for future use

The initial value is read from these bits.

[bit0] vram_LockStatus: Current status of lock protection

bit	Description
0	Current status of lock protection is inactive.
1	Current status of lock protection is active.

4.32 vram_sram_select

The vram_sram_select sets the size of the ECC protected memory region selection.

This register can be written before VRAM access.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved.							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved.							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved.				vram_sram_select			
Attribute	-				R/W			
Initial value	0x0				0x0			

bit	7	6	5	4	3	2	1	0
Field	vram_sram_select							
Attribute	R/W							
Initial value	0x00							

Register functions

[bit3:12] Reserved: Reserved for future use

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit11:0] vram_sram_select: Selects the size of the ECC protected region

For detail, refer to Table 4-1, Table 4-2, Table 4-3, and Table 4-4.

Table 4-1 ECC Protected Region (1/4)

sram_select	ECC-protected user space			Reagion reserved for ECC			ECC-unprotected user space		
	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]
0	–	–	0	–	–	0	0x00000	0x7FFFF	512
1	0x00000	0x007F8	2	0x00800	0x00FF8	2	0x01000	0x7FFFF	508
2	0x00000	0x00FF8	4	0x01000	0x01FF8	4	0x02000	0x7FFFF	504
3	0x00000	0x017F8	6	0x01800	0x02FF8	6	0x03000	0x7FFFF	500
4	0x00000	0x01FF8	8	0x02000	0x03FF8	8	0x04000	0x7FFFF	496
5	0x00000	0x027F8	10	0x02800	0x04FF8	10	0x05000	0x7FFFF	492
6	0x00000	0x02FF8	12	0x03000	0x05FF8	12	0x06000	0x7FFFF	488
7	0x00000	0x037F8	14	0x03800	0x06FF8	14	0x07000	0x7FFFF	484
8	0x00000	0x03FF8	16	0x04000	0x07FF8	16	0x08000	0x7FFFF	480
9	0x00000	0x047F8	18	0x04800	0x08FF8	18	0x09000	0x7FFFF	476
10	0x00000	0x04FF8	20	0x05000	0x09FF8	20	0x0A000	0x7FFFF	472
11	0x00000	0x057F8	22	0x05800	0x0AFF8	22	0x0B000	0x7FFFF	468
12	0x00000	0x05FF8	24	0x06000	0x0BFF8	24	0x0C000	0x7FFFF	464
13	0x00000	0x067F8	26	0x06800	0x0CFF8	26	0x0D000	0x7FFFF	460
14	0x00000	0x06FF8	28	0x07000	0x0DFF8	28	0x0E000	0x7FFFF	456
15	0x00000	0x077F8	30	0x07800	0x0EFF8	30	0x0F000	0x7FFFF	452
16	0x00000	0x07FF8	32	0x08000	0x0FFF8	32	0x10000	0x7FFFF	448
17	0x00000	0x087F8	34	0x08800	0x10FF8	34	0x11000	0x7FFFF	444
18	0x00000	0x08FF8	36	0x09000	0x11FF8	36	0x12000	0x7FFFF	440
19	0x00000	0x097F8	38	0x09800	0x12FF8	38	0x13000	0x7FFFF	436
20	0x00000	0x09FF8	40	0x0A000	0x13FF8	40	0x14000	0x7FFFF	432
21	0x00000	0x0A7F8	42	0x0A800	0x14FF8	42	0x15000	0x7FFFF	428
22	0x00000	0x0AFF8	44	0x0B000	0x15FF8	44	0x16000	0x7FFFF	424
23	0x00000	0x0B7F8	46	0x0B800	0x16FF8	46	0x17000	0x7FFFF	420
24	0x00000	0x0BFF8	48	0x0C000	0x17FF8	48	0x18000	0x7FFFF	416
25	0x00000	0x0C7F8	50	0x0C800	0x18FF8	50	0x19000	0x7FFFF	412
26	0x00000	0x0CFF8	52	0x0D000	0x19FF8	52	0x1A000	0x7FFFF	408
27	0x00000	0x0D7F8	54	0x0D800	0x1AFF8	54	0x1B000	0x7FFFF	404
28	0x00000	0x0DFF8	56	0x0E000	0x1BFF8	56	0x1C000	0x7FFFF	400
29	0x00000	0x0E7F8	58	0x0E800	0x1CFF8	58	0x1D000	0x7FFFF	396
30	0x00000	0x0EFF8	60	0x0F000	0x1DFF8	60	0x1E000	0x7FFFF	392
31	0x00000	0x0F7F8	62	0x0F800	0x1EFF8	62	0x1F000	0x7FFFF	388

Table 4-2 ECC Protected Region (2/4)

sram_select	ECC-protected user space			Reagion reserved for ECC			ECC-unprotected user space		
	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]
32	0x00000	0xFFFFFFFFF8	0	0x00000	0xFFFFFFFFF8	0	0x00000	0x7FFFF	512
33	0x00000	0x007F8	2	0x00800	0x00FF8	2	0x01000	0x7FFFF	508
34	0x00000	0x00FF8	4	0x01000	0x01FF8	4	0x02000	0x7FFFF	504
35	0x00000	0x017F8	6	0x01800	0x02FF8	6	0x03000	0x7FFFF	500
36	0x00000	0x01FF8	8	0x02000	0x03FF8	8	0x04000	0x7FFFF	496
37	0x00000	0x027F8	10	0x02800	0x04FF8	10	0x05000	0x7FFFF	492
38	0x00000	0x02FF8	12	0x03000	0x05FF8	12	0x06000	0x7FFFF	488
39	0x00000	0x037F8	14	0x03800	0x06FF8	14	0x07000	0x7FFFF	484
40	0x00000	0x03FF8	16	0x04000	0x07FF8	16	0x08000	0x7FFFF	480
41	0x00000	0x047F8	18	0x04800	0x08FF8	18	0x09000	0x7FFFF	476
42	0x00000	0x04FF8	20	0x05000	0x09FF8	20	0x0A000	0x7FFFF	472
43	0x00000	0x057F8	22	0x05800	0x0AFF8	22	0x0B000	0x7FFFF	468
44	0x00000	0x05FF8	24	0x06000	0x0BFF8	24	0x0C000	0x7FFFF	464
45	0x00000	0x067F8	26	0x06800	0x0CFF8	26	0x0D000	0x7FFFF	460
46	0x00000	0x06FF8	28	0x07000	0x0DFF8	28	0x0E000	0x7FFFF	456
47	0x00000	0x077F8	30	0x07800	0x0EFF8	30	0x0F000	0x7FFFF	452
48	0x00000	0x07FF8	32	0x08000	0x0FFF8	32	0x10000	0x7FFFF	448
49	0x00000	0x087F8	34	0x08800	0x10FF8	34	0x11000	0x7FFFF	444
50	0x00000	0x08FF8	36	0x09000	0x11FF8	36	0x12000	0x7FFFF	440
51	0x00000	0x097F8	38	0x09800	0x12FF8	38	0x13000	0x7FFFF	436
52	0x00000	0x09FF8	40	0x0A000	0x13FF8	40	0x14000	0x7FFFF	432
53	0x00000	0x0A7F8	42	0x0A800	0x14FF8	42	0x15000	0x7FFFF	428
54	0x00000	0x0AFF8	44	0x0B000	0x15FF8	44	0x16000	0x7FFFF	424
55	0x00000	0x0B7F8	46	0x0B800	0x16FF8	46	0x17000	0x7FFFF	420
56	0x00000	0x0BFF8	48	0x0C000	0x17FF8	48	0x18000	0x7FFFF	416
57	0x00000	0x0C7F8	50	0x0C800	0x18FF8	50	0x19000	0x7FFFF	412
58	0x00000	0x0CFF8	52	0x0D000	0x19FF8	52	0x1A000	0x7FFFF	408
59	0x00000	0x0D7F8	54	0x0D800	0x1AFF8	54	0x1B000	0x7FFFF	404
60	0x00000	0x0DFF8	56	0x0E000	0x1BFF8	56	0x1C000	0x7FFFF	400
61	0x00000	0x0E7F8	58	0x0E800	0x1CFF8	58	0x1D000	0x7FFFF	396
62	0x00000	0x0EFF8	60	0x0F000	0x1DFF8	60	0x1E000	0x7FFFF	392
63	0x00000	0x0F7F8	62	0x0F800	0x1EFF8	62	0x1F000	0x7FFFF	388

Table 4-3 ECC Protected Region (3/4)

sram_select	ECC-protected user space			Reagion reserved for ECC			ECC-unprotected user space		
	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]
64	0x00000	0xFFFFFFFFF8	0	0x00000	0xFFFFFFFFF8	0	0x00000	0x7FFFF	512
65	0x00000	0x007F8	2	0x00800	0x00FF8	2	0x01000	0x7FFFF	508
66	0x00000	0x00FF8	4	0x01000	0x01FF8	4	0x02000	0x7FFFF	504
67	0x00000	0x017F8	6	0x01800	0x02FF8	6	0x03000	0x7FFFF	500
68	0x00000	0x01FF8	8	0x02000	0x03FF8	8	0x04000	0x7FFFF	496
69	0x00000	0x027F8	10	0x02800	0x04FF8	10	0x05000	0x7FFFF	492
70	0x00000	0x02FF8	12	0x03000	0x05FF8	12	0x06000	0x7FFFF	488
71	0x00000	0x037F8	14	0x03800	0x06FF8	14	0x07000	0x7FFFF	484
72	0x00000	0x03FF8	16	0x04000	0x07FF8	16	0x08000	0x7FFFF	480
73	0x00000	0x047F8	18	0x04800	0x08FF8	18	0x09000	0x7FFFF	476
74	0x00000	0x04FF8	20	0x05000	0x09FF8	20	0x0A000	0x7FFFF	472
75	0x00000	0x057F8	22	0x05800	0x0AFF8	22	0x0B000	0x7FFFF	468
76	0x00000	0x05FF8	24	0x06000	0x0BFF8	24	0x0C000	0x7FFFF	464
77	0x00000	0x067F8	26	0x06800	0x0CFF8	26	0x0D000	0x7FFFF	460
78	0x00000	0x06FF8	28	0x07000	0x0DFF8	28	0x0E000	0x7FFFF	456
79	0x00000	0x077F8	30	0x07800	0x0EFF8	30	0x0F000	0x7FFFF	452
80	0x00000	0x07FF8	32	0x08000	0x0FFF8	32	0x10000	0x7FFFF	448
81	0x00000	0x087F8	34	0x08800	0x10FF8	34	0x11000	0x7FFFF	444
82	0x00000	0x08FF8	36	0x09000	0x11FF8	36	0x12000	0x7FFFF	440
83	0x00000	0x097F8	38	0x09800	0x12FF8	38	0x13000	0x7FFFF	436
84	0x00000	0x09FF8	40	0x0A000	0x13FF8	40	0x14000	0x7FFFF	432
85	0x00000	0x0A7F8	42	0x0A800	0x14FF8	42	0x15000	0x7FFFF	428
86	0x00000	0x0AFF8	44	0x0B000	0x15FF8	44	0x16000	0x7FFFF	424
87	0x00000	0x0B7F8	46	0x0B800	0x16FF8	46	0x17000	0x7FFFF	420
88	0x00000	0x0BFF8	48	0x0C000	0x17FF8	48	0x18000	0x7FFFF	416
89	0x00000	0x0C7F8	50	0x0C800	0x18FF8	50	0x19000	0x7FFFF	412
90	0x00000	0x0CFF8	52	0x0D000	0x19FF8	52	0x1A000	0x7FFFF	408
91	0x00000	0x0D7F8	54	0x0D800	0x1AFF8	54	0x1B000	0x7FFFF	404
92	0x00000	0x0DFF8	56	0x0E000	0x1BFF8	56	0x1C000	0x7FFFF	400
93	0x00000	0x0E7F8	58	0x0E800	0x1CFF8	58	0x1D000	0x7FFFF	396
94	0x00000	0x0EFF8	60	0x0F000	0x1DFF8	60	0x1E000	0x7FFFF	392
95	0x00000	0x0F7F8	62	0x0F800	0x1EFF8	62	0x1F000	0x7FFFF	388

Table 4-4 ECC Protected Region (4/4)

sram_select	ECC-protected user space			Reagion reserved for ECC			ECC-unprotected user space		
	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]	start offset	end offset	capacity [KB]
96	0x00000	0xFFFFFFFFF8	0	0x00000	0xFFFFFFFFF8	0	0x00000	0x7FFFF	512
97	0x00000	0x007F8	2	0x00800	0x00FF8	2	0x01000	0x7FFFF	508
98	0x00000	0x00FF8	4	0x01000	0x01FF8	4	0x02000	0x7FFFF	504
99	0x00000	0x017F8	6	0x01800	0x02FF8	6	0x03000	0x7FFFF	500
100	0x00000	0x01FF8	8	0x02000	0x03FF8	8	0x04000	0x7FFFF	496
101	0x00000	0x027F8	10	0x02800	0x04FF8	10	0x05000	0x7FFFF	492
102	0x00000	0x02FF8	12	0x03000	0x05FF8	12	0x06000	0x7FFFF	488
103	0x00000	0x037F8	14	0x03800	0x06FF8	14	0x07000	0x7FFFF	484
104	0x00000	0x03FF8	16	0x04000	0x07FF8	16	0x08000	0x7FFFF	480
105	0x00000	0x047F8	18	0x04800	0x08FF8	18	0x09000	0x7FFFF	476
106	0x00000	0x04FF8	20	0x05000	0x09FF8	20	0x0A000	0x7FFFF	472
107	0x00000	0x057F8	22	0x05800	0x0AFF8	22	0x0B000	0x7FFFF	468
108	0x00000	0x05FF8	24	0x06000	0x0BFF8	24	0x0C000	0x7FFFF	464
109	0x00000	0x067F8	26	0x06800	0x0CFF8	26	0x0D000	0x7FFFF	460
110	0x00000	0x06FF8	28	0x07000	0x0DFF8	28	0x0E000	0x7FFFF	456
111	0x00000	0x077F8	30	0x07800	0x0EFF8	30	0x0F000	0x7FFFF	452
112	0x00000	0x07FF8	32	0x08000	0x0FFF8	32	0x10000	0x7FFFF	448
113	0x00000	0x087F8	34	0x08800	0x10FF8	34	0x11000	0x7FFFF	444
114	0x00000	0x08FF8	36	0x09000	0x11FF8	36	0x12000	0x7FFFF	440
115	0x00000	0x097F8	38	0x09800	0x12FF8	38	0x13000	0x7FFFF	436
116	0x00000	0x09FF8	40	0x0A000	0x13FF8	40	0x14000	0x7FFFF	432
117	0x00000	0x0A7F8	42	0x0A800	0x14FF8	42	0x15000	0x7FFFF	428
118	0x00000	0x0AFF8	44	0x0B000	0x15FF8	44	0x16000	0x7FFFF	424
119	0x00000	0x0B7F8	46	0x0B800	0x16FF8	46	0x17000	0x7FFFF	420
120	0x00000	0x0BFF8	48	0x0C000	0x17FF8	48	0x18000	0x7FFFF	416
121	0x00000	0x0C7F8	50	0x0C800	0x18FF8	50	0x19000	0x7FFFF	412
122	0x00000	0x0CFF8	52	0x0D000	0x19FF8	52	0x1A000	0x7FFFF	408
123	0x00000	0x0D7F8	54	0x0D800	0x1AFF8	54	0x1B000	0x7FFFF	404
124	0x00000	0x0DFF8	56	0x0E000	0x1BFF8	56	0x1C000	0x7FFFF	400
125	0x00000	0x0E7F8	58	0x0E800	0x1CFF8	58	0x1D000	0x7FFFF	396
126	0x00000	0x0EFF8	60	0x0F000	0x1DFF8	60	0x1E000	0x7FFFF	392
127	0x00000	0x0F7F8	62	0x0F800	0x1EFF8	62	0x1F000	0x7FFFF	388
128	0x00000	0x0FFF8	64	0x10000	0x1FFF8	64	–	–	384

4.33 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute								
Initial value	0x00							

Register functions

[bit31:0] Reserved: (for internal device test purposes)

These bits allow can be written as 0x00000000 only.

4.34 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute								
Initial value	0x00							

Register function

[bit31:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000000 only.

4.35 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved.							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved				Reserved			
Attribute	-				R/W			
Initial value	0x0				0x0			

bit	15	14	13	12	11	10	9	8
Field	Reservedi							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	1	0
Field	Reserved						
Attribute	R/W						
Initial value	0x00						

Register function

[bit31:20] Reserved: Reserved bits

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit19:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000 only.

4.36 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved.							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved				Reserved			
Attribute	-				R/W			
Initial value	0x0				0x0			

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	1	0
Field	Reserved						
Attribute	R/W						
Initial value	0x00						

Register functions

[bit31:20] Reserved: Reserved bit

The initial value is read from these bits.

Set the initial value to these bits when writing.

[bit19:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000 only.

4.37 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute								
Initial value	0x00							

Register function

[bit31:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000000 only.

4.38 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute								
Initial value	0x00							

Register functions

[bit31:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000000 only.

4.39 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved.							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved				Reserved			
Attribute	-				R/W			
Initial value	0x0				0x0			

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	1	0
Field	Reserved						
Attribute	R/W						
Initial value	0x00						

Register functions

[bit31:20] Reserved: Reserved bits

0x000 is read from these bits.

Set 0x000 to these bits when writing.

[bit19:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000 only.

4.40 TEST (Reserved)

This register is implemented for internal device test purposes.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved.							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved				Reserved			
Attribute	-				R/W			
Initial value	0x0				0x0			

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	1	0
Field	Reserved						
Attribute	R/W						
Initial value	0x00						

Register functions

[bit31:20] Reserved: Reserved bits

0x000 is read from these bits.

Set 0x000 to these bits when writing.

[bit19:0] Reserved: (for internal device test purposes)

These bits can be written as 0x00000 only.

4.41 vram_sberraddr_s0

The vram_sberraddr_s0 indicates GDC bus address of the read access at S0 interface which had a single-bit ECC error.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	vram_sberraddr_s0							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	vram_sberraddr_s0							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	vram_sberraddr_s0							
Attribute	R							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	vram_sberraddr_s0							
Attribute	R							
Initial value	0x00							

Register function

[bit31:0] vram_sberraddr_s0: Indicates address which had an ECC single bit error

4.42 vram_sberraddr_s1

The vram_sberraddr_s1 indicates GDC bus address of the read access at S1 interface which had a single-bit ECC error.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	vram_sberraddr_s1							
Attribute	R							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	vram_sberraddr_s1							
Attribute	R							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	vram_sberraddr_s1							
Attribute	R							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	vram_sberraddr_s1							
Attribute	R							
Initial value	0x00							

Register function

[bit31:0] vram_sberraddr_s1: Indicates address which had an ECC single bit error

4.43 vram_arbiter_priority

The vram_arviter_priority assigns fixed arbitration priorities to each GDC bus slave interface. An interface with a higher priority will always win over an interface with a lower one. Interfaces with equal priorities will be round-robin arbitrated. This register can be written during operation.

Register configuration

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved		vram_priority_s1_read		vram_priority_s0_read		vram_priority_s0_write	
Attribute	R/W		R/W		R/W		R/W	
Initial value	0b00		0b00		0b00		0b00	

Register function

[bit31:8] Reserved: Reserved for future use

The initial value is read from these bits.
Set the initial value to these bits when writing.

[bit7:6] Reserved:: (for internal device test purpose)

The initial value is read from these bits.
These bits allow writing 0b00 only.

[bit5:4] vram_priority_s1_read

bit1:0	Description
00	Highest priority
01	Second-highest priority
10	Third-highest priority
11	Lowest priority

[bit3:2] vram_priority_s0_read

bit1:0	Description
00	Highest priority
01	Second-highest priority
10	Third-highest priority
11	Lowest priority

[bit1:0] vram_priority_s0_write

bit1:0	Description
00	Highest priority
01	Second-highest priority
10	Third-highest priority
11	Lowest priority

CHAPTER 4: Software Interface

This chapter explains Software Interface of the GDC Subsystem.

1. Map Tables

1.1 Interrupt Map

The given GDC Core ID is the bit number of the corresponding event as used in the Common Control configuration of the GDC Core module.

Table 1-1 Interrupt Map

Interrupt Type	GDC Sub System IRQ Name	Interrupt Name	Interrupt Events	GDC Core ID	FM4Interrupt ID(IRQMON)
IRQ	irq[0]	GDCCORE_CommandSequencer	(Reserved)	(19)	92(bit8)
			This IRQ is controlled by the GDC Core.	20	
				21	
				22	
				23	
				24	
IRQ	irq[1]	GDCCORE_BlitEngine	This IRQ is controlled by the GDC Core.	0	93(bit8)
				1	
				2	
IRQ	irq[2]	(Reserved)	-	-	94(bit8)
IRQ	irq[3]	GDCCORE_ContentStream0	This IRQ is controlled by the GDC Core.	3	95(bit8)
				4	
				5	
				27	
				28	
				13	
IRQ	irq[4]	GDC_SaftyStream0	This IRQ is controlled by the GDC Core.	6	96(bit8)
				7	
				8	
				25	
				26	
				12	
IRQ	irq[5]	GDC_DisplayStream0	This IRQ is controlled by the GDC Core.	9	97(bit8)
				10	
				11	
IRQ	irq[6]	GDC_Signature0	This IRQ is controlled by the GDC Core.	16	98(bit8)
				17	
				18	
IRQ	irq[7]	GDC_Display0_Sync0	This IRQ is controlled by the GDC Core.	14	99(bit8)
IRQ	irq[8]	GDC_Display0_Sync1		15	100(bit8)
IRQ	irq[9]	(Reserved)	-	-	101(bit8)
IRQ	irq[10]	(Reserved)	-	-	102(bit8)
IRQ	irq[11]	(Reserved)	-	-	103(bit8)
IRQ	irq[12]	(Reserved)	-	-	104(bit8)
IRQ	irq[13]	(Reserved)	-	-	105(bit8)
IRQ	irq[14]	(Reserved)	-	-	106(bit8)
IRQ	irq[15]	(Reserved)	-	-	107(bit8)
IRQ	irq[16]	(Reserved)	-	-	108(bit8)
IRQ	irq[17]	(Reserved)		-	109(bit8)
IRQ	irq[18]	VramEccError_or_GDCBusError	VRAM_ECC_Disp or GDC_Bus_Error	-	110(bit8)
IRQ	qspi_irq_rx	FIP006.IRQ_RX	HS_SPI_Tx_FIFO		120(bit8)
IRQ	qspi_irq_tx	FIP006.IRQ_TX	HS_SPI_Rx_FIFO		121(bit8)
IRQ	qspi_irq_fault	FIP006.IRQ_FAULT	HS_SPI Fault		122(bit8)
IRQ	sdram_merrint	BMEMCSE.MerrInt	Sdramc_MerrInt		49(bit1)
IRQ	rpc_int	RPC2.IENOn	RPC2 Interrupt		123(bit8)

Appendixes

This chapter shows the register map, list of notes, and major changes.

A. Register Map

B. List of Notes

C. Major Changes

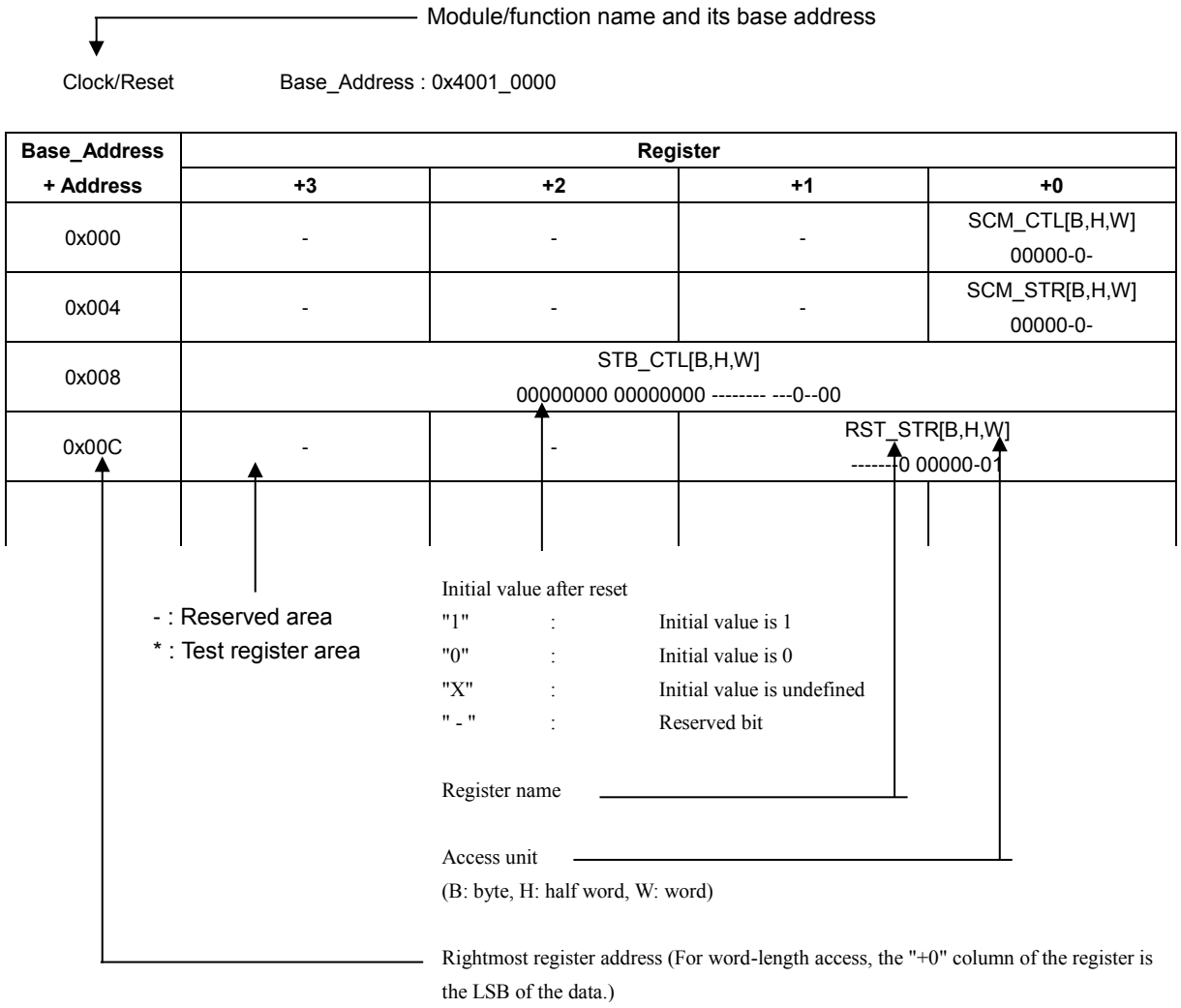
A. Register Map

This section shows the register map.

A.1 Register Map

Register map is shown on the table every module/function.

[How to read the each table]



Notes:

- *The register table is represented in the little-endian.*
- *When performing a data access, the addresses should be as below according to the access size.*
- *Word access: Address should be multiples of 4 (least significant 2 bits should be 0x00)*
- *Half word access: Address should be multiples of 2 (least significant bit should be 0x0)*
- *Byte access: -*
- *Do not access the test register area.*
- *Do not access the area that is not written in the register table.*
- *When the register is accessed by larger unit than register size, for the reserved area to access at the same time, the read value is undefined, and writing is invalid.*

A.1.1 FLASH_IF

A.1.1.1 TYPE1-M4, TYPE2-M4 products

FLASH_IF Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x1FC	-	-	-	-

Note:

- *For details of Flash I/F registers, see Flash Programming Manual of the product used.*

A.1.1.2 TYPE3-M4 product

FLASH_IF Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C	-	-	-	-
0x030	DFCTRLR[W]			
0x034 - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x10C	-	-	-	-
0x110	FGPDM1[B,H,W]			
0x114	FGPDM2[B,H,W]			
0x118	FGPDM3[B,H,W]			
0x11C	FGPDM4[B,H,W]			
0x120 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	DFASZR[B,H,W]			
0x404	DFRWTR[B,H,W]			
0x408	DFSTR[B,H,W]			
0x40C - 0x4FC	-	-	-	-

Note:

- *For details of Flash I/F registers, see Flash Programming Manual of the product used.*

A.1.1.3 TYPE4-M4, TYPE5-M4, TYPE6-M4 products

FLASH_IF Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FASZR[B,H,W]			
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C	*			
0x010	FSYNDN[B,H,W]			
0x014	FBFCR[B,H,W]			
0x018 - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0x10C	-	-	-	-
0x110	FGPDM1[B,H,W]			
0x114	FGPDM2[B,H,W]			
0x118	FGPDM3[B,H,W]			
0x11C	FGPDM4[B,H,W]			
0x120 - 0x1FC	-			

Note:

- *For details of Flash I/F registers, see Flash Programming Manual of the product used.*

A.1.2 Unique ID

Unique ID Base_Address : 0x4000_0200

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	UIDR0[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXX----			
0x004	UIDR1[W]			
	-------- -------- ---XXXXX XXXXXXXX			
0x008 - 0xDFC	-	-	-	-

A.1.3 ECC Capture Address

ECC Capture Address Base_Address : 0x4000_0300

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FERRAD[W] -------- -XXXXXXX XXXXXXXX XXXXXXXX			
0x004 - 0xFFC	-	-	-	-

A.1.4 Clock/Reset

A.1.4.1 TYPE1-M4, TYPE2-M4 products

Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W] -------0 0000--01	
0x010	-	-	-	BSC_PSR[W] -----000
0x014	-	-	-	APBC0_PSR[W] ------00
0x018	-	-	-	APBC1_PSR[W] 1--0--00
0x01C	-	-	-	APBC2_PSR[W] 1--0--00
0x020	-	-	-	SWC_PSR[W] ------00
0x024 – 0x027	-	-	-	-
0x028	-	-	-	TTC_PSR[W] ------00
0x02C – 0x02F	-	-	-	-
0x030	-	-	-	CSW_TMR[W] 00000000
0x034	-	-	-	PSW_TMR[W] ---0-000
0x038	-	-	-	PLL_CTL1[W] 00000000
0x03C	-	-	-	PLL_CTL2[W] --000000
0x040	-	-	CSV_CTL[W] -111--00 ------11	
0x044	-	-	-	CSV_STR[W] ------00
0x048	-	-	FCSWH_CTL[W] 11111111 11111111	
0x04C	-	-	FCSWL_CTL[W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W] 0-0-----
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] --0--000
0x064	-	-	-	INT_STR[W] --0–000
0x068	-	-	-	INT_CLR[W] --0--000
0x06C – 0xFFC	-	-	-	-

A.1.4.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 products

Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W] -------0 0000--01	
0x010	-	-	-	BSC_PSR[W] -----000
0x014	-	-	-	APBC0_PSR[W] ------00
0x018	-	-	-	APBC1_PSR[W] 1--0--00
0x01C	-	-	-	APBC2_PSR[W] 1--0--00
0x020	-	-	-	SWC_PSR[W] ------00
0x024 – 0x027	-	-	-	-
0x028	-	-	-	TTC_PSR[W] ------00
0x02C – 0x02F	-	-	-	-
0x030	-	-	-	CSW_TMR[W] 00000000
0x034	-	-	-	PSW_TMR[W] ---0-000
0x038	-	-	-	PLL_CTL1[W] 00000000
0x03C	-	-	-	PLL_CTL2[W] --000000
0x040	-	-	CSV_CTL[W] -111--00 ------11	
0x044	-	-	-	CSV_STR[W] ------00
0x048	-	-	FCSWH_CTL[W] 11111111 11111111	
0x04C	-	-	FCSWL_CTL[W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W] 0-0-----
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] --0--000
0x064	-	-	-	INT_STR[W] --0–000
0x068	-	-	-	INT_CLR[W] --0--000
0x06C – 0x070	-	-	-	-
0x074	PLLCG_CTL[W] -------- 11111111 00000000 00----00			
0x078 – 0xFFC	-	-	-	-

A.1.5 HW WDT

HW WDT Base_Address : 0x4001_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WDG_LDR[W] 00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	-	-	-	WDG_CTL[W] ------11
0x00C	-	-	-	WDG_ICL[W] XXXXXXXX
0x010	-	-	-	WDG_RIS[W] -------0
0x014	*			
0x018 – 0xBFC	-	-	-	-
0xC00	WDG_LCK[W] 00000000 00000000 00000000 00000001			
0xC04 – 0xFFC	-	-	-	-

A.1.6 SW WDT

SW WDTBase_Address : 0x4001_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WdogLoad[W] 11111111 11111111 11111111 11111111			
0x004	WdogValue[W] 11111111 11111111 11111111 11111111			
0x008	-	-	-	WdogControl[W] ---00000
0x00C	WdogIntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	-	-	-	WdogRIS[W] -------0
0x014	*			
0x018	-	-	-	WdogSPMC[W] -------0
0x01C – 0xBFC	-	-	-	-
0xC00	WdogLock[W] 00000000 00000000 00000000 00000000			
0xC04 - 0xDFC	-	-	-	-
0xF00 - 0xF04	*			
0xF08 - 0xFDF	-	-	-	-
0xFE0 - 0xFFC	*			

A.1.7 Dual_Timer

Dual_Timer Base_Address : 0x4001_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	Timer1Load[W] 00000000 00000000 00000000 00000000			
0x004	Timer1Value[W] 11111111 11111111 11111111 11111111			
0x008	Timer1Control[W] -------- -------- -------- 00100000			
0x00C	Timer1IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W] -------- -------- -------- -------0			
0x014	Timer1MIS[W] -------- -------- -------- -------0			
0x018	Timer1BGLoad[W] 00000000 00000000 00000000 00000000			
0x020	Timer2Load[W] 00000000 00000000 00000000 00000000			
0x024	Timer2Value[W] 11111111 11111111 11111111 11111111			
0x028	Timer2Control[W] -------- -------- -------- 00100000			
0x02C	Timer2IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W] -------- -------- -------- -------0			
0x034	Timer2MIS[W] -------- -------- -------- -------0			
0x038	Timer2BGLoad[W] 00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

A.1.8 MFT

A.1.8.1 TYPE1-M4, TYPE2-M4 products

MFT unit0 **Base_Address : 0x4002_0000**

MFT unit1 **Base_Address : 0x4002_1000**

MFT unit2 **Base_Address : 0x4002_2000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	OCCP0[H,W] 00000000 00000000		-	-
0x104	OCCP1[H,W] 00000000 00000000		-	-
0x108	OCCP2[H,W] 00000000 00000000		-	-
0x10C	OCCP3[H,W] 00000000 00000000		-	-
0x110	OCCP4[H,W] 00000000 00000000		-	-
0x114	OCCP5[H,W] 00000000 00000000		-	-
0x118	-	OCSD10[B,H,W] 00000000	OCSB10[B,H,W] 00000000	OCSA10[B,H,W] 00000000
0x11C	-	OCSD32[B,H,W] 00000000	OCSB32[B,H,W] 00000000	OCSA32[B,H,W] 00000000
0x120	-	OCSD54[B,H,W] 00000000	OCSB54[B,H,W] 00000000	OCSA54[B,H,W] 00000000
0x124	-	-	OCSC[B,H,W] --000000	-
0x128	-	-	OCSE0[B,H,W] 00000000 00000000	
0x12C	OCSE1[B,H,W] 00000000 00000000 00000000 00000000			
0x130	-	-	OCSE2[B,H,W] 00000000 00000000	
0x134	OCSE3[B,H,W] 00000000 00000000 00000000 00000000			
0x138	-	-	OCSE4[B,H,W] 00000000 00000000	
0x13C	OCSE5[B,H,W] 00000000 00000000 00000000 00000000			
0x140	TCCP0[H,W] 11111111 11111111		-	-
0x144	TCDT0[H,W] 00000000 00000000		-	-
0x148	TCSC0[H,W] 00000000 00000000		TCSA0[B,H,W] 00000000 01000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x14C	TCCP1[H,W] 11111111 11111111		-	-
0x150	TCDT1[H,W] 00000000 00000000		-	-
0x154	TCSC1[H,W] 00000000 00000000		TCSA1[B,H,W] 00000000 01000000	
0x158	TCCP2[H,W] 11111111 11111111		-	-
0x15C	TCDT2[H,W] 00000000 00000000		-	-
0x160	TCSC2[H,W] 00000000 00000000		TCSA2[B,H,W] 00000000 01000000	
0x164	TCAL[W] 00000000 00000000 11111111 11111111 *1			
	-	-	-	- *2
	*1 MFT unit0 *2 MFT unit1,unit2			
0x168	-	OCFS54[B,H,W] 00000000	OCFS32[B,H,W] 00000000	OCFS10[B,H,W] 00000000
0x16C	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000
0x174	ICCP0[H,W] 00000000 00000000		-	-
0x178	ICCP1[H,W] 00000000 00000000		-	-
0x17C	ICCP2[H,W] 00000000 00000000		-	-
0x180	ICCP3[H,W] 00000000 00000000		-	-
0x184	-	-	ICSB10[B,H,W] ------00	ICSA10[B,H,W] 00000000
0x188			ICSB32[B,H,W] ------00	ICSA32[B,H,W] 00000000
0x18C	WFTF10[H,W] 00000000 00000000		-	-
0x190	WFTB10[H,W] 00000000 00000000		WFTA10[H,W] 00000000 00000000	
0x194	WFTF32[H,W] 00000000 00000000		-	-
0x198	WFTB32[H,W] 00000000 00000000		WFTA32[H,W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x19C	WFTF54[H,W] 00000000 00000000		-	-
0x1A0	WFTB54[H,W] 00000000 00000000		WFTA54[H,W] 00000000 00000000	
0x1A4	-		-	WFSA10[B,H,W] --000000 000000
0x1A8	-		-	WFSA32[B,H,W] --000000 000000
0x1AC	-		-	WFSA54[B,H,W] --000000 000000
0x1B0	-		-	WFIR[H,W] 00000000 00000000
0x1B4	-		-	NZCL[H,W] 00000000 00000000
0x1B8	ACMP0[H,W] 00000000 00000000		-	-
0x1BC	ACMP1[H,W] 00000000 00000000		-	-
0x1C0	ACMP2[H,W] 00000000 00000000		-	-
0x1C4	ACMP3[H,W] 00000000 00000000		-	-
0x1C8	ACMP4[H,W] 00000000 00000000		-	-
0x1CC	ACMP5[H,W] 00000000 00000000		-	-
0x1D0	-	-	ACSA[B,H,W] 00000000 00000000	
0x1D4	-	-	ACSD0[B,H,W] 00000000	ACSC0[B,H,W] 00000000
0x1D8	-	-	ACSD1[B,H,W] 00000000	ACSC1[B,H,W] 00000000
0x1DC	-	-	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000
0x1E0	-	-	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000
0x1E4	-	-	ACSD4[B,H,W] 00000000	ACSC4[B,H,W] 00000000
0x1E8	-	-	ACSD5[B,H,W] 00000000	ACSC5[B,H,W] 00000000
0x1EC-0xFFC	-	-	-	-

A.1.8.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 products

MFT unit0 **Base_Address : 0x4002_0000**

MFT unit1 **Base_Address : 0x4002_1000**

MFT unit2 **Base_Address : 0x4002_2000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	OCCP0[H,W] 00000000 00000000		-	-
0x104	OCCP1[H,W] 00000000 00000000		-	-
0x108	OCCP2[H,W] 00000000 00000000		-	-
0x10C	OCCP3[H,W] 00000000 00000000		-	-
0x110	OCCP4[H,W] 00000000 00000000		-	-
0x114	OCCP5[H,W] 00000000 00000000		-	-
0x118	OCSD10[B,H,W] --000000 00000000		OCSB10[B,H,W] 00000000	OCSA10[B,H,W] 00000000
0x11C	OCSD32[B,H,W] --000000 00000000		OCSB32[B,H,W] 00000000	OCSA32[B,H,W] 00000000
0x120	OCSD54[B,H,W] --000000 00000000		OCSB54[B,H,W] 00000000	OCSA54[B,H,W] 00000000
0x124	-	-	OCSC[B,H,W] --000000	-
0x128	-	-	OCSE0[B,H,W] 00000000 00000000	
0x12C	OCSE1[B,H,W] 00000000 00000000 00000000 00000000			
0x130	-	-	OCSE2[B,H,W] 00000000 00000000	
0x134	OCSE3[B,H,W] 00000000 00000000 00000000 00000000			
0x138	-	-	OCSE4[B,H,W] 00000000 00000000	
0x13C	OCSE5[B,H,W] 00000000 00000000 00000000 00000000			
0x140	TCCP0[H,W] 11111111 11111111		-	-
0x144	TCDT0[H,W] 00000000 00000000		-	-
0x148	TCSC0[H,W] 00000000 00000000		TCSA0[B,H,W] 00000000 01000000	
0x14C	TCCP1[H,W] 11111111 11111111		-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x150	TCDT1[H,W] 00000000 00000000		-	-
0x154	TCSC1[H,W] 00000000 00000000		TCSA1[B,H,W] 00000000 01000000	
0x158	TCCP2[H,W] 11111111 11111111		-	-
0x15C	TCDT2[H,W] 00000000 00000000		-	-
0x160	TCSC2[H,W] 00000000 00000000		TCSA2[B,H,W] 00000000 01000000	
0x164	TCAL[W] 00000000 00000000 11111111 11111111 *1			
	-	-	-	- *2
	*1 MFT unit0 *2 MFT unit1,unit2			
0x168	-	OCFS54[B,H,W] 00000000	OCFS32[B,H,W] 00000000	OCFS10[B,H,W] 00000000
0x16C	-	-	ICFS32[B,H,W] 00000000	ICFS10[B,H,W] 00000000
0x170	-	ACFS54[B,H,W] 00000000	ACFS32[B,H,W] 00000000	ACFS10[B,H,W] 00000000
0x174	ICCP0[H,W] 00000000 00000000		-	-
0x178	ICCP1[H,W] 00000000 00000000		-	-
0x17C	ICCP2[H,W] 00000000 00000000		-	-
0x180	ICCP3[H,W] 00000000 00000000		-	-
0x184	-	-	ICSB10[B,H,W] ------00	ICSA10[B,H,W] 00000000
0x188			ICSB32[B,H,W] ------00	ICSA32[B,H,W] 00000000
0x18C	WFTF10[H,W] 00000000 00000000		-	-
0x190	WFTB10[H,W] 00000000 00000000		WFTA10[H,W] 00000000 00000000	
0x194	WFTF32[H,W] 00000000 00000000		-	-
0x198	WFTB32[H,W] 00000000 00000000		WFTA32[H,W] 00000000 00000000	
0x19C	WFTF54[H,W] 00000000 00000000		-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1A0	WFTB54[H,W] 00000000 00000000		WFTA54[H,W] 00000000 00000000	
0x1A4	-	-	WFSA10[B,H,W] --000000 000000	
0x1A8	-	-	WFSA32[B,H,W] --000000 000000	
0x1AC	-	-	WFSA54[B,H,W] --000000 000000	
0x1B0	-	-	WFIR[H,W] 00000000 00000000	
0x1B4	-	-	NZCL[H,W] 00000000 00000000	
0x1B8	ACMP0[H,W] 00000000 00000000		-	-
0x1BC	ACMP1[H,W] 00000000 00000000		-	-
0x1C0	ACMP2[H,W] 00000000 00000000		-	-
0x1C4	ACMP3[H,W] 00000000 00000000		-	-
0x1C8	ACMP4[H,W] 00000000 00000000		-	-
0x1CC	ACMP5[H,W] 00000000 00000000		-	-
0x1D0	-	-	ACSA[B,H,W] 00000000 00000000	
0x1D4	-	ACMC0[B,H,W] 00--0000	ACSD0[B,H,W] 00000000	ACSC0[B,H,W] 00000000
0x1D8	-	ACMC1[B,H,W] 00--0000	ACSD1[B,H,W] 00000000	ACSC1[B,H,W] 00000000
0x1DC	-	ACMC2[B,H,W] 00--0000	ACSD2[B,H,W] 00000000	ACSC2[B,H,W] 00000000
0x1E0	-	ACMC3[B,H,W] 00--0000	ACSD3[B,H,W] 00000000	ACSC3[B,H,W] 00000000
0x1E4	-	ACMC4[B,H,W] 00--0000	ACSD4[B,H,W] 00000000	ACSC4[B,H,W] 00000000
0x1E8	-	ACMC5[B,H,W] 00--0000	ACSD5[B,H,W] 00000000	ACSC5[B,H,W] 00000000
0x1EC	-	-	-	TCSD[B,H,W] ------00
0x1F0-0xFFC	-	-	-	-

A.1.9 PPG

PPG Base_Address : 0x4002_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	TTCR0 [B,H,W] 11110000	-
0x004	-	-	-	*
0x008	-	-	COMP0 [B,H,W] 00000000	-
0x00C	-	-	-	COMP2 [B,H,W] 00000000
0x010	-	-	COMP4 [B,H,W] 00000000	-
0x014	-	-	-	COMP6 [B,H,W] 00000000
0x018 - 0x01C	-	-	-	-
0x020	-	-	TTCR1 [B,H,W] 11110000	-
0x024	-	-	-	*
0x028	-	-	COMP1 [B,H,W] 00000000	-
0x02C	-	-	-	COMP3 [B,H,W] 00000000
0x030	-	-	COMP5 [B,H,W] 00000000	-
0x034	-	-	-	COMP7 [B,H,W] 00000000
0x038 - 0x03C	-	-	-	-
0x040	-	-	TTCR2 [B,H,W] 11110000	-
0x044	-	-	-	*
0x048	-	-	COMP8 [B,H,W] 00000000	-
0x04C	-	-	-	COMP10 [B,H,W] 00000000
0x050	-	-	COMP12 [B,H,W] 00000000	-
0x054	-	-	-	COMP14 [B,H,W] 00000000
0x058 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	-	-	TRG0 [B,H,W] 00000000 00000000	
0x104	-	-	REVC0 [B,H,W] 00000000 00000000	
0x108 - 0x13C	-	-	-	-
0x140	-	-	TRG1 [B,H,W] -------- 00000000	
0x144	-	-	REVC1 [B,H,W] -------- 00000000	
0x148 - 0x1FC	-	-	-	-
0x200	-	-	PPGC0 [B,H,W] 00000000	PPGC1 [B,H,W] 00000000
0x204	-	-	PPGC2 [B,H,W] 00000000	PPGC3 [B,H,W] 00000000
0x208	-	-	PRLH0 [B,H,W] XXXXXXXX	PRLL0 [B,H,W] XXXXXXXX
0x20C	-	-	PRLH1 [B,H,W] XXXXXXXX	PRLL1 [B,H,W] XXXXXXXX
0x210	-	-	PRLH2 [B,H,W] XXXXXXXX	PRLL2 [B,H,W] XXXXXXXX
0x214	-	-	PRLH3 [B,H,W] XXXXXXXX	PRLL3 [B,H,W] XXXXXXXX
0x218	-	-	-	GATEC0 [B,H,W] --00---00
0x21C - 0x23C	-	-	-	-
0x240	-	-	PPGC4 [B,H,W] 00000000	PPGC5 [B,H,W] 00000000
0x244	-	-	PPGC6 [B,H,W] 00000000	PPGC7 [B,H,W] 00000000
0x248	-	-	PRLH4 [B,H,W] XXXXXXXX	PRLL4 [B.H.W] XXXXXXXX
0x24C	-	-	PRLH5 [B,H,W] XXXXXXXX	PRLL5 [B,H,W] XXXXXXXX
0x250	-	-	PRLH6 [B,H,W] XXXXXXXX	PRLL6 [B,H,W] XXXXXXXX
0x254	-	-	PRLH7 [B,H,W] XXXXXXXX	PRLL7 [B,H,W] XXXXXXXX
0x258	-	-	-	GATEC4 [B,H,W] ------00
0x25C - 0x27C	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x280	-	-	PPGC8 [B,H,W] 00000000	PPGC9 [B,H,W] 00000000
0x284	-	-	PPGC10 [B,H,W] 00000000	PPGC11 [B,H,W] 00000000
0x288	-	-	PRLH8 [B,H,W] XXXXXXXX	PRLL8 [B,H,W] XXXXXXXX
0x28C	-	-	PRLH9 [B,H,W] XXXXXXXX	PRLL9 [B,H,W] XXXXXXXX
0x290	-	-	PRLH10 [B,H,W] XXXXXXXX	PRLL10 [B,H,W] XXXXXXXX
0x294	-	-	PRLH11 [B,H,W] XXXXXXXX	PRLL11 [B,H,W] XXXXXXXX
0x298	-	-	-	GATEC8 [B,H,W] --00--00
0x29C - 0x2BC	-	-	-	-
0x2C0	-	-	PPGC12 [B,H,W] 00000000	PPGC13 [B,H,W] 00000000
0x2C4	-	-	PPGC14 [B,H,W] 00000000	PPGC15 [B,H,W] 00000000
0x2C8	-	-	PRLH12 [B,H,W] XXXXXXXX	PRLL12 [B,H,W] XXXXXXXX
0x2CC	-	-	PRLH13 [B,H,W] XXXXXXXX	PRLL13 [B,H,W] XXXXXXXX
0x2D0	-	-	PRLH14 [B,H,W] XXXXXXXX	PRLL14 [B,H,W] XXXXXXXX
0x2D4	-	-	PRLH15 [B,H,W] XXXXXXXX	PRLL15 [B,H,W] XXXXXXXX
0x2D8	-	-	-	GATEC12 [B,H,W] ------00
0x2DC - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	-	-	PPGC16 [B,H,W] 00000000	PPGC17 [B,H,W] 00000000
0x304	-	-	PPGC18 [B,H,W] 00000000	PPGC19 [B,H,W] 00000000
0x308	-	-	PRLH16 [B,H,W] XXXXXXXX	PRLL16 [B,H,W] XXXXXXXX
0x30C	-	-	PRLH17 [B,H,W] XXXXXXXX	PRLL17 [B,H,W] XXXXXXXX
0x310	-	-	PRLH18 [B,H,W] XXXXXXXX	PRLL18 [B,H,W] XXXXXXXX
0x314	-	-	PRLH19 [B,H,W] XXXXXXXX	PRLL19 [B,H,W] XXXXXXXX
0x318	-	-	-	GATEC16 [B,H,W] --00---00
0x31C - 0x33C	-	-	-	-
0x340	-	-	PPGC20 [B,H,W] 00000000	PPGC21 [B,H,W] 00000000
0x344	-	-	PPGC22 [B,H,W] 00000000	PPGC23 [B,H,W] 00000000
0x348	-	-	PRLH20 [B,H,W] XXXXXXXX	PRLL20 [B.H.W] XXXXXXXX
0x34C	-	-	PRLH21 [B,H,W] XXXXXXXX	PRLL21 [B,H,W] XXXXXXXX
0x350	-	-	PRLH22 [B,H,W] XXXXXXXX	PRLL22 [B,H,W] XXXXXXXX
0x354	-	-	PRLH23 [B,H,W] XXXXXXXX	PRLL23 [B,H,W] XXXXXXXX
0x358	-	-	-	GATEC20 [B,H,W] ------00
0x35C - 0x37C	-	-	-	-
0x380	-	-	-	-
0x384 - 0xFFC	-	-	-	-

A.1.10 Base Timer

Base Timer ch.0 Base Address : 0x4002_5000

Base Timer ch.1 Base Address : 0x4002_5040

Base Timer ch.2 Base Address : 0x4002_5080

Base Timer ch.3 Base Address : 0x4002_50C0

Base Timer ch.4 Base Address : 0x4002_5200

Base Timer ch.5 Base Address : 0x4002_5240

Base Timer ch.6 Base Address : 0x4002_5280

Base Timer ch.7 Base Address : 0x4002_52C0

Base Timer ch.8 Base Address : 0x4002_5400

Base Timer ch.9 Base Address : 0x4002_5440

Base Timer ch.10 Base Address : 0x4002_5480

Base Timer ch.11 Base Address : 0x4002_54C0

Base Timer ch.12 Base Address : 0x4002_5600

Base Timer ch.13 Base Address : 0x4002_5640

Base Timer ch.14 Base Address : 0x4002_5680

Base Timer ch.15 Base Address : 0x4002_56C0

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL [H,W] XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF [H,W] XXXXXXXX XXXXXXXX	
0x008	-	-	TMR [H,W] 00000000 00000000	
0x00C	-	-	TMCR [B,H,W] -0000000 00000000	
0x010	-	-	TMCR2 [B,H,W] 0------0	STC [B,H,W] 0000-000
0x014 - 0x03C	-	-	-	-

A.1.11 IO Selector for Base Timer

IO Selector for ch.0-ch.3 (Base Timer) Base Address : 0x4002_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL0123 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7(Base Timer) Base Address : 0x4002_5300

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL4567 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.8-ch.11(Base Timer) Base Address : 0x4002_5500

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL89AB [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.12-ch.15(Base Timer) Base Address : 0x4002_5700

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSELCDEF [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

Software-based Simultaneous Startup(Base Timer) Base Address : 0x4002_5F00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR [B,H,W] XXXXXXXX XXXXXXXX	

A.1.12 QPRC

A.1.12.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 products

QPRC ch.0 Base Address : 0x4002_6000

QPRC ch.1 Base Address : 0x4002_6040

QPRC ch.2 Base Address : 0x4002_6080

QPRC ch.3 Base Address : 0x4002_60C0

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	-	-	QPCR [H,W] 00000000 00000000	
0x0004	-	-	QRCR [H,W] 00000000 00000000	
0x0008	-	-	QPCCR [H,W] 00000000 00000000	
0x000C	-	-	QPRCR [H,W] 00000000 00000000	
0x0010	-	-	QMPR [H,W] 11111111 11111111	
0x0014	-	-	QICRH [B,H,W] --000000	QICRL [B,H,W] 00000000
0x0018	-	-	QCRH [B,H,W] 00000000	QCRL [B,H,W] 00000000
0x001C	-	-	QECR [B,H,W] -------- -----000	
0x0020 - 0x003B	-	-	-	-
0x003C	QPCRR[B,H,W] 00000000 00000000		QRCRR[B,H,W] 00000000 00000000	

A.1.12.2 TYPE3-M4, TYPE4-M4, TYPE5-M4 products

QPRC ch.0 Base Address : 0x4002_6000

QPRC ch.1 Base Address : 0x4002_6040

QPRC ch.2 Base Address : 0x4002_6080

QPRC ch.3 Base Address : 0x4002_60C0

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	-	-	QPCR [H,W] 00000000 00000000	
0x0004	-	-	QRCR [H,W] 00000000 00000000	
0x0008	-	-	QPCCR [H,W] 00000000 00000000	
0x000C	-	-	QPRCR [H,W] 00000000 00000000	
0x0010	-	-	QMPR [H,W] 11111111 11111111	
0x0014	-	-	QICRH [B,H,W] --000000	QICRL [B,H,W] 00000000
0x0018	-	-	QCRH [B,H,W] 00000000	QCRL [B,H,W] 00000000
0x001C	-	-	QECR [B,H,W] -------- ----0000	
0x0020 - 0x003B	-	-	-	-
0x003C	QPCRR[B,H,W] 00000000 00000000		QRCRR[B,H,W] 00000000 00000000	

A.1.13 QPRC NF

QPRC ch.0 NF Base Address : 0x4002_6100

QPRC ch.1 NF Base Address : 0x4002_6110

QPRC ch.2 NF Base Address : 0x4002_6120

QPRC ch.3 NF Base Address : 0x4002_6130

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	-	-	-	NFCTLA[B,H,W] --00-000
0x0004	-	-	-	NFCTLB[B,H,W] --00-000
0x0008	-	-	-	NFCTLZ[B,H,W] --00-000
0x000C	-	-	-	-

A.1.14 A/DC

12bit A/DC unit0 Base_Address : 0x4002_7000

12bit A/DC unit1 Base_Address : 0x4002_7100

12bit A/DC unit2 Base_Address : 0x4002_7200

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W] 000-0000	ADSR[B,H,W] 00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W] 1000-000	SFNS[B,H,W] ----0000
0x00C	SCFD[B,H,W] XXXXXXXX XXXX---- ---1--XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W] 00000000	SCIS2[B,H,W] 00000000
0x014	-	-	SCIS1[B,H,W] 00000000	SCIS0[B,H,W] 00000000
0x018	-	-	PCCR[B,H,W] 10000000	PFNS[B,H,W] --XX--00
0x01C	PCFD[B,H,W] XXXXXXXX XXXX---- ---1-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W] 00000000
0x024	CMPD[B,H,W] 00000000 00------		-	CMPCR[B,H,W] 00000000
0x028	-	-	ADSS3[B,H,W] 00000000	ADSS2[B,H,W] 00000000
0x02C	-	-	ADSS1[B,H,W] 00000000	ADSS0[B,H,W] 00000000
0x030	-	-	ADST0[B,H,W] 00010000	ADST1[B,H,W] 00010000
0x034	-	-	-	ADCT[B,H,W] 00000111
0x038	-	-	SCTSL[B,H,W] ----0000	PRTSL[B,H,W] ----0000
0x03C	-	-	ADCEN[B,H,W] 11111111 ------00	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x040	CALSR[B,H,W] -------- -------- -------0 00000000			
0x044	-	-	-	WCMRCIF[B,H,W] 00000000
0x048	-	-	-	WCMRCOT [B,H,W] 00000000
0x04C	-	-	WCMPSR[B,H,W] 00000000	WCMPCR[B,H,W] 00100000
0x050	WCMPDH[B,H,W] 00000000 00000000		WCMPDL[B,H,W] 00000000 00000000	
0x040 - 0x0FC	-	-	-	-

A.1.15 CR Trim

CR Trim Base_Address : 0x4002_E000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	MCR_PSR[B,H,W] -----001
0x004	-	-	MCR_FTRM[B,H,W] ------01 11101111	
0x008	-	-	-	MCR_TTRM[B,H,W] ---10000
0x00C	MCR_RLR[W] 00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

A.1.16 EXTI

A.1.16.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE4-M4 products

EXTI Base_Address : 0x4003_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ENIR[B,H,W] 00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W] 00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W] 00000000 00000000 00000000 00000000			
0x014	-	-	-	NMIRR[B,H,W] -------0
0x018	-	-	-	NMICL[B,H,W] -------1
0x01C	-	-	-	-
0x020 - 0x0FC	-	-	-	-

A.1.16.2 TYPE5-M4, TYPE6-M4 products

EXTI Base_Address : 0x4003_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ENIR[B,H,W] 00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	ELVR[B,H,W] 00000000 00000000 00000000 00000000			
0x010	ELVR1[B,H,W] 00000000 00000000 00000000 00000000			
0x014	-	-	-	NMIRR[B,H,W] -------0
0x018	-	-	-	NMICL[B,H,W] -------1
0x01C	ELVR2[B,H,W] 00000000 00000000 00000000 00000000			
0x020 - 0x0FC	-	-	-	-

A.1.17 INT-Req. READ

A.1.17.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 products

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004 – 0x00C	-			
0x010	-	-	-	ODDPKS[B] ---00000
0x014	-	-	-	-
0x018	-	*	-	*
0x01C – 0x10C	-	-	-	-
0x110	IRQ003SEL[B,H,W] -------- 00000000 -------- 00000000			
0x114	IRQ004SEL[B,H,W] -------- 00000000 -------- 00000000			
0x118	IRQ005SEL[B,H,W] -------- 00000000 -------- 00000000			
0x11C	IRQ006SEL[B,H,W] -------- 00000000 -------- 00000000			
0x120	IRQ007SEL[B,H,W] -------- 00000000 -------- 00000000			
0x124	IRQ008SEL[B,H,W] -------- 00000000 -------- 00000000			
0x128	IRQ009SEL[B,H,W] -------- 00000000 -------- 00000000			
0x12C	IRQ010SEL[B,H,W] -------- 00000000 -------- 00000000			
0x130 – 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x204	IRQ000MON[B,H,W] -------- -------- -------- -------0			
0x208	IRQ001MON[B,H,W] -------- -------- -------- -------0			
0x20C	IRQ002MON[B,H,W] -------- -------- -------- -------0			
0x210	IRQ003MON[B,H,W] -------- -------- -------- 00000000			
0x214	IRQ004MON[B,H,W] -------- -------- -------- 00000000			
0x218	IRQ005MON[B,H,W] -------- -------- -------- 00000000			
0x21C	IRQ006MON[B,H,W] -------- -------- -------- 00000000			
0x220	IRQ007MON[B,H,W] -------- -------- -------- 00000000			
0x224	IRQ008MON[B,H,W] -------- -------- -------- 00000000			
0x228	IRQ009MON[B,H,W] -------- -------- -------- 00000000			
0x22C	IRQ010MON[B,H,W] -------- -------- -------- 00000000			
0x230	IRQ011MON[B,H,W] -------- -------- -------- -------0			
0x234	IRQ012MON[B,H,W] -------- -------- -------- -------0			
0x238	IRQ013MON[B,H,W] -------- -------- -------- -------0			
0x23C	IRQ014MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x240	IRQ015MON[B,H,W] -------- -------- -------- -------0			
0x244	IRQ016MON[B,H,W] -------- -------- -------- -------0			
0x248	IRQ017MON[B,H,W] -------- -------- -------- -------0			
0x24C	IRQ018MON[B,H,W] -------- -------- -------- -------0			
0x250	IRQ019MON[B,H,W] -------- -------- -------- --000000			
0x254	IRQ020MON[B,H,W] -------- -------- -------- --000000			
0x258	IRQ021MON[B,H,W] -------- -------- -------- ----0000			
0x25C	IRQ022MON[B,H,W] -------- -------- -------- ----0000			
0x260	IRQ023MON[B,H,W] -------- -------- -------- ----0000			
0x264	IRQ024MON[B,H,W] -------- -------- -------- -----000			
0x268	IRQ025MON[B,H,W] -------- -------- -------- -----000			
0x26C	IRQ026MON[B,H,W] -------- -------- -------- ----0000			
0x270	IRQ027MON[B,H,W] -------- -------- -------- --000000			
0x274	IRQ028MON[B,H,W] -------- -------- -------- -----000			
0x278	IRQ029MON[B,H,W] -------- -------- -------- -----000			
0x27C	IRQ030MON[B,H,W] -------- -------- -------- ----0000			
0x280	IRQ031MON[B,H,W] -------- -------- -------- --000000			
0x284	IRQ032MON[B,H,W] -------- -------- -------- -----000			
0x288	IRQ033MON[B,H,W] -------- -------- -------- -----000			
0x28C	IRQ034MON[B,H,W] -------- -------- -------- ---00000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x290	IRQ035MON[B,H,W] -------- -------- -------- --000000			
0x294	IRQ036MON[B,H,W] -------- -------- -------- -----000			
0x298	IRQ037MON[B,H,W] -------- -------- -------- -----000			
0x29C	IRQ038MON[B,H,W] -------- -------- -------- -----000			
0x2A0	IRQ039MON[B,H,W] -------- -------- -------- ------00			
0x2A4	IRQ040MON[B,H,W] -------- -------- -------- ------00			
0x2A8	IRQ041MON[B,H,W] -------- -------- -------- ------00			
0x2AC	IRQ042MON[B,H,W] -------- -------- -------- ------00			
0x2B0	IRQ043MON[B,H,W] -------- -------- -------- ------00			
0x2B4	IRQ044MON[B,H,W] -------- -------- -------- ------00			
0x2B8	IRQ045MON[B,H,W] -------- -------- -------- ------00			
0x2BC	IRQ046MON[B,H,W] -------- -------- -------- ------00			
0x2C0	IRQ047MON[B,H,W] -------- -------- -------- ------00			
0x2C4	IRQ048MON[B,H,W] -------- -------- -------- -------0			
0x2C8	IRQ049MON[B,H,W] -------- -------- -------- -------0			
0x2CC	IRQ050MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2D0	IRQ051MON[B,H,W] -------- -------- -------- -------0			
0x2D4	IRQ052MON[B,H,W] -------- -------- -------- -------0			
0x2D8	IRQ053MON[B,H,W] -------- -------- -------- -------0			
0x2DC	IRQ054MON[B,H,W] -------- -------- -------- -------0			
0x2E0	IRQ055MON[B,H,W] -------- -------- -------- -------0			
0x2E4	IRQ056MON[B,H,W] -------- -------- -------- -------0			
0x2E8	IRQ057MON[B,H,W] -------- -------- -------- -------0			
0x2EC	IRQ058MON[B,H,W] -------- -------- -------- -------0			
0x2F0	IRQ059MON[B,H,W] -------- -------- -------- ----0000			
0x2F4	IRQ060MON[B,H,W] -------- -------- -------- -------0			
0x2F8	IRQ061MON[B,H,W] -------- -------- -------- ------00			
0x2FC	IRQ062MON[B,H,W] -------- -------- -------- -------0			
0x300	IRQ063MON[B,H,W] -------- -------- -------- ------00			
0x304	IRQ064MON[B,H,W] -------- -------- -------- -------0			
0x308	IRQ065MON[B,H,W] -------- -------- -------- ------00			
0x30C	IRQ066MON[B,H,W] -------- -------- -------- -------0			
0x310	IRQ067MON[B,H,W] -------- -------- -------- ------00			
0x314	IRQ068MON[B,H,W] -------- -------- -------- -------0			
0x318	IRQ069MON[B,H,W] -------- -------- -------- ------00			
0x31C	IRQ070MON[B,H,W] -------- -------- -------- -------0			
0x320	IRQ071MON[B,H,W] -------- -------- -------- ------00			
0x324	IRQ072MON[B,H,W] -------- -------- -------- -------0			
0x328	IRQ073MON[B,H,W] -------- -------- -------- ------00			
0x32C	IRQ074MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x330	IRQ075MON[B,H,W] -------- -------- -------- ------00			
0x334	IRQ076MON[B,H,W] -------- -------- -------- ---00000			
0x338	IRQ077MON[B,H,W] -------- -------- -------- ---00000			
0x33C	IRQ078MON[B,H,W] -------- -------- -------- ---00000			
0x340	IRQ079MON[B,H,W] -------- -------- -------- --000000			
0x344	IRQ080MON[B,H,W] -------- -------- -------- -------0			
0x348	IRQ081MON[B,H,W] -------- -------- -------- -------0			
0x34C	IRQ082MON[B,H,W] -------- -------- -------- -----000			
0x350	IRQ083MON[B,H,W] -------- -------- -------- -------0			
0x354	IRQ084MON[B,H,W] -------- -------- -------- -------0			
0x358	IRQ085MON[B,H,W] -------- -------- -------- -------0			
0x35C	IRQ086MON[B,H,W] -------- -------- -------- -------0			
0x360	IRQ087MON[B,H,W] -------- -------- -------- -------0			
0x364	IRQ088MON[B,H,W] -------- -------- -------- -------0			
0x368	IRQ089MON[B,H,W] -------- -------- -------- -------0			
0x36C	IRQ090MON[B,H,W] -------- -------- -------- -------0			
0x370	IRQ091MON[B,H,W] -------- -------- -------- ------00			
0x374	IRQ092MON[B,H,W] -------- -------- -------- ----0000			
0x378	IRQ093MON[B,H,W] -------- -------- -------- ----0000			
0x37C	IRQ094MON[B,H,W] -------- -------- -------- ----0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x380	IRQ095MON[B,H,W] -------- -------- -------- ----0000			
0x384	IRQ096MON[B,H,W] -------- -------- -------- --000000			
0x388	IRQ097MON[B,H,W] -------- -------- -------- --000000			
0x38C	IRQ098MON[B,H,W] -------- -------- -------- ------00			
0x390	IRQ099MON[B,H,W] -------- -------- -------- ------00			
0x394	IRQ100MON[B,H,W] -------- -------- -------- ------00			
0x398	IRQ101MON[B,H,W] -------- -------- -------- ------00			
0x39C	IRQ102MON[B,H,W] -------- -------- -------- ------00			
0x3A0	IRQ103MON[B,H,W] -------- -------- -------- -------0			
0x3A4	IRQ104MON[B,H,W] -------- -------- -------- ------00			
0x3A8	IRQ105MON[B,H,W] -------- -------- -------- -------0			
0x3AC	IRQ106MON[B,H,W] -------- -------- -------- ------00			
0x3B0	IRQ107MON[B,H,W] -------- -------- -------- -------0			
0x3B4	IRQ108MON[B,H,W] -------- -------- -------- ------00			
0x3B8	IRQ109MON[B,H,W] -------- -------- -------- -------0			
0x3BC	IRQ110MON[B,H,W] -------- -------- -------- ------00			
0x3C0	IRQ111MON[B,H,W] -------- -------- -------- ---00000			
0x3C4	-	-	-	-
0x3C8	IRQ113MON[B,H,W] -------- -------- -------- ---00000			
0x3CC	IRQ114MON[B,H,W] -------- -------- -------- --000000			
0x3D0 – 0x3D8	-	-	-	-
0x3DC	IRQ118MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x3E0	IRQ119MON[B,H,W] -------- -------- -------- -------0			
0x3E4	IRQ120MON[B,H,W] -------- -------- -------- -------0			
0x3E8	IRQ121MON[B,H,W] -------- -------- -------- ------00			
0x3EC	IRQ122MON[B,H,W] -------- -------- -------- -------0			
0x3F0	IRQ123MON[B,H,W] -------- -------- -------- ------00			
0x3F4	IRQ124MON[B,H,W] -------- -------- -------- -------0			
0x3F8	IRQ125MON[B,H,W] -------- -------- -------- ------00			
0x3FC	IRQ126MON[B,H,W] -------- -------- -------- -------0			
0x400	IRQ127MON[B,H,W] -------- -------- -------- ------00			
0x404 – 0xFFC	-	-	-	-

A.1.17.2 TYPE3-M4, TYPE5-M4 product

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004 – 0x00C	-			
0x010	-	-	-	ODDPKS[B] ---00000
0x014	-	-	-	ODDPKS1[B] --00000
0x018	-	*	-	*
0x01C – 0x10C	-	-	-	-
0x110	IRQ003SEL[B,H,W] -------- 00000000 -------- 00000000			
0x114	IRQ004SEL[B,H,W] -------- 00000000 -------- 00000000			
0x118	IRQ005SEL[B,H,W] -------- 00000000 -------- 00000000			
0x11C	IRQ006SEL[B,H,W] -------- 00000000 -------- 00000000			
0x120	IRQ007SEL[B,H,W] -------- 00000000 -------- 00000000			
0x124	IRQ008SEL[B,H,W] -------- 00000000 -------- 00000000			
0x128	IRQ009SEL[B,H,W] -------- 00000000 -------- 00000000			
0x12C	IRQ010SEL[B,H,W] -------- 00000000 -------- 00000000			
0x130 – 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x204	IRQ000MON[B,H,W] -------- -------- -------- -------0			
0x208	IRQ001MON[B,H,W] -------- -------- -------- -------0			
0x20C	IRQ002MON[B,H,W] -------- -------- -------- -------0			
0x210	IRQ003MON[B,H,W] -------- -------- -------- 00000000			
0x214	IRQ004MON[B,H,W] -------- -------- -------- 00000000			
0x218	IRQ005MON[B,H,W] -------- -------- -------- 00000000			
0x21C	IRQ006MON[B,H,W] -------- -------- -------- 00000000			
0x220	IRQ007MON[B,H,W] -------- -------- -------- 00000000			
0x224	IRQ008MON[B,H,W] -------- -------- -------- 00000000			
0x228	IRQ009MON[B,H,W] -------- -------- -------- 00000000			
0x22C	IRQ010MON[B,H,W] -------- -------- -------- 00000000			
0x230	IRQ011MON[B,H,W] -------- -------- -------- -------0			
0x234	IRQ012MON[B,H,W] -------- -------- -------- -------0			
0x238	IRQ013MON[B,H,W] -------- -------- -------- -------0			
0x23C	IRQ014MON[B,H,W] -------- -------- -------- -------0			
0x240	IRQ015MON[B,H,W] -------- -------- -------- -------0			
0x244	IRQ016MON[B,H,W] -------- -------- -------- -------0			
0x248	IRQ017MON[B,H,W] -------- -------- -------- -------0			
0x24C	IRQ018MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x250	IRQ019MON[B,H,W] -------- -------- -------- --000000			
0x254	IRQ020MON[B,H,W] -------- -------- -------- --000000			
0x258	IRQ021MON[B,H,W] -------- -------- -------- ----0000			
0x25C	IRQ022MON[B,H,W] -------- -------- -------- ----0000			
0x260	IRQ023MON[B,H,W] -------- -------- -------- ----0000			
0x264	IRQ024MON[B,H,W] -------- -------- -------- -----000			
0x268	IRQ025MON[B,H,W] -------- -------- -------- -----000			
0x26C	IRQ026MON[B,H,W] -------- -------- -------- ----0000			
0x270	IRQ027MON[B,H,W] -------- -------- -------- --000000			
0x274	IRQ028MON[B,H,W] -------- -------- -------- -----000			
0x278	IRQ029MON[B,H,W] -------- -------- -------- -----000			
0x27C	IRQ030MON[B,H,W] -------- -------- -------- ----0000			
0x280	IRQ031MON[B,H,W] -------- -------- -------- --000000			
0x284	IRQ032MON[B,H,W] -------- -------- -------- -----000			
0x288	IRQ033MON[B,H,W] -------- -------- -------- -----000			
0x28C	IRQ034MON[B,H,W] -------- -------- -------- ---00000			
0x290	IRQ035MON[B,H,W] -------- -------- -------- --000000			
0x294	IRQ036MON[B,H,W] -------- -------- -------- -----000			
0x298	IRQ037MON[B,H,W] -------- -------- -------- -----000			
0x29C	IRQ038MON[B,H,W] -------- -------- -------- -----000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2A0	IRQ039MON[B,H,W] -------- -------- -------- ------00			
0x2A4	IRQ040MON[B,H,W] -------- -------- -------- ------00			
0x2A8	IRQ041MON[B,H,W] -------- -------- -------- ------00			
0x2AC	IRQ042MON[B,H,W] -------- -------- -------- ------00			
0x2B0	IRQ043MON[B,H,W] -------- -------- -------- ------00			
0x2B4	IRQ044MON[B,H,W] -------- -------- -------- ------00			
0x2B8	IRQ045MON[B,H,W] -------- -------- -------- ------00			
0x2BC	IRQ046MON[B,H,W] -------- -------- -------- ------00			
0x2C0	IRQ047MON[B,H,W] -------- -------- -------- ------00			
0x2C4	IRQ048MON[B,H,W] -------- -------- -------- -------0			
0x2C8	IRQ049MON[B,H,W] -------- -------- -------- -------0			
0x2CC	IRQ050MON[B,H,W] -------- -------- -------- -------0			
0x2D0	IRQ051MON[B,H,W] -------- -------- -------- -------0			
0x2D4	IRQ052MON[B,H,W] -------- -------- -------- -------0			
0x2D8	IRQ053MON[B,H,W] -------- -------- -------- -------0			
0x2DC	IRQ054MON[B,H,W] -------- -------- -------- -------0			
0x2E0	IRQ055MON[B,H,W] -------- -------- -------- -------0			
0x2E4	IRQ056MON[B,H,W] -------- -------- -------- -------0			
0x2E8	IRQ057MON[B,H,W] -------- -------- -------- -------0			
0x2EC	IRQ058MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2F0	IRQ059MON[B,H,W] -------- -------- -------- ---00000			
0x2F4	IRQ060MON[B,H,W] -------- -------- -------- -------0			
0x2F8	IRQ061MON[B,H,W] -------- -------- -------- ------00			
0x2FC	IRQ062MON[B,H,W] -------- -------- -------- -------0			
0x300	IRQ063MON[B,H,W] -------- -------- -------- ------00			
0x304	IRQ064MON[B,H,W] -------- -------- -------- -------0			
0x308	IRQ065MON[B,H,W] -------- -------- -------- ------00			
0x30C	IRQ066MON[B,H,W] -------- -------- -------- -------0			
0x310	IRQ067MON[B,H,W] -------- -------- -------- ------00			
0x314	IRQ068MON[B,H,W] -------- -------- -------- -------0			
0x318	IRQ069MON[B,H,W] -------- -------- -------- ------00			
0x31C	IRQ070MON[B,H,W] -------- -------- -------- -------0			
0x320	IRQ071MON[B,H,W] -------- -------- -------- ------00			
0x324	IRQ072MON[B,H,W] -------- -------- -------- -------0			
0x328	IRQ073MON[B,H,W] -------- -------- -------- ------00			
0x32C	IRQ074MON[B,H,W] -------- -------- -------- -------0			
0x330	IRQ075MON[B,H,W] -------- -------- -------- ------00			
0x334	IRQ076MON[B,H,W] -------- -------- -------- ---00000			
0x338	IRQ077MON[B,H,W] -------- -------- -------- ---00000			
0x33C	IRQ078MON[B,H,W] -------- -------- -------- ---00000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x340	IRQ079MON[B,H,W] -------- -------- -------- --000000			
0x344	IRQ080MON[B,H,W] -------- -------- -------- -------0			
0x348	IRQ081MON[B,H,W] -------- -------- -------- ---00000			
0x34C	IRQ082MON[B,H,W] -------- -------- -------- -----000			
0x350	IRQ083MON[B,H,W] -------- -------- -------- -------0			
0x354	IRQ084MON[B,H,W] -------- -------- -------- -------0			
0x358	IRQ085MON[B,H,W] -------- -------- -------- -------0			
0x35C	IRQ086MON[B,H,W] -------- -------- -------- -------0			
0x360	IRQ087MON[B,H,W] -------- -------- -------- -------0			
0x364	IRQ088MON[B,H,W] -------- -------- -------- -------0			
0x368	IRQ089MON[B,H,W] -------- -------- -------- -------0			
0x36C	IRQ090MON[B,H,W] -------- -------- -------- -------0			
0x370	IRQ091MON[B,H,W] -------- -------- -------- ------00			
0x374	IRQ092MON[B,H,W] -------- -------- -------- ----0000			
0x378	IRQ093MON[B,H,W] -------- -------- -------- ----0000			
0x37C	IRQ094MON[B,H,W] -------- -------- -------- ----0000			
0x380	IRQ095MON[B,H,W] -------- -------- -------- ----0000			
0x384	IRQ096MON[B,H,W] -------- -------- -------- --000000			
0x388	IRQ097MON[B,H,W] -------- -------- -------- --000000			
0x38C	IRQ098MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x390	IRQ099MON[B,H,W] -------- -------- -------- ------00			
0x394	IRQ100MON[B,H,W] -------- -------- -------- ------00			
0x398	IRQ101MON[B,H,W] -------- -------- -------- ------00			
0x39C	IRQ102MON[B,H,W] -------- -------- -------- ------00			
0x3A0	IRQ103MON[B,H,W] -------- -------- -------- -------0			
0x3A4	IRQ104MON[B,H,W] -------- -------- -------- ------00			
0x3A8	IRQ105MON[B,H,W] -------- -------- -------- -------0			
0x3AC	IRQ106MON[B,H,W] -------- -------- -------- ------00			
0x3B0	IRQ107MON[B,H,W] -------- -------- -------- -------0			
0x3B4	IRQ108MON[B,H,W] -------- -------- -------- ------00			
0x3B8	IRQ109MON[B,H,W] -------- -------- -------- -------0			
0x3BC	IRQ110MON[B,H,W] -------- -------- -------- ------00			
0x3C0	IRQ111MON[B,H,W] -------- -------- -------- ---00000			
0x3C4	IRQ112MON[B,H,W] -------- -------- -------- --000000			
0x3C8	IRQ113MON[B,H,W] -------- -------- -------- --000000			
0x3CC	IRQ114MON[B,H,W] -------- -------- -------- -0000000			
0x3D0	IRQ115MON[B,H,W] -------- -------- -------- -----000			
0x3D4	IRQ116MON[B,H,W] -------- -------- -------- --------			
0x3D8	IRQ117MON[B,H,W] -------- -------- -------- ------00			
0x3DC	IRQ118MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x3E0	IRQ119MON[B,H,W] -------- -------- -------- -------0			
0x3E4	IRQ120MON[B,H,W] -------- -------- -------- -------0			
0x3E8	IRQ121MON[B,H,W] -------- -------- -------- ------00			
0x3EC	IRQ122MON[B,H,W] -------- -------- -------- -------0			
0x3F0	IRQ123MON[B,H,W] -------- -------- -------- ------00			
0x3F4	IRQ124MON[B,H,W] -------- -------- -------- -------0			
0x3F8	IRQ125MON[B,H,W] -------- -------- -------- ------00			
0x3FC	IRQ126MON[B,H,W] -------- -------- -------- -------0			
0x400	IRQ127MON[B,H,W] -------- -------- -------- ------00			
0x404 – 0xFFC	-	-	-	-

A.1.17.3 TYPE4-M4 product

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004 – 0x00C	-			
0x010	-	-	-	ODDPKS[B] ---00000
0x014	-	-	-	ODDPKS1[B] --00000
0x018	-	*	-	*
0x01C – 0x10C	-	-	-	-
0x110	IRQ003SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x114	IRQ004SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x118	IRQ005SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x11C	IRQ006SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x120	IRQ007SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x124	IRQ008SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x128	IRQ009SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x12C	IRQ010SEL[B,H,W] 00000000 00000000 -------- 00000000			
0x130 – 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x204	IRQ000MON[B,H,W] -------- -------- -------- -------0			
0x208	IRQ001MON[B,H,W] -------- -------- -------- -------0			
0x20C	IRQ002MON[B,H,W] -------- -------- -------- -------0			
0x210	IRQ003MON[B,H,W] -------- -------- -------- 00000000			
0x214	IRQ004MON[B,H,W] -------- -------- -------- 00000000			
0x218	IRQ005MON[B,H,W] -------- -------- -------- 00000000			
0x21C	IRQ006MON[B,H,W] -------- -------- -------- 00000000			
0x220	IRQ007MON[B,H,W] -------- -------- -------- 00000000			
0x224	IRQ008MON[B,H,W] -------- -------- -------- 00000000			
0x228	IRQ009MON[B,H,W] -------- -------- -------- 00000000			
0x22C	IRQ010MON[B,H,W] -------- -------- -------- 00000000			
0x230	IRQ011MON[B,H,W] -------- -------- -------- -------0			
0x234	IRQ012MON[B,H,W] -------- -------- -------- -------0			
0x238	IRQ013MON[B,H,W] -------- -------- -------- -------0			
0x23C	IRQ014MON[B,H,W] -------- -------- -------- -------0			
0x240	IRQ015MON[B,H,W] -------- -------- -------- -------0			
0x244	IRQ016MON[B,H,W] -------- -------- -------- -------0			
0x248	IRQ017MON[B,H,W] -------- -------- -------- -------0			
0x24C	IRQ018MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x250	IRQ019MON[B,H,W] -------- -------- -------- --000000			
0x254	IRQ020MON[B,H,W] -------- -------- -------- --000000			
0x258	IRQ021MON[B,H,W] -------- -------- -------- ----0000			
0x25C	IRQ022MON[B,H,W] -------- -------- -------- ----0000			
0x260	IRQ023MON[B,H,W] -------- -------- -------- ----0000			
0x264	IRQ024MON[B,H,W] -------- -------- -------- -----000			
0x268	IRQ025MON[B,H,W] -------- -------- -------- -----000			
0x26C	IRQ026MON[B,H,W] -------- -------- -------- ----0000			
0x270	IRQ027MON[B,H,W] -------- -------- -------- --000000			
0x274	IRQ028MON[B,H,W] -------- -------- -------- -----000			
0x278	IRQ029MON[B,H,W] -------- -------- -------- -----000			
0x27C	IRQ030MON[B,H,W] -------- -------- -------- ----0000			
0x280	IRQ031MON[B,H,W] -------- -------- -------- --000000			
0x284	IRQ032MON[B,H,W] -------- -------- -------- -----000			
0x288	IRQ033MON[B,H,W] -------- -------- -------- -----000			
0x28C	IRQ034MON[B,H,W] -------- -------- -------- ---00000			
0x290	IRQ035MON[B,H,W] -------- -------- -------- --000000			
0x294	IRQ036MON[B,H,W] -------- -------- -------- -----000			
0x298	IRQ037MON[B,H,W] -------- -------- -------- -----000			
0x29C	IRQ038MON[B,H,W] -------- -------- -------- -----000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2A0	IRQ039MON[B,H,W] -------- -------- -------- ------00			
0x2A4	IRQ040MON[B,H,W] -------- -------- -------- ------00			
0x2A8	IRQ041MON[B,H,W] -------- -------- -------- ------00			
0x2AC	IRQ042MON[B,H,W] -------- -------- -------- ------00			
0x2B0	IRQ043MON[B,H,W] -------- -------- -------- ------00			
0x2B4	IRQ044MON[B,H,W] -------- -------- -------- ------00			
0x2B8	IRQ045MON[B,H,W] -------- -------- -------- ------00			
0x2BC	IRQ046MON[B,H,W] -------- -------- -------- ------00			
0x2C0	IRQ047MON[B,H,W] -------- -------- -------- ------00			
0x2C4	IRQ048MON[B,H,W] -------- -------- -------- -------0			
0x2C8	IRQ049MON[B,H,W] -------- -------- -------- ------00			
0x2CC	IRQ050MON[B,H,W] -------- -------- -------- -------0			
0x2D0	IRQ051MON[B,H,W] -------- -------- -------- -------0			
0x2D4	IRQ052MON[B,H,W] -------- -------- -------- -------0			
0x2D8	IRQ053MON[B,H,W] -------- -------- -------- -------0			
0x2DC	IRQ054MON[B,H,W] -------- -------- -------- -------0			
0x2E0	IRQ055MON[B,H,W] -------- -------- -------- -------0			
0x2E4	IRQ056MON[B,H,W] -------- -------- -------- -------0			
0x2E8	IRQ057MON[B,H,W] -------- -------- -------- -------0			
0x2EC	IRQ058MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2F0	IRQ059MON[B,H,W] -------- -------- -------- --000000			
0x2F4	IRQ060MON[B,H,W] -------- -------- -------- -------0			
0x2F8	IRQ061MON[B,H,W] -------- -------- -------- ------00			
0x2FC	IRQ062MON[B,H,W] -------- -------- -------- -------0			
0x300	IRQ063MON[B,H,W] -------- -------- -------- ------00			
0x304	IRQ064MON[B,H,W] -------- -------- -------- -------0			
0x308	IRQ065MON[B,H,W] -------- -------- -------- ------00			
0x30C	IRQ066MON[B,H,W] -------- -------- -------- -------0			
0x310	IRQ067MON[B,H,W] -------- -------- -------- ------00			
0x314	IRQ068MON[B,H,W] -------- -------- -------- -------0			
0x318	IRQ069MON[B,H,W] -------- -------- -------- ------00			
0x31C	IRQ070MON[B,H,W] -------- -------- -------- -------0			
0x320	IRQ071MON[B,H,W] -------- -------- -------- ------00			
0x324	IRQ072MON[B,H,W] -------- -------- -------- -------0			
0x328	IRQ073MON[B,H,W] -------- -------- -------- ------00			
0x32C	IRQ074MON[B,H,W] -------- -------- -------- -------0			
0x330	IRQ075MON[B,H,W] -------- -------- -------- ------00			
0x334	IRQ076MON[B,H,W] -------- -------- -------- ---00000			
0x338	IRQ077MON[B,H,W] -------- -------- -------- ---00000			
0x33C	IRQ078MON[B,H,W] -------- -------- -------- ---00000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x340	IRQ079MON[B,H,W] -------- -------- -------- --000000			
0x344	IRQ080MON[B,H,W] -------- -------- -------- -------0			
0x348	IRQ081MON[B,H,W] -------- -------- -------- ---00000			
0x34C	IRQ082MON[B,H,W] -------- -------- -------- -----000			
0x350	IRQ083MON[B,H,W] -------- -------- -------- -------0			
0x354	IRQ084MON[B,H,W] -------- -------- -------- -------0			
0x358	IRQ085MON[B,H,W] -------- -------- -------- -------0			
0x35C	IRQ086MON[B,H,W] -------- -------- -------- -------0			
0x360	IRQ087MON[B,H,W] -------- -------- -------- -------0			
0x364	IRQ088MON[B,H,W] -------- -------- -------- -------0			
0x368	IRQ089MON[B,H,W] -------- -------- -------- -------0			
0x36C	IRQ090MON[B,H,W] -------- -------- -------- -------0			
0x370	IRQ091MON[B,H,W] -------- -------- -------- ------00			
0x374	IRQ092MON[B,H,W] -------- -------- -------0 ----0000			
0x378	IRQ093MON[B,H,W] -------- -------- -------0 ----0000			
0x37C	IRQ094MON[B,H,W] -------- -------- -------0 ----0000			
0x380	IRQ095MON[B,H,W] -------- -------- -------0 ----0000			
0x384	IRQ096MON[B,H,W] -------- -------- -------0 --000000			
0x388	IRQ097MON[B,H,W] -------- -------- -------0 --000000			
0x38C	IRQ098MON[B,H,W] -------- -------- -------0 ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x390	IRQ099MON[B,H,W] -------- -------- -------0 ------00			
0x394	IRQ100MON[B,H,W] -------- -------- -------0 ------00			
0x398	IRQ101MON[B,H,W] -------- -------- -------0 ------00			
0x39C	IRQ102MON[B,H,W] -------- -------- -------0 ------00			
0x3A0	IRQ103MON[B,H,W] -------- -------- -------0 -------0			
0x3A4	IRQ104MON[B,H,W] -------- -------- -------0 ------00			
0x3A8	IRQ105MON[B,H,W] -------- -------- -------0 -------0			
0x3AC	IRQ106MON[B,H,W] -------- -------- -------0 ------00			
0x3B0	IRQ107MON[B,H,W] -------- -------- -------0 -------0			
0x3B4	IRQ108MON[B,H,W] -------- -------- -------0 ------00			
0x3B8	IRQ109MON[B,H,W] -------- -------- -------0 -------0			
0x3BC	IRQ110MON[B,H,W] -------- -------- -------0 ------00			
0x3C0	IRQ111MON[B,H,W] -------- -------- -------- ---00000			
0x3C4	IRQ112MON[B,H,W] -------- -------- ------00 00000000			
0x3C8	IRQ113MON[B,H,W] -------- -------- -------- --000000			
0x3CC	IRQ114MON[B,H,W] -------- -------- -------- -0000000			
0x3D0	IRQ115MON[B,H,W] -------- -------- -------- -----000			
0x3D4	IRQ116MON[B,H,W] -------- -------- -------- --------			
0x3D8	IRQ117MON[B,H,W] -------- -------- -------- -----000			
0x3DC	IRQ118MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x3E0	IRQ119MON[B,H,W] -------- -------- -------- -------0			
0x3E4	IRQ120MON[B,H,W] -------- -------- -------0 -------0			
0x3E8	IRQ121MON[B,H,W] -------- -------- -------0 ------00			
0x3EC	IRQ122MON[B,H,W] -------- -------- -------0 -------0			
0x3F0	IRQ123MON[B,H,W] -------- -------- -------0 ------00			
0x3F4	IRQ124MON[B,H,W] -------- -------- -------- -------0			
0x3F8	IRQ125MON[B,H,W] -------- -------- -------- ------00			
0x3FC	IRQ126MON[B,H,W] -------- -------- -------- -------0			
0x400	IRQ127MON[B,H,W] -------- -------- -------- ------00			
0x404 – 0xFFC	-	-	-	-

A.1.18 D/AC

12bit D/AC unit0 Base_Address : 0x4003_3000

12bit D/AC unit1 Base_Address : 0x4003_3008

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	DACR[B,H,W] --00--00
0x004	-	-	DADR[H,W] ----XXXX XXXXXXXX	
0x010 – 0xFFC	-	-	-	-

A.1.19 HDMI-CEC

HDMI-CEC/Remote Control Receiver ch.0 Base_Address : 0x4003_4000

HDMI-CEC/Remote Control Receiver ch.1 Base_Address : 0x4003_4100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	TXCTRL[B,H,W] --0000-0
0x004	-	-	-	TXDATA[B,H,W] 00000000
0x008	-	-	-	TXSTS[B,H,W] --00---0
0x00C	-	-	-	SFREE[B,H,W] ----0000
0x010 – 0x03C	-	-	-	-
0x040	-	-	RCCR[B,H,W] 0---0000	RCST[B,H,W] 00000000
0x044	-	-	RCSHW[B,H,W] 00000000	RCDAHW[B,H,W] 00000000
0x048	-	-	RCDBHW[B,H,W] 00000000	-
0x04C	-	-	RCADR1[B,H,W] ---00000	RCADR2[B,H,W] ---00000
0x050	-	-	RCDTHH[B,H,W] 00000000	RCDTHL[B,H,W] 00000000
0x054	-	-	RCDTLH[B,H,W] 00000000	RCDTLL[B,H,W] 00000000
0x058	-	-	RCCKD[B,H,W] ---00000 00000000	
0x05C	-	-	RCRC[B,H,W] ---0---0	RCRHW[B,H,W] 00000000
0x060	-	-	RCLE[B,H,W] 00000-00	-
0x064	-	-	RCLELW[B,H,W] 00000000	RCLESW[B,H,W] 00000000
0x068 – 0x0FC	-	-	-	-

A.1.20 GPIO

A.1.20.1 TYPE1-M4, TYPE2-M4, TYPE6-M4 products

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- --00 ---- --11 --0- --0- 0000 --00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 ----			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			
0x654 – 0x6FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

A.1.20.2 TYPE3-M4 product

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- 0000 ---- --11 --0- --0- 0000 –00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 0000			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x654	EPFR21[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x658	EPFR22[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x65C	EPFR23[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x660	EPFR24[B,H,W] ---- ---- ---- ---- ---- 0000 0000 0000			
0x664	EPFR25[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x668	EPFR26[B,H,W] ---- ---- ---- --00 0000 0000 0000 0000			
0x66C – 0x6FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740	PDSR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x744	PDSR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x748	PDSR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x74C	PDSR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x750	PDSR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x754	PDSR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x758	PDSR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x75C	PDSR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x760	PDSR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x764	PDSR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x768	PDSRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x76C	PDSRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x770	PDSRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x774	PDSRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x778	PDSRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x77C	PDSRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x780 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

A.1.20.3 TYPE4-M4 product

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- 0000 ---- --11 --0- --0- 0000 –00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- 0000 0000 0000 0000 0000 0000 ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 0000			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			
0x654	EPFR21[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x658	EPFR22[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x65C	EPFR23[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x660	EPFR24[B,H,W] ---- 0000 0000 0000 ---- 0000 0000 0000			
0x664	EPFR25[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x668	EPFR26[B,H,W] ---- ---- ---- --00 0000 0000 0000 0000			
0x66C	EPFR27[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x670	EPFR28[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x674	EPFR29[B,H,W] 0000 0000 0000 00-- 0000 0000 0000 0000			
0x67C	EPFR30[B,H,W] ---- --00 0000 0000 ---- 0000 0000 0000			
0x680 – 0x6FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

A.1.20.4 TYPE5-M4 product

GPIO Base_Address : 0x4006_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C	PFR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x020	PFR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x024	PFR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x028	PFRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x02C	PFRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x030	PFRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x034	PFRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C	PFRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x040 - 0x0FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	PCR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x118	PCR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x11C	PCR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x120	-			
0x124	PCR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x128	PCRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x12C	PCRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x130	PCRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x134	PCRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x138	PCRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x13C	PCRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x140 - 0x1FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C	DDR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x220	DDR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x224	DDR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x228	DDRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x22C	DDRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x230	DDRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x234	DDRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C	DDRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x240 - 0x2FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C	PDIR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x320	PDIR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x324	PDIR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x328	PDIRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x32C	PDIRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x330	PDIRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x334	PDIRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C	PDIRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x340 - 0x3FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C	PDOR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x420	PDOR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x424	PDOR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x428	PDORA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x42C	PDORB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x430	PDORC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x434	PDORD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C	PDORF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x440 - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] 1111 1111 1111 1111 1111 1111 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 01--			
0x584 - 0x5FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x600	EPFR00[B,H,W] ---- 0000 ---- --11 --0- --0- 0000 –00			
0x604	EPFR01[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x608	EPFR02[B,H,W] 0000 0000 0000 0000 ---0 0000 0000 0000			
0x60C	EPFR03[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] 0000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	EPFR10[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x62C	EPFR11[B,H,W] ---- --00 0000 0000 0000 0000 0000 0000			
0x630	EPFR12[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x634	EPFR13[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x638	EPFR14[B,H,W] --00 0000 0000 00-- ---- ---- --00 0000			
0x63C	EPFR15[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x640	EPFR16[B,H,W] --00 0000 0000 0000 0000 0000 0000 0000			
0x644	EPFR17[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x648	EPFR18[B,H,W] --00 0000 0000 0000 00-- --00 0000 0000			
0x64C	EPFR19[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x650	EPFR20[B,H,W] ---- ---0 0000 0000 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x654	EPFR21[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x658	EPFR22[B,H,W] ---- ---- ---- ---- ---- ---- ---- ----			
0x65C	EPFR23[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x660	EPFR24[B,H,W] ---- ---- ---- ---- ---- 0000 0000 0000			
0x664	EPFR25[B,H,W] ---- ---- ---- ---- ---- ---- ---- 0000			
0x668	EPFR26[B,H,W] ---- ---- ---- --00 0000 0000 0000 0000			
0x66C – 0x680	-	-	-	-
0x684	EPFR33[B,H,W] ---- 0000 0000 0000 ---- 0000 0000 0000			
0x688	-	-	-	-
0x68C	EPFR35[B,H,W] ---- 0000 0000 0000 ---- ---- ---- ----			
0x690 – 0x6FC	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	PZR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x720	PZR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x724	PZR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x728	PZRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x72C	PZRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x730	PZRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x734	PZRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C	PZRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x740	PDSR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x744	PDSR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x748	PDSR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x74C	PDSR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x750	PDSR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x754	PDSR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x758	PDSR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x75C	PDSR7[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x760	PDSR8[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x764	PDSR9[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x768	PDSRA[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x76C	PDSRB[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x770	PDSRC[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x774	PDSRD[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x778	PDSRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x77C	PDSRF[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x780 - 0xEFC	-	-	-	-
0xF00 – 0xF04	*			
0xF08 – 0xFDC	-	-	-	-
0xFE0	*			
0xFE4 - 0xFFC	-	-	-	-

A.1.21 LVD

LVD Base_Address : 0x4003_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	LVD_CTL[B,H,W] 000111--
0x004	-	-	-	LVD_STR[B,H,W] 0-------
0x008	-	-	-	LVD_CLR[B,H,W] 1-------
0x00C	LVD_RLR[W] 00000000 00000000 00000000 00000001			
0x010	-	-	-	LVD_STR2 [B,H,W] 0-------
0x014 - 0x0FC	-	-	-	-

A.1.22 DS_Mode

DS_Mode Base_Address : 0x4003_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	*
0x004	-	-	-	RCK_CTL[B,H,W] ------01
0x008 - 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL[B,H,W] -------0
0x704	-	-	-	WRFSR[B,H,W] ------00
0x708	-	-	WIFSR[B,H,W] ------00 00000000	
0x70C	-	-	WIER[B,H,W] ------00 00000-00	
0x710	-	-	-	WILVR[B,H,W] ---00000
0x714	-	-	-	DSRAMR[B,H,W] ------00
0x718 - 0x7FC	-	-	-	-
0x800	BUR04[B,H,W] 00000000	BUR03[B,H,W] 00000000	BUR02[B,H,W] 00000000	BUR01[B,H,W] 00000000
0x804	BUR08[B,H,W] 00000000	BUR07[B,H,W] 00000000	BUR06[B,H,W] 00000000	BUR05[B,H,W] 00000000
0x808	BUR012[B,H,W] 00000000	BUR11[B,H,W] 00000000	BUR10[B,H,W] 00000000	BUR09[B,H,W] 00000000
0x80C	BUR16[B,H,W] 00000000	BUR15[B,H,W] 00000000	BUR14[B,H,W] 00000000	BUR13[B,H,W] 00000000
0x810 - 0xEFC	-	-	-	-

A.1.23 USB Clock

USB Clock Base_Address : 0x4003_6000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	UCCR[B,H,W] -0000000
0x004	-	-	-	UPCR1[B,H,W] ------00
0x008	-	-	-	UPCR2[B,H,W] -----000
0x00C	-	-	-	UPCR3[B,H,W] ---00000
0x010	-	-	-	UPCR4[B,H,W] -0111011
0x014	-	-	-	UP_STR[B,H,W] -------0
0x018	-	-	-	UPINT_ENR[B,H,W] -------0
0x01C	-	-	-	UPINT_CLR[B,H,W] -------0
0x020	-	-	-	UPINT_STR[B,H,W] -------0
0x024	-	-	-	UPCR5[B,H,W] ----0100
0x028	-	-	-	UPCR6[B,H,W] ----0010
0x02C	-	-	-	UPCR7[B,H,W] -------0
0x030	-	-	-	USBEN0[B,H,W] -------0
0x034	-	-	-	USBEN1[B,H,W] -------0
0x038 - 0x0FC	-	-	-	-

A.1.24 CAN_Prescaler

CAN_Prescaler Base_Address : 0x4003_7000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	CANPRE[B,H,W] ----1011
0x004 - 0xFFC	-	-	-	-

A.1.25 MFS

MFS ch.0 **Base_Address : 0x4003_8000**

MFS ch.1 **Base_Address : 0x4003_8100**

MFS ch.2 **Base_Address : 0x4003_8200**

MFS ch.3 **Base_Address : 0x4003_8300**

MFS ch.4 **Base_Address : 0x4003_8400**

MFS ch.5 **Base_Address : 0x4003_8500**

MFS ch.6 **Base_Address : 0x4003_8600**

MFS ch.7 **Base_Address : 0x4003_8700**

MFS ch.8 **Base_Address : 0x4003_8800**

MFS ch.9 **Base_Address : 0x4003_8900**

MFS ch.10 **Base_Address : 0x4003_8A00**

MFS ch.11 **Base_Address : 0x4003_8B00**

MFS ch.12 **Base_Address : 0x4003_8C00**

MFS ch.13 **Base_Address : 0x4003_8D00**

MFS ch.14 **Base_Address : 0x4003_8E00**

MFS ch.15 **Base_Address : 0x4003_8F00**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	SCR / IBCR[B,H,W] 0--00000	SMR[B,H,W] 000-00-0
0x004	-	-	SSR[B,H,W] 0-000011	ESCR / IBSR[B,H,W] 00000000
0x008	-	-	RDR/TDR[H,W] 00000000 00000000	
	(*1) RDR/TDR[H,W] 00000000 00000000 00000000 00000000			
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x010	-	-	ISMK[B,H,W] --------	ISBA[B,H,W] --------
0x014	-	-	FCR1[B,H,W] ---00100	FCR0[B,H,W] -0000000
0x018	-	-	FBYTE2[B,H,W] 00000000	FBYTE1[B,H,W] 00000000
0x01C	-	-	SCSTR1/ EIBCR[B,H,W] 00000000	SCSTR0/ NFCR[B,H,W] 00000000
0x020	-	-	SCSTR3[B,H,W] 00000000	SCSTR2[B,H,W] 00000000
0x024	-	-	SACSR1[B,H,W] 00000000	SACSR0[B,H,W] 00000000
0x028	-	-	STMR1[B,H,W] 00000000	STMR0[B,H,W] 00000000
0x02C	-	-	STMCR1[B,H,W] 00000000	STMCR0[B,H,W] 00000000
0x030	-	-	SCSCR1[B,H,W] 00000000	SCSCR0[B,H,W] 00100000
0x034	-	-	SCSFR1[B,H,W] 10000000	SCSFR0[B,H,W] 10000000
0x038	-	-	-	SCSFR2[B,H,W] 10000000
0x03C	-	-	TBYTE1[B,H,W] 00000000	TBYTE0[B,H,W] 00000000
0x040	-	-	TBYTE3[B,H,W] 00000000	TBYTE2[B,H,W] 00000000
0x0144 - 0x1FC	-	-	-	-

Note:

- *(*1): RDR/TDR register's higher 16 bits can be accessed by word operation in I2S mode.*

A.1.26 CRC

CRC Base_Address : 0x4003_9000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W] -0000000
0x004	CRCINIT[B,H,W] 11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W] 00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W] 11111111 11111111 11111111 11111111			

A.1.27 Watch Counter

Watch Counter Base_Address : 0x4003_A000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	WCCR[B,H,W] 00--0000	WCRL[B,H,W] --000000	WCRD[B,H,W] --000000
0x004 - 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W] -----000 ------00	
0x014	-	-	-	CLK_EN[B,H,W] ------00
0x018 - 0xFFC	-	-	-	-

A.1.28 RTC

A.1.28.1 TYPE1-M4, TYPE2-M4, TYPE3-M4, TYPE6-M4 products

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	-	-	-	WTCR10[B,H,W] 00000000
0x104	-	-	-	WTCR11[B,H,W] ---00000
0x108	-	-	-	WTCR12[B,H,W] 00000000
0x10C	-	-	-	WTCR13[B,H,W] 00000000
0x110	-	-	-	WTCR20[B,H,W] --000000
0x114	-	-	-	WTCR21[B,H,W] -----000
0x118	-	-	-	*
0x11C	-	-	-	WTSR[B,H,W] -0000000
0x120	-	-	-	WTMIR[B,H,W] -0000000
0x124	-	-	-	WTHR[B,H,W] --000000
0x128	-	-	-	WTDR[B,H,W] --000000
0x12C	-	-	-	WTDW[B,H,W] -----000
0x130	-	-	-	WTMOR[B,H,W] ---00000
0x134	-	-	-	WTYR[B,H,W] 00000000
0x138	-	-	-	ALMIR[B,H,W] -0000000
0x13C	-	-	-	ALHR[B,H,W] --000000
0x140	-	-	-	ALDR[B,H,W] --000000
0x144	-	-	-	ALMOR[B,H,W] ---00000
0x148	-	-	-	ALYR[B,H,W] 00000000
0x14C	-	-	-	WTTR0[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x150	-	-	-	WTTR1[B,H,W] 00000000
0x154	-	-	-	WTTR2[B,H,W] ------00
0x158	-	-	-	WTCAL0[B,H,W] 00000000
0x15C	-	-	-	WTCAL1[B,H,W] ------00
0x160	-	-	-	WTCALEN[B,H,W] -------0
0x164	-	-	-	WTDIV[B,H,W] ----0000
0x168	-	-	-	WTDIVEN[B,H,W] ------00
0x16C	-	-	-	WTCALPRD[B,H,W] --010011
0x170	-	-	-	WTCOSEL[B,H,W] -------0
0x174	-	-	-	VB_CLKDIV[B,H,W] 00000111
0x178	-	-	-	WTOSCCNT[B,H,W] ------01
0x17C	-	-	-	CCS[B,H,W] 00001000
0x180	-	-	-	CCB[B,H,W] 00010000
0x184	-	-	-	*
0x188	-	-	-	BOOST[B,H,W] ------11
0x18C	-	-	-	EWKUP[B,H,W] -------0
0x190	-	-	-	VDET[B,H,W] 00------
0x194	-	-	-	*
0x198	-	-	-	HIBRST[B,H,W] -------0
0x19C	-	-	-	VBPFR[B,H,W] --011100
0x1A0	-	-	-	VBPCR[B,H,W] ----0000
0x1A4	-	-	-	VBDDR[B,H,W] ----XXXX
0x1A8	-	-	-	VBDIR[B,H,W] ----0000
0x1AC	-	-	-	VBDOR[B,H,W] ----1111

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1B0	-	-	-	VBPZR[B,H,W] ------11
0x1B4-1FF	-	-	-	-
0x200	BREG03[B,H,W] 00000000	BREG02[B,H,W] 00000000	BREG01[B,H,W] 00000000	BREG00[B,H,W] 00000000
0x204	BREG07[B,H,W] 00000000	BREG06[B,H,W] 00000000	BREG05[B,H,W] 00000000	BREG04[B,H,W] 00000000
0x208	BREG0B[B,H,W] 00000000	BREG0A[B,H,W] 00000000	BREG09[B,H,W] 00000000	BREG08[B,H,W] 00000000
0x20C	BREG0F[B,H,W] 00000000	BREG0E[B,H,W] 00000000	BREG0D[B,H,W] 00000000	BREG0C[B,H,W] 00000000
0x210	BREG13[B,H,W] 00000000	BREG12[B,H,W] 00000000	BREG11[B,H,W] 00000000	BREG10[B,H,W] 00000000
0x214	BREG17[B,H,W] 00000000	BREG16[B,H,W] 00000000	BREG15[B,H,W] 00000000	BREG14[B,H,W] 00000000
0x218	BREG1B[B,H,W] 00000000	BREG1A[B,H,W] 00000000	BREG19[B,H,W] 00000000	BREG18[B,H,W] 00000000
0x21C	BREG1F[B,H,W] 00000000	BREG1E[B,H,W] 00000000	BREG1D[B,H,W] 00000000	BREG1C[B,H,W] 00000000
0x220	BREG23[B,H,W] 00000000	BREG22[B,H,W] 00000000	BREG21[B,H,W] 00000000	BREG20[B,H,W] 00000000
0x224	BREG27[B,H,W] 00000000	BREG26[B,H,W] 00000000	BREG25[B,H,W] 00000000	BREG24[B,H,W] 00000000
0x228	BREG2B[B,H,W] 00000000	BREG2A[B,H,W] 00000000	BREG29[B,H,W] 00000000	BREG28[B,H,W] 00000000
0x22C	BREG2F[B,H,W] 00000000	BREG2E[B,H,W] 00000000	BREG2D[B,H,W] 00000000	BREG2C[B,H,W] 00000000
0x230	BREG33[B,H,W] 00000000	BREG32[B,H,W] 00000000	BREG31[B,H,W] 00000000	BREG30[B,H,W] 00000000
0x234	BREG37[B,H,W] 00000000	BREG36[B,H,W] 00000000	BREG35[B,H,W] 00000000	BREG34[B,H,W] 00000000
0x238	BREG3B[B,H,W] 00000000	BREG3A[B,H,W] 00000000	BREG39[B,H,W] 00000000	BREG38[B,H,W] 00000000
0x23C	BREG3F[B,H,W] 00000000	BREG3E[B,H,W] 00000000	BREG3D[B,H,W] 00000000	BREG3C[B,H,W] 00000000
0x240	BREG43[B,H,W] 00000000	BREG42[B,H,W] 00000000	BREG41[B,H,W] 00000000	BREG40[B,H,W] 00000000
0x244	BREG47[B,H,W] 00000000	BREG46[B,H,W] 00000000	BREG45[B,H,W] 00000000	BREG44[B,H,W] 00000000
0x248	BREG4B[B,H,W] 00000000	BREG4A[B,H,W] 00000000	BREG49[B,H,W] 00000000	BREG48[B,H,W] 00000000
0x24C	BREG4F[B,H,W] 00000000	BREG4E[B,H,W] 00000000	BREG4D[B,H,W] 00000000	BREG4C[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x250	BREG53[B,H,W] 00000000	BREG52[B,H,W] 00000000	BREG51[B,H,W] 00000000	BREG50[B,H,W] 00000000
0x254	BREG57[B,H,W] 00000000	BREG56[B,H,W] 00000000	BREG55[B,H,W] 00000000	BREG54[B,H,W] 00000000
0x258	BREG5B[B,H,W] 00000000	BREG5A[B,H,W] 00000000	BREG59[B,H,W] 00000000	BREG58[B,H,W] 00000000
0x25C	BREG5F[B,H,W] 00000000	BREG5E[B,H,W] 00000000	BREG5D[B,H,W] 00000000	BREG5C[B,H,W] 00000000
0x260	BREG63[B,H,W] 00000000	BREG62[B,H,W] 00000000	BREG61[B,H,W] 00000000	BREG60[B,H,W] 00000000
0x264	BREG67[B,H,W] 00000000	BREG66[B,H,W] 00000000	BREG65[B,H,W] 00000000	BREG64[B,H,W] 00000000
0x268	BREG6B[B,H,W] 00000000	BREG6A[B,H,W] 00000000	BREG69[B,H,W] 00000000	BREG68[B,H,W] 00000000
0x26C	BREG6F[B,H,W] 00000000	BREG6E[B,H,W] 00000000	BREG6D[B,H,W] 00000000	BREG6C[B,H,W] 00000000
0x270	BREG73[B,H,W] 00000000	BREG72[B,H,W] 00000000	BREG71[B,H,W] 00000000	BREG70[B,H,W] 00000000
0x274	BREG77[B,H,W] 00000000	BREG76[B,H,W] 00000000	BREG75[B,H,W] 00000000	BREG74[B,H,W] 00000000
0x278	BREG7B[B,H,W] 00000000	BREG7A[B,H,W] 00000000	BREG79[B,H,W] 00000000	BREG78[B,H,W] 00000000
0x27C	BREG7F[B,H,W] 00000000	BREG7E[B,H,W] 00000000	BREG7D[B,H,W] 00000000	BREG7C[B,H,W] 00000000
0x280-0xFFC	-	-	-	-

A.1.28.2 TYPE4-M4 product

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100	-	-	-	WTCR10[B,H,W] 00000000
0x104	-	-	-	WTCR11[B,H,W] ---00000
0x108	-	-	-	WTCR12[B,H,W] 00000000
0x10C	-	-	-	WTCR13[B,H,W] 00000000
0x110	-	-	-	WTCR20[B,H,W] --000000
0x114	-	-	-	WTCR21[B,H,W] -----000
0x118	-	-	-	*
0x11C	-	-	-	WTSR[B,H,W] -0000000
0x120	-	-	-	WTMIR[B,H,W] -0000000
0x124	-	-	-	WTHR[B,H,W] --000000
0x128	-	-	-	WTDR[B,H,W] --000000
0x12C	-	-	-	WTDW[B,H,W] -----000
0x130	-	-	-	WTMOR[B,H,W] ---00000
0x134	-	-	-	WTYR[B,H,W] 00000000
0x138	-	-	-	ALMIR[B,H,W] -0000000
0x13C	-	-	-	ALHR[B,H,W] --000000
0x140	-	-	-	ALDR[B,H,W] --000000
0x144	-	-	-	ALMOR[B,H,W] ---00000
0x148	-	-	-	ALYR[B,H,W] 00000000
0x14C	-	-	-	WTTR0[B,H,W] 00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x150	-	-	-	WTTR1[B,H,W] 00000000
0x154	-	-	-	WTTR2[B,H,W] ------00
0x158	-	-	-	WTCAL0[B,H,W] 00000000
0x15C	-	-	-	WTCAL1[B,H,W] ------00
0x160	-	-	-	WTCALEN[B,H,W] -------0
0x164	-	-	-	WTDIV[B,H,W] ----0000
0x168	-	-	-	WTDIVEN[B,H,W] ------00
0x16C	-	-	-	WTCALPRD[B,H,W] --010011
0x170	-	-	-	WTCOSEL[B,H,W] -------0
0x174	-	-	-	VB_DIVCLK[B,H,W] 00000111
0x178	-	-	-	WTOSCCNT[B,H,W] ------01
0x17C	-	-	-	CCS[B,H,W] 11001110
0x180	-	-	-	CCB[B,H,W] 11001110
0x184	-	-	-	*
0x188	-	-	-	BOOST[B,H,W] ------11
0x18C	-	-	-	EWKUP[B,H,W] -------0
0x190	-	-	-	VDET[B,H,W] 00------
0x194	-	-	-	*
0x198	-	-	-	HIBRST[B,H,W] -------0
0x19C	-	-	-	VBPFR[B,H,W] --011100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x1A0	-	-	-	VBPCR[B,H,W] ----0000
0x1A4	-	-	-	VBDDR[B,H,W] ----0000
0x1A8	-	-	-	VBDIR[B,H,W] ----XXXX
0x1AC	-	-	-	VBDOR[B,H,W] ----1111
0x1B0	-	-	-	VBPZR[B,H,W] ------11
0x1B4-1FF	-	-	-	-
0x200	BREG03[B,H,W]	BREG02[B,H,W]	BREG01[B,H,W]	BREG00[B,H,W]
	00000000	00000000	00000000	00000000
0x204	BREG07[B,H,W]	BREG06[B,H,W]	BREG05[B,H,W]	BREG04[B,H,W]
	00000000	00000000	00000000	00000000
0x208	BREG0B[B,H,W]	BREG0A[B,H,W]	BREG09[B,H,W]	BREG08[B,H,W]
	00000000	00000000	00000000	00000000
0x20C	BREG0F[B,H,W]	BREG0E[B,H,W]	BREG0D[B,H,W]	BREG0C[B,H,W]
	00000000	00000000	00000000	00000000
0x210	BREG13[B,H,W]	BREG12[B,H,W]	BREG11[B,H,W]	BREG10[B,H,W]
	00000000	00000000	00000000	00000000
0x214	BREG17[B,H,W]	BREG16[B,H,W]	BREG15[B,H,W]	BREG14[B,H,W]
	00000000	00000000	00000000	00000000
0x218	BREG1B[B,H,W]	BREG1A[B,H,W]	BREG19[B,H,W]	BREG18[B,H,W]
	00000000	00000000	00000000	00000000
0x21C	BREG1F[B,H,W]	BREG1E[B,H,W]	BREG1D[B,H,W]	BREG1C[B,H,W]
	00000000	00000000	00000000	00000000
0x220	BREG23[B,H,W]	BREG22[B,H,W]	BREG21[B,H,W]	BREG20[B,H,W]
	00000000	00000000	00000000	00000000
0x224	BREG27[B,H,W]	BREG26[B,H,W]	BREG25[B,H,W]	BREG24[B,H,W]
	00000000	00000000	00000000	00000000
0x228	BREG2B[B,H,W]	BREG2A[B,H,W]	BREG29[B,H,W]	BREG28[B,H,W]
	00000000	00000000	00000000	00000000
0x22C	BREG2F[B,H,W]	BREG2E[B,H,W]	BREG2D[B,H,W]	BREG2C[B,H,W]
	00000000	00000000	00000000	00000000
0x230	BREG33[B,H,W]	BREG32[B,H,W]	BREG31[B,H,W]	BREG30[B,H,W]
	00000000	00000000	00000000	00000000
0x234	BREG37[B,H,W]	BREG36[B,H,W]	BREG35[B,H,W]	BREG34[B,H,W]
	00000000	00000000	00000000	00000000
0x238	BREG3B[B,H,W]	BREG3A[B,H,W]	BREG39[B,H,W]	BREG38[B,H,W]
	00000000	00000000	00000000	00000000
0x23C	BREG3F[B,H,W]	BREG3E[B,H,W]	BREG3D[B,H,W]	BREG3C[B,H,W]
	00000000	00000000	00000000	00000000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x240	BREG43[B,H,W]	BREG42[B,H,W]	BREG41[B,H,W]	BREG40[B,H,W]
	00000000	00000000	00000000	00000000
0x244	BREG47[B,H,W]	BREG46[B,H,W]	BREG45[B,H,W]	BREG44[B,H,W]
	00000000	00000000	00000000	00000000
0x248	BREG4B[B,H,W]	BREG4A[B,H,W]	BREG49[B,H,W]	BREG48[B,H,W]
	00000000	00000000	00000000	00000000
0x24C	BREG4F[B,H,W]	BREG4E[B,H,W]	BREG4D[B,H,W]	BREG4C[B,H,W]
	00000000	00000000	00000000	00000000
0x250	BREG53[B,H,W]	BREG52[B,H,W]	BREG51[B,H,W]	BREG50[B,H,W]
	00000000	00000000	00000000	00000000
0x254	BREG57[B,H,W]	BREG56[B,H,W]	BREG55[B,H,W]	BREG54[B,H,W]
	00000000	00000000	00000000	00000000
0x258	BREG5B[B,H,W]	BREG5A[B,H,W]	BREG59[B,H,W]	BREG58[B,H,W]
	00000000	00000000	00000000	00000000
0x25C	BREG5F[B,H,W]	BREG5E[B,H,W]	BREG5D[B,H,W]	BREG5C[B,H,W]
	00000000	00000000	00000000	00000000
0x260	BREG63[B,H,W]	BREG62[B,H,W]	BREG61[B,H,W]	BREG60[B,H,W]
	00000000	00000000	00000000	00000000
0x264	BREG67[B,H,W]	BREG66[B,H,W]	BREG65[B,H,W]	BREG64[B,H,W]
	00000000	00000000	00000000	00000000
0x268	BREG6B[B,H,W]	BREG6A[B,H,W]	BREG69[B,H,W]	BREG68[B,H,W]
	00000000	00000000	00000000	00000000
0x26C	BREG6F[B,H,W]	BREG6E[B,H,W]	BREG6D[B,H,W]	BREG6C[B,H,W]
	00000000	00000000	00000000	00000000
0x270	BREG73[B,H,W]	BREG72[B,H,W]	BREG71[B,H,W]	BREG70[B,H,W]
	00000000	00000000	00000000	00000000
0x274	BREG77[B,H,W]	BREG76[B,H,W]	BREG75[B,H,W]	BREG74[B,H,W]
	00000000	00000000	00000000	00000000
0x278	BREG7B[B,H,W]	BREG7A[B,H,W]	BREG79[B,H,W]	BREG78[B,H,W]
	00000000	00000000	00000000	00000000
0x27C	BREG7F[B,H,W]	BREG7E[B,H,W]	BREG7D[B,H,W]	BREG7C[B,H,W]
	00000000	00000000	00000000	00000000
0x280-0xFFC	-	-	-	-

A.1.28.3 TYPE5-M4 product

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WTCR1 [B,H,W] 00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W] -------- -------- -----000 -------0			
0x008	WTBR [B,H,W] -------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W] --000000	WTHR[B,H,W] --000000	WTMIR[B,H,W] -0000000	WTSR[B,H,W] -0000000
0x010	-	WTYR[B,H,W] 00000000	WTMOR[B,H,W] ---00000	WTDW[B,H,W] -----000
0x014	ALDR[B,H,W] --000000	ALHR[B,H,W] --000000	ALMIR[B,H,W] -0000000	-
0x018	-	ALYR[B,H,W] 00000000	ALMOR[B,H,W] ---00000	-
0x01C	WTTR [B,H,W] -------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W] ------00	WTCLKS[B,H,W] -------0
0x024	-	WTCALEN[B,H,W] -------0	WTCAL[B,H,W] ------00 00000000	
0x028	-	-	WTDIVEN[B,H,W] ------00	WTDIV[B,H,W] ----0000
0x02C	-	-	-	WTCALPRD[B,H,W], --010011
0x030	-	-	-	WTCOSEL[B,H,W], -------0
0x034-0x0FF	-	-	-	-

A.1.29 Low-speed CR Prescaler

Low-speed CR Prescaler Base_Address : 0x4003_C000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	LCR_PRSLD[B,H,W], --000000
0x004 – 0x0FC	-	-	-	-

A.1.30 Peripheral Clock Gating

A.1.30.1 TYPE1-M1, TYPE2-M4 products

Peripheral Clock Gating **Base_Address : 0x4003_C100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CKEN0[B,H,W] ---1-1-1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W] -----0-0 ----0000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0x010	CKEN1[B,H,W] -------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W] -------- ----0000 ----0000 ----0000			
0x018 – 0x01F	-	-	-	-
0x020	CKEN2[B,H,W] -------- -------- -------0 --**--00 Products with CAN : *="1" Products without CAN : *="0"			
0x024	MRST2[B,H,W] -------- -------- -------0 --00--00			
0x028 – 0x67C	-	-	-	-

A.1.30.2 TYPE3-M4, TYPE4-M4 products

Peripheral Clock Gating **Base_Address : 0x4003_C100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CKEN0[B,H,W] ---1-1-1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W] -----0-0 ----0000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0x010	CKEN1[B,H,W] -------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W] -------- ----0000 ----0000 ----0000			
0x018 – 0x01F	-	-	-	-
0x020	CKEN2[B,H,W] ---0--11 ---1--00 -------0 -***--00 Products with : *="1" Products without CAN : *="0"			
0x024	MRST2[B,H,W] ---0--00 ---0--00 -------0 -000--00			
0x028 – 0x67C	-	-	-	-

A.1.30.3 TYPE5-M4, TYPE6-M4 products

Peripheral Clock Gating **Base_Address : 0x4003_C100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CKEN0[B,H,W] ---1-1-1 ----1111 11111111 11111111			
0x004	MRST0[B,H,W] -----0-0 ----0000 00000000 00000000			
0x008 – 0x00F	-	-	-	-
0x010	CKEN1[B,H,W] -------- ----1111 ----1111 ----1111			
0x014	MRST1[B,H,W] -------- ----0000 ----0000 ----0000			
0x018 – 0x01F	-	-	-	-
0x020	CKEN2[B,H,W] ---0--11 ---1--00 1111---0 -***--00 Products with : *="1" Products without CAN : *="0"			
0x024	MRST2[B,H,W] ---0--00 ---0--00 0000---0 -000--00			
0x028 – 0x67C	-	-	-	-

A.1.31 Smart Card Interface

Smart Card Interface ch.0 Base_Address : 0x4003_C900

Smart Card Interface ch.1 Base_Address : 0x4003_C980

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	GLOBALCONTROL1[H,W] -0001000 00000000	
0x04	-	-	STATUS[H,W] --000000 00000001	
0x08	-	-	PORTCONTROL[H,W] 0000--00 00-0-0-0	
0x0C	-	-	DATA[H,W] -------0 00000000	
0x10	-	-	CARDCLOCK [H,W] 00000000 00101000	
0x14	-	-	BAUDRATE[H,W] 0000001 01110100	
0x18	-	-	GUARDTIMER[H,W] -------- 00000000	
0x1C	-	-	IDLETIMER[H,W] 00000000 00000000	
0x20	-	-	GLOBALCONTROL2[H,W] -------- ----1-00	
0x24	-	-	DATA_FIFO[H,W] -------0 00000000	
0x28	-	-	FIFO_LEVEL_READ[H,W] 00000000 00000000	
0x2C	-	-	FIFO_LEVEL_WRITE[H,W] 00000000 00000000	
0x30	-	-	FIFO_MODE[H,W] 00000000 ----0000	
0x34	-	-	FIFO_CLEAR_MSB_WRITE[H,W] -------- -------0	
0x38	-	-	FIFO_CLEAR_MSB_ READ[H,W] -------- -------0	
0x3C	-	-	-	-
0x40	-	-	IRQ_STATUS[H,W] -------- 00000000	
0x44- 0x7C	-	-	-	-

A.1.32 MFSI2S

MFSI2S ch.A Base_Address : 0x4003_CA00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x00	-	-	CNTLREG[B, H,W] -----0-0 -0000-01	
0x04	-	-	I2SCLK[B, H,W] 00------ 00000000	
0x08	-	-	I2SST[B,H,W] ------00	I2SRST[B,H,W] 00000000
0x0C- 0xFC	-	-	-	-

Note:

- *In TYPE5-M4 product, MFSI2S ch.A applies to MFS ch.1.*

A.1.33 I2S Prescaler

A.1.33.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 products

I2S_Prescaler Base_Address : 0x4003_D000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ICCR[B,H,W] -------- -------- -------- ------00			
0x004	IPCR1[B,H,W] -------- -------- -------- -------0			
0x008	IPCR2[B,H,W] -------- -------- -------- -----000			
0x00C	IPCR3[B,H,W] -------- -------- -------- ---00001			
0x010	IPCR4[B,H,W] -------- -------- -------- -0011111			
0x014	IP_STR[B,H,W] -------- -------- -------- -------0			
0x018	IPINT_ENR[B,H,W] -------- -------- -------- -------0			
0x01C	IPINT_CLR[B,H,W] -------- -------- -------- -------0			
0x020	IPINT_STR[B,H,W] -------- -------- -------- -------0			
0x024	IPCR5[B,H,W] -------- -------- -------- -0011000			
0x028 – 0xFFC	-	-	-	-

A.1.33.2 TYPE4-M4 product

I2S_Prescaler **Base_Address : 0x4003_D000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ICCR[B,H,W] -------- -------- -------- ------00			
0x004	IPCR1[B,H,W] -------- -------- -------- -------0			
0x008	IPCR2[B,H,W] -------- -------- -------- -----000			
0x00C	IPCR3[B,H,W] -------- -------- -------- ---00001			
0x010	IPCR4[B,H,W] -------- -------- -------- -0011111			
0x014	IP_STR[B,H,W] -------- -------- -------- -------0			
0x018	IPINT_ENR[B,H,W] -------- -------- -------- -------0			
0x01C	IPINT_CLR[B,H,W] -------- -------- -------- -------0			
0x020	IPINT_STR[B,H,W] -------- -------- -------- -------0			
0x024	IPCR5[B,H,W] -------- -------- -------- -0011000			
0x028 – 0x02C	-	-	-	-
0x030	ICCR_1[B,H,W] -------- -------- -------- -----000			
0x034	IPCR5_1[B,H,W] -------- -------- -------- -0000000			
0x038 – 0xFFC	-	-	-	-

A.1.34 GDC_Prescaler

GDC_Prescaler Base_Address : 0x4003_D100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	GCCR[B,H,W] -------- -------- -------- -------0			
0x004	GPCR1[B,H,W] -------- -------- -------- ------00			
0x008	GPCR2[B,H,W] -------- -------- -------- -----000			
0x00C	GPCR3 [B,H,W] -------- -------- -------- ---00000			
0x010	GPCR4 [B,H,W] -------- -------- -------- -0000000			
0x014	GP_STR[B,H,W] -------- -------- -------- -------0			
0x018	GPINT_ENR[B,H,W] -------- -------- -------- -------0			
0x01C	GPINT_CLR[B,H,W] -------- -------- -------- -------0			
0x020	GPINT_STR[B,H,W] -------- -------- -------- -------0			
0x024	-	-	-	-
0x028	GCSR[B,H,W] -------- -------- ---0---0 ---0--00			
0x02C	GRCR[B,H,W] -------- -------- -------- -------0			
0x030	GMCR[B,H,W] -------- -------- -------- -------0			
0x034- 0xFFC	-	-	-	-

Note:

- *For the register details of GDC, refer to the Chapter:GDC.*

A.1.35 EXT-Bus I/F

A.1.35.1 TYPE1-M4 product

EXT-Bus I/F Base_Address : 0x4003_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	MODE0[W] -------- -------- --000-00 00000000			
0x0004	MODE1[W] -------- -------- --000-00 00000000			
0x0008	MODE2[W] -------- -------- --000-00 00000000			
0x000C	MODE3[W] -------- -------- --000-00 00000000			
0x0010	MODE4[W] -------- -------- --000-00 00000001			
0x0014	MODE5[W] -------- -------- --000-00 00000000			
0x0018	MODE6[W] -------- -------- --000-00 00000000			
0x001C	MODE7[W] -------- -------- --000-00 00000000			
0x0020	TIM0[W] 00000101 01011111 11110000 00001111			
0x0024	TIM1[W] 00000101 01011111 11110000 00001111			
0x0028	TIM2[W] 00000101 01011111 11110000 00001111			
0x002C	TIM3[W] 00000101 01011111 11110000 00001111			
0x0030	TIM4[W] 00000101 01011111 11110000 00001111			
0x0034	TIM5[W] 00000101 01011111 11110000 00001111			
0x0038	TIM6[W] 00000101 01011111 11110000 00001111			
0x003C	TIM7[W] 00000101 01011111 11110000 00001111			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0040	AREA0[W] -------- -0001111 -------- 00000000			
0x0044	AREA1[W] -------- -0001111 -------- 00010000			
0x0048	AREA2[W] -------- -0001111 -------- 00100000			
0x004C	AREA3[W] -------- -0001111 -------- 00110000			
0x0050	AREA4[W] -------- -0001111 -------- 01000000			
0x0054	AREA5[W] -------- -0001111 -------- 01010000			
0x0058	AREA6[W] -------- -0001111 -------- 01100000			
0x005C	AREA7[W] -------- -0001111 -------- 01110000			
0x0060	ATIM0[W] -------- -------- ----0100 01011111			
0x0064	ATIM1[W] -------- -------- ----0100 01011111			
0x0068	ATIM2[W] -------- -------- ----0100 01011111			
0x006C	ATIM3[W] -------- -------- ----0100 01011111			
0x0070	ATIM4[W] -------- -------- ----0100 01011111			
0x0074	ATIM5[W] -------- -------- ----0100 01011111			
0x0078	ATIM6[W] -------- -------- ----0100 01011111			
0x007C	ATIM7[W] -------- -------- ----0100 01011111			
0x0080 - 0x00FC	-	-	-	-
0x0100	SDMODE[W] -------- -------0 00010011 --00-000			
0x0104	REFTIM[W] -------0 00000000 0000000000110011			
0x0108	PWRDWN[W] -------- -------- 00000000 00000000			
0x010C	SDTIM[W] ------00 01000010 00010001 0100--01			
0x0110	SDCMD[W] 0------- ---00000 00000000 00000000			
0x0114 - 0x01FC	-	-	-	-

Base_Address + Address	Register			
	+3	+ 2	+1	+ 0
0x0200	MEMCERR[W] -------- -------- -------- ----0000			
0x0204 – 0x02FC	-	-	-	-
0x0300	DCLKR[W] -------- -------- -------- ---01111			
0x0304	EST -------- -------- -------- -------0			
0x0308	WEAD 00000000 00000000 000000000 00000000			
0x030C	ESCLR[W] -------- -------- -------- -------1			
0x0310	AMODE[W] -------- -------- -------- -------1			
0x031C - 0x0EFC	-	-	-	-
0x0F00 – 0x0F14	*	*	*	*
0x0F18 – 0x0FFC	-	-	-	-

A.1.35.2 TYPE3-M4, TYPE4-M4, TYPE5-M4, TYPE6-M4 products

EXT-Bus I/F Base_Address : 0x4003_F000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	MODE0[W] -------- -------- --000-00 00000000			
0x0004	MODE1[W] -------- -------- --000-00 00000000			
0x0008	MODE2[W] -------- -------- --000-00 00000000			
0x000C	MODE3[W] -------- -------- --000-00 00000000			
0x0010	MODE4[W] -------- -------- --000-00 00000001			
0x0014	MODE5[W] -------- -------- --000-00 00000000			
0x0018	MODE6[W] -------- -------- --000-00 00000000			
0x001C	MODE7[W] -------- -------- --000-00 00000000			
0x0020	TIM0[W] 00000101 01011111 11110000 00001111			
0x0024	TIM1[W] 00000101 01011111 11110000 00001111			
0x0028	TIM2[W] 00000101 01011111 11110000 00001111			
0x002C	TIM3[W] 00000101 01011111 11110000 00001111			
0x0030	TIM4[W] 00000101 01011111 11110000 00001111			
0x0034	TIM5[W] 00000101 01011111 11110000 00001111			
0x0038	TIM6[W] 00000101 01011111 11110000 00001111			
0x003C	TIM7[W] 00000101 01011111 11110000 00001111			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0040	AREA0[W] -------- -0001111 -------- 00000000			
0x0044	AREA1[W] -------- -0001111 -------- 00010000			
0x0048	AREA2[W] -------- -0001111 -------- 00100000			
0x004C	AREA3[W] -------- -0001111 -------- 00110000			
0x0050	AREA4[W] -------- -0001111 -------- 01000000			
0x0054	AREA5[W] -------- -0001111 -------- 01010000			
0x0058	AREA6[W] -------- -0001111 -------- 01100000			
0x005C	AREA7[W] -------- -0001111 -------- 01110000			
0x0060	ATIM0[W] -------- -------- ----0100 01011111			
0x0064	ATIM1[W] -------- -------- ----0100 01011111			
0x0068	ATIM2[W] -------- -------- ----0100 01011111			
0x006C	ATIM3[W] -------- -------- ----0100 01011111			
0x0070	ATIM4[W] -------- -------- ----0100 01011111			
0x0074	ATIM5[W] -------- -------- ----0100 01011111			
0x0078	ATIM6[W] -------- -------- ----0100 01011111			
0x007C	ATIM7[W] -------- -------- ----0100 01011111			
0x0080 - 0x00FC	-	-	-	-
0x0100	SDMODE[W] -------- -------0 00010011 --00-000			
0x0104	REFTIM[W] -------0 00000000 0000000000110011			
0x0108	PWRDWN[W] -------- -------- 00000000 00000000			
0x010C	SDTIM[W] 0-----00 01000010 00010001 0100--01			
0x0110	SDCMD[W] 0------- ---00000 00000000 00000000			
0x0114 - 0x01FC	-	-	-	-

Base_Address + Address	Register			
	+3	+ 2	+1	+ 0
0x0200	MEMCERR[W] -------- -------- -------- ----0000			
0x0204 – 0x02FC	-	-	-	-
0x0300	DCLKR[W] -------- -------- -------- ---01111			
0x0304	EST -------- -------- -------- -------0			
0x0308	WEAD 00000000 00000000 000000000 00000000			
0x030C	ESCLR[W] -------- -------- -------- -------1			
0x0310	AMODE[W] -------- -------- -------- -------1			
0x031C - 0x0EFC	-	-	-	-
0x0F00 – 0x0F14	*	*	*	*
0x0F18 – 0x0FFC	-	-	-	-

A.1.36 USB

USB ch.0 Base_Address : 0x4004_0000

USB ch.1 Base_Address : 0x4005_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2100	-	-	HCNT1[B,H,W] -----001	HCNT0[B,H,W] 00000000
0x2104	-	-	HERR[B,H,W] 00000011	HIRQ[B,H,W] 0-000000
0x2108	-	-	HFCOMP[B,H,W] 00000000	HSTATE[B,H,W] --010010
0x210C	-	-	HRTIMER(1/0)[B,H,W] 00000000 00000000	
0x2110	-	-	HADR[B,H,W] -0000000	HRTIMER(2)[B,H,W] ------00
0x2114	-	-	HEOF(1/0)[B,H,W] --000000 00000000	
0x2118	-	-	HFRAME(1/0)[B,H,W] -----000 00000000	
0x211C	-	-	-	HTOKEN[B,H,W] 00000000
0x2120	-	-	UDCC[B,H,W] -------- 10100-00	
0x2124	-	-	EP0C[H,W] ------0- -1000000	
0x2128	-	-	EP1C[H,W] 01100001 00000000	
0x212C	-	-	EP2C[H,W] 0110000- -1000000	
0x2130	-	-	EP3C[H,W] 0110000- -1000000	
0x2134	-	-	EP4C[H,W] 0110000- -1000000	
0x2138	-	-	EP5C[H,W] 0110000- -1000000	
0x213C	-	-	TMSP[H,W] -----000 00000000	
0x2140	-	-	UDCIE[B,H,W] --000000	UDCS[B,H,W] --000000
0x2144	-	-	EP0IS[H,W] 10---1-- --------	
0x2148	-	-	EP0OS[H,W] 100--00- -XXXXXXX	
0x214C	-	-	EP1S[H,W] 100-000X XXXXXXXX	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x2150	-	-	EP2S[H,W] 100-000- -XXXXXXX	
0x2154	-	-	EP3S[H,W] 100-000- -XXXXXXX	
0x2158	-	-	EP4S[H,W] 100-000- -XXXXXXX	
0x215C	-	-	EP5S[H,W] 100-000- -XXXXXXX	
0x2160	-	-	EP0DTH[B,H,W] XXXXXXXX	EP0DTL[B,H,W] XXXXXXXX
0x2164	-	-	EP1DTH[B,H,W] XXXXXXXX	EP1DTL[B,H,W] XXXXXXXX
0x2168	-	-	EP2DTH[B,H,W] XXXXXXXX	EP2DTL[B,H,W] XXXXXXXX
0x216C	-	-	EP3DTH[B,H,W] XXXXXXXX	EP3DTL[B,H,W] XXXXXXXX
0x2170	-	-	EP4DTH[B,H,W] XXXXXXXX	EP4DTL[B,H,W] XXXXXXXX
0x2174	-	-	EP5DTH[B,H,W] XXXXXXXX	EP5DTL[B,H,W] XXXXXXXX
0x2178 - 0x217C	-	-	-	-

A.1.37 DMAC

DMAC **Base_Address : 0x4006_0000**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	DMACR[B,H,W] 00-00000 -------- -------- --------			
0x0010	DMACA0[B,H,W] 00000000 0---0000 00000000 00000000			
0x0014	DMACB0[B,H,W] --000000 00000000 00000000 -------0			
0x0018	DMACSA0[B,H,W] 00000000 00000000 00000000 00000000			
0x001C	DMACDA0[B,H,W] 00000000 00000000 00000000 00000000			
0x0020	DMACA1[B,H,W] 00000000 0---0000 00000000 00000000			
0x0024	DMACB1[B,H,W] --000000 00000000 00000000 -------0			
0x0028	DMACSA1[B,H,W] 00000000 00000000 00000000 00000000			
0x002C	DMACDA1[B,H,W] 00000000 00000000 00000000 00000000			
0x0030	DMACA2[B,H,W] 00000000 0---0000 00000000 00000000			
0x0034	DMACB2[B,H,W] --000000 00000000 00000000 -------0			
0x0038	DMACSA2[B,H,W] 00000000 00000000 00000000 00000000			
0x003C	DMACDA2[B,H,W] 00000000 00000000 00000000 00000000			
0x0040	DMACA3[B,H,W] 00000000 0---0000 00000000 00000000			
0x0044	DMACB3[B,H,W] --000000 00000000 00000000 -------0			
0x0048	DMACSA3[B,H,W] 00000000 00000000 00000000 00000000			
0x004C	DMACDA3[B,H,W] 00000000 00000000 00000000 00000000			
0x0050	DMACA4[B,H,W] 00000000 0---0000 00000000 00000000			
0x0054	DMACB4[B,H,W] --000000 00000000 00000000 -------0			
0x0058	DMACSA4[B,H,W] 00000000 00000000 00000000 00000000			
0x005C	DMACDA4[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0060	DMACA5[B,H,W] 00000000 0---0000 00000000 00000000			
0x0064	DMACB5[B,H,W] --000000 00000000 00000000 -------0			
0x0068	DMACSA5[B,H,W] 00000000 00000000 00000000 00000000			
0x006C	DMACDA5[B,H,W] 00000000 00000000 00000000 00000000			
0x0070	DMACA6[B,H,W] 00000000 0---0000 00000000 00000000			
0x0074	DMACB6[B,H,W] --000000 00000000 00000000 -------0			
0x0078	DMACSA6[B,H,W] 00000000 00000000 00000000 00000000			
0x007C	DMACDA6[B,H,W] 00000000 00000000 00000000 00000000			
0x0080	DMACA7[B,H,W] 00000000 0---0000 00000000 00000000			
0x0084	DMACB7[B,H,W] --000000 00000000 00000000 -------0			
0x0088	DMACSA7[B,H,W] 00000000 00000000 00000000 00000000			
0x008C	DMACDA7[B,H,W] 00000000 00000000 00000000 00000000			
0x0090 - 0x00FC	-	-	-	-

A.1.38 DSTC

DSTC Base_Address : 0x4006_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	DESTP[B,H,W] 00000000 00000000 00000000 00000000			
0x0004	HWDESP[B,H,W] 00XXXXXX XXXXXX00 00000000 00000000			
0x0008	SWTR[H] 00000000 00000000		CFG[B] 01000000	CMD[B] 00000001
0x000C	MONERS[B,H,W] 00XXXXXX XXXXXX00 XXXXXXXX XXX00000			
0x0010	DREQENB[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x0014	DREQENB[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x0018	DREQENB[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x001C	DREQENB[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x0020	DREQENB[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x0024	DREQENB[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x0028	DREQENB[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x002C	DREQENB[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x0030	HWINT[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x0034	HWINT[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x0038	HWINT[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x003C	HWINT[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x0040	HWINT[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x0044	HWINT[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x0048	HWINT[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x004C	HWINT[255:224] [B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0050	HWINTCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x0054	HWINTCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x0058	HWINTCLR[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x005C	HWINTCLR[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x060	HWINTCLR[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x064	HWINTCLR[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x068	HWINTCLR[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x06C	HWINTCLR[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x070	DQMSK[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x074	DQMSK[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x078	DQMSK[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x07C	DQMSK[127:96] [B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x080	DQMSK[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x084	DQMSK[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x088	DQMSK[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x08C	DQMSK[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x090	DQMSKCLR[31:0] [B,H,W] 00000000 00000000 00000000 00000000			
0x094	DQMSKCLR[63:32] [B,H,W] 00000000 00000000 00000000 00000000			
0x098	DQMSKCLR[95:64] [B,H,W] 00000000 00000000 00000000 00000000			
0x09C	DQMSKCLR[127:96] [B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	DQMSKCLR[159:128] [B,H,W] 00000000 00000000 00000000 00000000			
0x0A4	DQMSKCLR[191:160] [B,H,W] 00000000 00000000 00000000 00000000			
0x0A8	DQMSKCLR[223:192] [B,H,W] 00000000 00000000 00000000 00000000			
0x0AC	DQMSKCLR[255:224] [B,H,W] 00000000 00000000 00000000 00000000			
0x00B0 - 0x0FFC	-	-	-	-

A.1.39 CAN

CAN ch.0 Base_Address : 0x4006_2000

CAN ch.1 Base_Address : 0x4006_3000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	STATR[B,H,W] -------- 00000000		CTRLR[B,H,W] -------- 000-0001	
0x0004	BTR[B,H,W] -0100011 00000001		ERRCNT[B,H,W] 00000000 00000000	
0x0008	TESTR[B,H,W] -------- X00000--		INTR[B,H,W] 00000000 00000000	
0x000C	-	-	BRPER[B,H,W] -------- ----0000	
0x0010	IF1CMSK[B,H,W] -------- 00000000		IF1CREQ[B,H,W] 0------- 00000001	
0x0014	IF1MSK2[B,H,W] 11-11111 11111111		IF1MSK1[B,H,W] 11111111 11111111	
0x0018	IF1ARB2[B,H,W] 00000000 00000000		IF1ARB1[B,H,W] 00000000 00000000	
0x001C	-	-	IF1MCTR[B,H,W] 00000000 0---0000	
0x0020	IF1DTA2[B,H,W] 00000000 00000000		IF1DTA1[B,H,W] 00000000 00000000	
0x0024	IF1DTB2[B,H,W] 00000000 00000000		IF1DTB1[B,H,W] 00000000 00000000	
0x0028 - 0x002F	-	-	-	-
0x0030	IF1DTA1[B,H,W] 00000000 00000000		IF1DTA2[B,H,W] 00000000 00000000	
0x0034	IF1DTB1[B,H,W] 00000000 00000000		IF1DTB2[B,H,W] 00000000 00000000	
0x0038 - 0x003C	-	-	-	-
0x0040	IF2CMSK[B,H,W] -------- 00000000		IF2CREQ[B,H,W] 0------- 00000001	
0x0044	IF2MSK2[B,H,W] 11-11111 11111111		IF2MSK1[B,H,W] 11111111 11111111	
0x0048	IF2ARB2[B,H,W] 00000000 00000000		IF2ARB1[B,H,W] 00000000 00000000	
0x004C	-	-	IF2MCTR[B,H,W] 00000000 0---0000	
0x0050	IF2DTA2[B,H,W] 00000000 00000000		IF2DTA1[B,H,W] 00000000 00000000	
0x0054	IF2DTB2[B,H,W] 00000000 00000000		IF2DTB1[B,H,W] 00000000 00000000	
0x0058 - 0x005C	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0060	IF2DTA1[B,H,W] 00000000 00000000		IF2DTA2[B,H,W] 00000000 00000000	
0x0064	IF2DTB1[B,H,W] 00000000 00000000		IF2DTB2[B,H,W] 00000000 00000000	
0x0068 - 0x007C	-	-	-	-
0x0080	TREQR2[B,H,W] 00000000 00000000		TREQR1[B,H,W] 00000000 00000000	
0x0084 - 0x008F	-	-	-	-
0x0090	NEWDT2[B,H,W] 00000000 00000000		NEWDT1[B,H,W] 00000000 00000000	
0x0094 - 0x009F	-	-	-	-
0x00A0	INTPND2[B,H,W] 00000000 00000000		INTPND1[B,H,W] 00000000 00000000	
0x00A4 - 0x00AF	-	-	-	-
0x00B0	MSGVAL2[B,H,W] 00000000 00000000		MSGVAL1[B,H,W] 00000000 00000000	
0x00B4 - 0x0FFC	-	-	-	-

A.1.40 Ethernet-MAC

Ethernet-MAC Base_Address : 0x4006_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000 – 0x1FFC	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Note:

- *For the register details of Ethernet-MAC block, refer to the "Ethernet part".*

A.1.41 Ethernet-Control

Ethernet-Control Base_Address : 0x4006_6000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 - 0xFFC	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Note:

- *For the register details of Ethernet-Control block, refer to the Ethernet part.*

A.1.42 I2S

I2S ch.0 Base_Address : 0x4006_C000

I2S ch.1 Base_Address : 0x4006_C800

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	RXFDAT[B,H,W] 00000000 00000000 00000000 00000000			
0x004	TXFDAT[B,H,W] 00000000 00000000 00000000 00000000			
0x008	CNTREG[B,H,W] 00000000 00000000 00000000 00000000			
0x00C	MCR0REG[B,H,W] -0000000 00000000 -0000000 00000000			
0x010	MCR1REG[B,H,W] 00000000 00000000 00000000 00000000			
0x014	MCR2REG[B,H,W] 00000000 00000000 00000000 00000000			
0x018	OPRREG[B,H,W] -------0 -------0 -------- -------0			
0x01C	SRST[B,H,W] -------- -------- -------- -------0			
0x020	INTCNT[B,H,W] -1111111 --111111 ----0000 --000000			
0x024	STATUS[B,H,W] 00000000 ----0000 00000000 00000000			
0x028	DMAACT[B,H,W] -------0 -------0 -------0 -------0			
0x02C	TSTREG[B,H,W] -------- -------- -------- -------0			
0x030 - 0xFFC	-	-	-	-

A.1.43 SD-Card

SD-Card Base_Address : 0x4006_E000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 – 0xFFC	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Note:

- *For the register details of SD-Card block, refer to the Chapter SD Card Interface.*

A.1.44 CAN FD

CAN FD Base_Address : 0x4007_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CREL[B,H,W] 00110000 00010011 00000101 0000110			
0x004	ENDN[B,H,W] 10000111 01100101 01000011 00100001			
0x008	-	-	-	-
0x00C	FBTP[B,H,W] ---00000 0--00000 ----1010 -011--11			
0x010	TEST[B,H,W] -------- -------- --000000 X000----			
0x014	RWD[B,H,W] -------- -------- 00000000 00000000			
0x018	CCCR[B,H,W] -------- -------- -0000000 00000001			
0x01C	BTP[B,H,W] ------00 00000000 --001010 00110011			
0x020	TSCC[B,H,W] -------- ----0000 -------- ------00			
0x024	TSCV[B,H,W] -------- -------- 00000000 00000000			
0x028	TOCC[B,H,W] 11111111 11111111 -------- -----000			
0x02C	TOCV[B,H,W] -------- -------- 11111111 11111111			
0x030 - 0x03C	-	-	-	-
0x040	ECR[B,H,W] -------- 00000000 00000000 00000000			
0x044	PSR[B,H,W] -------- -------- --000111 00000111			
0x048 - 0x04C	-	-	-	-
0x050	IR[B,H,W] 00000000 00000000 00000000 00000000			
0x054	IE[B,H,W] 00000000 00000000 00000000 00000000			
0x058	ILS[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	ILE[B,H,W] -------- -------- -------- ------00			
0x060 - 0x07C	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x080	GFC[B,H,W] -------- -------- -------- --000000			
0x084	SIDFC[B,H,W] -------- 00000000 00000000 000000--			
0x088	XIDFC[B,H,W] -------- -0000000 00000000 000000--			
0x08C	-	-	-	-
0x090	XIDAM[B,H,W] ---11111 11111111 11111111 11111111			
0x094	HPMS[B,H,W] -------- -------- 00000000 00000000			
0x098	NDAT1[B,H,W] 00000000 00000000 00000000 00000000			
0x09C	NDAT2[B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	RXF0C[B,H,W] 00000000 -0000000 00000000 000000--			
0x0A4	RXF0S[B,H,W] ------00 --000000 --000000 -0000000			
0x0A8	RXF0A[B,H,W] -------- -------- -------- --000000			
0x0AC	RXBC[B,H,W] -------- -------- 00000000 000000--			
0x0B0	RXF1C[B,H,W] 00000000 -0000000 00000000 000000--			
0x0B4	RXF1S[B,H,W] 00----00 --000000 --000000 -0000000			
0x0B8	RXF1A[B,H,W] -------- -------- -------- --000000			
0x0BC	RXESC[B,H,W] -------- -------- -----000 -000-000			
0x0C0	TXBC[B,H,W] -0000000 --000000 00000000 000000--			
0x0C4	TXFQS[B,H,W] -------- --000000 ---00000 –000000			
0x0C8	TXESC[B,H,W] -------- -------- -------- -----000			
0x0CC	TXBRP[B,H,W] 00000000 00000000 00000000 00000000			
0x0D0	TXBAR[B,H,W] 00000000 00000000 00000000 00000000			
0x0D4	TXBCR[B,H,W] 00000000 00000000 00000000 00000000			
0x0D8	TXBTO[B,H,W] 00000000 00000000 00000000 00000000			
0x0DC	TXBCF[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0E0	TXBTIE[B,H,W] 00000000 00000000 00000000 00000000			
0x0E4	TXBCIE[B,H,W] 00000000 00000000 00000000 00000000			
0x0E8 - 0x0EC	-	-	-	-
0x0F0	TXEFC[B,H,W] --000000 --000000 00000000 000000--			
0x0F4	TXEFS[B,H,W] ------00 ---00000 ---00000 --000000			
0x0F8	TXEFA[B,H,W] -------- -------- -------- ---00000			
0x0FC - 0x1FC	-	-	-	-
0x200	FDSEAR[B,H,W] 00000000 00000000		FDESR[B,H,W] ------00	FDECR[B,H,W] ----0000
0x204	FDDEAR[B,H,W] 00000000 00000000		FDESCR[B,H,W] ------00	-
0x208	FDFECR[B,H,W] 0------- -----000 00000000 00000000			
0x20C	-	-	-	-
0x210	TSMDR[B,H,W] -------- -------0		TSCNTR[B,H,W] -------- -------0	
0x214	TSDIVR[B,H,W] -------- -------- 00000000 00000000			
0x218	TSCPCLR[B,H,W] 00000000 00000000		TSCDTR[B,H,W] 00000000 00000000	
0x21C - 0xFFC	-	-	-	-

CAN FD Message RAM

Base_Address + Address	Message RAM			
	+3	+2	+1	+0
0x8000 - 0xBFFC	Rx Buffer and FIFO Element [W] Tx Buffer Element [W] Tx Event FIFO Element [W] Standard Message ID Filter Element [W] Extended Message ID Filter Element [W]			

Note:

- *For the register details of CAN FD Message RAM block, refer to the Chapter CAN FD Controller.*

A.1.45 Programmable-CRC

Programmable-CRC Base_Address : 0x4008_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CRCn_PORY[B,H,W] 00000100 11000001 00011101 10110111			
0x004	CRCn_SEED[B,H,W] 11111111 11111111 11111111 11111111			
0x008	CRCn_FXOR[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	CRCn_CFG[B,H,W] 00000000 11100000 00000000 00000000			
0x010	CRCn_WR[B,H,W] 00000000 00000000 00000000 00000000			
0x014	CRCn_RD[B,H,W] 00000000 00000000 00000000 00000000			
0x018 - 0xFFC	-	-	-	-

A.1.46 WorkFlash_IF

WorkFlash_IF Base_Address : 0x200E_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WFASZR[B,H,W]			
0x004	WFRWTR[B,H,W]			
0x008	WFSTR[B,H,W]			
0x00C - 0xFFF	-	-	-	-

Note:

- *For the register details of Workflash IF block, refer to the Flash Programming Manual of the product used.*

A.1.47 High-Speed Quad SPI Controller

A.1.47.1 TYPE1-M4, TYPE2-M4, TYPE3-M4 products

High-Speed Quad SPI Controller Base_Address : 0xD000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	HSSPIn_MCTRL[B,H,W] -------- -------- -------- --000-00			
0x004	HSSPIn_PCC0[B,H,W] -------- -1111111 00000000 00000000			
0x008	HSSPIn_PCC1[B,H,W] -------- -1111111 00000000 00000000			
0x00C	HSSPIn_PCC2[B,H,W] -------- -1111111 00000000 00000000			
0x010	HSSPIn_PCC3[B,H,W] -------- -1111111 00000000 00000000			
0x014	HSSPIn_TXF[B,H,W] -------- -------- -------- -0000000			
0x018	HSSPIn_TXE[B,H,W] -------- -------- -------- -0000000			
0x01C	HSSPIn_TXC[B,H,W] -------- -------- -------- -0000000			
0x020	HSSPIn_RXF[B,H,W] -------- -------- -------- -0000000			
0x024	HSSPIn_RXE[B,H,W] -------- -------- -------- -0000000			
0x028	HSSPIn_RXC[B,H,W] -------- -------- -------- -0000000			
0x02C	HSSPIn_FAULTF[B,H,W] -------- -------- -------- ---00000			
0x030	HSSPIn_FAULTC[B,H,W] -------- -------- -------- ---00000			
0x034	-	-	HSSPIn_DMDMAEN [B,H,W] ------00	HSSPIn_DMCFG [B,H,W] -----001
0x038	HSSPIn_DMTRP [B,H,W] ----0000	HSSPIn_DMPSEL [B,H,W] ------00	HSSPIn_DMSTOP [B,H,W] -------0	HSSPIn_DMSTART [B,H,W] -------0
0x03C	HSSPIn_DMBCS[B,H,W] 00000000 00000000		HSSPIn_DMBCC[B,H,W] 00000000 00000000	
0x040	HSSPIn_DMSTATUS[B,H,W] -------- ---00000 ---00000 ------00			
0x044	-	-	-	-
0x048	-	-	-	-
0x04C	HSSPIn_FIFOCFG[B,H,W] --------_--------_---00000_01110111			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	HSSPIn_TXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x054	HSSPIn_TXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x058	HSSPIn_TXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	HSSPIn_TXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x060	HSSPIn_TXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x064	HSSPIn_TXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x068	HSSPIn_TXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x06C	HSSPIn_TXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x070	HSSPIn_TXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			
0x074	HSSPIn_TXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x078	HSSPIn_TXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x07C	HSSPIn_TXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x080	HSSPIn_TXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x084	HSSPIn_TXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x088	HSSPIn_TXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x08C	HSSPIn_TXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x090	HSSPIn_RXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x094	HSSPIn_RXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x098	HSSPIn_RXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x09C	HSSPIn_RXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0A0	HSSPIn_RXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x0A4	HSSPIn_RXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x0A8	HSSPIn_RXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x0AC	HSSPIn_RXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x0B0	HSSPIn_RXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			
0x0B4	HSSPIn_RXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x0B8	HSSPIn_RXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x0BC	HSSPIn_RXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x0C0	HSSPIn_RXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x0C4	HSSPIn_RXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x0C8	HSSPIn_RXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x0CC	HSSPIn_RXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x0D0	HSSPIn_CSCFG[B,H,W] -------- ----0000 ----0000 --000000			
0x0D4	HSSPIn_CSITIME[B,H,W] -------- -------- 11111111 11111111			
0x0D8	HSSPIn_CSAEXT[B,H,W] 00000000 00000000 000----- --------			
0x0DC	HSSPIn_RDCSDC1[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC0[B,H,W] 00000000 ----0000	
0x0E0	HSSPIn_RDCSDC3[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC2[B,H,W] 00000000 ----0000	
0x0E4	HSSPIn_RDCSDC5[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC4[B,H,W] 00000000 ----0000	
0x0E8	HSSPIn_RDCSDC7[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC6[B,H,W] 00000000 ----0000	
0x0EC	HSSPIn_WRCSDC1[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC0[B,H,W] 00000000 ----0000	
0x0F0	HSSPIn_WRCSDC3[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC2[B,H,W] 00000000 ----0000	
0x0F4	HSSPIn_WRCSDC5[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC4[B,H,W] 00000000 ----0000	
0x0F8	HSSPIn_WRCSDC7[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC6[B,H,W] 00000000 ----0000	
0x0FC	HSSPIn_MID[B,H,W] 00000000 00000000 00000110 00110000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x100 - 0x3FC	-	-	-	-
0x400	-	-	-	QDCLKR[B,H,W] ----1111
0x404	-	-	-	DBCNT[B,H,W] ------00
0x408 - 0xFFC	-	-	-	-

A.1.47.2 TYPE4-M4 Product

High-Speed Quad SPI Controller Base_Address : 0xD0A0_4000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	HSSPIn_MCTRL[B,H,W] -------- -------- -------- --000-00			
0x004	HSSPIn_PCC0[B,H,W] -------- -1111111 00000000 00000000			
0x008	HSSPIn_PCC1[B,H,W] -------- -1111111 00000000 00000000			
0x00C	HSSPIn_PCC2[B,H,W] -------- -1111111 00000000 00000000			
0x010	HSSPIn_PCC3[B,H,W] -------- -1111111 00000000 00000000			
0x014	HSSPIn_TXF[B,H,W] -------- -------- -------- -0000000			
0x018	HSSPIn_TXE[B,H,W] -------- -------- -------- -0000000			
0x01C	HSSPIn_TXC[B,H,W] -------- -------- -------- -0000000			
0x020	HSSPIn_RXF[B,H,W] -------- -------- -------- -0000000			
0x024	HSSPIn_RXE[B,H,W] -------- -------- -------- -0000000			
0x028	HSSPIn_RXC[B,H,W] -------- -------- -------- -0000000			
0x02C	HSSPIn_FAULTF[B,H,W] -------- -------- -------- ---00000			
0x030	HSSPIn_FAULTC[B,H,W] -------- -------- -------- ---00000			
0x034	-	-	HSSPIn_DMDMAEN [B,H,W] ------00	HSSPIn_DMCFG [B,H,W] -----001
0x038	HSSPIn_DMTRP [B,H,W] ----0000	HSSPIn_DMPSEL [B,H,W] ------00	HSSPIn_DMSTOP [B,H,W] -------0	HSSPIn_DMSTART [B,H,W] -------0
0x03C	HSSPIn_DMBCS[B,H,W] 00000000 00000000		HSSPIn_DMBCC[B,H,W] 00000000 00000000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x040	HSSPIn_DMSTATUS[B,H,W] -------- ---00000 ---00000 ------00			
0x044	-	-	-	-
0x048	-	-	-	-
0x04C	HSSPIn_FIFOCFG[B,H,W] --------_--------_---00000_01110111			
0x050	HSSPIn_TXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x054	HSSPIn_TXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x058	HSSPIn_TXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x05C	HSSPIn_TXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x060	HSSPIn_TXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x064	HSSPIn_TXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x068	HSSPIn_TXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x06C	HSSPIn_TXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x070	HSSPIn_TXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			
0x074	HSSPIn_TXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x078	HSSPIn_TXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x07C	HSSPIn_TXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x080	HSSPIn_TXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x084	HSSPIn_TXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x088	HSSPIn_TXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x08C	HSSPIn_TXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x090	HSSPIn_RXFIFO0[B,H,W] 00000000 00000000 00000000 00000000			
0x094	HSSPIn_RXFIFO1[B,H,W] 00000000 00000000 00000000 00000000			
0x098	HSSPIn_RXFIFO2[B,H,W] 00000000 00000000 00000000 00000000			
0x09C	HSSPIn_RXFIFO3[B,H,W] 00000000 00000000 00000000 00000000			
0x0A0	HSSPIn_RXFIFO4[B,H,W] 00000000 00000000 00000000 00000000			
0x0A4	HSSPIn_RXFIFO5[B,H,W] 00000000 00000000 00000000 00000000			
0x0A8	HSSPIn_RXFIFO6[B,H,W] 00000000 00000000 00000000 00000000			
0x0AC	HSSPIn_RXFIFO7[B,H,W] 00000000 00000000 00000000 00000000			
0x0B0	HSSPIn_RXFIFO8[B,H,W] 00000000 00000000 00000000 00000000			
0x0B4	HSSPIn_RXFIFO9[B,H,W] 00000000 00000000 00000000 00000000			
0x0B8	HSSPIn_RXFIFO10[B,H,W] 00000000 00000000 00000000 00000000			
0x0BC	HSSPIn_RXFIFO11[B,H,W] 00000000 00000000 00000000 00000000			
0x0C0	HSSPIn_RXFIFO12[B,H,W] 00000000 00000000 00000000 00000000			
0x0C4	HSSPIn_RXFIFO13[B,H,W] 00000000 00000000 00000000 00000000			
0x0C8	HSSPIn_RXFIFO14[B,H,W] 00000000 00000000 00000000 00000000			
0x0CC	HSSPIn_RXFIFO15[B,H,W] 00000000 00000000 00000000 00000000			
0x0D0	HSSPIn_CSCFG[B,H,W] -------- ----0000 ----0000 --000000			
0x0D4	HSSPIn_CSITIME[B,H,W] -------- -------- 11111111 11111111			
0x0D8	HSSPIn_CSAEXT[B,H,W] 00000000 00000000 000----- --------			
0x0DC	HSSPIn_RDCSDC1[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC0[B,H,W] 00000000 ----0000	
0x0E0	HSSPIn_RDCSDC3[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC2[B,H,W] 00000000 ----0000	
0x0E4	HSSPIn_RDCSDC5[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC4[B,H,W] 00000000 ----0000	
0x0E8	HSSPIn_RDCSDC7[B,H,W] 00000000 ----0000		HSSPIn_RDCSDC6[B,H,W] 00000000 ----0000	
0x0EC	HSSPIn_WRCSDC1[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC0[B,H,W] 00000000 ----0000	

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0F0	HSSPIn_WRCSDC3[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC2[B,H,W] 00000000 ----0000	
0x0F4	HSSPIn_WRCSDC5[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC4[B,H,W] 00000000 ----0000	
0x0F8	HSSPIn_WRCSDC7[B,H,W] 00000000 ----0000		HSSPIn_WRCSDC6[B,H,W] 00000000 ----0000	
0x0FC	HSSPIn_MID[B,H,W] 00000000 00000000 00000110 00110000			
0x100 - 0x3FC	-	-	-	-
0x400	-	-	-	QDCLKR[B,H,W] ----1111
0x404	-	-	-	DBCNT[B,H,W] ------00
0x408 - 0xFFC	-	-	-	-

A.1.48 HyperBus Interface

HyperBus Interface Base_Address : 0xD0A0_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	CSR[B,H,W] -----000 -------0 ----0000 -------0			
0x004	IEN[B,H,W] 0------- -------- -------- -------0			
0x008	ISR[B,H,W] -------- -------- -------- -------0			
0x024	-	-	-	-
0x010	MBR0[B,H,W] 00000000 00000000 00000000 00000000			
0x014	MBR1[B,H,W] 00000000 00000000 00000000 00000000			
0x018	MCR0[B,H,W] -------- ------00 -------- --00--11			
0x01C	MCR1[B,H,W] -------- ------00 -------- --00--11			
0x020	MTR0[B,H,W] 00000000 00000000 00000000 ----0000			
0x024	MTR1[B,H,W] 00000000 00000000 00000000 ----0000			
0x028	GPOR[B,H,W] -------- -------- -------- ------00			
0x02C	WPR[B,H,W] -------- -------- -------- -------0			
0x030	TEST[B,H,W] -------- -------- -------- -------0			
0x034- 0xFFC	-	-	-	-

A.1.49 GDC Sub System Controller

GDC Sub System Controller Base_Address : 0xD0A0_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	LockUnlock[W] 00000000 00000000 00000000 00000000			
0x004	LockStatus[W] -------- -------- -------0 ---0---0			
0x008	*[W]			
0x00C	CnfigClockControl[W] -------- -------- -------- -----001			
0x010	VramInterruptEnable[W] -------- -------- -------- ------11			
0x014	*[W]			
0x018	VramInterruptClear[W] -------- -------- -------- ------00			
0x01C	VramInterruptStatus[W] -------- -------- -------- ------00			
0x020	ExtFlashDevSelect[W] -------- -------- -------- -------1			
0x024	VramRemapDisable[W] -------- -------- -------- -------0			
0x028	PanicSwitch[W] -------- -------- -------- -------1			
0x02C	GDC_ClockDivider[W] -------- -----100 00000000 --------			
0x030	WkupTriggerMask[W] -----000 -----000 00000000 00000000			
0x034	ClockDomainStatus[W] -------- -------- -------- ----0000			
0x038	-			
0x03C	-			
0x040	dsp_LockUnlock[W] 00000000 00000000 00000000 00000000			
0x044	dsp_LockStatus[W] -------- -------- -------0 ---0---0			
0x048	dsp0_ClockDivider[W] -------- 01000001 11100000 --------			
0x04C	dsp0_DomainControl[W] -------- -------1 -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x050	dsp0_ClockShift[W] -------- -------- -------- -------1			
0x054	*[W]			
0x058	dsp0_PowerEnControl[W] -------- -------- -------- -------0			
0x05C	dsp0_ClockGateModeLock[W] 00000000 00000000 00000000 00000000			
0x060	dsp0_ClockGateControl[W] -------- -------- -------- -------0			
0x064	-			
0x068	-			
0x06C	-			
0x070	-			
0x074	-			
0x078	SDRAMC_ClcokDivider[W] -------- 00000100 00000000 --------			
0x07C	SDRAMC_DomainControl[W] -------- -------1 -------- -------0			
0x080	HSSPIC_ClockDivider[W] -------- 00000100 00000000 --------			
0x084	HSSPIC_DomainControl[W] -------- -------1 -------- -------0			
0x088	RPCC_ClcokDivider[W] -------- -------- -------- -----000			
0x08C	RPCC_DomainControl[W] -------- -------1 -------- -------0			
0x090	-			
0x094	-			
0x098	-			
0x09C	-			
0x100	vram_LockUnlock[W] 00000000 00000000 00000000 00000000			
0x104	vram_LockStatus[W] -------- -------- -------0 ---0---0			
0x108	vram_sram_select[W] -------- -------- ----0000 00000000			
0x10C	*[W]			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x110	*[W]			
0x114	*[W]			
0x118	*[W]			
0x11C	*[W]			
0x120	*[W]			
0x124	*[W]			
0x128	*[W]			
0x12C	-			
0x130	-			
0x134	-			
0x138	-			
0x13C	vram_sberraddr_s0[W] 00000000 00000000 0000000 00000000			
0x140	vram_sberraddr_s1[W] 00000000 00000000 0000000 00000000			
0x144	-			
0x148	vram_arbiter_priority[W] -------- -------- -------- 00000000			
0x14C-0xFFC	-			

A.1.50 GDC Sub System SDRAM Controller

GDC Sub System SDRAM Controller Base_Address : 0xD0A0_3000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000-0x0FF	-			
0x100	SDMODE[W] -------- -------0 00010011 --00-000			
0x104	REFTIM[W] -------0 00000000 0000000000110011			
0x108	PWRDWN[W] -------- -------- 00000000 00000000			
0x10C	SDTIM[W] 0-----00 01000010 00010001 0100--01			
0x110	SDCMD[W] 0------- ---00000 00000000 00000000			
0x114-0xFFC	-			

B. List of Notes

This section explains notes for each function.

B.1 Notes When High-speed CR is Used for the Master Clock

This section explains notes when the high-speed CR is used for the master clock.

The frequency of the high-speed CR varies depending on the temperature and/or the power supply voltage.
The following table shows notes on each function macro when the high-speed CR is used for the master clock.

Furthermore, pay attention to notes when the high-speed CR is used as an input clock of the PLL and the master clock is selected for PLL.

■ Notes on Each Macro

Macro	Function/mode	Notes
Internal Bus Clock	HCLK/FCLK/PCLK0/ PCLK1/PCLK2/ TPIUCLK	When the frequency of the high-speed CR is the maximum value, the setting of the internal operating clock frequency shall not exceed the upper limit specified in the "data sheet" for the product that you are using.
Timer	Multi-function Timer Base Timer Watch Timer Dual Timer Watch Dog Timer Quadrature	The frequency variation of the high-speed CR should be considered for the timer count value of each macro.
A/D Converter	Sampling Time Compare Time	Considering the frequency variation of the high-speed CR, the sampling time and the compare time of the A/D converter shall satisfy the specification specified in the "data sheet" for the product that you are using.
USB	-	As the frequency accuracy does not meet the required specification, these macros cannot be used when the high-speed CR is used for the master clock.
Ethernet-MAC		
CAN		
CAN-FD		
I^2S		
Multi-Function Serial Interface	UART	Even if the frequency of the high-speed CR is the minimum or the maximum value, the baud rate error should be considered. The baud rate error shall not exceed the limit.
	CSIO	The frequency variation of the high-speed CR should be considered for the communication of each macro.
	I^2C	
	LIN	As the required frequency accuracy cannot be met, this function cannot be used as master. As a slave, the specified baud rate has more error at the maximum/minimum frequency of high-speed clock. So, if the error limit of the baud rate is exceeded, this function cannot be used.
Debug Interface	Serial Wire	As the frequency variation of the high-speed CR, the SWV(Serial Wire View) may not be used.
External Bus Interface	Clock Output	When the external bus clock output is used, the frequency variation of the high-speed CR should be considered for devices to be connected.
Hi-Speed Quad SPI	-	The frequency variation of the high-speed CR should be considered for devices to be connected.
SD card Interface	-	The frequency variation of the high-speed CR should be considered for devices to be connected.
GDC	Panel Output High-Speed Quad SPI HyperBus Interface SDRAM Interface	The frequency variation of the high-speed CR should be considered for devices to be connected.

C. Major Changes

Spansion Publication Number: MN709-00014

Page	Section	Changes
Revision 1.0		
-	-	Initial release

NOTE: Please see “Revision History” about later revised information.

Revision History

Document Revision History

Document Title:	32-Bit Microcontroller FM4 Family Peripheral Manual GDC Part
Document Number:	002-04917

Revision	ECN No.	Origin of Change	Description of Change
**	-	TOYO	Migrated to Cypress and assigned document number 002-04917. No change to document contents or format.
*A	5318667	NOSU	Update to Cyress template. Appendixes - A. Register Map - 1. Rejister Map − Changed "Software-based Simulation Startup(Base Timer)" to "Software-based Simultaneous Startup(Base Timer)" in 1.11 IO Selector for Base Timer. (Page 136) − Changed SCFD bit12 initial values "X" to "1" in 1.14 A/DC. (Page 140) − Changed PCFD bit12 initial values "X" to "1" in 1.14 A/DC. (Page 140) − Changed LVD_STR2 initial values "0------" to "0-------" in 1.21 LDV. (Page 203) − Changed CLK_SEL bit1 initial values "-" to "0" in 1.27 Wacrh Counter. (Page 209) − Changed WTDIVEN initial values "-----00" to "------00" in 1.28.3 TYPE5-M4 of 1.28 RTC. (Page 218)
*B	5738584	YSAT	Adapted Cypress new logo
*C	5879432	NOSU	Preface – Purpose of This Manual / Intended Readers − Added a note to refer to datasheets for supported peripheral functions. How to Use This Manual − Updated Table 1 TYPE4-M4 Product List with the latest part numbers and removed suffixes for ordering options from each part number. Chapter 1: Overview – 1.1.1 General Features − Added a note about usage of internal VRAM and HyperRAM for GDC Chapter 2: Reference Clock Selector – 4.5 GPCR4 − Fixed incorrect information in the table of “GPLLN: PLL feedback frequency division ration setting bits”. Chapter 3: Subsystem Control − Updated procedure to setup display clock. in section 3.4.1 and 3.4.3. − Added notes for maximum frequency in section 3.5, 3.6 and 3.7. − Fixed incorrect information at Remark of HyperBus interface clock in 3.8.1.2 Output Frequency of Each Clock table. − Fixed incorrect setting values of GPLLEN and GPLLK in 3.8.2.1 Register Field Setting table. − Removed notes for write to read-only bit in 4.7 VramInterruptClear register.

Revision	ECN No.	Origin of Change	Description of Change
*C	5879432	NOSU	− Added a table of Division ratio in 4.12 GDC_ClockDivider register. − Fixed incorrect names of bit fields in 4.16 dsp_LockStatus register. − Removed notes for write to read-only bit in 4.16 dsp_LockStatus register. − Added notes for maximum frequency in 4.17 dsp0_ClockDivider register. − Updated a note of RPCC_ClockDivider bits in 4.28 RPCC_ClockDivider register. − Fixed incorrect names of bit fields in 4.31 vram_LockStatus register. − Removed notes for write to read-only bit in 4.31 vram_LockStatus register. − Removed incorrect bit field in 4.43 vram_arbiter_priority register.
*D	6050278	NOSU	Preface Added Microcontroller support information.