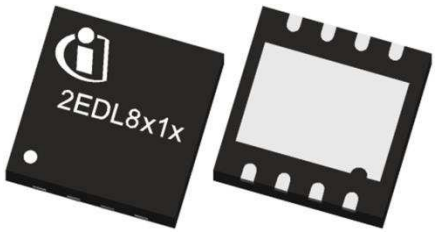
EiceDRIVER™

2EDL8012/3/4 & 2EDL8112/3/4

Features

- Level-shift high-side low-side dual channel driver
- (2EDL801x) Independently controlled high-side and low-side gate drivers
- (2EDL811x) Differential input for superb robustness with inherent shoot-through protection
- 2 A/3 A/4 A source current capability for high-side/ low side drivers
- Strong 5 A high side/6 A low side sink current capability
- 120 V on-chip bootstrap diode
- Support operating frequency up to 1 MHz
- VDD/VHB under voltage lockout (UVLO)
- -10 V to 20 V Input pin capability for increased robustness
- (2EDL811x) -8V to 15 V input pin common mode rejection
- -5 A output pin reverse current capability
- 8 V to 17 V supply voltage operating range
- Fast propagation delay
- <5 ns delay matching
- Small 4 mm x 4 mm x 0.9 mm QFN package
- Lead free RoHS compliant package



Potential Applications

- DC-to-DC converter
- Low voltage motor drive
- Isolate bus converter
- Synchronous rectification for SMPS
- Solar µ-Inverter

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

2EDL8x1x is a high-side low-side driver designed for advanced switching converters such as in telecom, low voltage drive and solar applications. 2EDL801x takes in independent inputs with built-in hysteresis for enhanced noise immunity, whereas 2EDL811x takes in differential input with built-in hysteresis for enhanced noise immunity. 2EDL811x's inherent shoot-through protection ensures the robustness of the system. 4ns maximum delay matching ensures volt-second balance and avoids magnetic core saturation.

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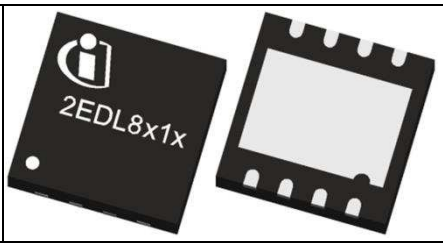
1 Package Information

VDSON-8	RoHS HAL	

1.1 Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
2EDL8012G	VDSON-8	Tape and Reel	6000	2EDL8012GXUMA1
2EDL8013G	VDSON-8	Tape and Reel	6000	2EDL8013GXUMA1
2EDL8014G	VDSON-8	Tape and Reel	6000	2EDL8014GXUMA1
2EDL8112G	VDSON-8	Tape and Reel	6000	2EDL8112GXUMA1
2EDL8113G	VDSON-8	Tape and Reel	6000	2EDL8113GXUMA1
2EDL8114G	VDSON-8	Tape and Reel	6000	2EDL8114GXUMA1

1.2 Pin Configuration and Descriptions

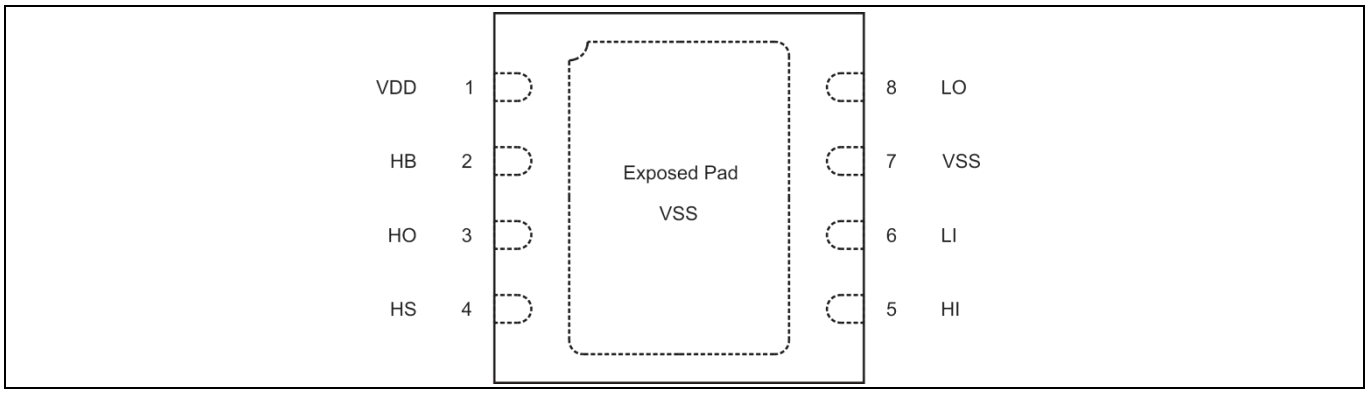


Figure 1 Pin Configuration of PG-VDSON-8-4, Top Transparent View

Pin #	Pin Name	Pin Description
1	VDD	Gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side FET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return, internally connected to exposed pad
8	LO	low-side gate driver output

2 Block Diagram

A simplified functional block diagram is given in the figure below

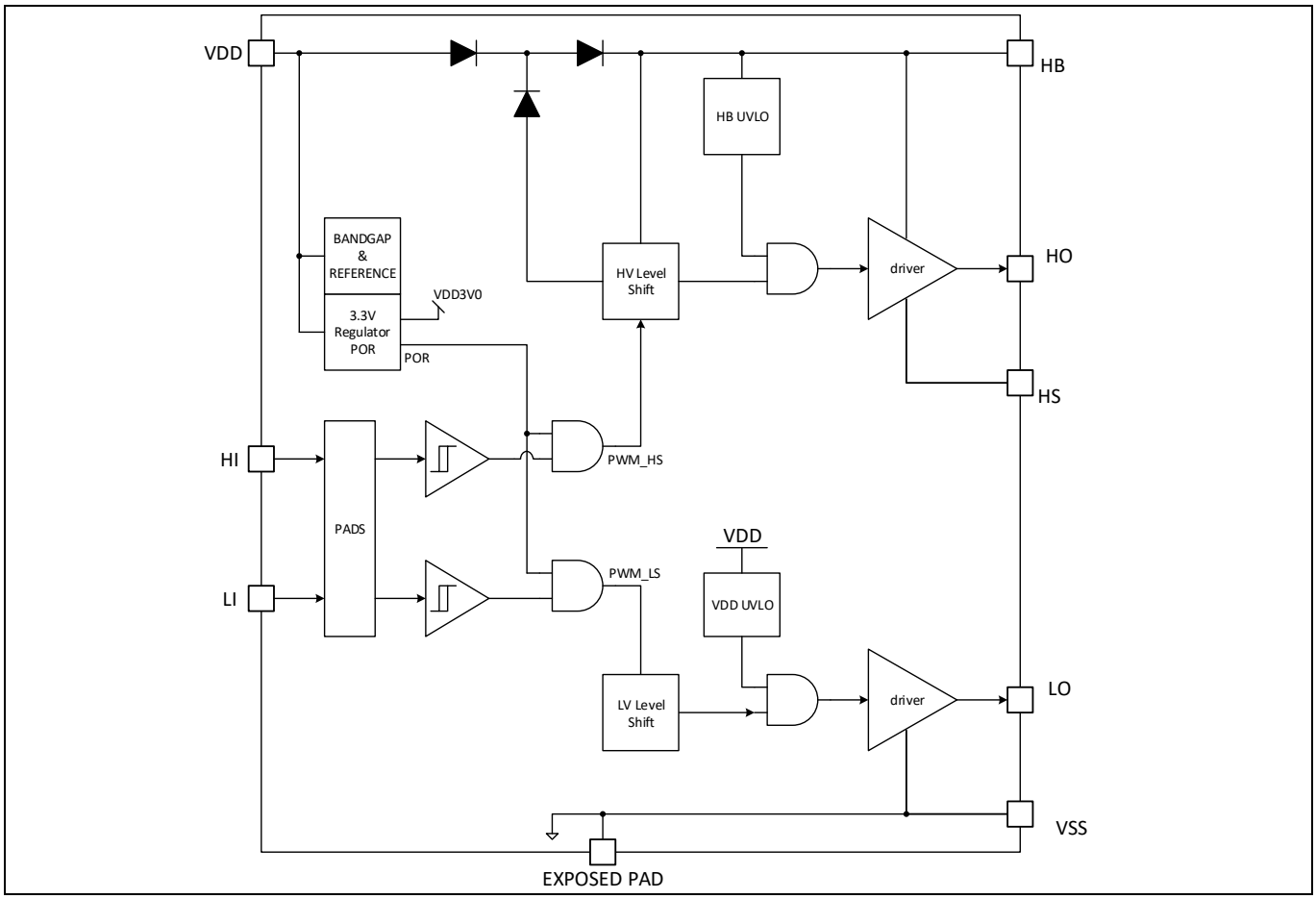


Figure 2 Block Diagram

3 Functional Description

The device is a level-shift 2-channel driver designed to support topologies with high-side and low-side configurations. The high side is level shifted by the combination of an on-chip 120V rated bootstrap diode and an external bootstrap capacitor. The device provides 2 A/3 A/4 A peak source current capability for high-side/ low side drivers and strong 5 A high-side and 6 A low-side sink current capability. This allows driving large power MOSFETs with minimize switching losses during the transition through the MOSFET's Miller Plateau.

2EDL801x's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are independently controlled and matched to typical 2 ns between the turn on and turn off of each other.

2EDL811x's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V and ground potential shifts from -8 to 15V, allowing the device to interfac with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are differentially controlled and matched to typical 1 ns between the turn on and turn off of each other. The differential inputs provide inherent shoot-through protection and ensure high-side and low-side outputs are never on at the same time.

The switching node (HS pin) is able to handle negative voltages down to –(24 - V_{DD}) V which allows the high-side channel to be protected from inherent negative voltages caused parasitic inductance and stray capacitance.

Under-voltage lockout circuits are provided for both high- and low-side drivers. UVLO protects the system by forcing the output low when the supply voltage is lower than the specified threshold.

The following sections describe key functionalities.

3.1 Supply Voltage

The absolute maximum supply voltage is 20 V. The minimum operating supply voltage is set by the under voltage lockout function to a typical default value of 7.0 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

3.2 Input Control

2EDL801x device responds to the two inputs signals (HI and LI) independently according to the following truth table.

Table 1 2EDL801x Truth Table

LI	HI	LO	HO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

The high-side and low-side outputs respond to high-side and low-side inputs independently.

2EDL811x device responds to the combination of two inputs signals (HI and LI) according to the following truth table.

Table 2 2EDL811x Truth Table

LI	HI	LO	HO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	L	L

True differential input comes with inherent shoot through protection by preventing both low and high side to be on at the same time. It also provides noise immunity against ground bounce. The input stage is designed to operate reliably against –8/+15 V ground voltage drift. Input logic hysteresis also helps combat disturbances to the input signal.

3.3 Driver Outputs

The low output impedances allow fast transition of the load transistor. Specifically, the ultra-low impedance pull down resistances, typically 0.6 Ω for the high side and 0.35 Ω for the low side, keep the gate of the load transistor down during fast transient events – avoiding dv/dt induced re-turn-on.

3.4 Under Voltage Lockout (UVLO)

The under voltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch on the device, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 7.0 V with 0.5 V hysteresis for supply voltage (V_{DD}) and 5.75 V with 0.25 V hysteresis for high side boot voltage (V_{HB}).

UVLO threshold trigger is synchronous. The clock gating ensures minimum pulse width set by the controller is obeyed at all times. This increases robustness of the integrated boot diode due to the controllability of the reserve recovery behavior.

3.5 Minimum Pulse Width

The device responds to input level according to the truth table in section 3.2 as long as the logic signal complies with the minimum pulse width requirement. Signal pulse longer than the minimum allowable input pulse width yields valid output. Any output in response to shorter pulses or glitches should be disregarded and filtered out by the user. Under all allowable operation above input minimum pulse width of 40ns, the output behaves one to one to the input with minimal pulse width distortion.

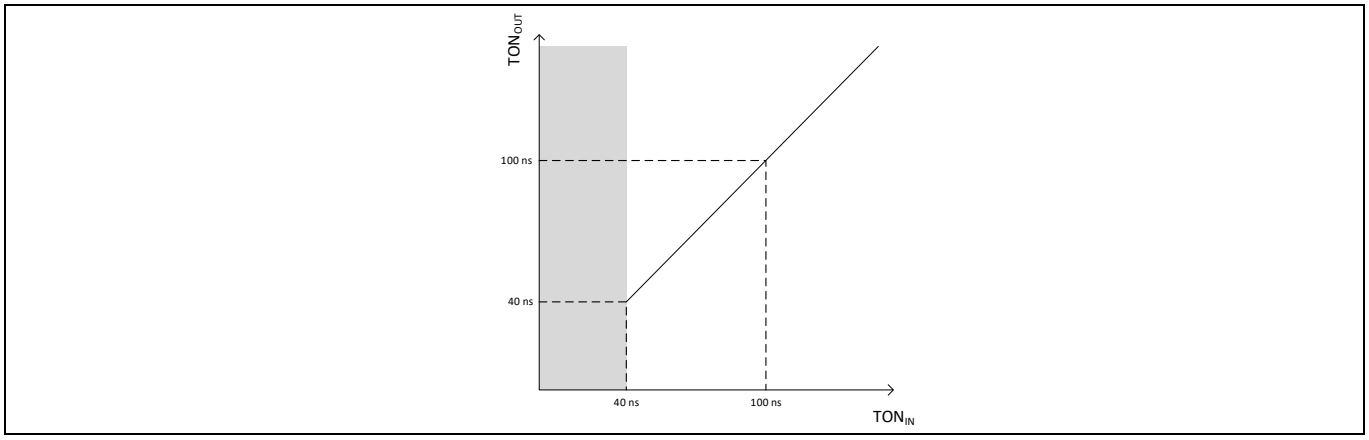


Figure 3 Minimum Pulse Width Input-output On-time Transfer Function

This is diagram is illustrative only with typical value. Actual value and pulse width distortion is subject to process variation. Output pulse width could in some case be shortened or extended to prevent retoggling. See propagation delay parameter footnote.

4 Characteristics

4.1 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Symbol	Description	Min	Max	Unit
V_{DD}	Driver Supply Voltage[1]	-0.3	20	V
V_{HS}	Phase Voltage	-(24 - V_{DD})	V_{HB} + 0.3	V
V_{HB}	High Side Bootstrap Voltage	-0.3	120	V
V_{HI}, V_{LI}	LI and HI Input Voltage	-10	20	V
V_{LO}	Output voltage on LO	-0.3	V_{DD} + 0.3	V
V_{HO}	Output voltage on HO	V_{HS} – 0.3	V_{HB} + 0.3	V
I_{OR}	LO and HO Peak Reverse Current[2]	---	5	A
T_J	Operating Junction Temperature	-40	150	°C
T_S	Storage Temperature	-55	150	°C

4.2 Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in the subsequent tables refer to these operating conditions.

Symbol	Description	Min	Typ	Max	Unit
V_{HS}	Phase Voltage to VSS	-(24 - V_{DD})	---	80	V
V_{DD}	Driver Supply Voltage	8	10	17	V
V_{HB}	High Side Bootstrap Voltage	-0.3	---	90	V
T_J	Junction Temperature	-40	---	125	°C
dv/dt	HS Slew Rate	---	---	50	V/ns
V_I	Differential Input Voltage[3] (2EDL811x)	0	3.3	5	V
V_{ICMR}	Input Signal Common Mode Rejection (2EDL811x)	-8 + V_I/2	---	15 – V_I/2	V

4.3 Static Electrical Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} =V_{SS}=0V. T_C = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}.

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{DDR}	V_{DD} UVLO Rising Threshold	6.6	7.0	7.4	V	
V_{DDH}	V_{DD} UVLO Threshold Hysteresis	---	0.5	---	V	
V_{HBR}	V_{HB} UVLO Rising Threshold[4]	5.5	5.75	6.0	V	

[1] All voltage ratings in this section referenced to ground.

[2] For <500ns pulses

[3] Absolute voltage difference between HI And LI ($|V_{HI}-V_{LI}|$)

[4] HB (high side bootstrap) related ratings referenced to V_{HS}

V_{HBH}	V_{HB} UVLO Threshold Hysteresis	---	0.275	---	V	
I_{HB}	Boot voltage Quiescent Current	---	0.55	0.7	mA	V_{LI}=V_{HI}=0V
I_{HBO}	Boot Voltage Operating Current	---	2.6	2.9	mA	f=500kHz, C_{LOAD}=0nF, 2EDL8x12
		---	2.7	3.0		f=500kHz, C_{LOAD}=0nF, 2EDL8x13
		---	2.9	3.2		f=500kHz, C_{LOAD}=0nF, 2EDL8x14
I_{DD}	V_{DD} Quiescent Current	---	0.55	0.7	mA	V_{LI}=V_{HI}=0V
I_{DDO}	V_{DD} Operating Current	---	2.7	3.0	mA	f=500kHz, C_{LOAD}=0nF, 2EDL8x12
		---	2.8	3.1		f=500kHz, C_{LOAD}=0nF, 2EDL8x13
		---	2.9	3.2		f=500kHz, C_{LOAD}=0nF, 2EDL8x14
R_{IN}	Input Pulldown Resistance	54	68	82	kΩ	
V_{IR}	Rising Input Voltage Threshold	---	2.25	2.9	V	
V_{IF}	Falling Input Voltage Threshold	1.0	1.65	---	V	
V_{IH}	Input Logic Voltage Hysteresis	---	0.6	---	V	
R_{PUH}	High Side Pull Up Resistance	---	2.7	---	Ω	2EDL8x12
		---	1.3	---		2EDL8x13
		---	0.9	---		2EDL8x14
R_{PDH}	High Side Pull Down Resistance	---	0.5	---	Ω	
R_{PUL}	Low Side Pull Up Resistance	---	2.7	---	Ω	2EDL8x12
		---	1.3	---		2EDL8x13
		---	0.9	---		2EDL8x14
R_{PDL}	Low Side Pull Down Resistance	---	0.35	---	Ω	

4.4 Dynamic Electrical Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} =V_{SS}=0V. T_C = 25°C unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
I_{PUH}	High Side Peak Pull Up Current[1]	---	2	---	A	V_{HO} = 0 V , 2EDL8x12
		---	3	---		V_{HO} = 0 V , 2EDL8x13
		---	4	---		V_{HO} = 0 V , 2EDL8x14
I_{PDH}	High Side Peak Pull Down Current[1]	---	5	---	A	V_{HO} = 12 V
ratI_{PUL}	Low Side Peak Pull Up Current[1]	---	2	---	A	V_{LO} = 0 V , 2EDL8x12
		---	3	---		V_{LO} = 0 V , 2EDL8x13
		---	4	---		V_{LO} = 0 V , 2EDL8x14
I_{PDL}	Low Side Peak Pull Down Current[1]	---	6	---	A	V_{LO} = 12 V
T_{DR}	Rising Propagation Delay[2,3]	---	45	50	ns	C_{LOAD} = 0
T_{DF}	Falling Propagation Delay[3]	---	45	54	ns	C_{LOAD} = 0
T_{DM}	Delay Matching[4]	---	2	5	ns	
T_{PW}	Minimum Input Pulse Width[5]	---	---	40	ns	
T_{DRR}	Bootstrap Diode Turn off Time[1,6]	---	10	---	ns	I_F = 20 mA, I_{PRR} = 0.5 A

4.5 Thermal Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
R_{thJC}	Junction to Case Thermal Resistance	---	3	---	°C/W	Bottom
		---	46	---	°C/W	Top
R_{thJA}	Device on PCB	---	42	---	°C/W	6 cm^2 cooling area[7]

[1] Not subject to production test

[2] Rising propagation delay from LI to LO and from HI to HO

[3] A transient detector blocks the toggling of the high side output when it detects moving phase node (due to transition and/or oscillation). It prevents unwanted retoggling but may increase propogation delay. See transient detector activation in Figure 6.

[4] Consolidated delay matching (1) ON: between LO Rising and HO Falling and (2) OFF: betweenLO Falling and HO Rising

[5] Minimum input pulse width that produces valid output signal

[6] External schottky boot diode in parallel recommended for high dv/dt application

[7] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thick) copper area for drain connection. PCB vertical in still air.

5 Descriptive Illustration

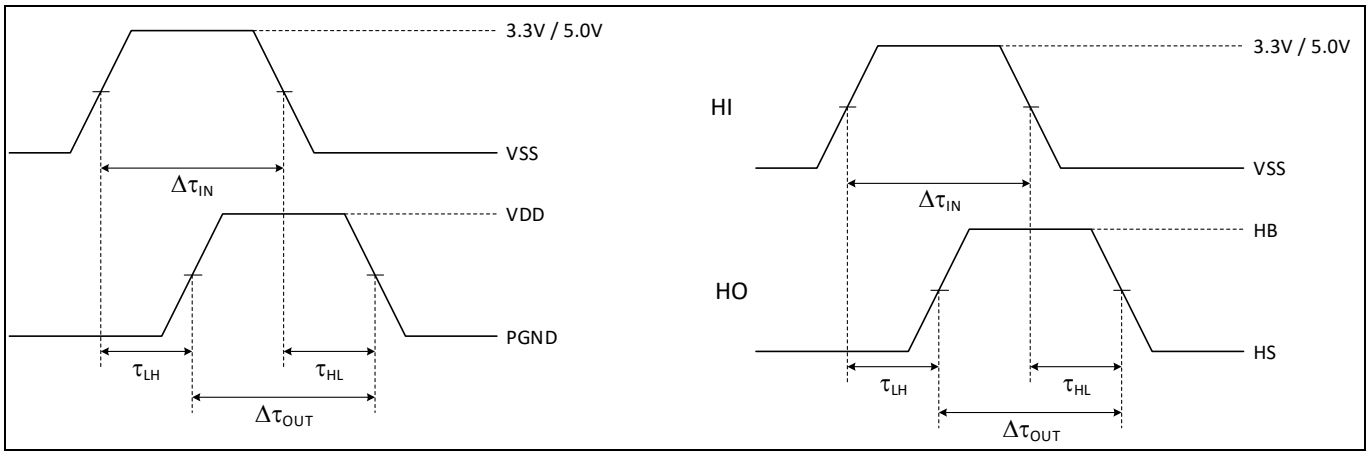


Figure 4 Propagation delay

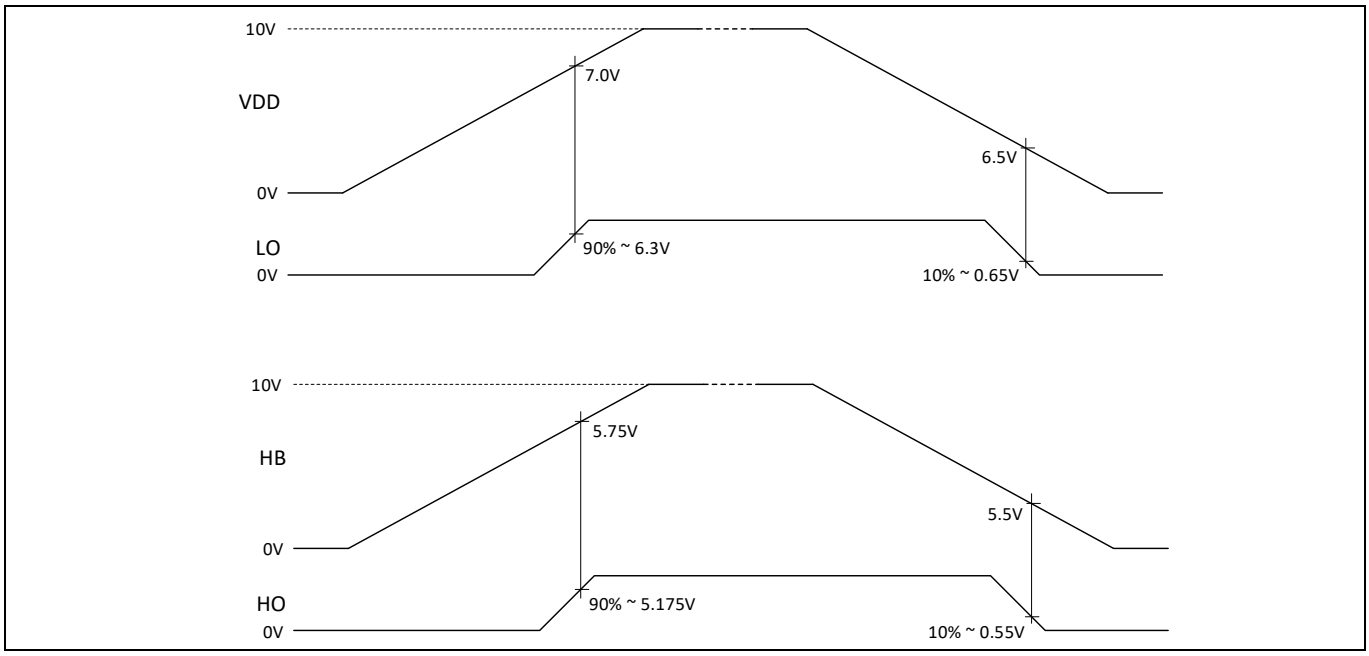


Figure 5 UVLO behavior

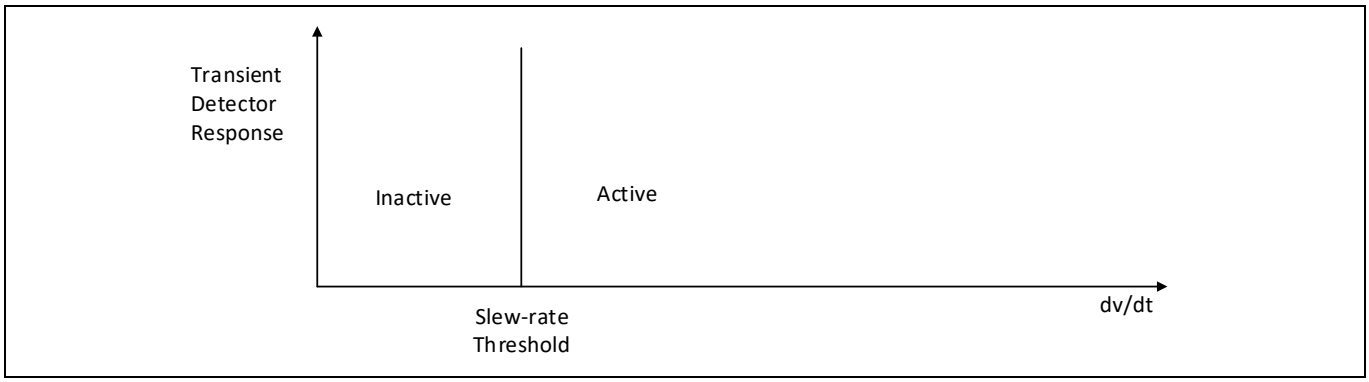
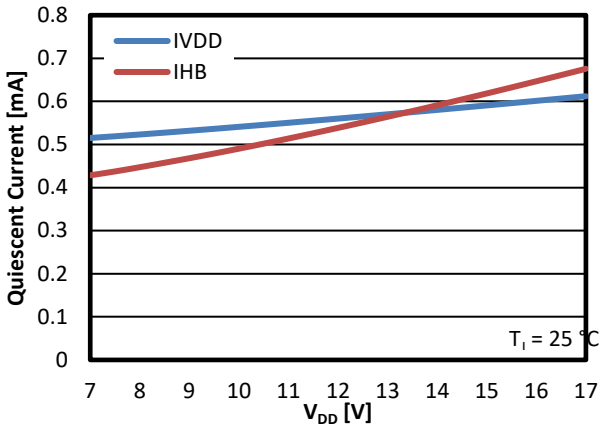


Figure 6 Transient Detector Response[1]

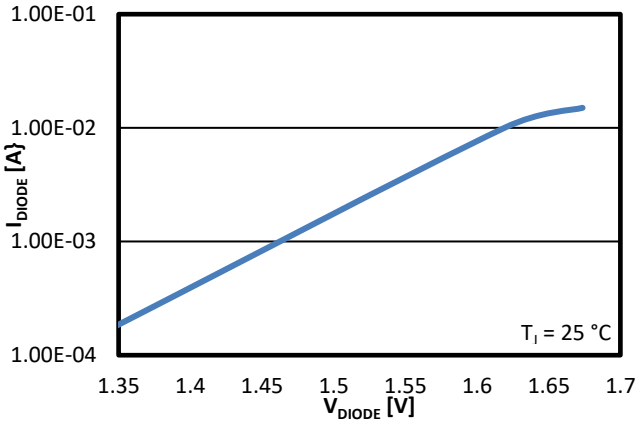
[1] Reference slew rate threshold versus temperature under Section 6 Typical Characteristics.

6 Typical Characteristics

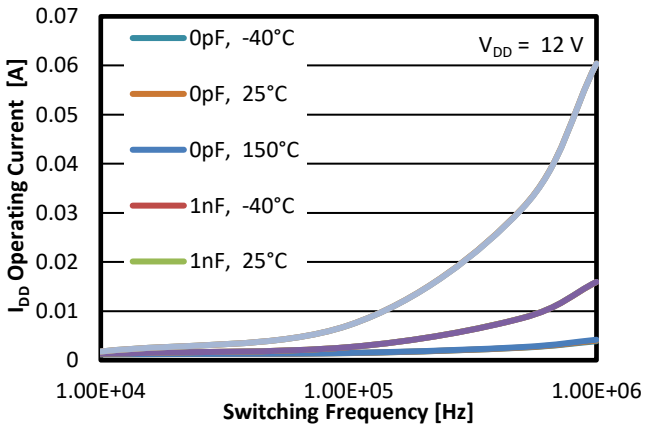
Quiescent Current vs. V_{DD}



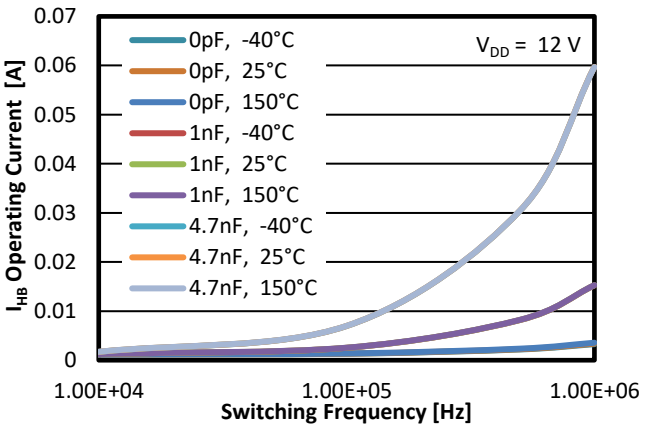
Diode Current vs. Voltage



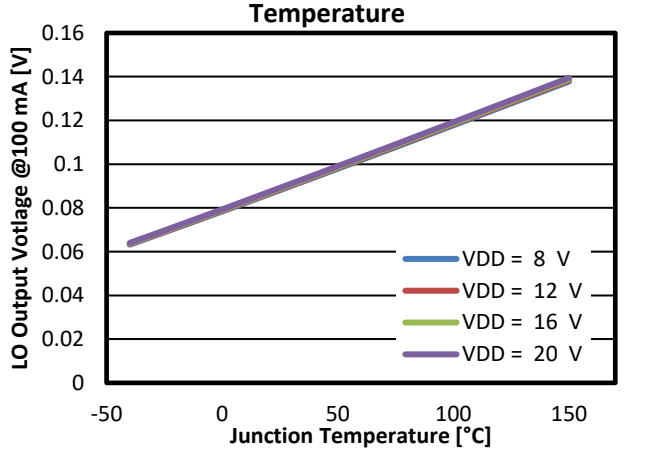
I_{DD} Operating Current vs. Temperature



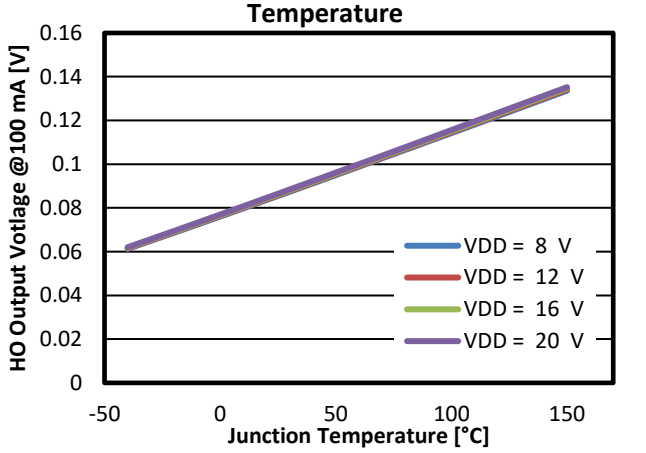
I_{HB} Operating Current vs. Temperature



LO Output Voltage (Pull-up) vs. Temperature

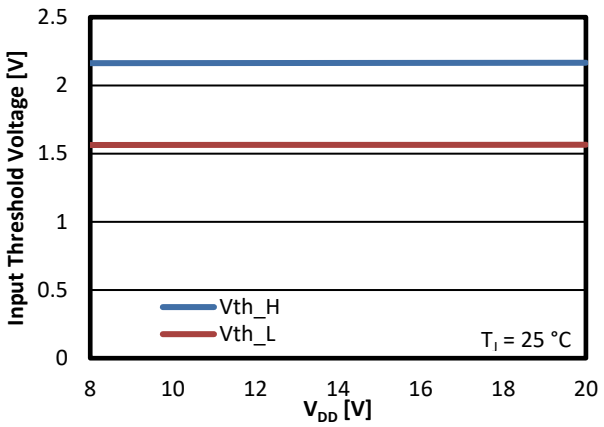


HO Output Voltage (Pull-up) vs. Temperature

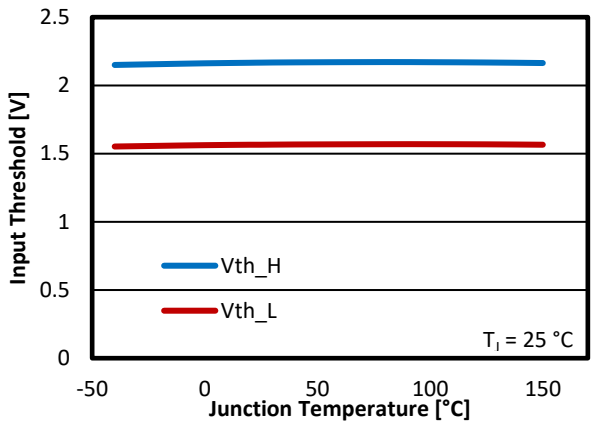


Typical Characteristics

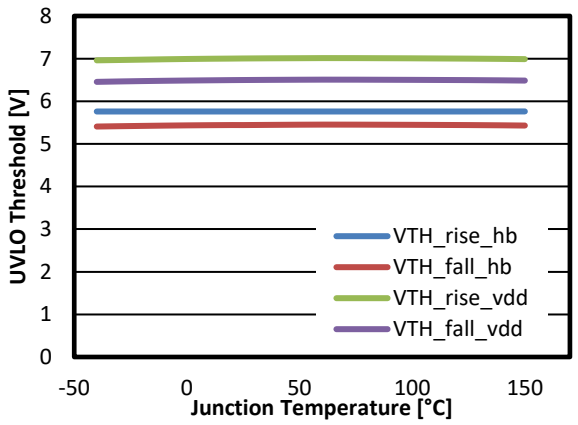
Input Threshold vs. Supply Voltage



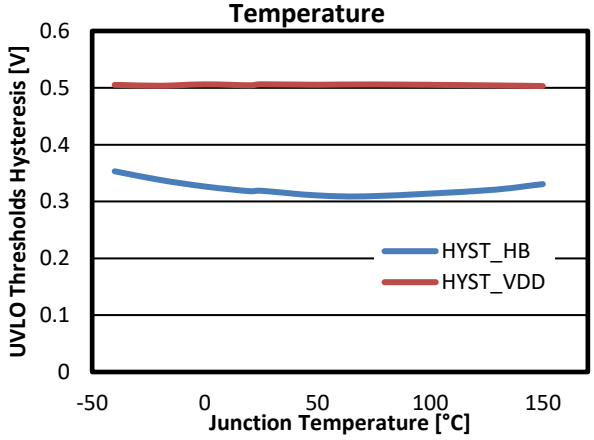
Input Threshold vs. Temperature



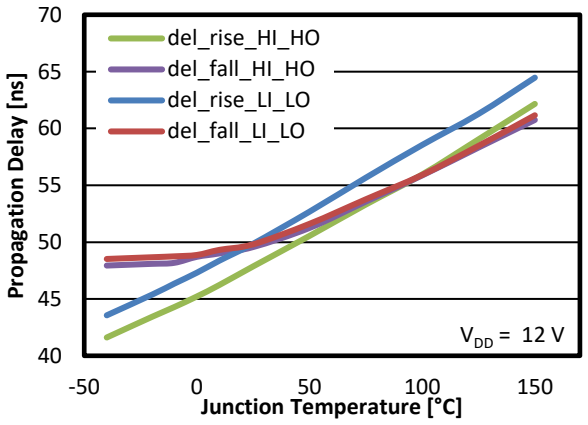
UVLO Threshold vs. Temperature



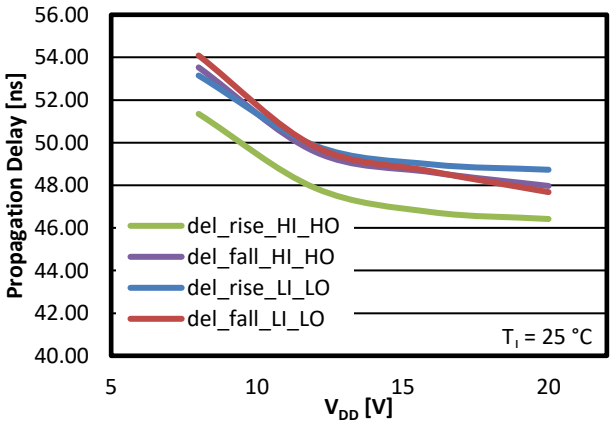
UVLO Threshold Hysteresis vs. Temperature



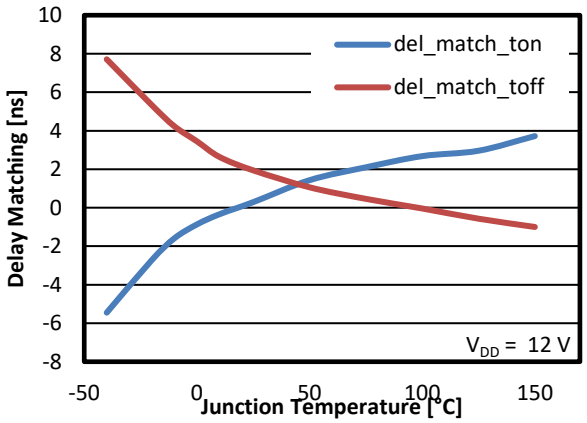
Propagation Delay vs. Temperature

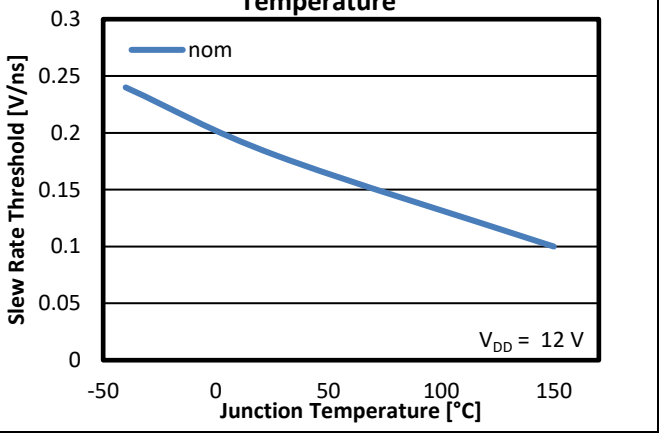


Propagation Delay vs. V_{DD}



Typical Characteristics





7 Typical Application

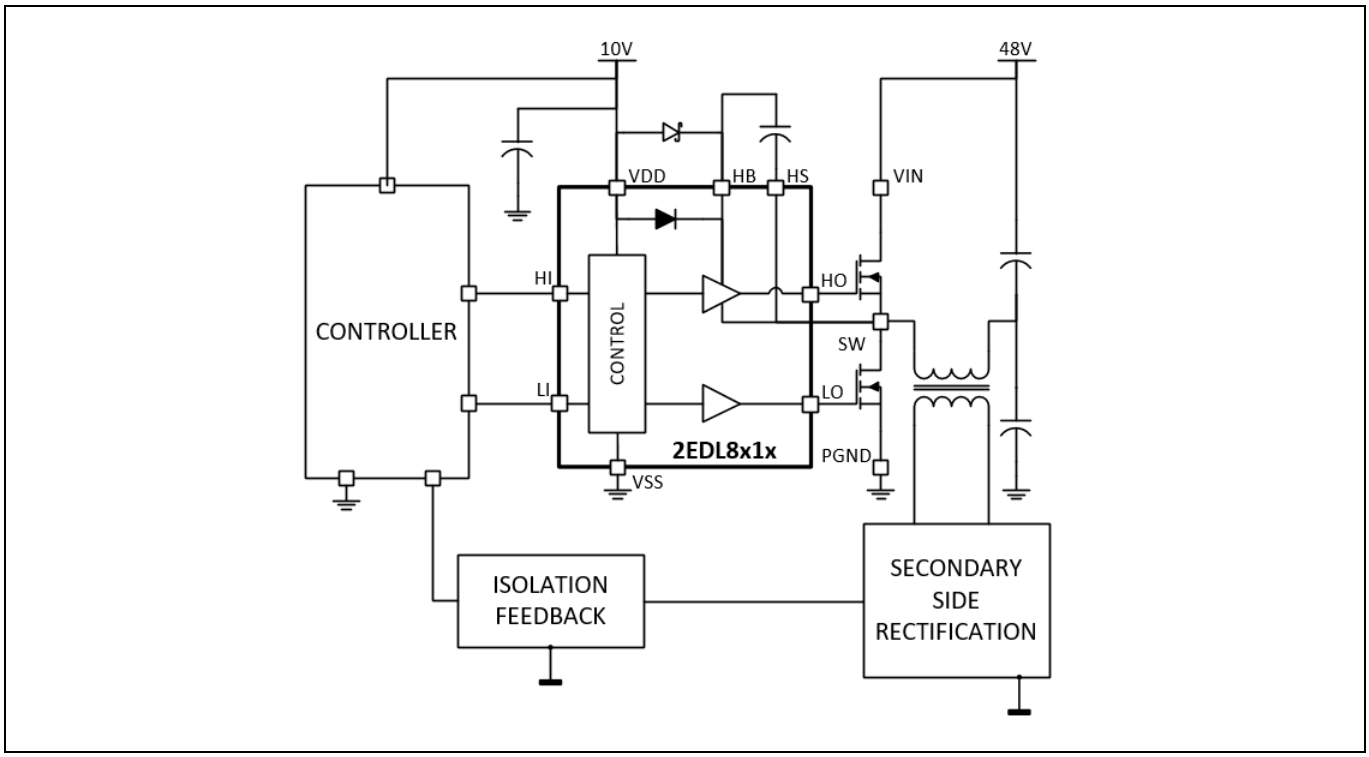


Figure 7 Typical Application 1

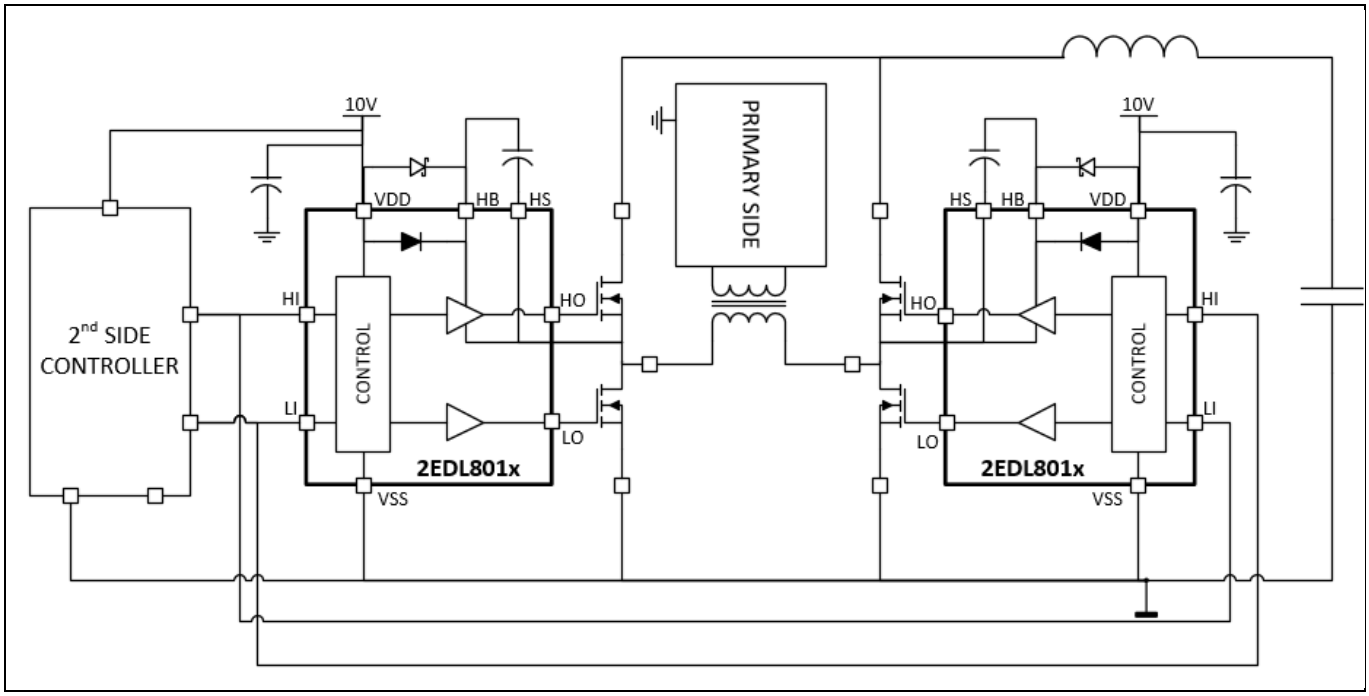
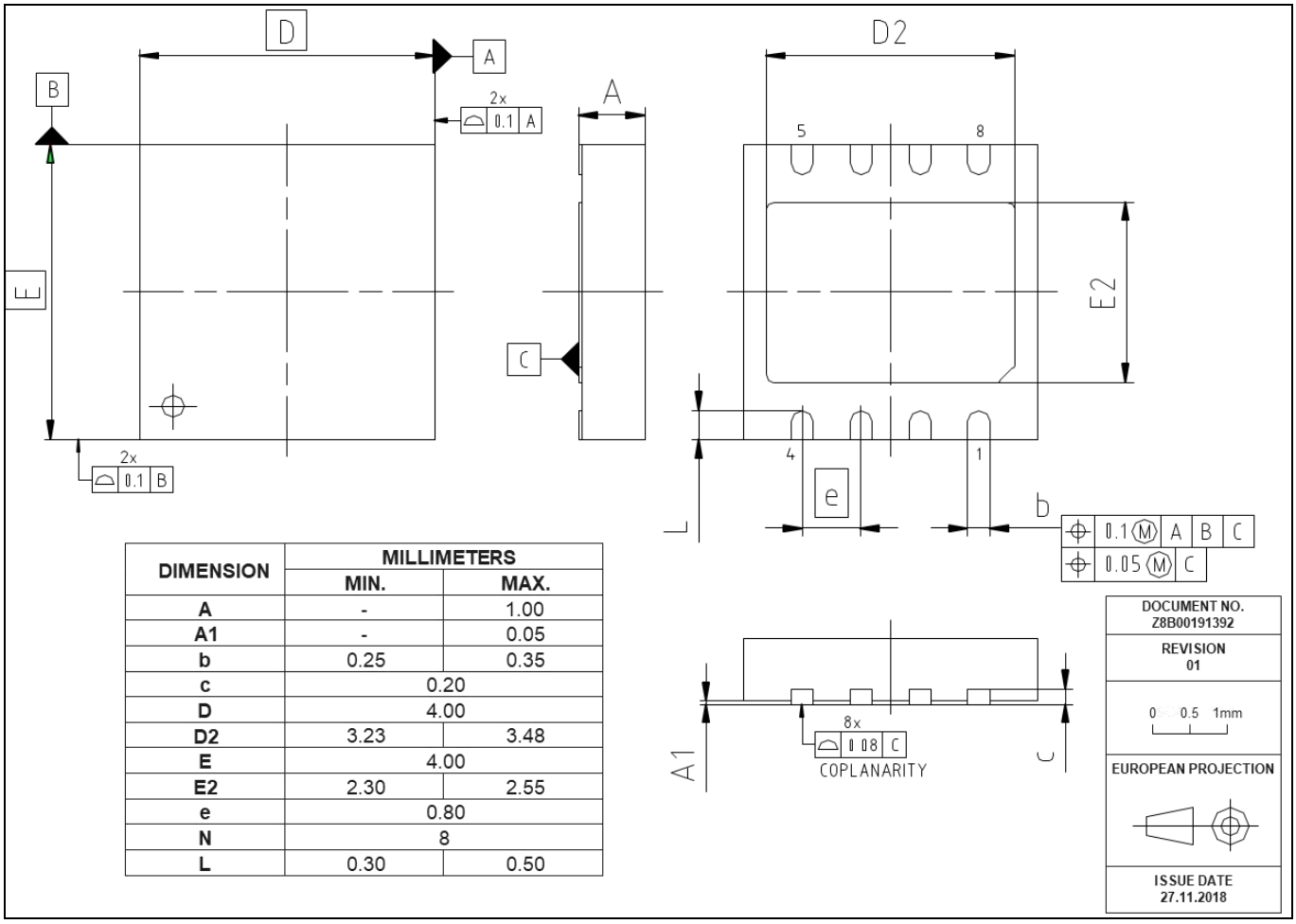


Figure 8 Typical Application 2

8 Outline Dimensions

8.1 VDSON-8 Package Outline



DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	-	1.00
A1	-	0.05
b	0.25	0.35
c	0.20	
D	4.00	
D2	3.23	3.48
E	4.00	
E2	2.30	2.55
e	0.80	
N	8	
L	0.30	0.50

Figure 9 VDSON-8 Outline Dimensions

9 Reel and Tape

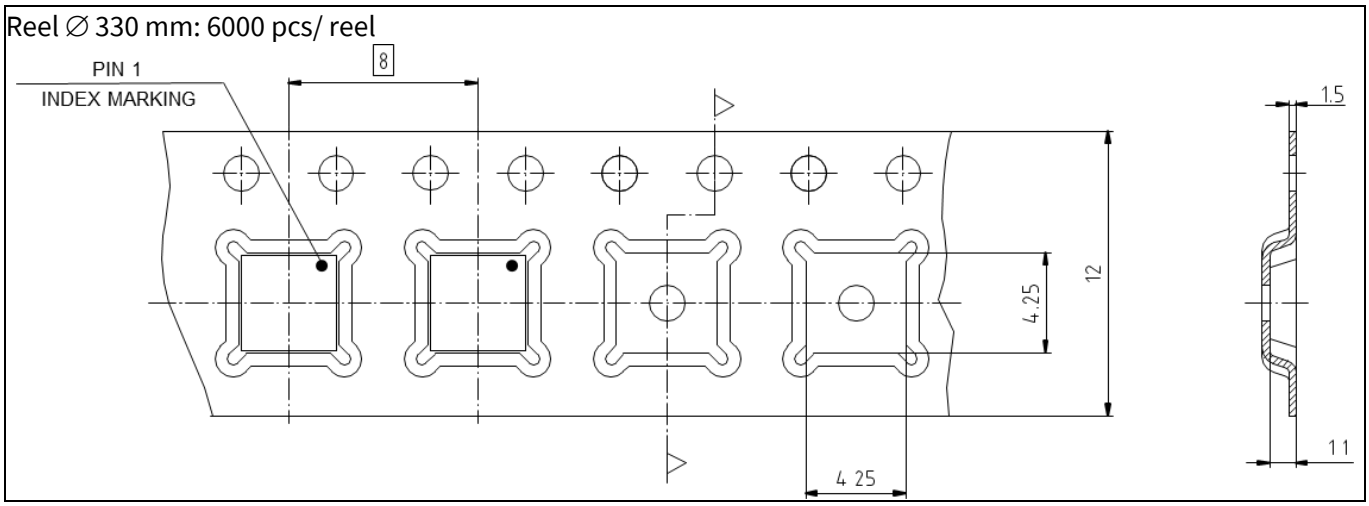


Figure 10 Reel and Tape

Revision History

2EDL8012/3/4 & 2EDL8112/3/4

Revision: 2019-06-03, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2019-06-03	Release of final version

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