Getting started with 2ED2410-EM

Application note

About this document

Scope and purpose

This application note explains how to design-in Infineon EiceDRIVER™ APD 2ED2410-EM.

The set-up of external components based on practical considerations using datasheet [1] parameters is described and tips on how to use this unique gate driver flexibility are provided.

Intended audience

This document is intended for all electrical and electronic engineers who need to replace relays and fuses effectively and simply so that they make a reliable and self-protected solid-state switch, based on MOSFET and a shunt resistor.

Note: *Values shown in this application note are measured under lab conditions and will vary for different cooling conditions and setups.*

Note: *In this document, [PRQ-xxx] numbers refer to 2ED2410-EM datasheet [1] parameters.*

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1 Basic functions and mandatory external components

This chapter describes the minimal required as well as most necessary components to operate the 2ED2410-EM.

2ED2410-EM is a high-side gate driver and therefore needs a power supply that elevates voltage above battery voltage to drive the MOSFETs. A boost converter supply is chosen, to have improved efficiency compared to a charge pump, and therefore, pulls less current from the car's battery. The diode (D) and switching element (K1) are implemented inside the chip and the inductor (L), output capacitor (C_{BC}) and resistor for current peak sense (R_{RS}) must be added externally.

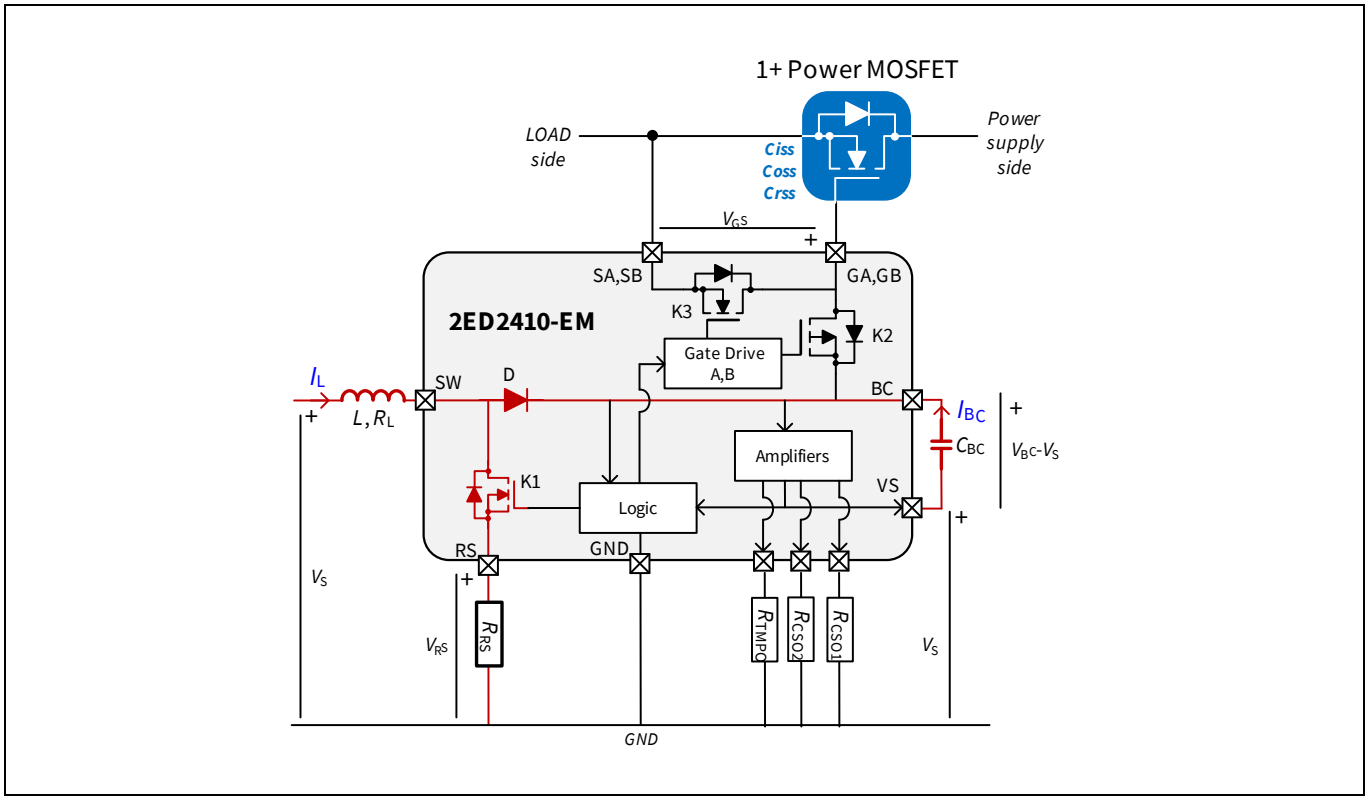


Figure 1 2ED2410-EM Boost converter supply concept with currents and voltages definition

1.1 Sizing C_{BC}

The C_{BC} capacitor is the output capacitor of the boost converter, normally used to filter the output on regular boost converters.

Here, it is also used as a charge buffer for the external MOSFETs parasitic C_{iss} at turn-on: during turn-on, the charges are transferred from C_{BC} to the external MOSFET C_{iss}. This allows 2ED2410-EM to drive many MOSFETs in parallel, up 100 nF equivalent C_{GS} per gate driver output. Therefore, it has to be ensured that during turn-on, the voltage of C_{BC} capacitor does not drop below the boost converter "gate UVLO" limit. The range between "gate UVLO" [PRQ-140] and regulating output voltage of the boost converter $V_{BC(TH)}$ [PRQ-139] above battery voltage, is called $V_{BC(RG)}$ [PRQ-141].

Therefore, the MOSFET reference and the total number of MOSFET driven by the driver must be known at this stage.

Assuming the charge is conserved between tank capacitor C_{BC} and the sum of the MOSFET C_{iss}, $C_{iss(TOT)}$, using Q = C * V,

(1) $$C_{BC} * \Delta V_{BC} = C_{iss(TOT)} * V_{BC(TH)}$$

Therefore, because the minimum ΔV_{BC} we have to sustain with C_{BC}, is $V_{BC(RG)MIN}$ (Min. of $V_{BC(RG)}$);

(2) $$C_{BC(MIN)} = \frac{C_{iss(TOT)} * V_{BC(TH)MAX}}{V_{BC(RG)MIN}}$$

As an example, using eight IAUT300N08S5N012 (four in parallel on each gate output), the computed $C_{BC(MIN)}$ is given by:

(3) $$C_{BC(MIN)} = \frac{8 * 1.625 * 10^{-8} * 14}{1.9} = 0.96\ \mu F$$

Therefore, a suitable capacitor for this application could be a 1 µF capacitor. Considering a 30 % shift of capacitor value over lifetime as well as 20% ceramic capacitor accuracy, here it is necessary to use a 2.2 µF capacitor for C_{BC}.

The automated calculation can be found in the excel workbook, tab “boost converter cap CBC”[2] .

A regular turn-on is shown in figure 3. When the MOSFETs are turned-on, the charges are taken from C_{BC} and the boost converter pumps again to compensate the charged transferred to the MOSFET, hence the activation of RS (green). The activation is monitored by DG0 pin (pink) in ON mode.

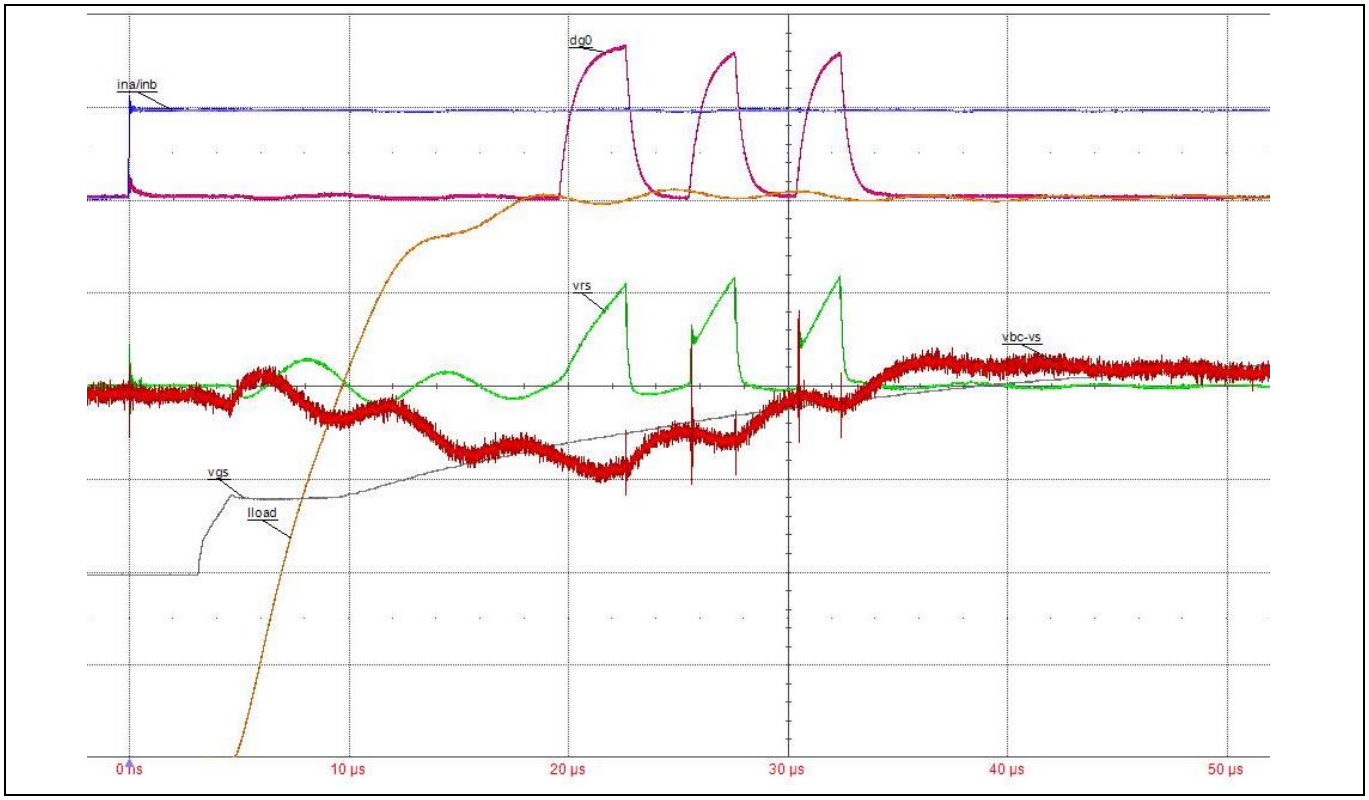


Figure 2 Switching waveform from IDLE to ON mode [**blue: INx; green: V_{RS}; red: V_{BC}-VS (AC mode) (boost converter output); pink: DG0; grey: gate-source on MOSFET; orange: LOAD current**]

1.2 Sizing *L* and R_{RS}

The boost converter is designed for very small duty cycles (<1 %), open loop and current peak control operation in discontinuous conduction mode.

Therefore, the most important parameter to observe is the $I_L = I_{peak}$ limitation in the switching element, K1 (refer to Figure 1), defined by maximum of parameter I_{SW} [PRQ-16]. This condition $I_L < I_{SW}$ must be true at all temperatures over the application voltage range.

The current in the inductor is limited by the $V_{RS(TH)}$ comparator, inside the driver (see Figure 26 in datasheet [1] and is duplicated below), which monitors the voltage across R_{RS}. Due to the delay in the loop ($t_{D\,(OFF)K1}$ [PRQ-155]), the inductor current exceeds the threshold set by: $V_{RS(TH)}$ [PRQ-147].

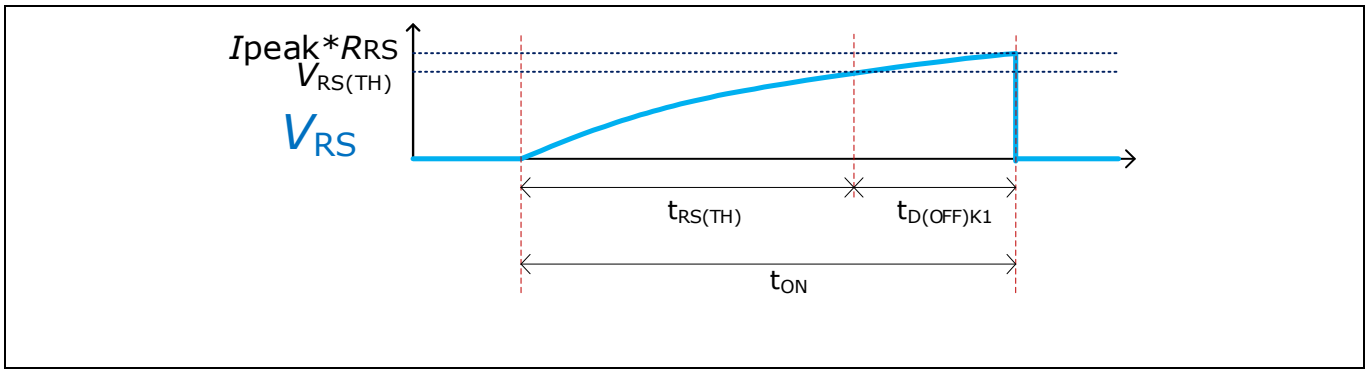


Figure 3 Switching waveform of boost converter, V_{RS} voltage

The current waveform in the inductor is not linear, but exponential because the sum of the resistor of K1, of the parasitic inductor of *L* (R_L) and R_{RS} are not negligible in the K1 short activation timeframe.

Therefore, the time to reach $t_{RS(TH)}$ is computed by:

(4) $$t_{RS(TH)} = -\frac{L}{R_{DS(ON)K1}+R_{RS}+R_L} \times ln(1 - V_{RS(TH)} \times \frac{R_{DS(ON)K1}+R_{RS}+R_L}{R_{RS} \times V_S})$$

Referring to Figure 3:

(5) $$t_{ON} = t_{RS(TH)} + t_{D(OFF)K1}$$

Ideally R_{RS} should be as low as possible: a high R_{RS} resistor would lower output current capability. In addition, boost converter operating frequency could be in the audible range. By design of the I_{peak} detection loop, a minimum is given in the datasheet [1] $R_{RS(MIN)}$ = 10 Ω (PRQ-138). Additionally, the computed power must be sustained by the resistor R_{RS} across the whole application range, meaning I_{peak} must be computed for 18 V if the operating range expected in the application is 8 V to 18 V, for example.

(6) $$P_{RRS} \geq I_{peak(V_{S(MAX)})}{}^2 \times R_{RS}$$

Therefore, from equation (4), having chosen R_{RS} value, the I_{peak} can be computed with the available inductor. As there are three unknowns in the equation, there is no simple way to compute the minimum inductor that can be used. It has to be ensured that I_{peak} parameter is not violated over the application V_S range given the characteristics of the inductor used.

Therefore, the I_{peak} current can be solved by:

(7) $$I_{peak} = \frac{V_S}{R_{DS(ON)K1}+R_{RS}+R_L} \times \left(1 - e^{-t_{ON} \times \frac{R_{DS(ON)K1}+R_{RS}+R_L}{L}}\right)$$

The automated calculation can be found in the workbook [2], tab “L, RS and driver consumption”.

Typically, an inductor between 100 µH and 470 µH can be selected with $R_{RS(MIN)}$. Where a 100 µH can be cost-optimized compared to a 470 µH inductor, the latter improves the efficiency and therefore will optimize the current consumption from the battery. Also, choosing an inductor with a small parasitic series resistance R_L, will increase the boost converter efficiency and reduce the current drawn from the battery See Chapter 7, Quiescent current example for detailed quiescent current calculations.

To sum up: the choice of the inductor is driven by the I_{peak} and its optimization by three parameters:

1. The parasitic resistance of the coil
2. Current consumption of the driver in the application
3. Application target cost

1.3 Computing boost converter frequency

Figure 1 shows the gates are supplied directly out of the gate driver through the PMOS of a push-pull (PMOS K2, see Figure 1). Therefore, in on-mode, the output of the boost converter is directly connected to the MOSFET gate through K2. Consequently, monitoring the boost frequency monitors the health of the gate source junction. Any leakage or short connection in the power MOSFET can be detected by a much higher frequency in boost converter operation compared to normal.

The activation frequency depends on the boost converter current I_{BC}. The current seen by the boost converter is given in the datasheet [1], depending on the mode the driver is in $I_{BC(IDLE)}$; $I_{BC(ON)}$; $I_{BC(SAFESTATE)}$ which are PRQ-144, PRQ-145 and PRQ-146 respectively.

Assuming no leakage losses in C_{BC} capacitor, the charges going out of C_{BC} with an I_{BC} current over the period T of the boost converter is equivalent to the charges received from the inductor over that same period of time. Therefore, assuming the number of charges stays the same in and out C_{BC}, the time and current to transfer from L to C_{BC}, using Q = I * t, T can be computed easily:

(8) $$T = \frac{t_{transfert} * \frac{I_{peak}}{2}}{I_{BC}}$$

With

(9) $$t_{transfert} = L * \frac{I_{peak}}{(V_{BC(TH)} + V_{FBC})}$$

Equation (9) uses $V = L * \frac{di}{dt}$ approximation where V_{FBC} is the integrated boost converter diode (PRQ-148) and adds up to the boost converter output voltage.

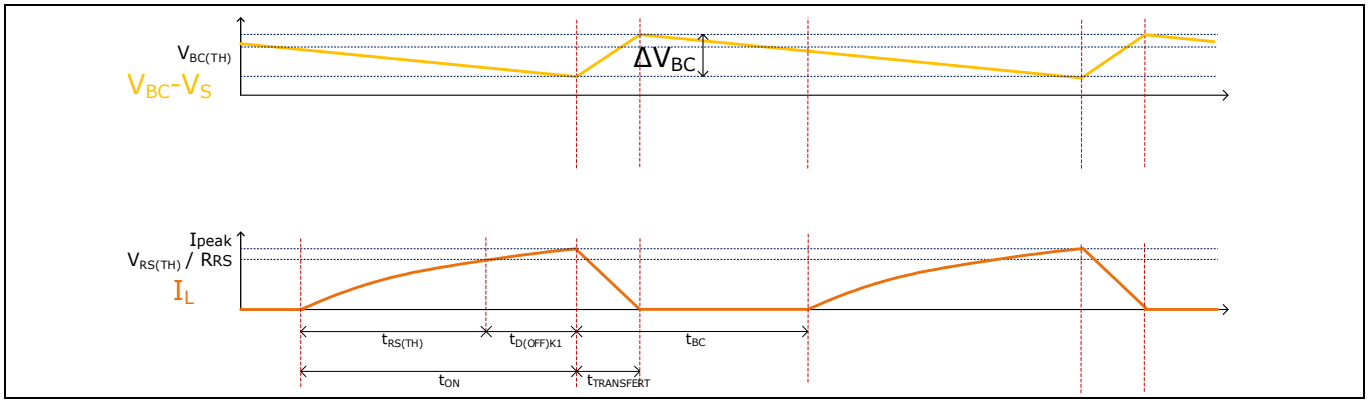


Figure 4 Boost converter theoretical waveform in discontinuous conduction mode (not to scale)

Note that I_{BC} varies with application temperature and therefore boost frequency varies with temperature.

The DG0 frequency can be simply monitored on pin DG0 in ON mode.

The automated calculations for expected boost converter frequency can be found in the excel workbook [2], tab “L, RS and driver consumption”.

1.4 Sizing R_{GATE} for gate-source leakage detection of MOSFET

In power distribution applications, power availability is a critical topic. The 2ED2410-EM driver connects the gate of external MOSFET to the boost converter output, and therefore if a gate source degradation occurs in one MOSFET, it could trigger gate UVLO protection. However, it also gives the opportunity to identify such a failure by sizing R_{GATE} properly without turning-off the switch.

R_{GATE} can be sized so it limits the current to the maximum boost converter output current. As a result, the boost converter frequency will operate with greater frequency and can be easily monitored on pin DG0 in ON mode.

Since the boost converter frequency can be monitored by a microcontroller, it allows the car central computer unit to make power management decisions in case of gate-source short detection on one MOSFET such as turn-off of some non-essential load to reduce power losses through the remaining MOSFET.

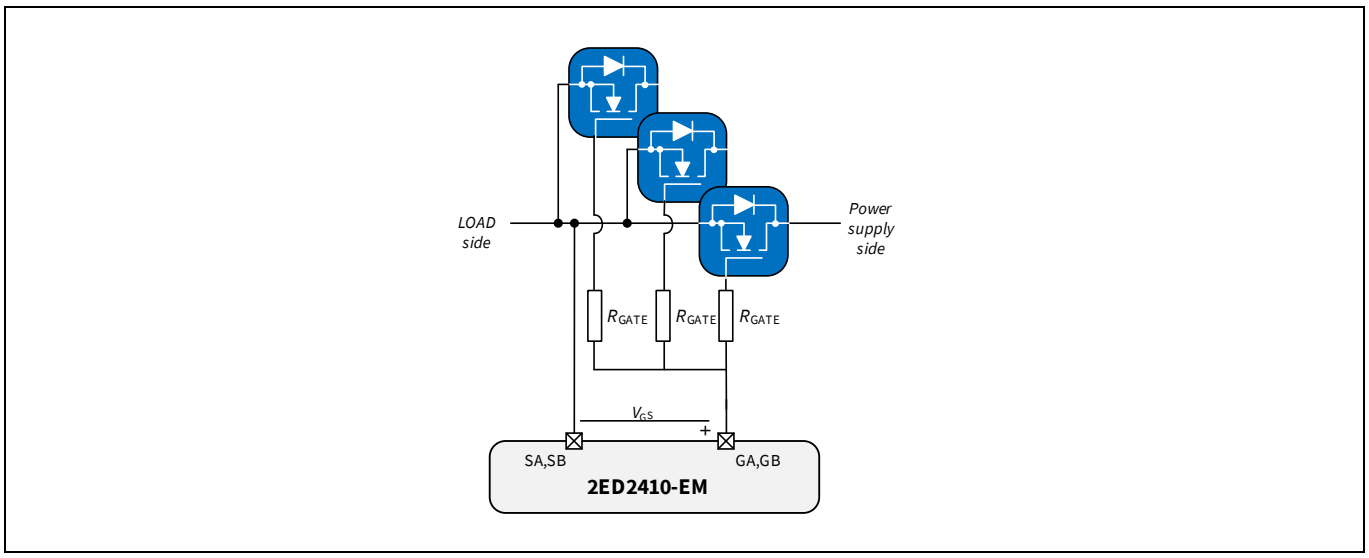


Figure 5 Schematic of principle to identify R_{GATE} in the application

The maximum current which can be delivered by the boost converter is computed by:

$$I_{BC(MAX),disc.} = \frac{\Delta I_{peak} * t_{transfert}}{2*(t_{ON(K1)}+t_{BC})} \quad (10)$$

This gives a minimum value for R_{GATE} according to:

$$R_{GATE(MIN)} = \frac{V_{BC(TH)}}{I_{BC(MAX)}} \quad (11)$$

The automated calculation can be found in the workbook [2], cell 51, tab “L, RS and driver consumption”.

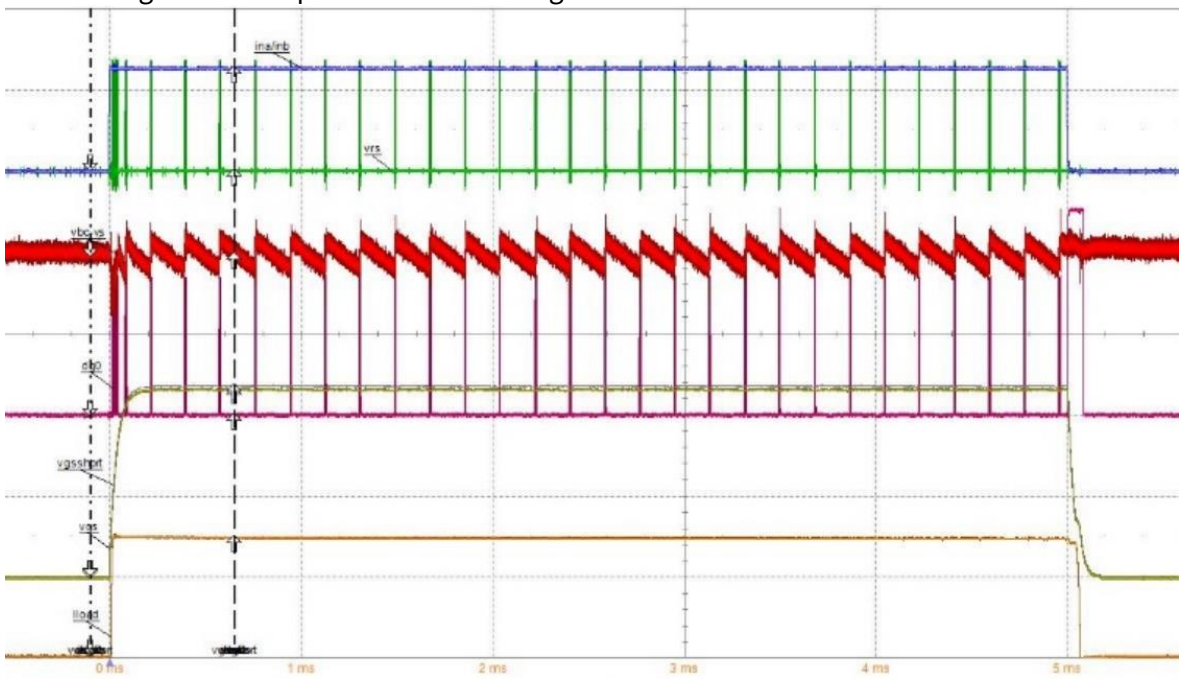
Note: The min./max. R_{GATE} is not discussed here. Of course, R_{GATE} values down to a few ohms can be used, especially for increased switch-off speed. Fast-off circuitry can used between gate driver and MOSFET.

1.4.1 Example in application

The figure below shows an example R_{GATE} designed to sustain gate-source short and shows the effects on the gate driver signals. It uses 12 V demoboard with ES samples.

It is clear that the boost converter frequency is increased in case of gate-source short and proper R_{GATE} value. As a result, the driver does not enter SAFESTATE but keeps the switch operating.

With shorted gate and adapted resistor so that gate UVLO is avoided and the switch is maintained ON



With no shorted gate, normal boost converter activity can be monitored out of DG0 pin in on-mode

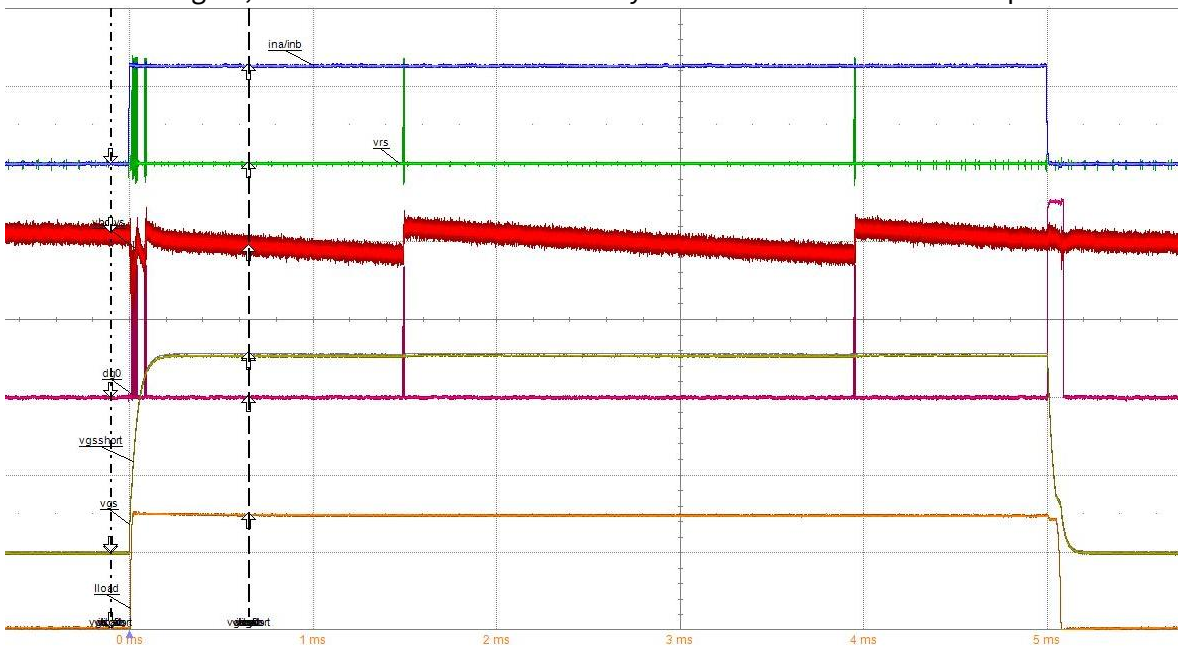


Figure 6 **R_{GATE} to prevent UVLO when gate-source short: with and without failure** ***[blue: INx; green: V_{RS}; red: V_{BC}-VS (boost converter output); pink: DG0; yellow: gate-source on MOSFET; orange: LOAD current]***

1.5 Reverse battery behavior

In this chapter, the behavior of the driver when reverse battery is applied, is described. Two case are examined, common drain and common source MOSFET configuration.

Note: *For a third case, single high-side MOSFET control, there is no protection: no turn-on mechanism of the MOSFET in reverse battery is implemented. Therefore, if reverse battery occurs in this configuration, MOSFET destruction may occur because of power dissipated with the inverse current in the MOSFET body diode.*

1.5.1 Common drain in reverse battery

The following figure describes the current leaking through the driver, in reverse battery at - 36 V, in common drain configuration. Refer to diodes block diagram, Chapter 1 in datasheet [1].

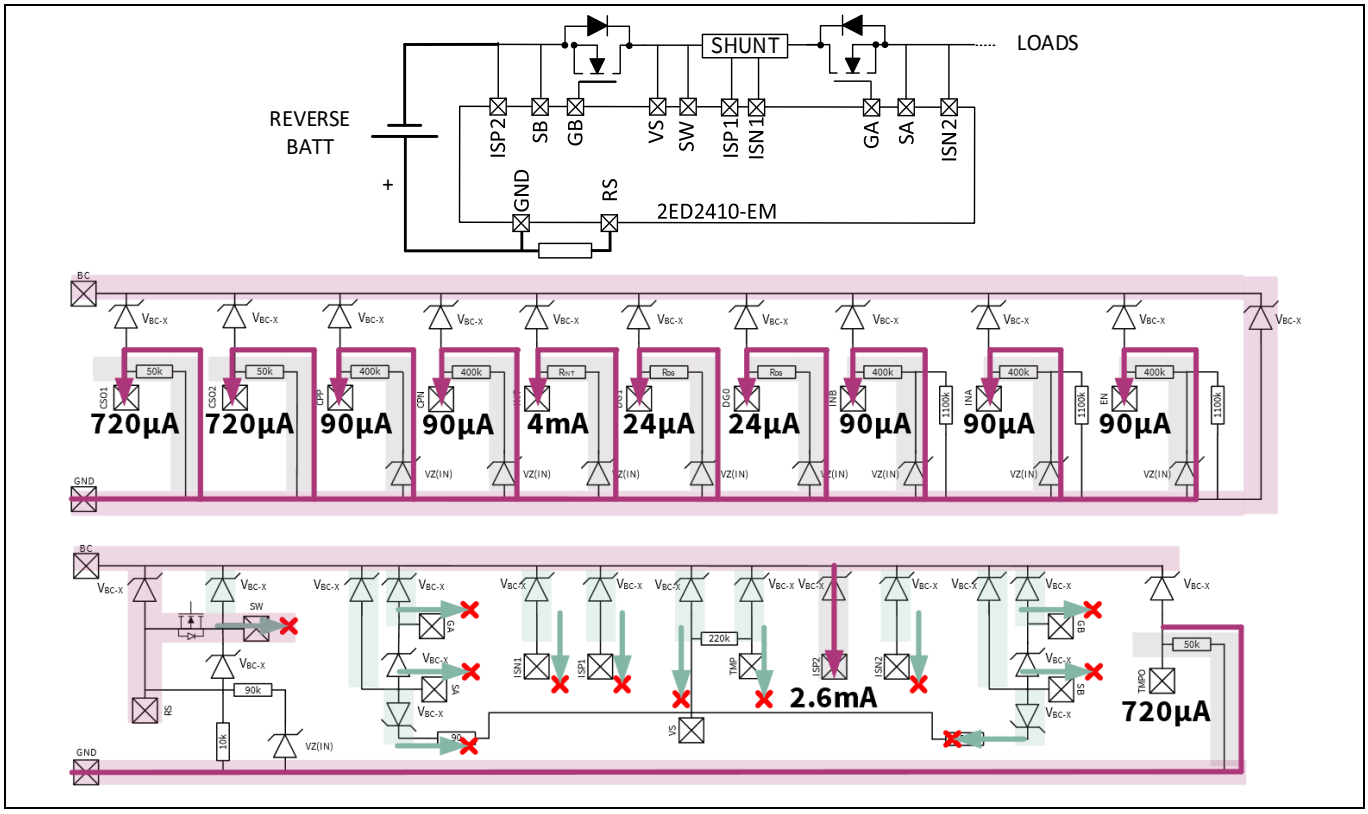


Figure 7 2ED2410-EM diodes diagram with typical leakages at -36 V in common drain configuration

Due to the common drain structure, there is no current flowing back from load to battery. A 2-minute test was conducted with reverse battery at -58 V, as can be seen in the figure below.

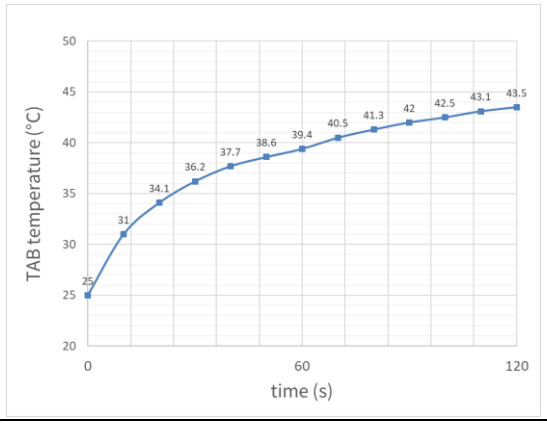


Figure 8 Driver TAB temperature under -58 V reverse battery

1.5.2 Common source in reverse battery

The following figure describes the current leaking through the driver, in reverse battery at -36 V, in common source configuration. Refer to diodes block diagram, Chapter 1 in datasheet [1].

Due to the common source structure, current flows back from GND to battery mainly through RS to SW, the current being limited only by R_{RS} resistor. As a result, K1 MOSFET is likely to be destroyed because of the power dissipated in its body diode.

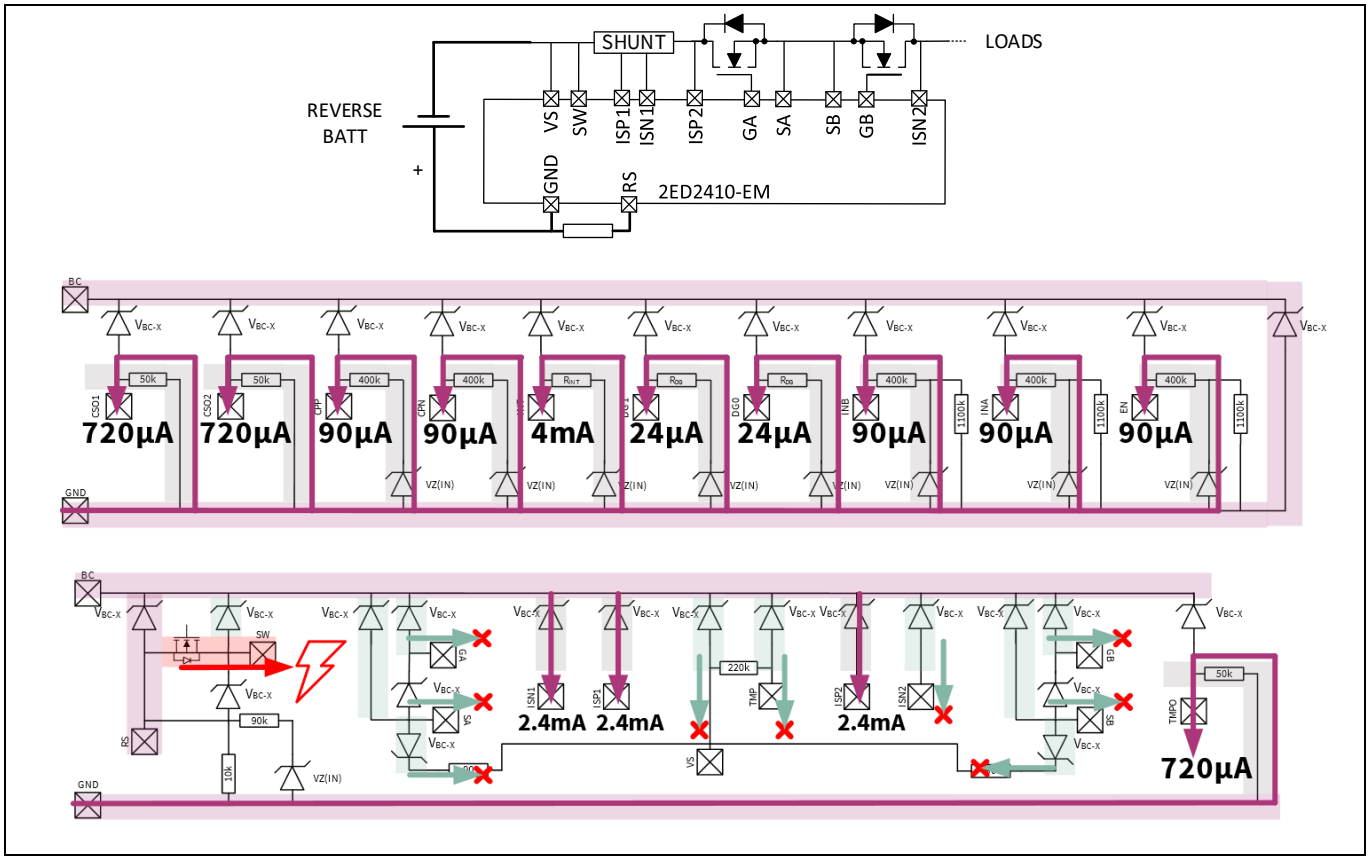


Figure 9 2ED2410-EM diodes diagram with typical leakages at -36 V in common drain configuration

A diode must be used on SW in order to prevent inverse current during reverse battery.

This diode needs to have a rating sufficient, to handle 200 mA, as per 2ED2410-EM driver datasheet [1], PRQ-16. Ideally, the voltage drop across this diode is as small as possible for example, a 0.3 V Schottky diode. The breakdown should be able to handle the expected worst case of reverse battery voltage where 100 V is recommended.

Note: The diode on VS reduces short-circuit performance in case of terminal short-circuit, e.g. VS < 3 V

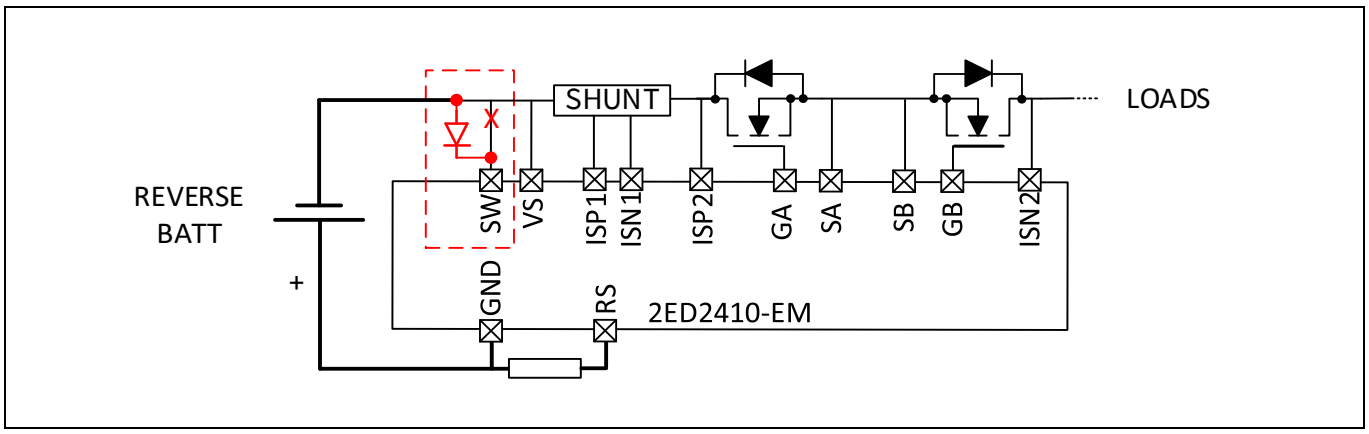


Figure 10 Handling reverse battery and bi-directional switch with common source configuration

Note: This protection for common source in reverse battery is also valid for single high-side MOSFETs to protect the driver, even though the external MOSFET would not be protected.

2 What to do with non-used pins?

2ED2410-EM has several features and possibilities. After setting up the basics for driver operation, all functions may not be needed. Therefore, the non-used features can be disabled to save some current consumption or simplify routing on PCB. Disabling the non-used feature, in the correct manner also ensures correct driver operation. The table below shows how to connect the pins in order to disable the corresponding features.

Table 1 Connection of non-used pins

Pin #	Pin name	Pin type	How to connect pin to disable corresponding function
1	CSO1	I/O	GND (FLOAT can trigger random latch on CSO1 internal comparator)
2	CSO2	O	GND
3	CPP	I	GND (FLOAT can trigger random latch CPP)
4	CPN	I	EN (VS induces 'large' current consumption. GND can trigger random latch)
5	INT	O	FLOAT
6	DG1	O	FLOAT
7	DG0	O	FLOAT
8	INB	I	GND (FLOAT potential IBC increase, DPI sensitivity increased if SB GB floating, no IDLE mode)
9	INA	I	GND (FLOAT potential IBC increase, DPI sensitivity increased if SA GA floating, no IDLE mode)
10	EN	I	5V (@GND driver will always remain in SLEEP mode. EN can also be connected to VS with 100k+diode so driver is by default in IDLE mode as long as a power supply is connected > Vzener+Vrev_diode is present on VS pin. diode: cathode on VS.)
11	GND	I/O	GND (never leave open: can randomly activate boost converter, IC destruction)
12	RS	O	FLOAT (when using external supply directly on BC, RS connection to GND could cause IC destruction)
13	SW	I	FLOAT (in case of boost supply converter disconnection and driver external supply directly on BC)
14	SA	O	FLOAT (if GA not used)
15	GA	I/O	FLOAT
16	ISN1	I	GND/VS
17	ISP1	I	VS/GND
18	VS	I/O	VS (FLOAT: BC is not regulated, external MOSFET gate destruction expected)
19	TMP	I	FLOAT
20	ISP2	I	GND/VS
21	ISN2	I	VS/GND
22	GB	I/O	FLOAT
23	SB	O	FLOAT (if GB not used)
24	TMPO	O	FLOAT or GND
TAB	BC	O	Boost capacitor C_{BC} or external supply (see datasheet for V_{BC}-V_S functional range [PRQ-339]).

3 Enhanced functions and optional external components

Attention: ***The electrical diagrams in this chapter are circuit propositions that need optimization and verification by the customer in the real application. The objective is to show the possibilities offered by the 2ED2410-EM driver. Other circuits may achieve the same goals.***

3.1 Simple pre-charge circuit

In this paragraph, a simple circuit and its control options are discussed. The goal is to enable pre-charging of board net circuit capacitances while making the best out of the 2ED2410-EM driver. The ability to pre-charge is mandatory in primary power distribution.

2ED2410-EM Driver uses a boost converter as a supply and can be seen in Chapter 1. Therefore, this supply can be reused with a level shifter to drive a bypass circuit, including a current-limiter power-resistor, so that capacitances will be charged with a limited current. In this way 2ED2410-EM protections will not be triggered due to the current inrush at turn-on.

Three options are proposed for operating the pre-charge circuit and described in the example of power supply protection switch (PSP) below. More are possible and this list aims to give an outlook on the possibilities with 2ED2410-EM driver.

1. First option uses another GPIO from the controller to drive the pre-charge on demand.
2. Second option ties the pre-charge circuit to EN pin, as soon as the driver enters IDLE mode, pre-charge will be enabled as well. Therefore, depending on EN pin type of connection (see Chapter 3.2), pre-charge could be enabled without microcontroller. It also has the advantage of saving one GPIO.
   In IDLE mode, it is possible to monitor the pre-charge status with DG0. DG0 monitors if SA node voltage is within $V_{DS\_DIAG(TH)}$ range from VS voltage (see Datasheet [1], Chapter 7.1).
3. Third option sets the driver in ON mode. It also saves one GPIO compared to option 1. It has the advantage of setting MOSFET B on, so that there is no power dissipation in the body diode of MOSFET B compared to option 2. Additionally, protections from the driver are operational (including I-t wire protection) and measurements such as current sense can be used to check the pre-charge operation.

Note: *PSP in the example below, features I-t wire protection, common drain configuration, MOSFET tab temperature measurement. Many MOSFETs can be used in parallel on each gate output because of strong gate drive (Datasheet [1], Chapter. 4.3).*

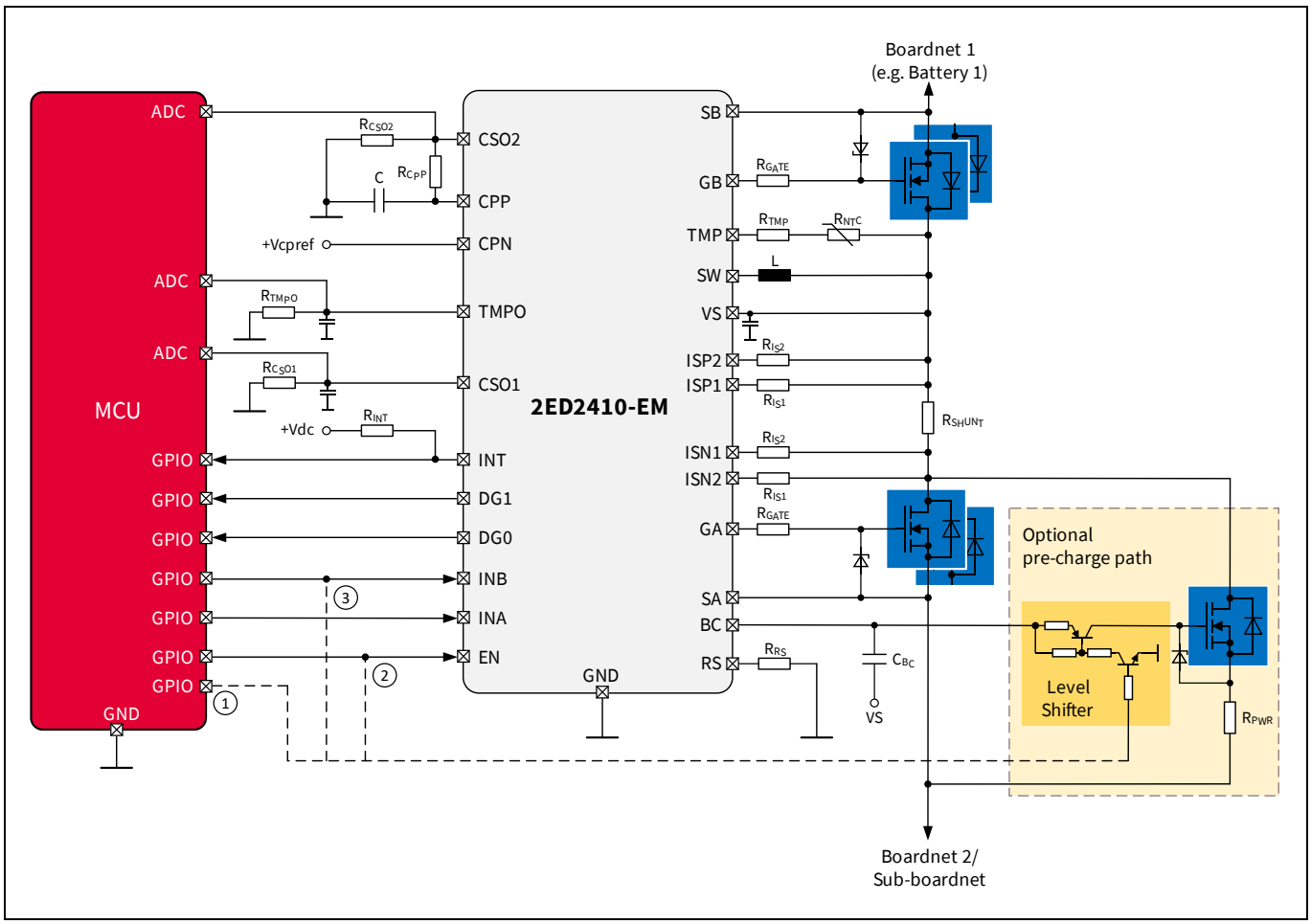


Figure 11 Power supply protection (PSP) switch example, with pre-charge circuit and its different control options

Note: Infineon enhanced BSS83P PMOS and 2N7002 NMOS can replace PNP and NPN in the level shifter.

Note: Gate-source resistor is needed for the pre-charge MOSFET to keep it off when PNP (or PMOS) is open. Gate-source resistors are not needed for power MOSFET in the main current path because the driver has an integrated gate-source pull-down by default as long as a VS voltage is present.

The figure below is another example that features a single high-side switch and makes use of the second gate driver output to drive the pre-charge.

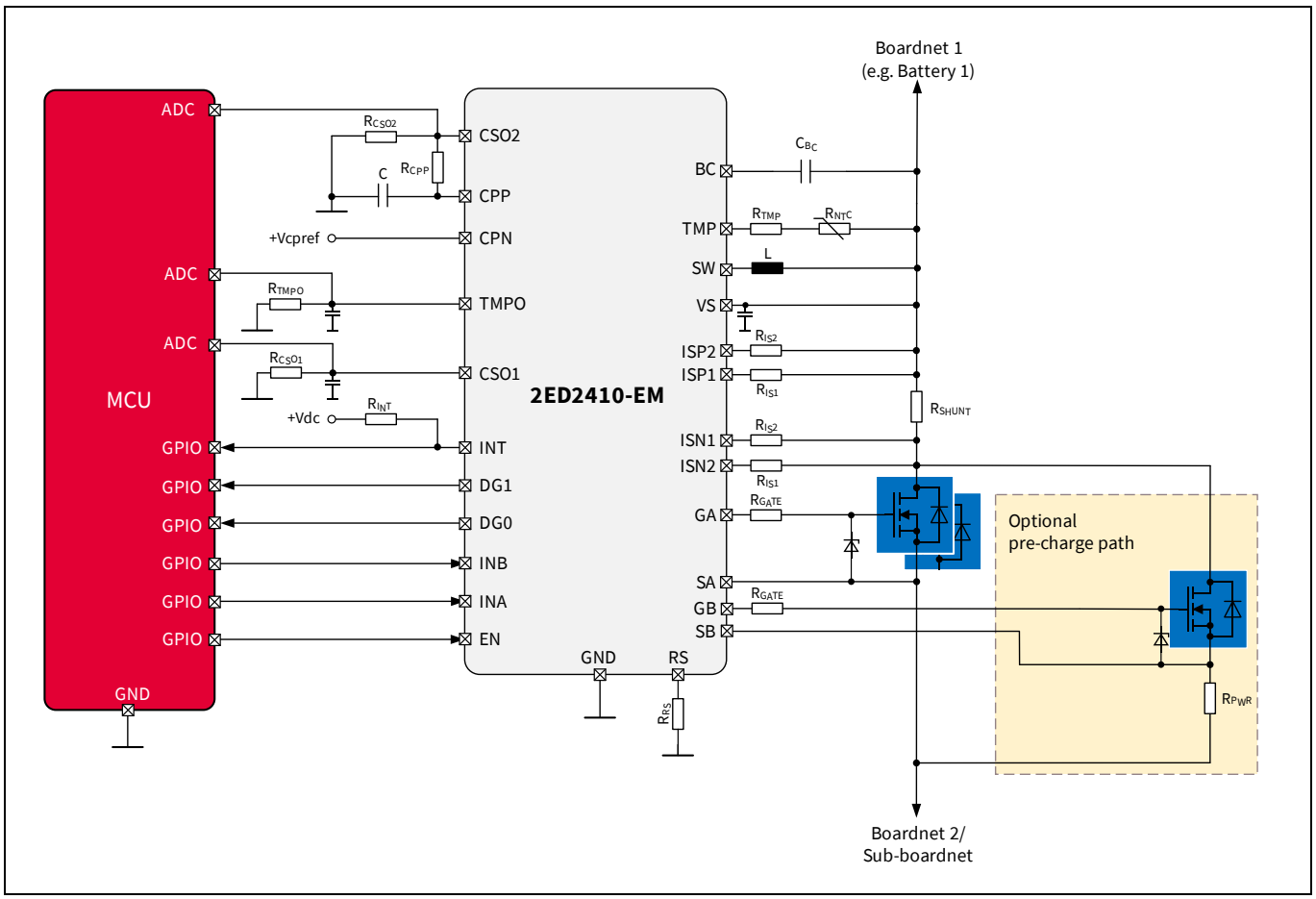


Figure 12 Power supply protection (PSP) switch example where inverse current blocking is not needed, with pre-charge circuit

3.2 IDLE as default mode (undervoltage auto-restart)

In automotive power distribution, it can be mandatory for the switch to auto-restart in case of micro-cuts on the power supply. A simple way to do so with 2ED2410-EM is to link the EN pin to VS with a very high-ohmic resistor and use a Zener between EN and GND to fix the EN pin voltage to any custom value that suits the application. As a result, the driver is in IDLE mode by default.

In order for the driver to be reset externally, a simple small signal NMOS can be used to pull-down EN pin voltage.

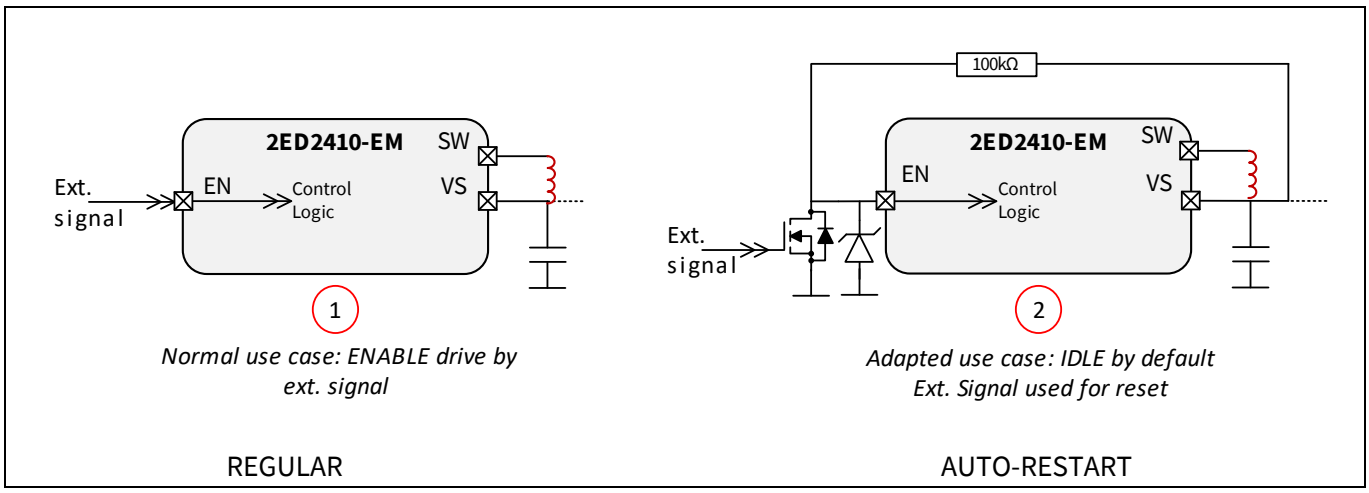


Figure 13 Schematic from datasheet, improved. Regular and UV auto-restart configuration

In case of undervoltage, if VS < 0.7 V, EN will reset if it goes to SAFESTATE. In configuration 2, the driver will go to SAFESTATE because of C_{BC} discharge (when VS is close to 0 V, the boost converter cannot maintain C_{BC} charged. C_{BC} discharges and as a result the driver would enter SAFESTATE because of gate UVLO.
See Datasheet for more details on UVLO feature [1].

Note: If the expected voltage drops on V_S is ≥ 3 V, there is no need for the auto-restart configuration, because the driver will keep operating in ON mode normally. Only the current sense amplifiers outputs would be affected by desaturation, and as a result a lower short-circuit limit during the drop. see Datasheet [1] Chapter 8.1, Figure 23 & 24

The auto-restart and regular 2ED2410-EM configurations were tested against well-known ISO16750-2-4.6.2 standard reset behavior down to 0 V voltage drop.
The two tables below show the functional status expected from the ISO16750-2 and the actual status observed during the test in each configuration. Refer to ISO16750-2 for the functional status definition.

Table 2 ISO16750-2 results in regular configuration - 3.3 µF capacitor between VS and GND

t1	Functional status expected	Functional status observed
>10 µs to 100 µs - int = 10 µs	A	A
100 µs to 1 ms - int = 100 µs	C	D
1 ms to 10 ms - int = 1 ms	C	D
10 ms to 100 ms - int = 10 ms	C	D
100 ms to 2 s - int = 100 ms	C	D

Table 3 ISO16750-2 results in auto-restart configuration -3.3 µF capacitor between VS and GND

t1	Functional status expected	Functional status observed
>10 µs to 100 µs - int = 10 µs	A	A
100 µs to 1 ms - int = 100 µs	C	C
1 ms to 10 ms - int = 1 ms	C	C
10 ms to 100 ms - int = 10 ms	C	C
100 ms to 2 s - int = 100 ms	C	C

4 Sensing interfaces

Please note that wire protection is not covered in this application note and is described in a separate application note.

4.1 Current sense amplifier set-up

This chapter gives details for calculations on how to set-up a correct short-circuit limit. The sensing element, here a shunt resistor, is assumed already chosen by the customer based on application thermal requirements. The EN pin voltage is either fixed by the low voltage power supply or the microcontroller. To set-up the correct protection threshold and consistent current reading, R_{ISP}, R_{ISN} and R_{CSO} need to be determined according the customer target.

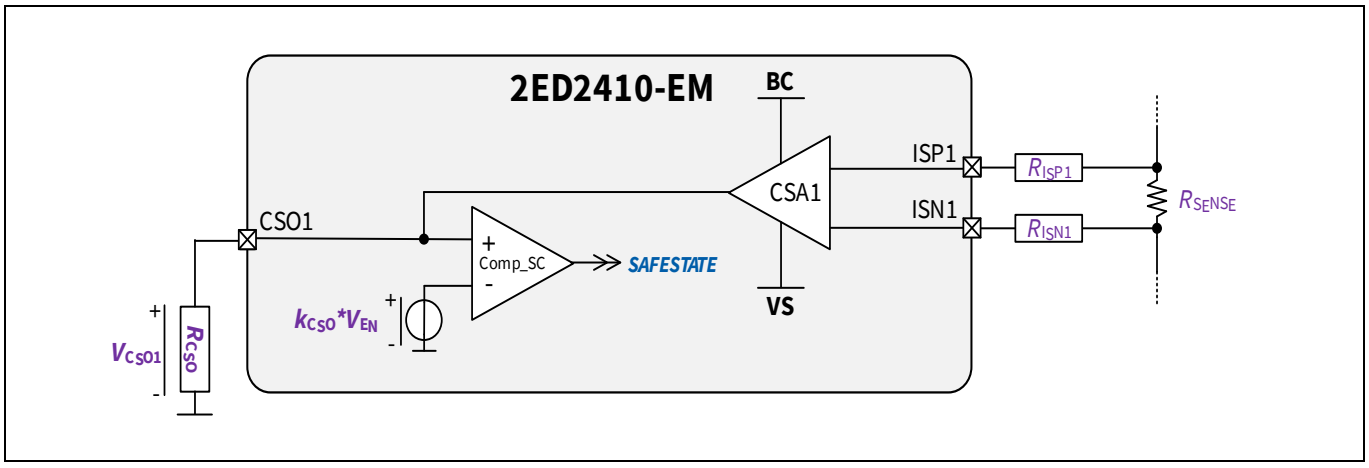


Figure 14 Overview of bi-directional current sense amplifier CSA1

Note: CSA2 is identical, but does not feature comparator on output for protection.

Target: Set a short circuit protection at I_{SC} = 200 A, with shunt resistor R_{SENSE} = 200 µΩ, V_{EN} = 3.3 V

Calculation steps:

- Compute the voltage drop across the sensing element at the desired short-circuit limit:
  $V_{SENSE(SC=200A)} = R_{SENSE} * I_{SC} = 200 * 2e\text{-}4 = 40$ mV
- Compute the threshold detection voltage of CSO1 comparator that needs to be matched by $V_{SENSE(SC=200A)}$:
  $V_{CSO(TH)} = k_{CSO(TH)} * V_{EN} = 0.74 * 3.3 = 2.44$ V
- Compute the gain needed for matching $V_{SENSE(SC=200A)}$ and $V_{CSO(TH)}$:
  $G_{CSO} = V_{CSO(TH)}/V_{SENSE} = 2.44$ V/0.04 V = 61 V/V
- Once the gain is computed, resistors setting the gain need to be selected. For example, amplifier output resistor R_{CSO} is chosen typical at 20 kΩ [PRQ-326]
- Therefore, the amplifier inputs resistors can be computed by:
  $R_{ISP/ISN} = R_{CSO}/G_{CSO} = 20000 / 61 = 327$ Ω

Using the values {R_{CSO}, $R_{ISP/ISN}$} = {20 kΩ; 327 Ω} with a R_{SENSE} = 200 µΩ shunt will provide a turn-off managed by 2ED2410-EM enabled at V_{EN} = 3.3 V when the current reaches 200 A.

The automated calculations can be found in the workbook [2], tab “Protection profile set-up”.

Note: *The current sense amplifier CSA2 does not feature an internal comparator on its output for protection. Therefore, the gain can be set freely according to customer needs. The gain of amplifier CSA2 does not need to be equal to the gain of amplifier CSA1.*

Note: *The current sense amplifiers in 2ED2410-EM drivers are based on operational transconductance amplifier theory, as they convert a differential voltage input into a current. The current is then converted to a voltage because of the R_{CSO} resistor.*

4.1.1 Current sense error

The 2ED2410-EM driver's current sense has a very low offset [PRQ-323]. Therefore, in order to get the lowest error possible, at least 1% resistors are recommended for R_{SENSE}, $R_{ISP/ISN}$, R_{CSO}.

The typical error between V_{SENSE} and V_{CSO1} is shown in the next figure based on V_{SENSE} values. This figure is an average based on a limited number of productive samples based on lab test conditions.

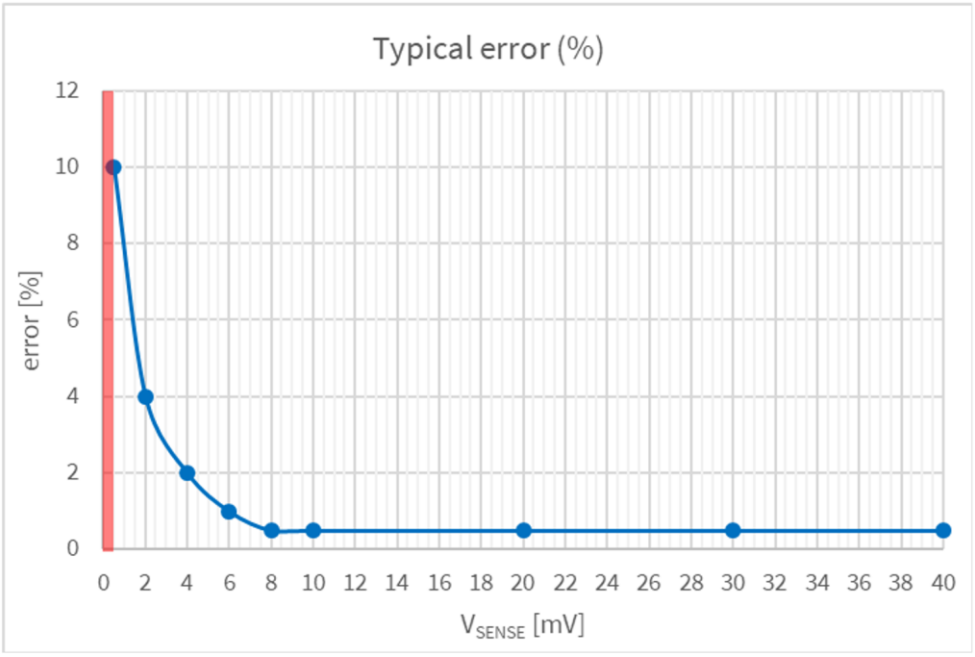


Figure 15 **Typical CSA error at 25°C, VS = 12 V** (in red: blind zone, see Chapter 4.1.3)

Note: *The current sense amplifier input is not limited to 40 mV. 400 mV is also possible. The limitation, if any, would be the combination of the chosen R_{SENSE}, the gain range of 2ED2410-EM [PRQ-317] and the amplifier output saturation, [PRQ-310]*

4.1.2 Minimum readable current

The table below show the minimum readable current by the current sense amplifier, based on typical shunt/sense resistor values and the driver blind zone (in red in the above figure). The minimum readable current can be read with 10% accuracy typically, according to Figure 15, above.

The table below also examines how useful it is to split the shunt resistor into two bigger values in order to achieve a higher nominal current, while observing the "1 W" thumb rule per element for thermal power dissipation.

Note: The blind zone of the current sense amplifier is explained in the next chapter

Table 4 Minimum readable current and typical nominal current based on shunt value and shunt arrangement

Total R_{SENSE} resistor value [Ω]	Minimum readable current |A|	Number and arrangement of shunt/sense resistors		Typical nominal current [A]	Power dissipated in each shunt [W]	2ED2410 Blind zone max. |µV|
0.001	0.5	1	1 * 1mΩ	30	0.90	500
0.0005	1	1	1 * 0.5mΩ	40	0.80	500
0.0005	1	2	2 * 0.5mΩ	60	0.90	500
0.0003	1.7	1	1 * 0.3mΩ	55	0.91	500
0.00025	2.0	2	2 * 0.5mΩ	85	0.90	500
0.0002	2.5	1	1 * 0.2mΩ	70	0.98	500
0.00015	3.3	2	2 * 0.3mΩ	110	0.91	500
0.0001	5	1	1 * 0.1mΩ	100	1.00	500
0.0001	5	2	2 * 0.2mΩ	140	0.98	500
0.00005	10	1	1 * 0.05mΩ	140	0.98	500
0.00005	10	2	2 * 0.1mΩ	200	1.00	500

4.1.3 Current sense blind zone

The minimum current reading depends on the R_{SENSE} used. See table Table 4 in previous chapter. Below this minimum reading of the differential input, the current sense amplifiers cannot read the current accurately. In addition, the current direction information bit from DG1 in ON mode signals an open load condition only for CSA1.

The blind zone is noted in the datasheet [1] V_{BLIND} [PRQ-324]. This is unique to 2ED2410-EM product because in order to maximize accuracy across the reading range, the driver outputs from 0 V to $V_{AMP(SAT)}$ [PRQ-310].

The next figures illustrate the DG1 pin behavior in blind zone, which can be observed during slow current ramps of 7.6 µA/µs and 0.5 mA/µs.

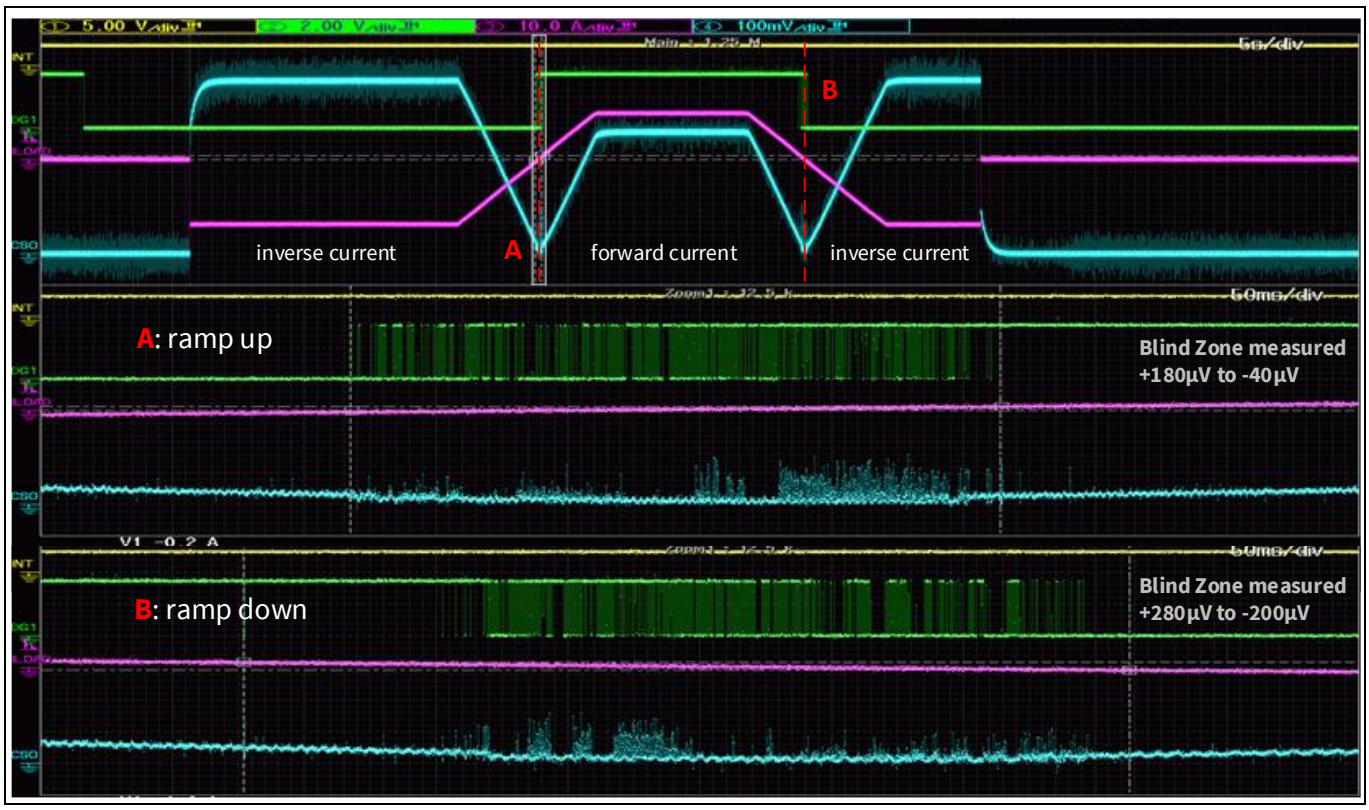


Figure 16 **DG1 behavior in blind zone with slow ramp 7.6 µA/µs**

V_S = 24 V, V_{EN} = 3.3 V, G = 100, R_{SENSE} = 200 µΩ [Yellow V_{INT}; Green V_{DG1}; Purple I_{LOAD}; Blue V_{CSO1}]

Figure 17 **DG1 behavior in blind zone with slow ramp 0.5mA/µs.**

V_S = 24 V, V_{EN} = 3.3 V, G = 100, R_{SENSE} = 200 µΩ [Yellow V_{INT}; Green V_{DG1}; Purple I_{LOAD}; Blue V_{CSO1}]

If the current ramp is faster, for example, 10 mA/µs, the blind zone would not be seen on DG1. Delay t_{ISD} applies when the current direction changes.

When the current sense input is within the blind zone, the DG1 pin in ON mode outputs a frequency f_{DG1}:

(12) $$f_{DG1(OPENLOAD)} \leq \frac{1}{t_{ISD}}$$

where t_{ISD} [PRQ-164] is the delay for DG1 change according to current direction.

Note: *This behavior is also useful to detect an open load condition: the open load condition can then be easily detected by a microcontroller, e.g. counting rising or falling edges of DG1 signal over a defined period of time*

4.2 Temperature sense amplifier set-up

The main drawback of the "standard solution", is that it needs to use the V_{DD} of a microcontroller.

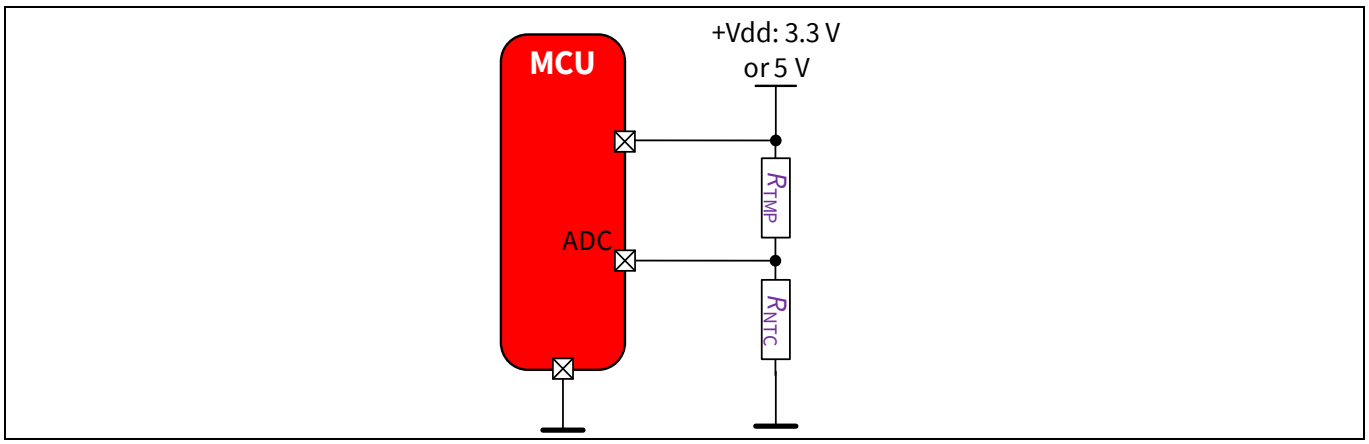


Figure 18 Basic temperature sense circuit

Therefore, it is complicated to route on layout the NTC (or another thermistor used) to the MOSFET TAB and back to the microcontroller. This basic circuit also draws additional consumption permanently; as long as V_{DD} is still on, meaning, it would need additional components to control it with a small NPN or NMOS to activate or deactivate it and therefore an additional µC GPIO used.

The purpose of 2ED2410-EM's temperature amplifier is to sense switch temperature which is the equivalent of MOSFET TAB temperature. The advantage of 2ED2410-EM solution is that the V_{DD} is replaced by the battery line voltage and therefore the thermistor being either PTC or NTC is in the upper position. Therefore, it is very easy to route the layout of the thermistor close to MOSFET TAB. See Chapter 6.2 for routing example.

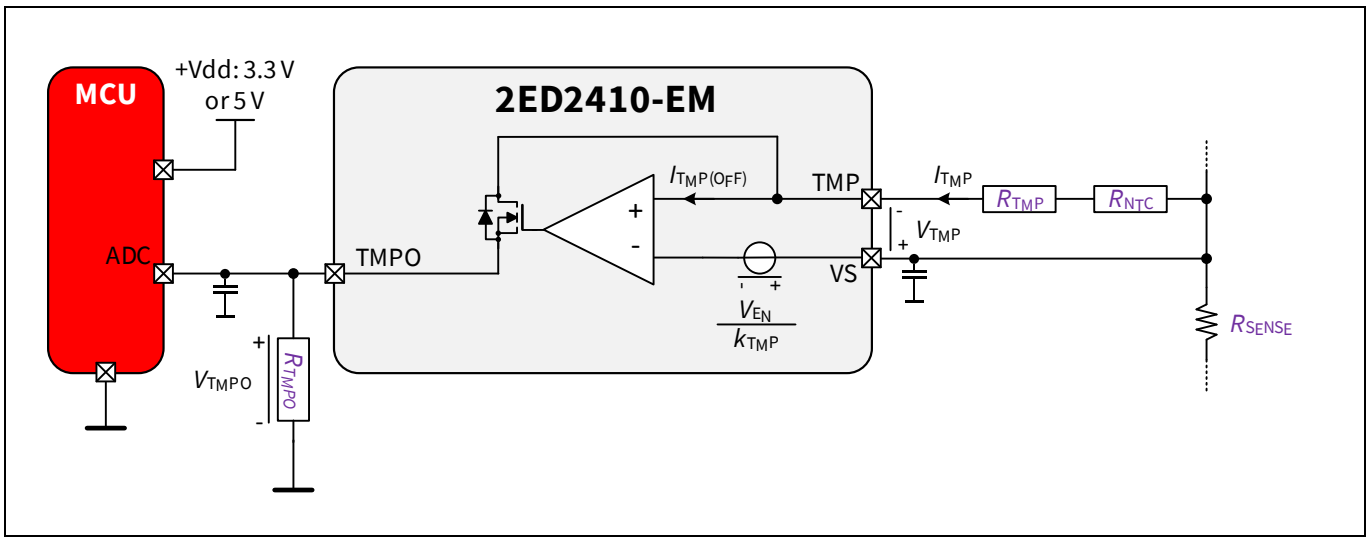


Figure 19 Overview of temperature amplifier sense TMPA

Other advantages are the following:

- The output of TMPA amplifier is independent of battery voltage, and varies according to the resistors' settings. Not the case with basic temperature sensing circuit shown in Figure 10
- The consumption of TMPA amplifier itself is low. In addition, this additional self-consumption current is not present in IDLE or SLEEP mode, because the amplifier is not activated in these modes
- The output can be linearized easily using R_{TMP} resistor. Therefore, temperature can be sensed accurately over a wide range for example from 0°C to 150°C. It can be verified with demoboard + a temperature sensor
- It is advised to use 10 nF on TMPO, see Chapter 0, DPI protections

4.2.1 TMPA target curve calculation example

TMPA is an amplifier of current. The current I_{TMP} is conserved through the temperature amplifier, which, by neglecting $I_{TMP(OFF)}$, can be written:

$$I_{TMP} = \frac{V_{TMP}}{(R_{NTC}+R_{TMP})} = \frac{V_{TMPO}}{R_{TMPO}} \quad (13)$$

In Equation (13), R_{NTC} is the thermistor (in this case an NTC thermistor) resistance which varies with the temperature, and R_{TMP} is a normal resistor used to linearize the thermistor behavior with respect to temperature, positioned as per Figure 11. Therefore, V_{TMPO} can be written as:

$$V_{TMPO} = \frac{V_{TMP} \times R_{TMPO}}{(R_{NTC}+R_{TMP})} \quad (14)$$

By replacing V_{TMP} from k_{TMP} [PRQ-187] (referring to the datasheet [1] equation (3) page 27), in Equation (14) here, also considering the input offset of TMPA [PRQ-186], it gives:

$$V_{TMPO} = \left(\frac{V_{EN}}{k_{TMP}} + V_{TMP(OFFSET)}\right) \times \frac{R_{TMPO}}{(R_{NTC}+R_{TMP})} \quad (15)$$

Computed for different temperature values, it allows to trace V_{TMPO} [V] = $f(T$ [°C]), depending on the law used to describe the temperature variation of the thermistor.

The example in the figure below, is given for V_{EN} = 3.3 V, an automotive qualified 47 kΩ NTC and R_{TMP} = 1.2 kΩ. The Equation (16) was used to compute $R_{NTC} = f(T\,[°C])$ (where T and $T(25°C)$ are expressed in Kelvin):

(16) $$R_{NTC} = R_{(T=25°C)} \times e^{\beta \times (\frac{1}{T} - \frac{1}{T(25°C)})}$$

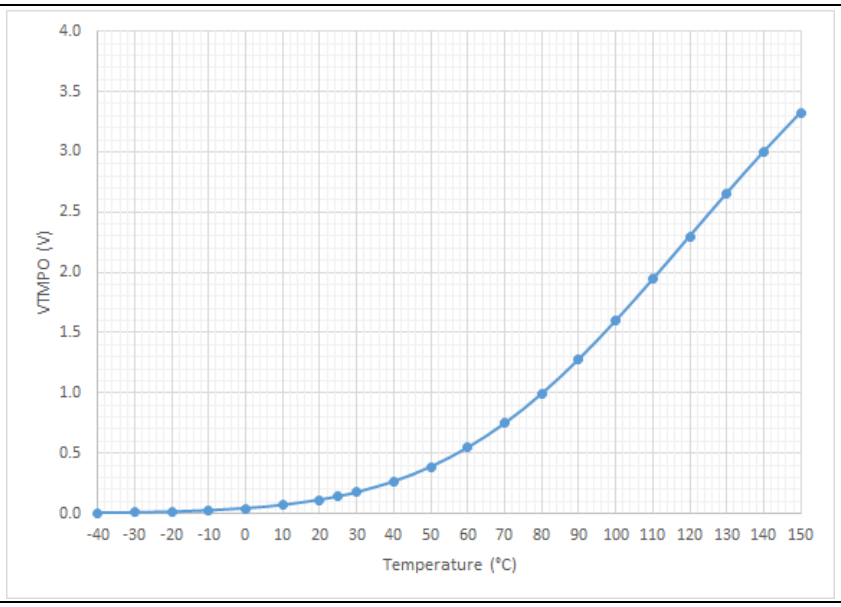


Figure 20 Example of curve V_{TMPO} [V] = $f(T\,[°C])$ for V_{EN} = 3.3 V

The automated calculations can be found in the workbook [2], tab “Temperature sense set-up”.

5 External parts for driver protection

5.1 Protecting the VS node

The 2ED2410-EM diode diagram shows us than the Zener diode between BC and GND is the critical path that should be protected against overvoltage in order to preserve the driver integrity.

- Due to the boost converter between BC and VS, the VS node must be protected against spikes greater than $V_{BC\text{-}GND}$-$V_{BC(TH)MAX}$, giving 75 V-14 V = 61 V

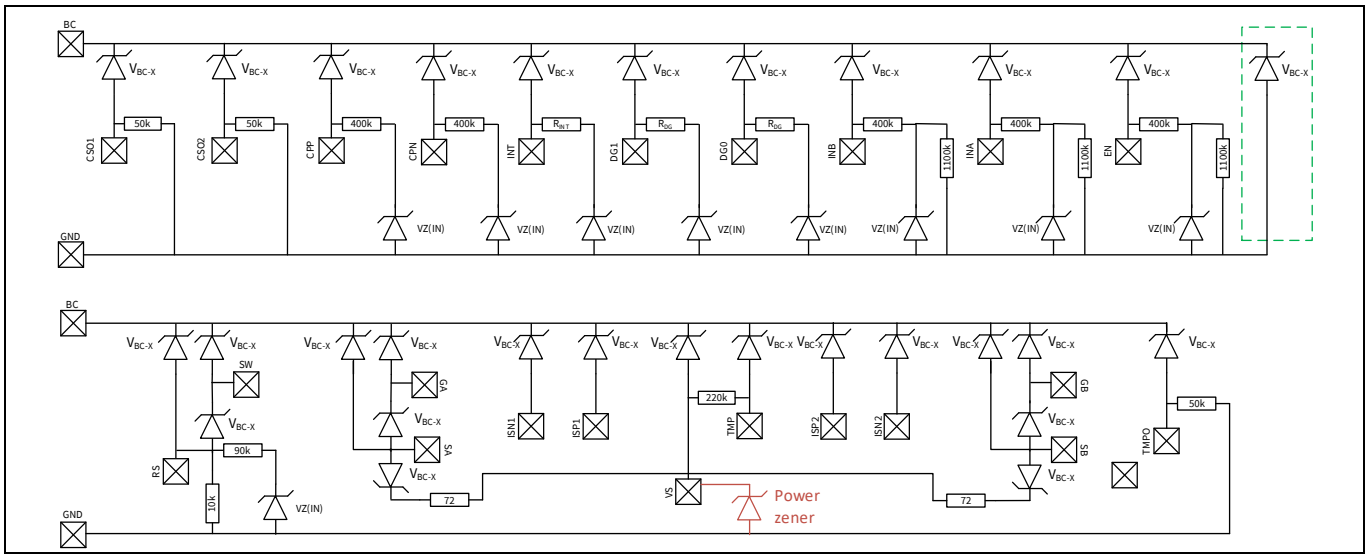


Figure 21 Diode diagram with BC-GND highlighted (green) and optional power diode (red)

- 1 W to 5 W power Zener is advised, when using MOSFET with a breakdown voltage equal or greater than 60 V. For example, this protection diode is not needed when using 40 V MOSFET, because the breakdown voltage of a 40 V MOSFET is below 61 V

5.2 ISO7637 transient pulses

Note: This section does not give a list of mandatory components that must be used in the application. It gives a list of possible solutions that can improve 2ED2410-EM behavior during EMC tests.

Table 5 ISO7637 transient pulses counter-measures

Pin connection	Purpose	Counter-measure	PCB layout recommendation	Criticality
VS-GND	ISO7637 pulse 3b	C_{VS} = 3.3 µF/ 100 V min.	According to Chapter 6.2. Zener in Chapter 6.1 can replace C_{VS}	recommended

5.3 DPI protections

Note: This section does not give a list of mandatory components that must be used in the application. It gives a list of possible solutions that can improve 2ED2410-EM behavior during EMC tests.

Table 6 DPI counter-measures

Pin connection	Purpose	Counter-measure	PCB layout recommendation	Criticality
SA-GND and SB-GND	DPI robustness	C_{SX} = 10 nF/50 V min. (12 V systems) or 100 V min. (24 V systems)	Between MOSFET source and GND plane (power)	optional
TMPO-GND	DPI robustness	$C_{TMPO-GND}$ = 10 nF/10 V min.	Between TMPO pin and GND	optional
ISPx-BC and ISNx-BC	DPI robustness	$C_{ISXX-BC}$ = 1 nF/25 V min.	As close as possible from driver for shortest path to BC	recommended
ISPx-BC and ISNx-BC	DPI robustness	$C_{ISXX-BC}$ = 1 nF/25 V min.	Located in between the split R_{ISXX} resistance	recommended
CSOx-GND	dV/dt robustness	$C_{CSOX-GND}$ = 220 pF/15 V min.	As close as possible to driver pin. A greater value would delay short-circuit reaction time	recommended

Note: Details of 2ED2410-EM EMC tests can be delivered on-demand.

In the figure below, two variations for implementation of the $C_{ISXX-BC}$ resistor are shown. At minima, configuration (a) should be observed for CSA1 and configuration (b) is recommended for noisy environments.

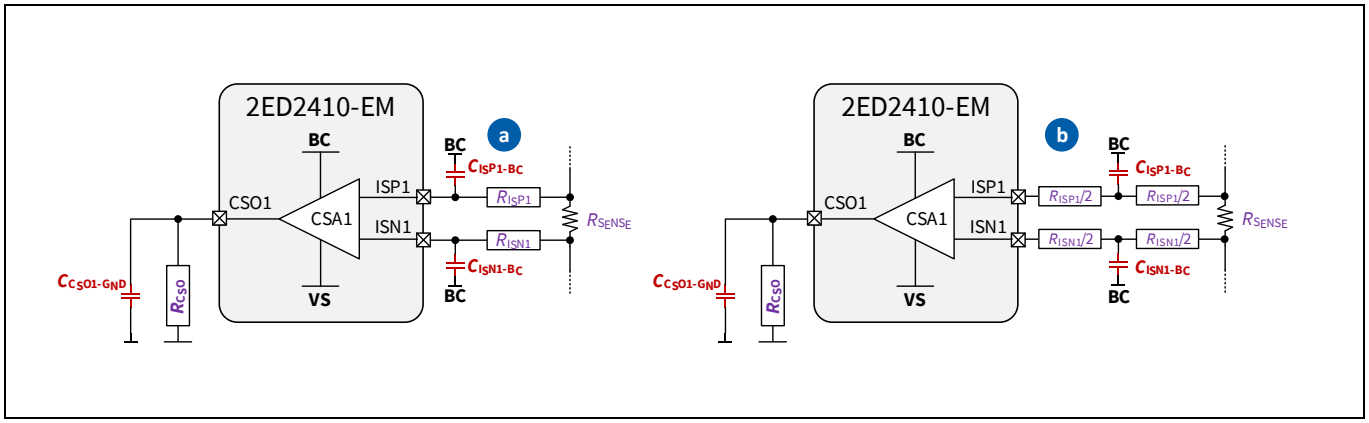


Figure 22 DPI recommendation minimal (a) and optimal (b) applied in this example to CSA1

5.4 ESD components and layout recommendation

Note: This section does not give a list of mandatory components that must be used in the application. It gives a list of possible solutions that can fix a behavior, based on experiments and experience of the Infineon application and design team with gate drivers.

For ESD automotive qualification, at device level, there are no additional components used. The bare driver passed the qualification HBM AEC-Q100 as specified in the datasheet [1] in PRQ-130.

For ESD module level ESD tests, options as depicted in the table below are available if the driver in typical application does not comply with customer end test at module level.

Table 7 ESD counter measures

Pin connection	Purpose	Counter-measure	PCB layout recommendation	Criticality
GND	Improve BC-GND Zener diode robustness	R_{GND} = 50 -100 Ω	PCB trace as short as possible (to limit stray inductance) to GND PCB plane (analog). See Ch. 6.4. This component is optional.	optional
VS-GND	Improve module ESD robustness, dV/dt filtering	C_{VS} = 1-470 nF/50 V min. (12 V systems) or 100 V min. (24 V systems)	PCB trace as short as possible (to limit stray inductance) to GND PCB plane (power). See capacitor C2 in Figure 24.	Mandatory (100 nF typical value from datasheet [1] front page)

6 PCB layout recommendations

Attention: ***The PCB traces examples in this chapter are proposed layout solutions and are not mandatory. Those propositions are standard and final implementation depends on customer layer stack and must be verified by the customer in the real application. Other layouts may achieve the same goals.***

6.1 SW, BC and RS pin routing

In this sub-chapter a non-exhaustive list of advice in order to route the 2ED2410-EM amplifiers on the PCB in the correct manner, is given.

- SW is the main supply of the driver (input of boost converter, see datasheet [1] Chapter 9). The maximum current peak is 200 mA (driver max. ratings, see datasheet [1] Chapter 3 PRQ-16), therefore standard trace length on standard thickness is sufficient (35 µm, 0.254 mm/10 mil) for power dissipation considerations. However, in order to optimize boost converter efficiency, parasitic resistance of the trace must be kept to minimum.

Note: *The SW pin must be routed separately from current senses and temperature senses strips, because the pulses in the range of hundreds of mA would highly disturb current sense reading and may cause unintended SAFESTATE trigger in some situations. Only VS could be routed together from the main power line.*

Table 8 SW pin routing

Optimization	Power/Thermal reasons	Parasitic resistance	Parasitic capacitance
Width	According to PRQ-16 datasheet [1]. Standard width trace is generally sufficient	Augment width based on PCB thickness. Ideally, $(R_L + R_{TRACE}) < 3\Omega$	Reduce width based on distance between top layer strip and embedded plane
Inductance choice	No specific adjustment	Choose an inductor with a parasitic resistor as small as possible. Ideally, $(R_L + R_{TRACE}) < 3\Omega$	As close as possible to SW-pin (<10 mm) to limit parasitic capacitance (<10 pF)

- If a diode is used in series with SW in order to block inverse current because of reverse battery situation, the diode voltage rating must be chosen greater than the driver maximum rating (75 V, see Absolute maximum ratings in datasheet [1]). A breakdown value of minimum 100 V is advised
- For BC tab, C_{BC} capacitor should be placed as close as possible from driver tab, ideally < 10 mm, to minimize stray inductance. Connection to VS must be direct with no capacitor to GND in between

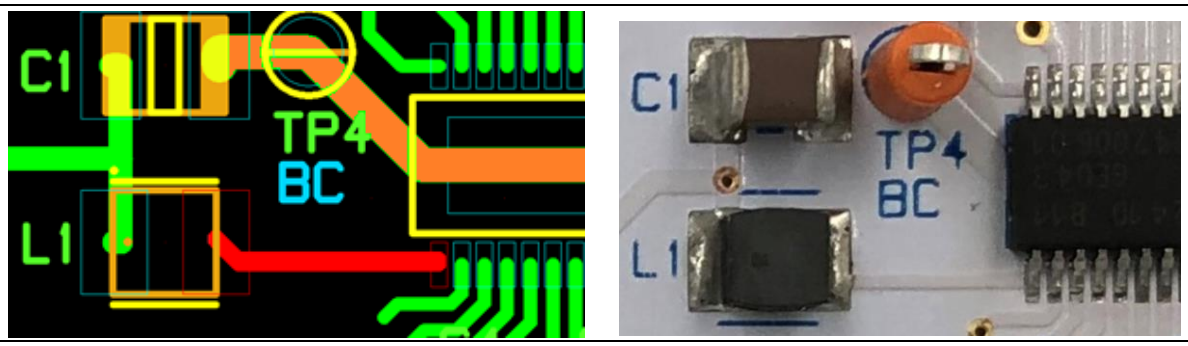


Figure 23 SW pin correct routing example (red) with VLS3015CX-101M-H and C_{BC} routing (orange)

- RS-pin is the output of the boost converter. Therefore, connection to GND through the RS resistor should also be as short as possible. See Chapter 5.4, same recommendation than GND-pin after RS resistor

6.2 VS node routing

For protection purposes (ESD, ISO7637 transient disturbances), it may be needed to use capacitors and/or a Zener diode on the VS pin depending on the conditions. See Chapter 5.1, Protecting the VS node.

However, it has to be noted that in order to supply the amplifiers correctly, the V_{BC}-V_S voltage must be kept stable [PRQ-339]. Therefore, any filtering on the VS pin should also apply to BC capacitor and *L* connection to VS node.

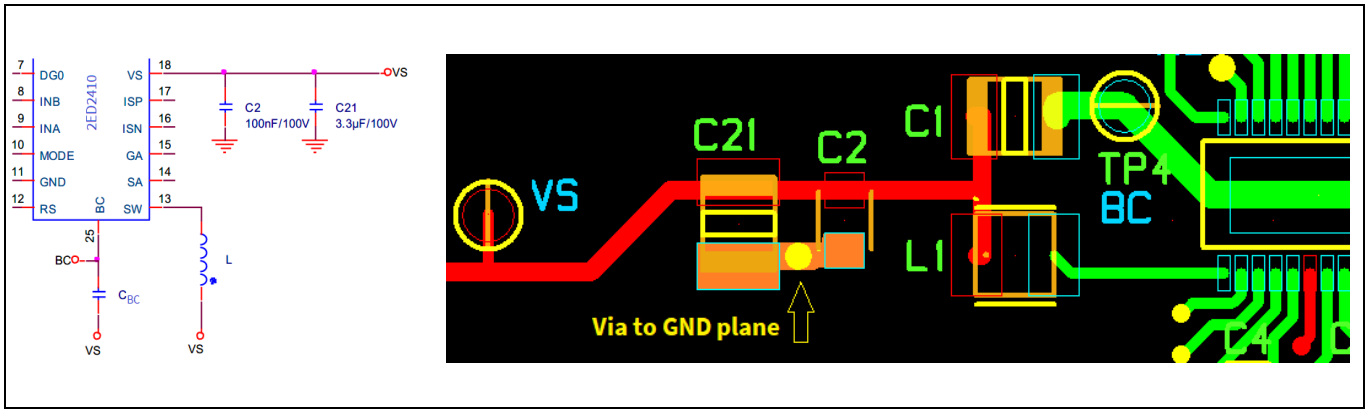


Figure 24 VS pin schematic and correct routing example (red) with filtering caps and GND (orange)

Because amplifiers are supplied between BC and VS, one of the two inputs of the amplifier ideally must be placed on the VS node for better amplifier performance.

6.3 Amplifiers routing

In this sub-chapter a non-exhaustive list of advice in order to route the 2ED2410-EM amplifiers on the PCB in the correct manner is given.

- Amplifiers are supplied between BC and VS. See datasheet [1] Chapter 7.2 for details. Therefore, it is not advised to use capacitors between the amplifiers input pins and GND
- Output amplifier resistor R_{CSOx} [PRQ-326] and amplifier gain *G* [PRQ-317] parameters must be respected in the application
- Input and output amplifiers resistors are advised at 1% accuracy or better and ideally close to the device
- Ideally the two input traces should be routed together. The parasitic resistance of the traces must not influence the desired gain in the application. Straight lines are advised to avoid any antenna/loop effects
- To optimize the noise on current reading, the input amplifiers resistors $R_{ISPx/Nx}$ have to be minimal, as parasitic noise increases with resistance
- Even if R_{ISPx} or R_{ISNx} is electrically on the same node as VS and L1 connection, they must be routed separately to avoid interference from VS and SW pin current, that could create a parasitic voltage drop across R_{ISPx} or R_{ISNx} (R6 or R7 in the diagram below) and therefore perturbate amplifier operation

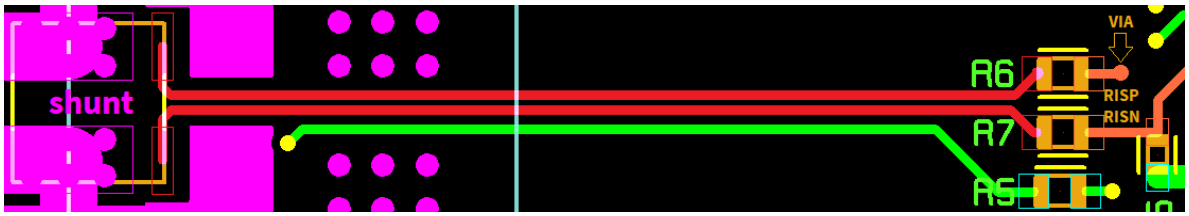


Figure 25 Example of amplifier correct routing from shunt resistor (red) and from input resistance to pins (orange)

Note: Vias can be copper-filled. In most cases, it can be assumed that their internal resistance does not impact the current sense accuracy, as it would be negligible in comparison to R_{ISXX} resistances.

6.4 GND pin

The GND pin trace should be as short as possible to a GND plane or to the GND connector. If a GND plane is used, located below the driver, it is good practice to separate signal GND from power GND (for example if a freewheeling diode is used on PCB where the 2ED2410-EM is located).

A small, optional, resistor (see Chapter 6.3) could be used on the GND pin to increase ESD module robustness or BCI robustness in case of failures, or for safety reasons (see 2ED2410-EM Safety Application Note). In this case, again, the path should be as shorter as possible.

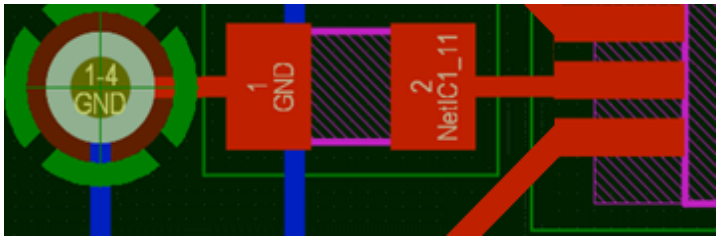


Figure 26 Example of GND correct routing with the optional additional resistor and connection to GND plane with standard via (green)

7 Quiescent current example

This chapter shows the formulas for computing quiescent current and shows real-life examples of consumption in 4 operating modes of the 2ED2410-EM driver.

- Power supply of driver is a boost DC-DC converter with integrated diode and switch (K1 MOSFET, see Figure 1)
- The quiescent current of 2ED2410-EM is then related to the efficiency of the boost converter and to the battery voltage
- The efficiency depends on the boost converter external components

For this reason, quiescent current is measured from the battery line rather than the ground connection of the device.

- Due to the variety of choices of external components, Infineon cannot commit on a specific quiescent current value from battery
- Infineon can only commit to the driver consumption itself, measured on pins BC and VS in production test and characterisation. See datasheet [1] Chapter 4.5 for the current consumption parameters

7.1 SLEEP mode

In SLEEP mode, the boost converter is not active. The quiescent current can be measured on GND+RS pin plus the source SA or SB pin depending on connection in application.

(17) $$I_{q(SLEEP)} = I_{GND+RS(SLEEP)} + I^{1)}_{SA(SLEEP)} + I^{1)}_{SB(SLEEP)}$$

1) To be considered only if SA or SB is below VS voltage

Figure 27 Current paths in SLEEP mode

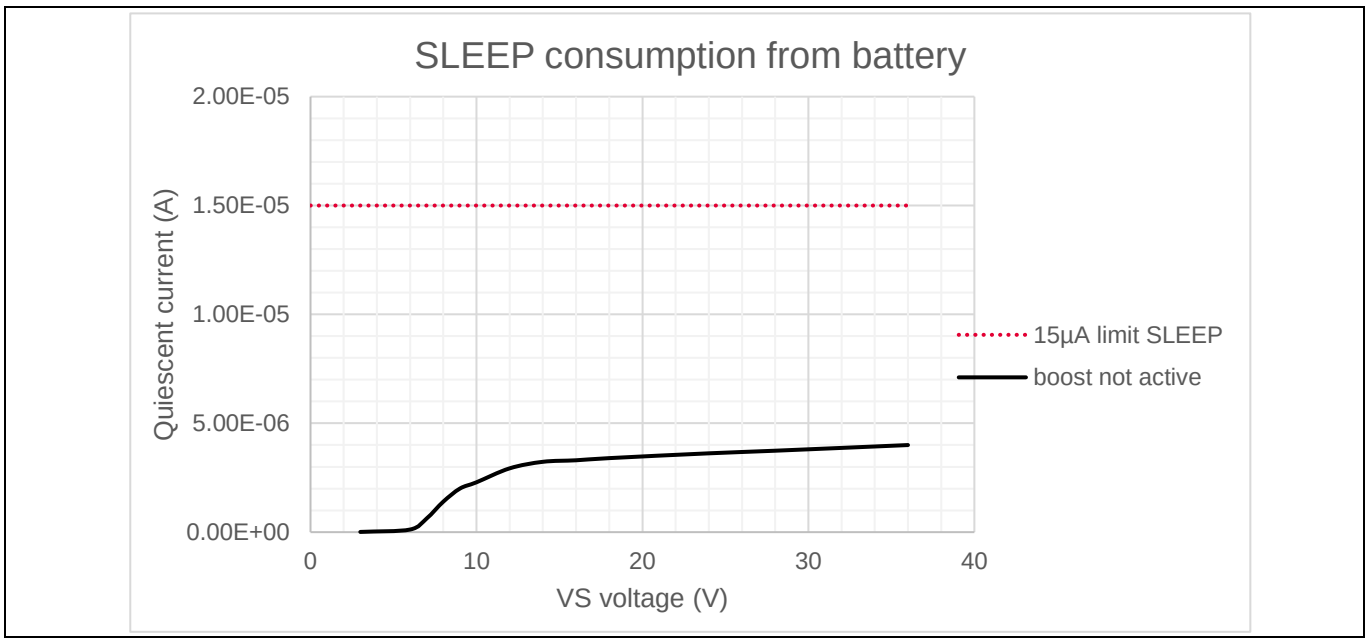


Figure 28 Quiescent current measurement of 2ED2140-EM in SLEEP mode @25°C (boost converter not active)

7.2 IDLE mode

In IDLE mode, the boost converter is active. However, amplifiers and comparators, main contributors to current consumption, are not active. External MOSFETs are OFF.

(18) is the general efficiency equation applied to our boost converter:

(18) $$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_{BC} * V_{BC}}{\overline{I_{SW}} * V_S}$$

The current drawn from the battery in IDLE is the sum of the current pulled by the boost input (SW) and VS pin.

(19) $$I_{q(IDLE)} = I_{BAT} = \overline{I_{SW}} + I_{VS(IDLE)}$$

Combining (18) and (19) gives:

(20) $$I_{q(IDLE)} = \frac{I_{BC(IDLE)} * V_{BC}}{\eta * V_S} + I_{VS(IDLE)}$$

There is no easy way to compute efficiency; therefore, a tool will be provided at product release; in the meantime, excel calculation workbook can be used for estimation.

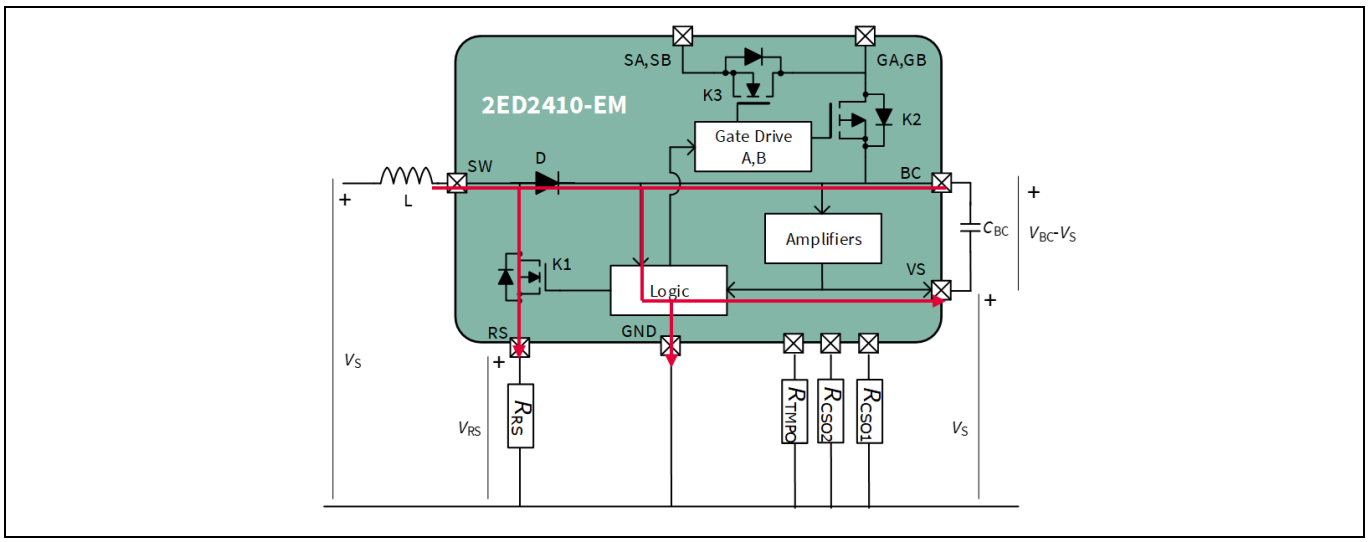


Figure 29 Current paths in IDLE mode

The graph below shows the correlation between theoretical calculation and measurement from evaluation board. It is measured in open load to avoid interference of the I_{SOURCE} function (see datasheet [1] Chapter 6).

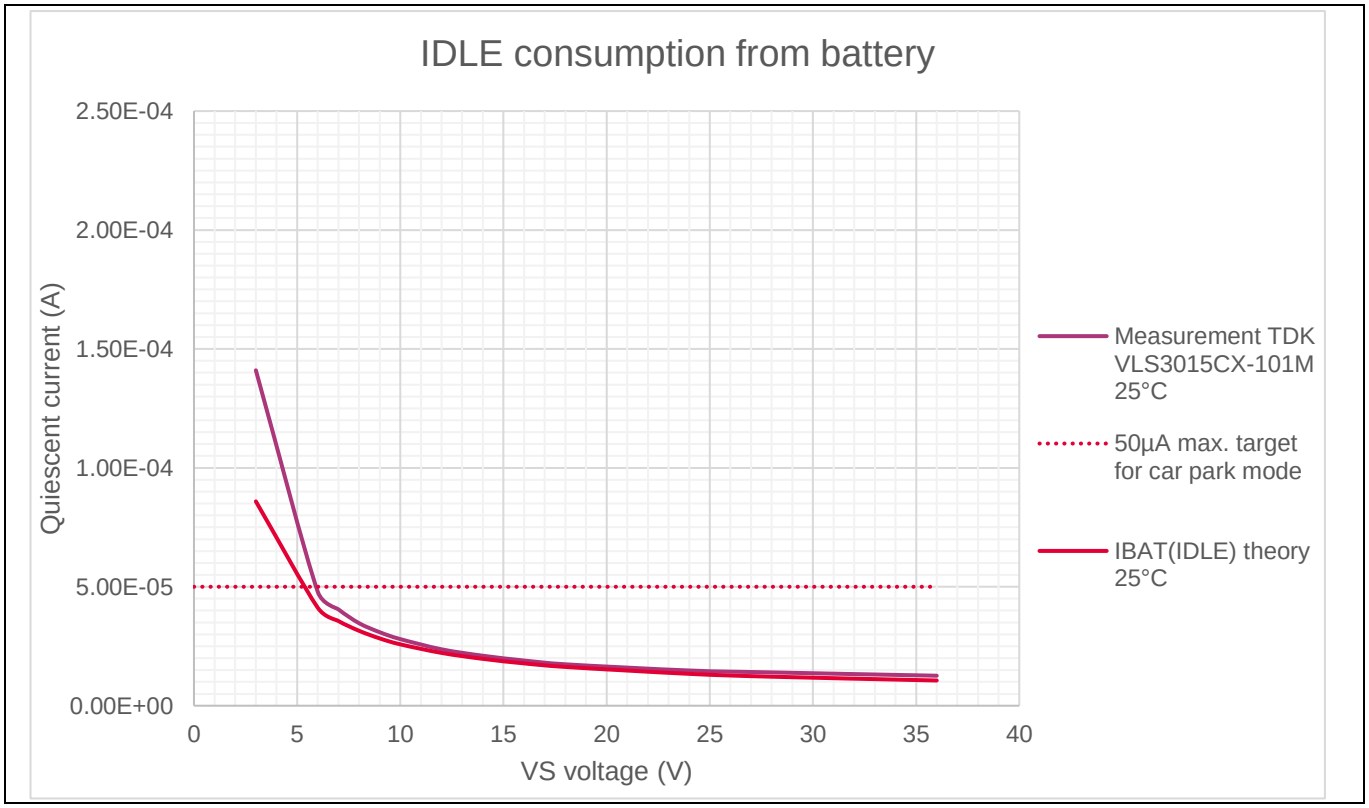


Figure 30 Quiescent current of 2ED2410-EM in IDLE mode @25°C, *open load*, using TDK VLS3015CX-101M-H and R_{RS}=10 Ω

7.3 ON/SAFESTATE mode

In ON and SAFESTATE mode, the boost converter is active. External MOSFET are turned-on. Amplifiers, main contributors to current consumption, are also active. Additionally, current going through the amplifiers has to be added, including current sense amplifiers 1 and 2, and temperature amplifier (unless the amplifier is disabled, see datasheet chap. 7.2 and 7.3).

Therefore, the current needed by the driver from the battery is:

(21) $$I_{q(ON)} = I_{BAT} = \overline{I_{SW}} + I_{CSA1}^{1)} + I_{CSA2}^{1)} + I_{TMPA}^{2)} + I_{VS(ON)}$$

1) to be considered only if amplifier is active and current flowing through sense
2) to be considered only if temperature amplifier is active

Where:

(22) $$I_{CSAx} = \frac{V_{CSOx}}{R_{CSOx}}$$

(23) $$I_{TMPA} = \frac{V_{ENABLE}}{k_{TMP}*(R_{NTC}+R_{TMP})}$$

Combining (18), (22) and (23) in (21) gives:

(24) $$I_{q(ON)} = \frac{I_{BC(ON)}*V_{BC}}{\eta*V_S} + I_{VS(ON)} + \frac{V_{SENSE1}}{R_{IS1}} + \frac{V_{SENSE2}}{R_{IS2}} + \frac{V_{ENABLE}}{k_{TMP}*(R_{NTC}+R_{TMP})}$$

There is no easy way to compute efficiency; therefore, a tool will be provided at product release; in the meantime, excel calculation workbook can be used for estimation.

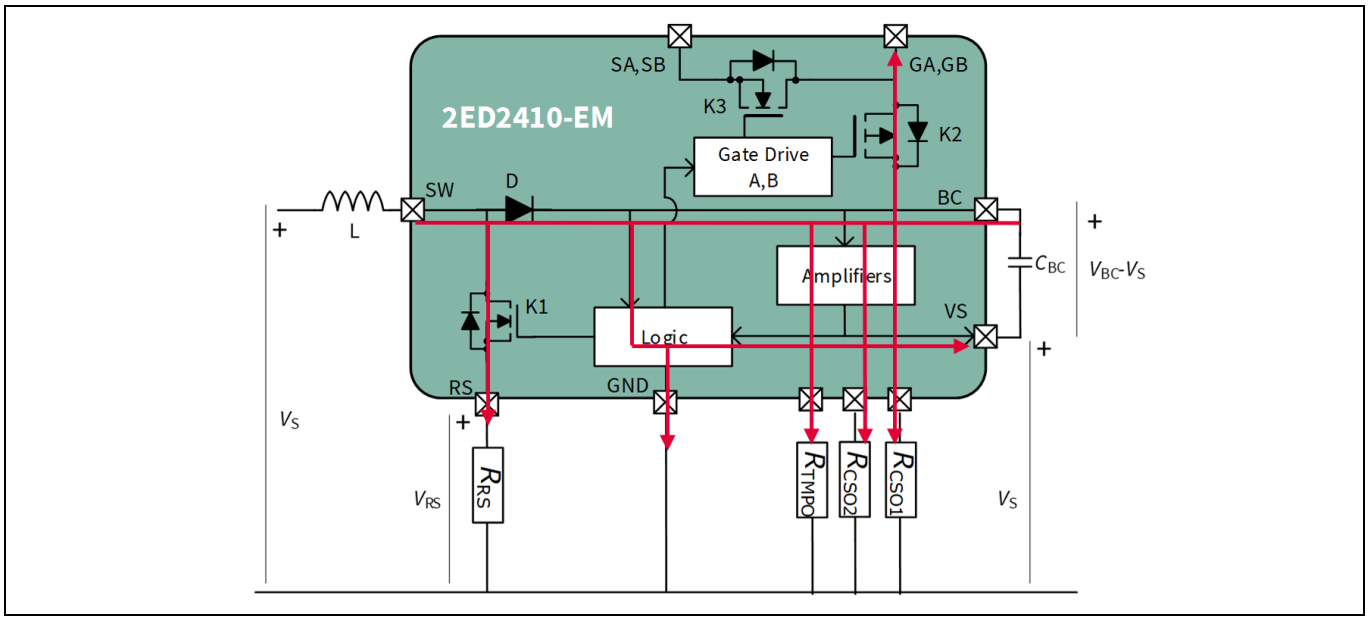


Figure 31 Current paths in ON/SAFESTATE mode

The graph below shows the correlation between theoretical calculation and measurement from evaluation board, in open load so no current is flowing through the sense element.

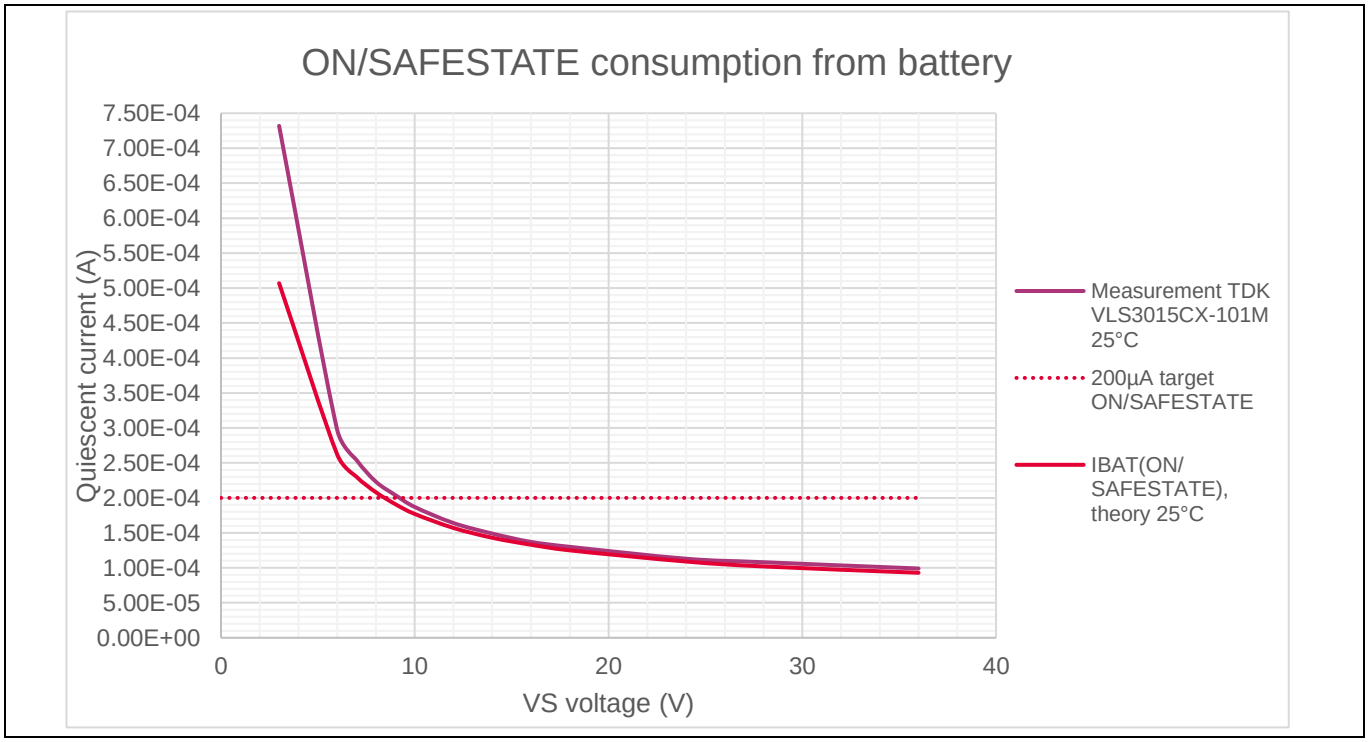


Figure 32 Quiescent current of 2ED2410-EM in ON and SAFESTATE modes @25°C, *open load*, using TDK VLS3015CX-101M-H and R_{RS}=10 Ω

References

[1] Infineon: 2ED2410-EM Datasheet Rev.2.10; Link from infineon website

[2] Infineon Getting started workbook Rev.2.01; Excel workbook from BP_myICP

[3] Infineon 2ED2410-EM Safety application note Rev.02.10

Revision history

Document revision	Date	Description of changes
1.0	2022-03-18	First release by Alexandre Valero, Senior Application Engineer
2.0	2022-12-13	• Updated Chapter 1.5.2 reverse batt protection in common source • Updated Chapter 3.1 pre-charge circuit • Updated Chapter 4.2 TMPO • Updated Chapter 5.2 DPI recommendations • Updated Chapter 6.1 SW routing • Added Chapter 4.1.1 current sense error • Updated Chapter 4.1.2 minimum readable current and Updated Chapter 4.1.3 current sense blind zone • Editorial changes
2.01	2023-02-22	• Editorial changes • Chapter 1.4 renamed for clarity and Note added

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