

# ISOFACE™ digital isolators 2DIBx41xF

## Basic dual-channel digital isolators qualified for industrial applications

### Description

The ISOFACE™ 2DIBx41xF dual-channel digital isolator family supports data rates of up to 40 Mbps and ensures robust data communication over a wide ambient operating temperature range (-40°C to +125°C) and across production spread. Infineon's robust Coreless Transformer (CT) technology ensures high immunity against system noise (CMTI of min. 100 kV/μs) and withstands up to 3000 V<sub>rms</sub> isolation voltage (V<sub>ISO</sub>). Two data channels in a PG-DSO-8 narrow-body 150-mil package allow simplified designs with high power density and improve system efficiency with low power consumption. Product variants with different channel configurations and fail-safe default output states are available.

### Features

- Data rates up to 40 Mbps
- Wide operating supply voltage 2.7 V to 6.5 V
- Low current consumption (max. 1.65 mA/ch @ 1 Mbps, 3.3 V, 15 pF)
- High CMTI: 100 kV/μs (min)
- Propagation delay: 26 ns (typ) with 3 ns (max) channel-to-channel mismatch
- Maximum pulse width distortion of 3 ns
- Fail-safe default output high (2DIBx411F) or low (2DIBx410F) options
- Fixed input thresholds (TTL)
- Wide ambient operating temperature range (-40°C to +125°C)
- RoHS-compliant PG-DSO-8 narrow-body 150-mil package



### Potential applications

- Server, telecom and industrial Switch-Mode Power Supplies (SMPS)
- Industrial automation systems
- Motor drives
- Medical equipment
- Solar inverters

### Product validation

Fully qualified according to JEDEC for industrial applications.

### Isolation and safety certificates

- UL1577 (Ed. 5) with V<sub>ISO</sub> = 3000 V<sub>rms</sub> (certification n. E311313)
- VDE 0884-17 and IEC 60747-17 <sup>1)</sup> with V<sub>IOTM</sub> = 4242 V<sub>pk</sub>, V<sub>IORM</sub> = 1000 V<sub>pk</sub>, V<sub>IOSM</sub> = 6000 V<sub>pk</sub> <sup>2)</sup>
- EN and CQC certification for IEC 62368-1, IEC 60601-1, IEC 61010-1 and GB4943.1 system standards <sup>2)</sup>

<sup>1</sup> IEC 60747-17 and its German equivalent VDE 0884-17 is the successor of the component standard VDE 0884-11, which will expire in 2023

<sup>2</sup> Certification planned

## ISOFACE™ 2DIBx41xF product portfolio

| Part number | Channel configuration     | Default output state | Input threshold | Isolation rating                                         | Package                                     |
|-------------|---------------------------|----------------------|-----------------|----------------------------------------------------------|---------------------------------------------|
| 2DIB0410F   | 2 forward 0 reverse (2+0) | Low                  | Fixed (TTL)     | $V_{\text{ISO}} = 3000 V_{\text{rms}}$<br>(UL1577 Ed. 5) | PG-DSO-8<br>narrow-body 150<br>mil 5 x 6 mm |
| 2DIB0411F   |                           | High                 |                 |                                                          |                                             |
| 2DIB1410F   | 1 forward 1 reverse (1+1) | Low                  |                 |                                                          |                                             |
| 2DIB1411F   |                           | High                 |                 |                                                          |                                             |

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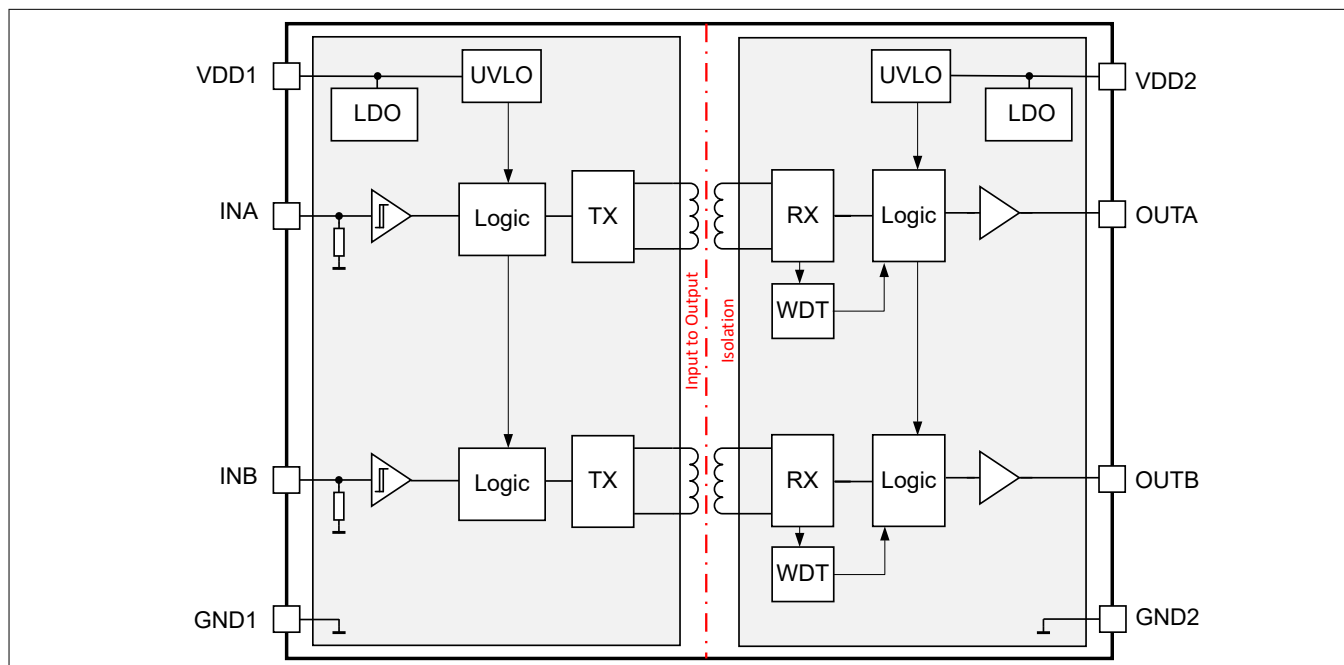
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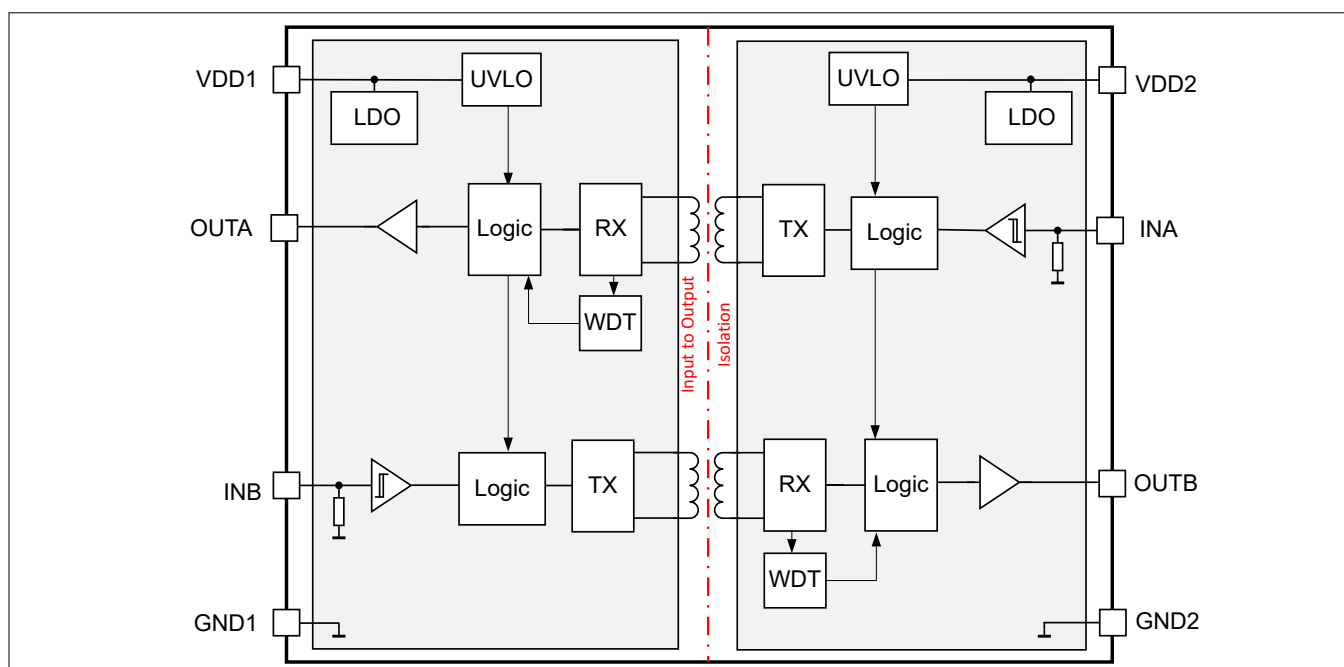
## 1 Functional block diagram

### 1 Functional block diagram

Figure 1 and Figure 2 illustrate the internal block diagram of the ISOFACE™ 2DIB041xF (2+0 channel configuration) and 2DIB141xF (1+1 channel configuration), respectively.



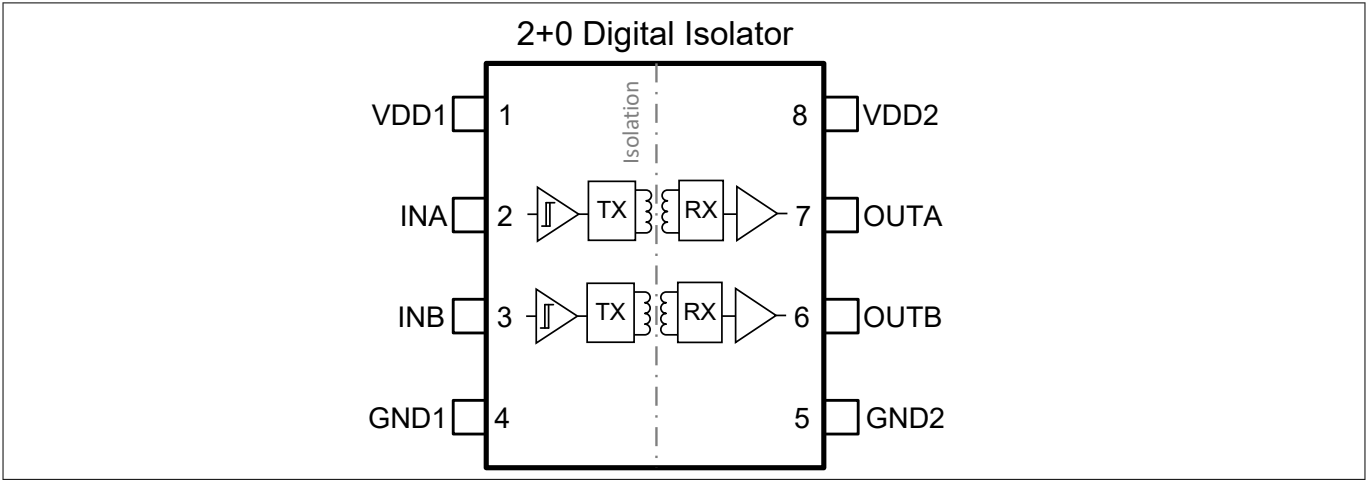
**Figure 1** ISOFACE™ 2DIB041xF (2+0 channel configuration)



**Figure 2** ISOFACE™ 2DIB141xF (1+1 channel configuration)

**2 Pin configuration**

**2 Pin configuration**

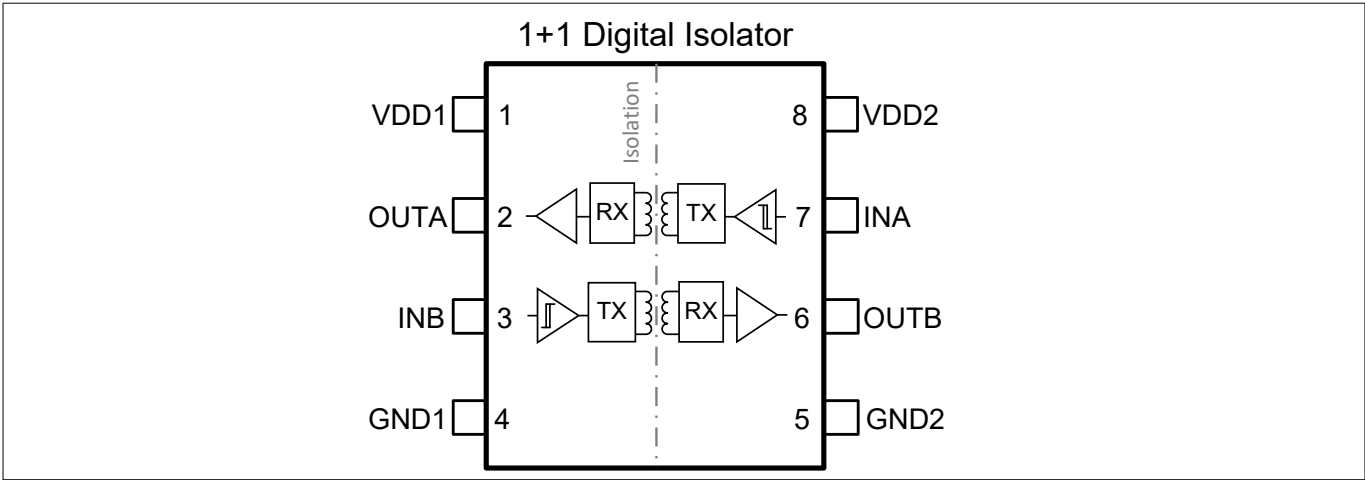


**Figure 3 Pin-out for ISOFACE™ 2DIB041xF**

**Table 1 Pin definitions and functions for ISOFACE™ 2DIB041xF**

| Name | Pin | Type | Function                  |
|------|-----|------|---------------------------|
| VDD1 | 1   | I    | Positive supply voltage 1 |
| INA  | 2   | I    | Channel A input           |
| INB  | 3   | I    | Channel B input           |
| GND1 | 4   | -    | Ground 1                  |
| GND2 | 5   | -    | Ground 2                  |
| OUTB | 6   | O    | Channel B output          |
| OUTA | 7   | O    | Channel A output          |
| VDD2 | 8   | I    | Positive supply voltage 2 |

**2 Pin configuration**



**Figure 4** Pin-out for ISOFACE™ 2DIB141xF

**Table 2** Pin definitions and functions for ISOFACE™ 2DIB141xF

| Name | Pin | Type | Function                  |
|------|-----|------|---------------------------|
| VDD1 | 1   | I    | Positive supply voltage 1 |
| OUTA | 2   | O    | Channel A output          |
| INB  | 3   | I    | Channel B input           |
| GND1 | 4   | -    | Ground 1                  |
| GND2 | 5   | -    | Ground 2                  |
| OUTB | 6   | O    | Channel B output          |
| INA  | 7   | I    | Channel A input           |
| VDD2 | 8   | I    | Positive supply voltage 2 |

## 3 Functional description

### 3 Functional description

This chapter provides a summary of the integrated functions and features, and describes the relationships between them. The parameters and equations are based on typical values at  $T_A = 25\text{ °C}$ .

#### 3.1 Truth tables

**Table 3 Truth table for 2-channel Digital Isolator**

| $V_{DDI}^{1)}$ | $V_{DDO}^{1)}$ | $V_{INX}$       | $V_{OUTX}$            |
|----------------|----------------|-----------------|-----------------------|
| Powered        | Powered        | H <sup>2)</sup> | H                     |
|                |                | L <sup>2)</sup> | L                     |
| Unpowered      | Powered        | X <sup>2)</sup> | Default <sup>3)</sup> |
| X              | Unpowered      | X               | Z <sup>2)</sup>       |

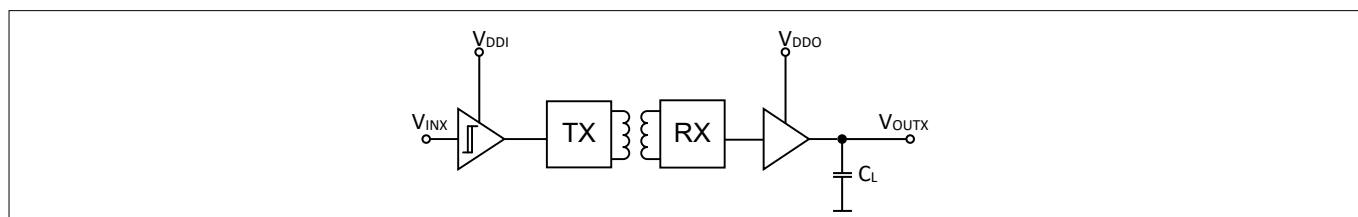
1)  $V_{DDI}$  and  $V_{DDO}$  refer to the supply voltages on the input and output sides of a given channel, respectively

2) H means "high" and L means "low", X means "irrelevant", Z means "high-impedance"

3) Refer to product variants in [Ordering guide](#)

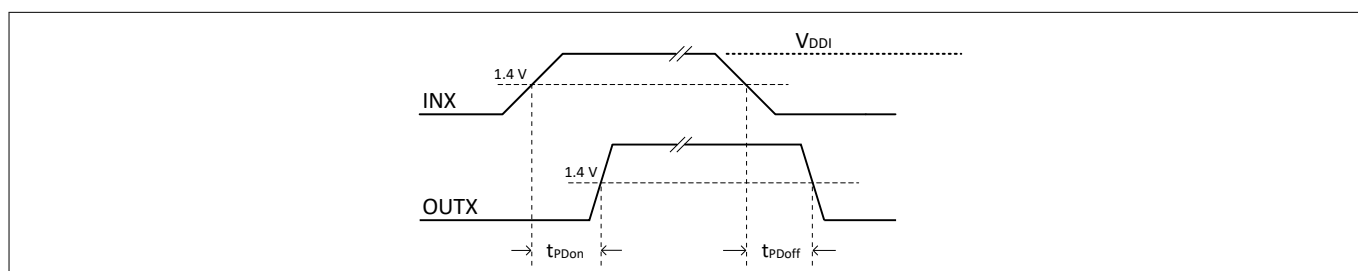
#### 3.2 Timing diagrams

Figure 5 illustrates the test set-up for the electrical characteristics described in [Electrical characteristics](#).



**Figure 5 Test circuit**

Figure 6 illustrates the input-to-output propagation delays as observed at the capacitively loaded output.

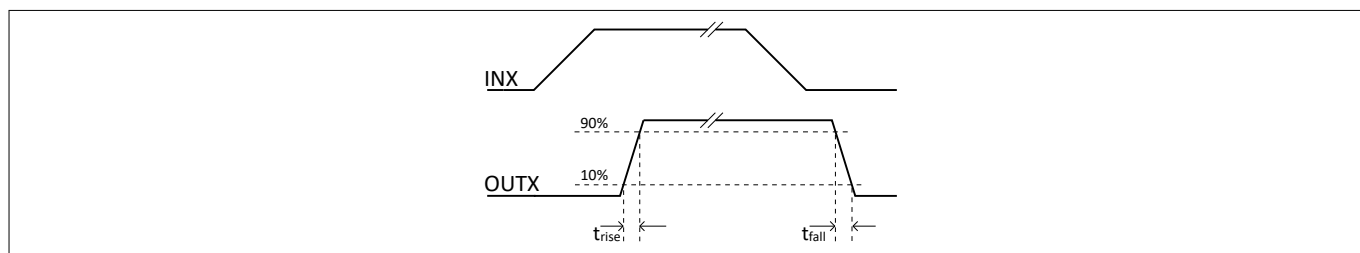


**Figure 6 Propagation delays**



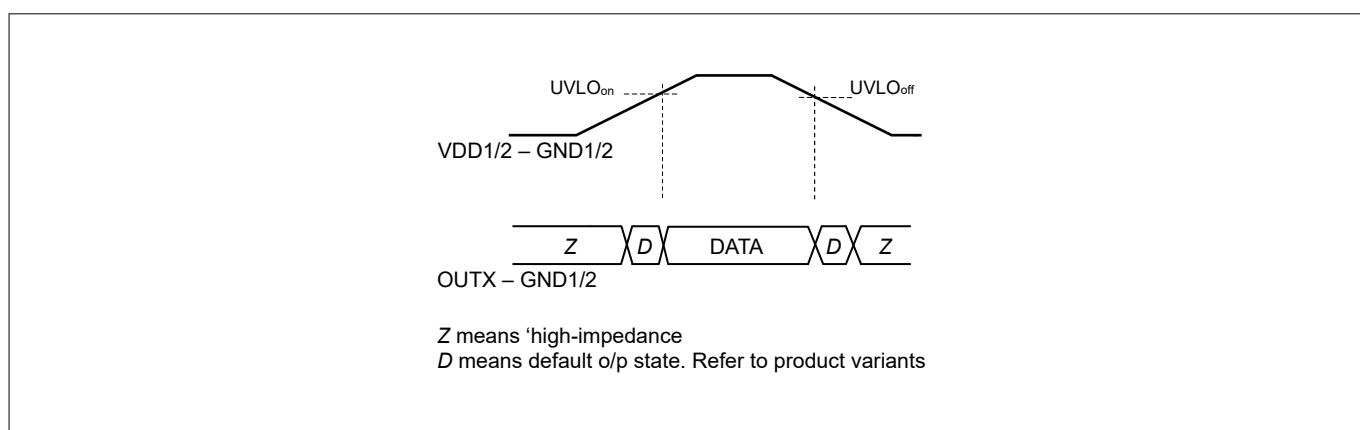
### 3 Functional description

Figure 7 illustrates the rise and fall times as observed at the capacitively loaded output.



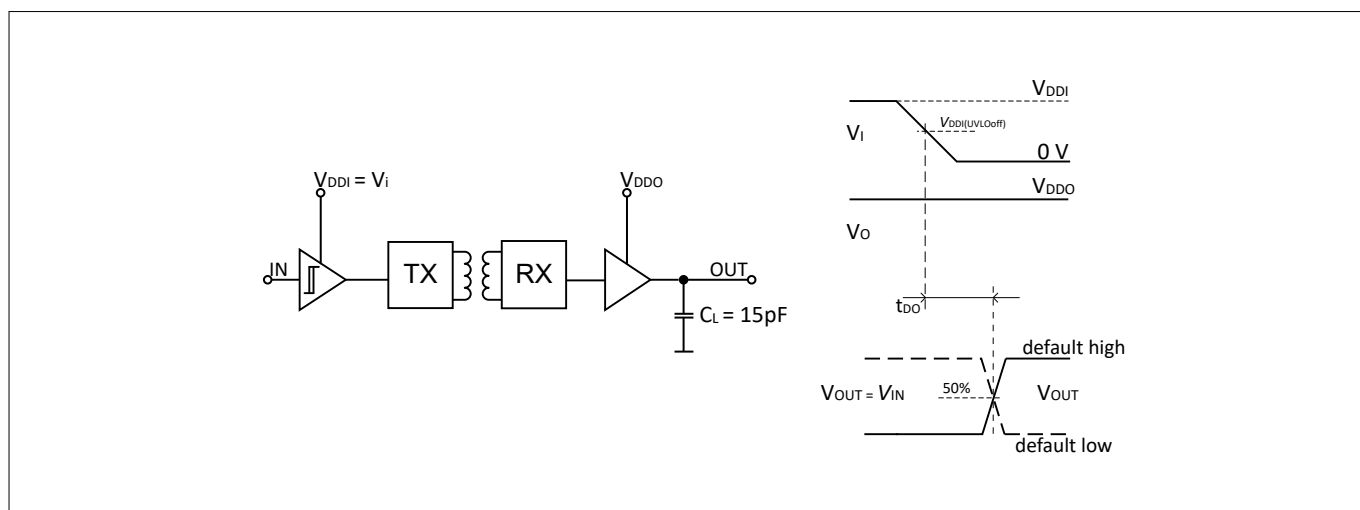
**Figure 7 Rise and fall times**

Figure 8 illustrates the output behavior to supply UVLO events when  $V_{DD1/2}$  crosses the UVLO thresholds during rising or falling transitions (power-up, power-down). Note that the input ( $V_{DD1}$ ) and output ( $V_{DD2}$ ) supplies are rising and falling at the same time.



**Figure 8 Under-voltage lockout**

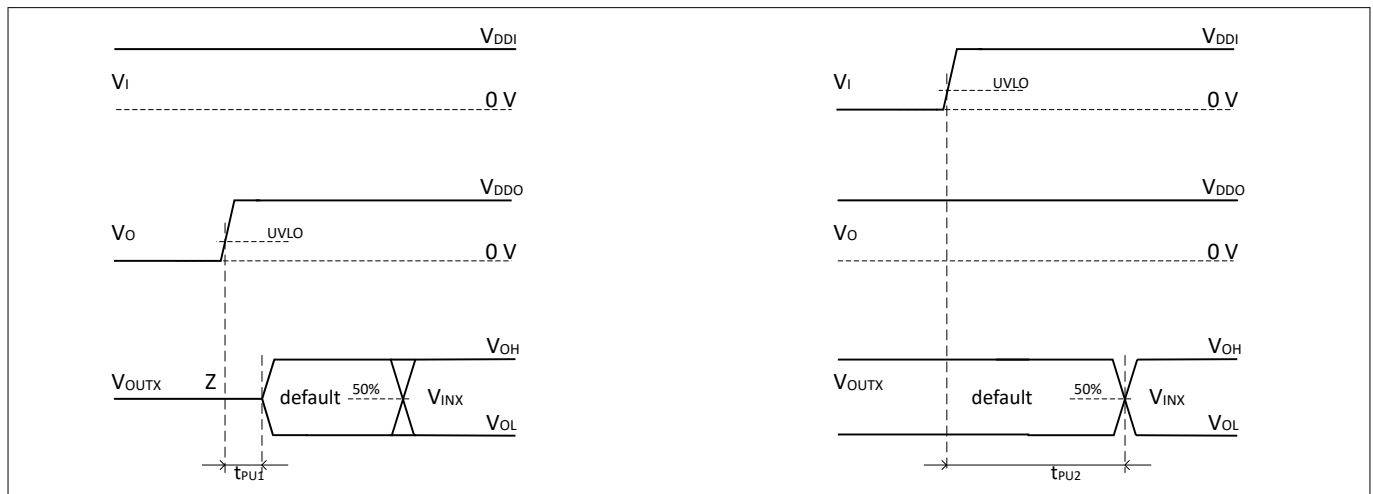
Figure 9 illustrates the time taken for the output to reach the default value when the power supply of the input channel goes below the UVLOoff value.



**Figure 9 Default output delay time**

### 3 Functional description

Figure 10 illustrates the time taken for the output to follow the input when the power supplies of the input and output sides of the digital isolator have different start-up timings. The power-up time is  $t_{PU} = \max \{t_{PU1}, t_{PU2}\}$ .

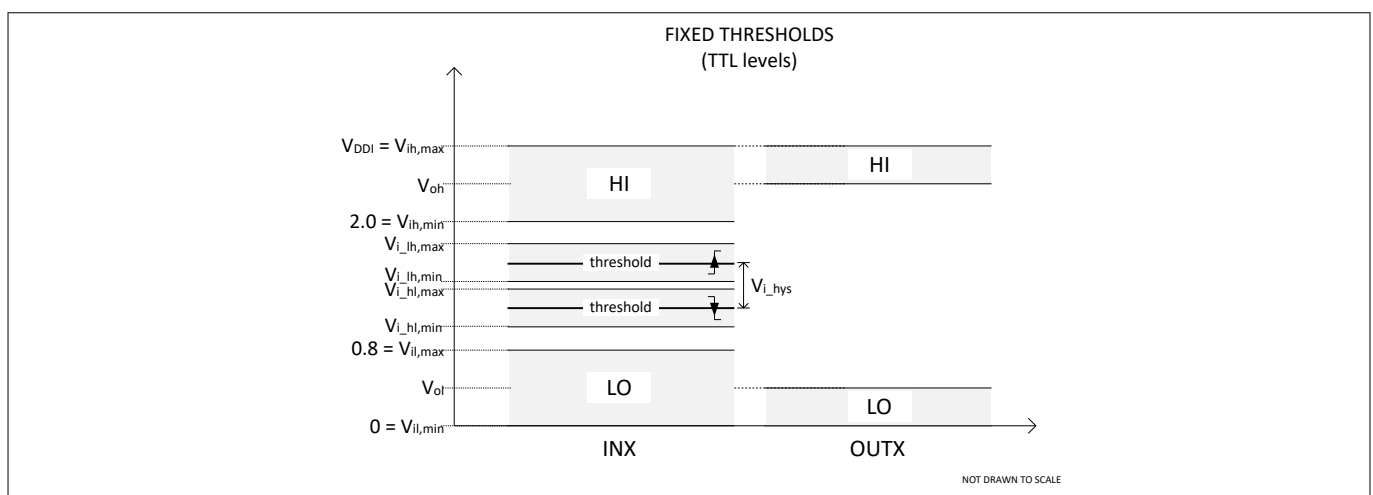


**Figure 10** Power-up delay time

### 3.3 Data transmission input-to-output

Communication based on Coreless Transformer (CT) is used for signal transfer between input and output channels. If a constant DC level within the operating range is applied at the input, a proven high resolution pulse repetition scheme ensure functionality, enabling the output to follow the constant DC input. It also enables recovery from communication fails and safe system shutdown. In case of a power loss at the input channel, the pulse repetition scheme will be disabled and a watch-dog timer at the output triggers approximately after  $t_{DO}$  time period and drives the channel output to the default state. In case of multiple channels on the output side, the first watch-dog timer detecting the power loss at the input will drive all output channels on that side to default value. Once the power supply on the input channels is above the threshold value ( $V_{DDX(UVLOon)}$ ), the communication is restored and the output will follow the input as shown in Figure 10.

### 3.4 Input/output voltage levels description



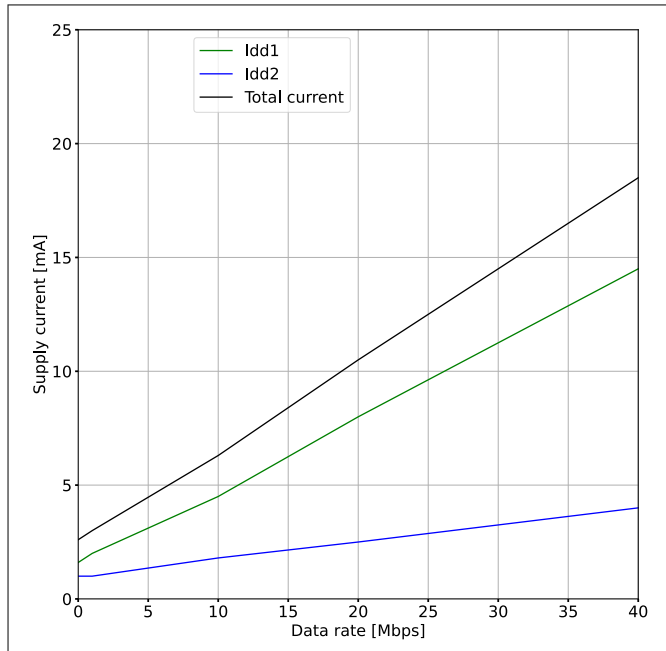
**Figure 11** TTL fixed thresholds description

### 3 Functional description

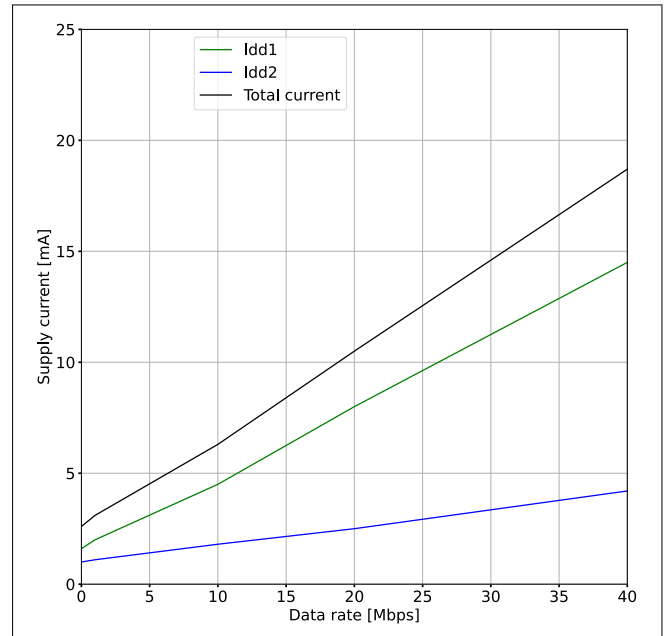
#### 3.5 Supply characteristics

Maximum values are given at  $T_A = 125^\circ\text{C}$ ,  $C_{\text{LOAD}} = 15\text{ pF}$  and 50% duty cycle input square wave.

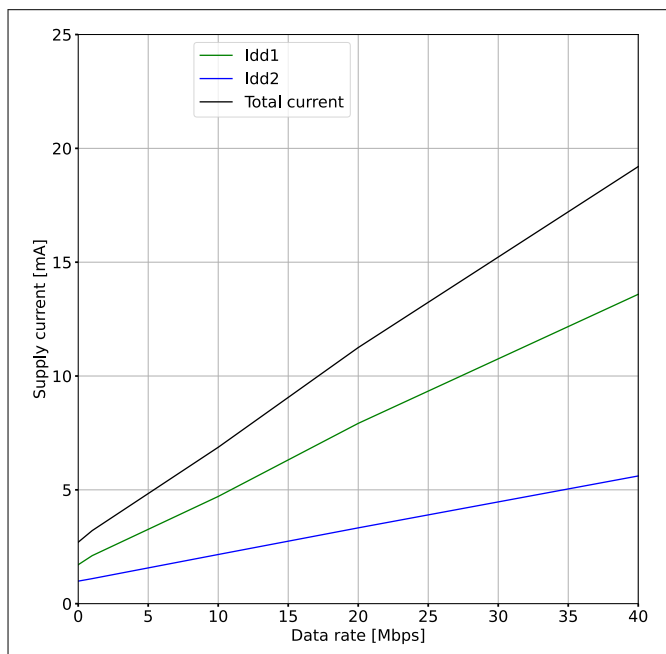
##### 2+0 digital isolator (2DIB041xF)



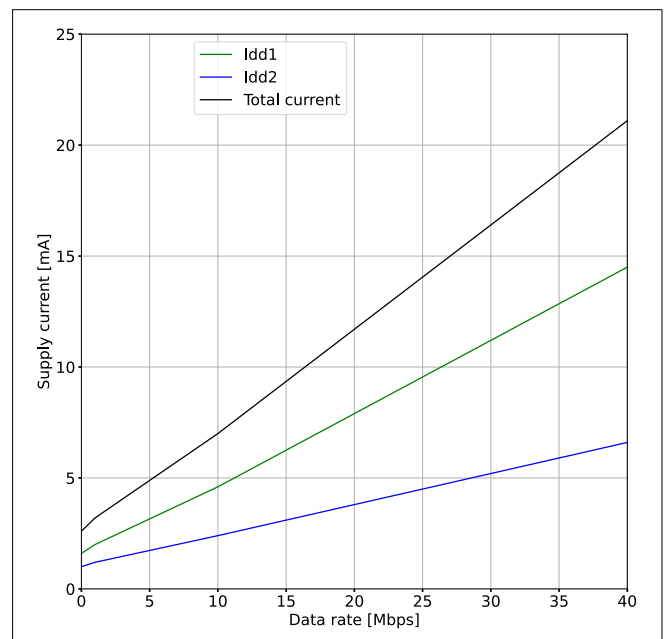
**Figure 12** Supply current vs. data rate  
( $V_{\text{DD1}} = V_{\text{DD2}} = 2.7\text{ V}$ )



**Figure 13** Supply current vs. data rate  
( $V_{\text{DD1}} = V_{\text{DD2}} = 3.3\text{ V}$ )



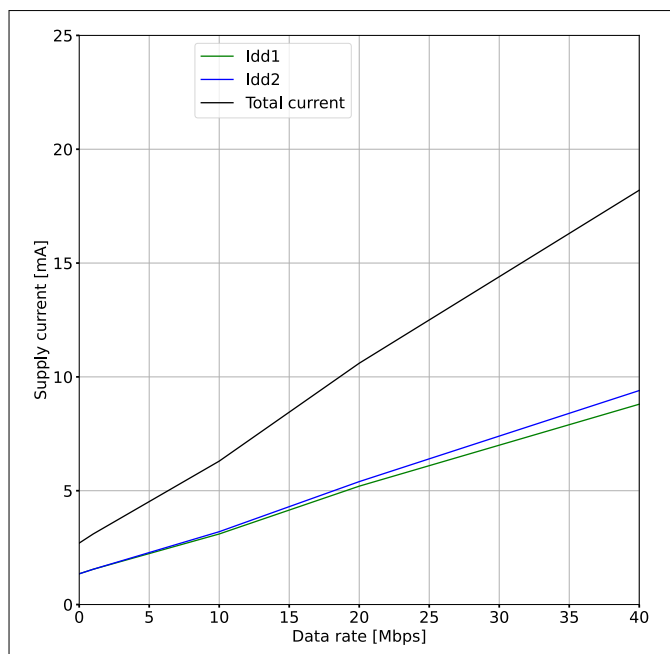
**Figure 14** Supply current vs. data rate  
( $V_{\text{DD1}} = V_{\text{DD2}} = 5.0\text{ V}$ )



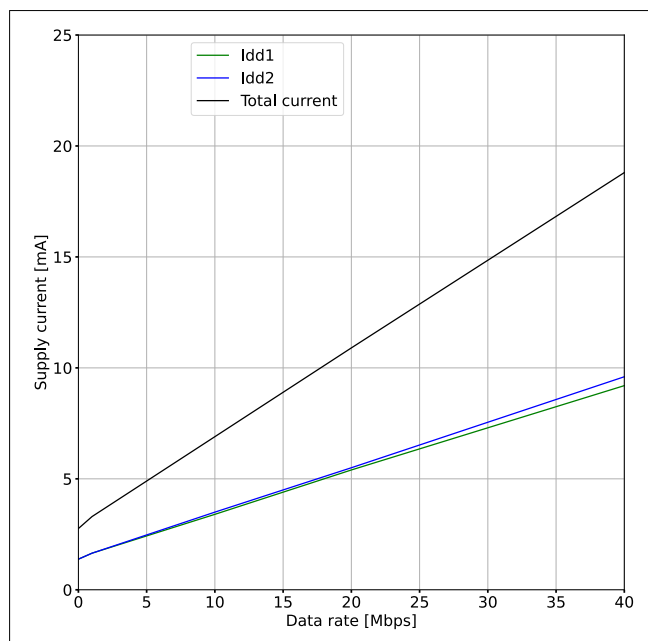
**Figure 15** Supply current vs. data rate  
( $V_{\text{DD1}} = V_{\text{DD2}} = 6.5\text{ V}$ )

### 3 Functional description

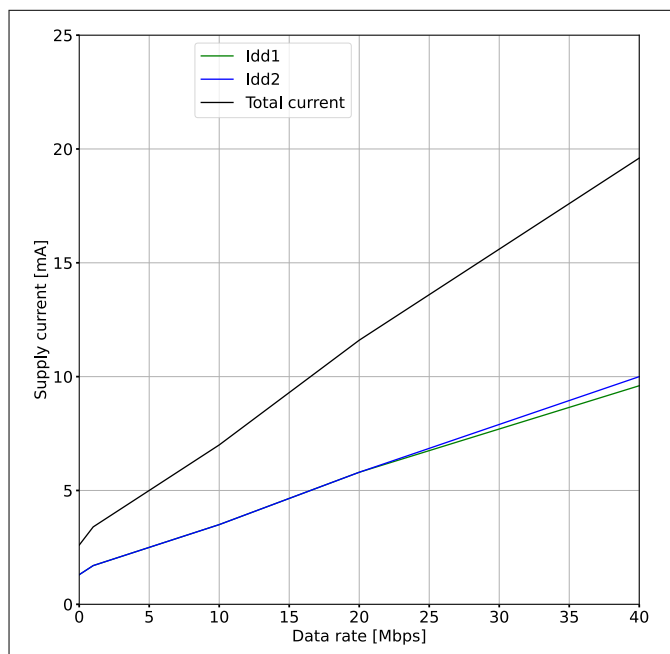
#### 1+1 digital isolator (2DIB141xF)



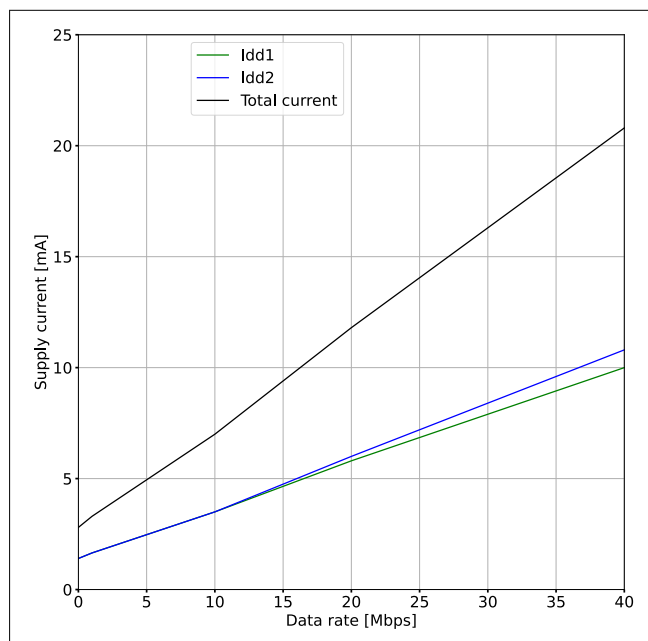
**Figure 16** Supply current vs. data rate  
(V<sub>DD1</sub> = V<sub>DD2</sub> = 2.7 V)



**Figure 17** Supply current vs. data rate  
(V<sub>DD1</sub> = V<sub>DD2</sub> = 3.3 V)



**Figure 18** Supply current vs. data rate  
(V<sub>DD1</sub> = V<sub>DD2</sub> = 5.0 V)



**Figure 19** Supply current vs. data rate  
(V<sub>DD1</sub> = V<sub>DD2</sub> = 6.5 V)

## 4 Thermal and electrical characteristics

### 4 Thermal and electrical characteristics

#### 4.1 Absolute maximum ratings

**Table 4 Absolute maximum ratings**

Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These values are not tested during production test.

| Parameter                      | Symbol             | Values |      |                 | Unit | Note or condition                                                                                              |
|--------------------------------|--------------------|--------|------|-----------------|------|----------------------------------------------------------------------------------------------------------------|
|                                |                    | Min.   | Typ. | Max.            |      |                                                                                                                |
| Supply voltage                 | $V_{DD1}, V_{DD2}$ | -0.5   |      | 7.5             | V    |                                                                                                                |
| Voltage at pins INx            | $V_{INX}$          | -0.5   |      | $V_{DD1} + 0.5$ | V    | 1) 2)                                                                                                          |
| Voltage at pins OUTx           | $V_{OUTX}$         | - 0.5  |      | $V_{DDO} + 0.5$ | V    | 1)                                                                                                             |
| Average output current per pin | $I_{OUT}$          | -10    |      | +10             | mA   |                                                                                                                |
| Junction temperature           | $T_J$              | -40    |      | 150             | °C   |                                                                                                                |
| Storage temperature            | $T_{STG}$          | -65    |      | 150             | °C   |                                                                                                                |
| Soldering temperature          | $T_{SOL}$          |        |      | 260             | °C   | reflow / wave soldering, according to JESD22A111                                                               |
| Electrostatic discharge HBM    | $V_{ESD\_HBM}$     |        |      | 2               | kV   | Human body model (HBM) according to JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)       |
| Electrostatic discharge CDM    | $V_{ESD\_CDM}$     |        |      | 500             | V    | Charged-device model (CDM) according to JESD22-002                                                             |
| Latch-up immunity              | $I_{LU}$           |        |      | 150             | mA   | Latch-up immunity characterization according to JEDEC78E Class II, pin voltages according to abs. max. ratings |

1)  $V_{DD1}$  and  $V_{DDO}$  refer to the supply voltages on the input and output sides of a given channel, respectively

2) Strongly driven inputs can power the  $V_{DD1}$  via an internal protection diode and can cause undetermined output

#### 4.2 Additional ESD ratings

**Table 5 Additional ESD ratings**

| Parameter                           | Symbol           | Values |      |      | Unit | Note or condition                      |
|-------------------------------------|------------------|--------|------|------|------|----------------------------------------|
|                                     |                  | Min.   | Typ. | Max. |      |                                        |
| Contact discharge per IEC 61000-4-2 | $ V_{ESD\_IEC} $ |        | 22   |      | kV   | Isolation barrier withstand test 1) 2) |

1) IEC ESD strike is applied across the barrier with all pins on each side tied together, creating a two-terminal device

2) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device

## 4 Thermal and electrical characteristics

### 4.3 Thermal characteristics

Typical thermal characteristics at  $T_A = 25^\circ\text{C}$

**Table 6 Thermal characteristics for JEDEC and reference PCB**

| Parameter                                    | Symbol        | JEDEC             | Reference PCB    | Unit | Note or condition                        |
|----------------------------------------------|---------------|-------------------|------------------|------|------------------------------------------|
| Thermal resistance junction-to-ambient       | $R_{thJA}$    | 113 <sup>1)</sup> | 89 <sup>2)</sup> | K/W  | JEDEC 2s2p (JED51-7), $P_{dis} = 186$ mW |
| Thermal resistance junction-to-case (top)    | $R_{thJC}$    | 58                | 58               | K/W  | <sup>3)</sup>                            |
| Thermal resistance junction-to-board         | $R_{thJB}$    | 35                | 44               | K/W  | <sup>4)</sup>                            |
| Characterization parameter junction-to-top   | $\Psi_{thJT}$ | 7.5               | 7                | K/W  | <sup>5)</sup>                            |
| Characterization parameter junction-to-board | $\Psi_{thJB}$ | 34                | 43               | K/W  | <sup>5)</sup>                            |

1) Obtained by simulating a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a

2) Obtained by simulating a JEDEC-standard, high-K board, as specified in JESD51-7 and in reference PCB specifications below, in an environment described in JESD51-2a

3) Obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a similar description can be found in the ANSI SEMI standard G30-88

4) Obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8

5) Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $R_{th}$ , using a procedure described in JESD51-2a (sections 6 and 7)

**Table 7 Reference PCB specifications**

| Parameter                             | Value                                                                 | $\lambda_{therm}$ [W/(m-K)] |
|---------------------------------------|-----------------------------------------------------------------------|-----------------------------|
| Dimension [mm <sup>3</sup> ]          | 76.2 x 114.3 x 1.5 (JEDEC)                                            |                             |
| Material                              | FR4                                                                   | 0.3                         |
| Metalization                          | JEDEC 2s2p (JESD 51-7)                                                | 388                         |
| Cooling area                          | Ground inner layer                                                    |                             |
| Thermal vias                          | Ø = 0.5 mm, plating 25 µm, 2 x 2 pcs. connected to inner ground layer |                             |
| Package attach [50 µm]                | Solder                                                                | 55                          |
| Inner ground layer [mm <sup>3</sup> ] | 74.2 x 74.2 x 0.03 (JEDEC), planes are 4 mm spaced                    |                             |

4 Thermal and electrical characteristics

Table 8                      Reference PCB layout

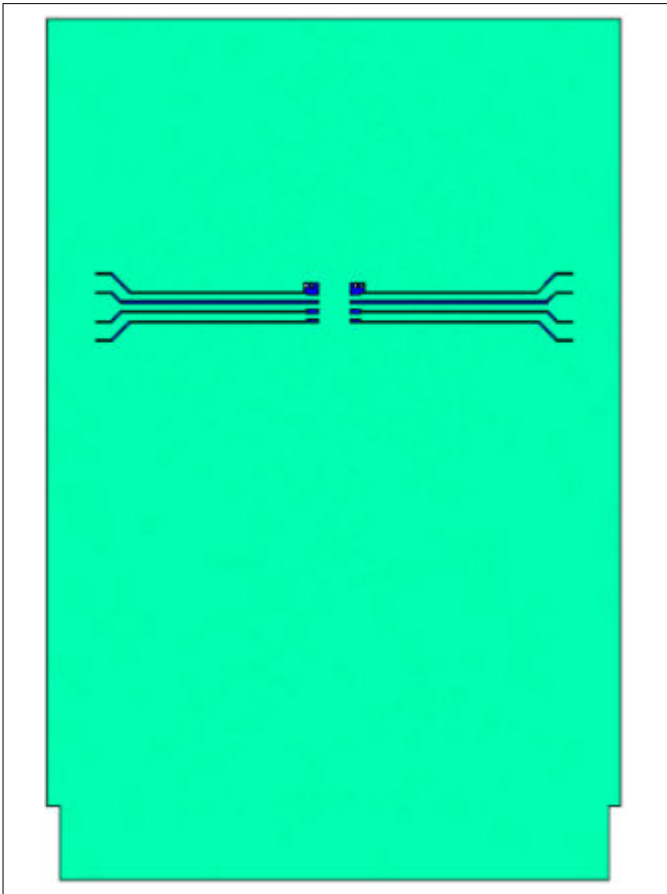


Figure 20                      Top footprint

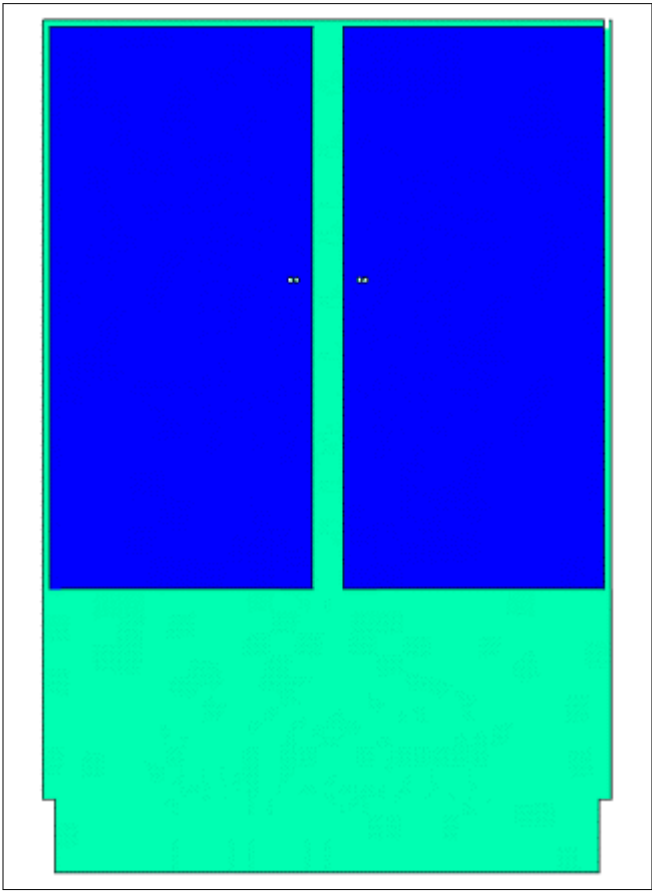


Figure 21                      Inner layers (connect to ground)

## 4 Thermal and electrical characteristics

### 4.4 Operating range

**Table 9** Operating range

| Parameter                      | Symbol             | Values |      |           | Unit | Note or condition |
|--------------------------------|--------------------|--------|------|-----------|------|-------------------|
|                                |                    | Min.   | Typ. | Max.      |      |                   |
| Data rate                      | $DR$               | 0      |      | 40        | Mbps |                   |
| Supply voltage                 | $V_{DD1}, V_{DD2}$ | 2.7    |      | 6.5       | V    |                   |
| High-level input voltage (TTL) | $V_{IH}$           | 2.0    |      | $V_{DDI}$ | V    |                   |
| Low-level input voltage (TTL)  | $V_{IL}$           | 0      |      | 0.8       | V    |                   |
| Ambient temperature            | $T_A$              | -40    |      | 125       | °C   |                   |

### 4.5 Common-mode transient immunity (CMTI)

**Table 10** Common-mode transient immunity (CMTI)

| Parameter                                    | Symbol   | Values |      |      | Unit  | Note or condition                                                         |
|----------------------------------------------|----------|--------|------|------|-------|---------------------------------------------------------------------------|
|                                              |          | Min.   | Typ. | Max. |       |                                                                           |
| Static common-mode transient immunity (CMTI) | $ CM_H $ | 100    |      |      | kV/μs | $V_{CM} = 1500\text{ V}; V_{INX}$ tied to $V_{DDI}$ <sup>1) 2) 3)</sup>   |
| Static common-mode transient immunity (CMTI) | $ CM_L $ | 100    |      |      | kV/μs | $V_{CM} = 1500\text{ V}; V_{INX}$ tied to 0 V <sup>2)</sup> <sup>3)</sup> |

1)  $V_{DDI}$  refers to the supply voltages on the input side of a given channel

2) Minimum slew rate of a common-mode voltage at which the output signal is disturbed

3) Parameter not tested in production

### 4.6 Power supply - UVLO

**Table 11** Power supply - UVLO

Typical values are given at  $T_A = 25^\circ\text{C}$  over operating range unless otherwise specified. Minimum/maximum values apply over the recommended operating range of  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

| Parameter                      | Symbol             | Values |      |      | Unit | Note or condition |
|--------------------------------|--------------------|--------|------|------|------|-------------------|
|                                |                    | Min.   | Typ. | Max. |      |                   |
| Supply UVLO turn-on threshold  | $V_{DDX(UVLOon)}$  | 2.42   | 2.55 | 2.68 | V    |                   |
| Supply UVLO turn-off threshold | $V_{DDX(UVLOoff)}$ | 2.35   | 2.45 | 2.55 | V    |                   |
| Supply UVLO hysteresis         | $V_{DDX(UVLOhys)}$ | 0.07   | 0.10 |      | V    |                   |



## 4 Thermal and electrical characteristics

### 4.7 Electrical characteristics

The electrical characteristics describe the behavior of the device under the specified operating conditions.

#### 4.7.1 Electrical characteristics - 6.5 V supply

Typical values are given at  $T_A = 25^\circ\text{C}$  with  $V_{DD1} = V_{DD2} = 6.5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range of  $V_{DD1} = V_{DD2} = 6.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching characteristics are tested with  $C_{LOAD} = 15\text{ pF}$  and 50% duty-cycle input square wave, over operating range unless otherwise specified. Supply current values are specified considering that all channels are switching at the same data rate. Parameters are not tested in production unless otherwise specified.

##### 4.7.1.1 Logic inputs

**Table 12** Logic inputs

| Parameter                                       | Symbol       | Values |      |      | Unit             | Note or condition                    |
|-------------------------------------------------|--------------|--------|------|------|------------------|--------------------------------------|
|                                                 |              | Min.   | Typ. | Max. |                  |                                      |
| High-level input current                        | $I_{IH}$     |        |      | 10   | $\mu\text{A}$    | $V_{INX} = V_{DDI}$ <sup>1) 2)</sup> |
| Low-level input current                         | $I_{IL}$     | -10    |      |      | $\mu\text{A}$    | $V_{INX} = 0\text{ V}$ <sup>2)</sup> |
| Input voltage threshold for LH transition (TTL) | $V_{I\_LH}$  | 1.4    |      | 1.9  | V                |                                      |
| Input voltage threshold for HL transition (TTL) | $V_{I\_HL}$  | 1.0    |      | 1.4  | V                |                                      |
| Input voltage threshold hysteresis (TTL)        | $V_{I\_HYS}$ | 0.38   |      |      | V                |                                      |
| Input pull-down resistor                        | $R_{IN}$     |        | 825  |      | $\text{k}\Omega$ | $V_{INX} = V_{DDI}$ <sup>1) 2)</sup> |

1)  $V_{DDI}$  = Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

2) Parameter tested in production

##### 4.7.1.2 Logic outputs

**Table 13** Logic outputs

| Parameter                 | Symbol   | Values          |      |      | Unit | Note or condition                    |
|---------------------------|----------|-----------------|------|------|------|--------------------------------------|
|                           |          | Min.            | Typ. | Max. |      |                                      |
| High-level output voltage | $V_{OH}$ | $V_{DDO} - 0.4$ |      |      | V    | $I_{OH} = 4\text{ mA}$ <sup>1)</sup> |
| Low-level output voltage  | $V_{OL}$ |                 |      | 0.4  | V    | $I_{OL} = -4\text{ mA}$              |

1)  $V_{DDO}$  - Output-side supply voltage. For output buffers on side 1 it is  $V_{DD1}$  and for output buffers on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.1.3 Power supply - 2DIB041xF (2+0)

**Table 14** Power supply - 2DIB041xF (2+0)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition      |
|---------------------------|-----------------|--------|------|------|------|------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                        |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.65 | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD2}$       |        |      | 1    | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.65 | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - DC input | $I_{DD2}$       |        |      | 1    | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 2.15 | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.2  | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 4.6  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 2.4  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 8    | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 3.8  | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 14.5 | mA   | $DR = 40\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 6.6  | mA   | $DR = 40\text{ Mbps}$  |

#### 4 Thermal and electrical characteristics

##### 4.7.1.4 Power supply - 2DIB141xF (1+1)

**Table 15** Power supply - 2DIB141xF (1+1)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition                 |
|---------------------------|-----------------|--------|------|------|------|-----------------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                                   |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.4  | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.4  | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.4  | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.4  | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 1.7  | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.7  | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 3.5  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 3.5  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 5.8  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 6    | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 10   | mA   | $DR = 40\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 10.8 | mA   | $DR = 40\text{ Mbps}$             |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.1.5 Dynamic characteristics

**Table 16** Dynamic characteristics

| Parameter                                                          | Symbol                | Values |      |      | Unit    | Note or condition                                                                                                                       |
|--------------------------------------------------------------------|-----------------------|--------|------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------|
|                                                                    |                       | Min.   | Typ. | Max. |         |                                                                                                                                         |
| INx to OUTx turn-on propagation delay                              | $t_{PDOn}$            | 21     | 26   | 33   | ns      | From 1.4 V level of rising input to 1.4 V level of corresponding rising output <sup>1)</sup>                                            |
| INx to OUTx turn-off propagation delay                             | $t_{PDOff}$           | 21     | 26   | 33   | ns      | From 1.4 V level of falling input to 1.4 V level of corresponding falling output <sup>1)</sup>                                          |
| Part-to-part propagation delays mismatch                           | $\Delta t_{PD,p-p}$   |        |      | 6    | ns      | <sup>2) 3)</sup>                                                                                                                        |
| Codirectional channel-to-channel propagation delay mismatch        | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns      | Within same sample, over operating temperature range, same-direction channels, switching in the same direction <sup>2)</sup>            |
| Opposite-directional channel-to-channel propagation delay mismatch | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns      | Within same sample, over operating temperature range, opposite-directional channels, switching with the same signal level <sup>2)</sup> |
| Pulse width distortion                                             | $PWD$                 |        |      | 3    | ns      | $ t_{PDOff} - t_{PDOn} $ <sup>2) 4)</sup>                                                                                               |
| Input pulse width that changes output state                        | $t_{pw,min}$          | 10     | 11.5 | 16   | ns      | Measured with full range of input signal $V_{IN} = V_{DDI}$ <sup>5)</sup>                                                               |
| Output signal rise time                                            | $t_{rise}$            |        |      | 4    | ns      | 10% to 90% rising output, $C_{LOAD} = 15$ pF                                                                                            |
| Output signal fall time                                            | $t_{fall}$            |        |      | 4    | ns      | 90% to 10% falling output, $C_{LOAD} = 15$ pF                                                                                           |
| Default output delay time from input power loss                    | $t_{DO}$              |        | 0.4  | 2.6  | $\mu s$ | Measured from $V_{DDX(UVLOoff)} = 2.55$ V. Power supply ramp rate = 1 V/ $\mu s$                                                        |
| Time from UVLO to valid output data                                | $t_{PU}$              |        |      | 3    | $\mu s$ | Power supply ramp rate = 1 V/ $\mu s$ , DR > 6.6 Mbps                                                                                   |

1) Parameter tested in production

2) Parameter tested in production

3) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature

4) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range

5)  $V_{DDI}$  = Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

## 4 Thermal and electrical characteristics

### 4.7.2 Electrical characteristics - 5 V supply

Typical values are given at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 5\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range of  $V_{DD1} = V_{DD2} = 5\text{ V} \pm 10\%$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching characteristics are tested with  $C_{LOAD} = 15\text{ pF}$  and 50% duty-cycle input square wave, over operating range unless otherwise specified. Supply current values are specified considering that all channels are switching at the same data rate. Parameters are tested in production unless otherwise specified. Supply current values are tested in production for data rates up to 1 Mbps.

#### 4.7.2.1 Logic inputs

**Table 17** Logic inputs

| Parameter                                       | Symbol       | Values |      |      | Unit             | Note or condition                 |
|-------------------------------------------------|--------------|--------|------|------|------------------|-----------------------------------|
|                                                 |              | Min.   | Typ. | Max. |                  |                                   |
| High-level input current                        | $I_{IH}$     |        |      | 10   | $\mu\text{A}$    | $V_{INX} = V_{DDI}$ <sup>1)</sup> |
| Low-level input current                         | $I_{IL}$     | -10    |      |      | $\mu\text{A}$    | $V_{INX} = 0\text{ V}$            |
| Input voltage threshold for LH transition (TTL) | $V_{I\_LH}$  | 1.4    |      | 1.9  | V                |                                   |
| Input voltage threshold for HL transition (TTL) | $V_{I\_HL}$  | 1.0    |      | 1.4  | V                |                                   |
| Input voltage threshold hysteresis (TTL)        | $V_{I\_HYS}$ | 0.38   |      |      | V                |                                   |
| Input pull-down resistor                        | $R_{IN}$     |        | 825  |      | $\text{k}\Omega$ | $V_{INX} = V_{DDI}$ <sup>1)</sup> |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

#### 4.7.2.2 Logic outputs

**Table 18** Logic outputs

| Parameter                 | Symbol   | Values          |      |      | Unit | Note or condition                    |
|---------------------------|----------|-----------------|------|------|------|--------------------------------------|
|                           |          | Min.            | Typ. | Max. |      |                                      |
| High-level output voltage | $V_{OH}$ | $V_{DDO} - 0.4$ |      |      | V    | $I_{OH} = 4\text{ mA}$ <sup>1)</sup> |
| Low-level output voltage  | $V_{OL}$ |                 |      | 0.4  | V    | $I_{OL} = -4\text{ mA}$              |

1)  $V_{DDO}$  - Output-side supply voltage. For output buffers on side 1 it is  $V_{DD1}$  and for output buffers on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.2.3 Power supply - 2DIB041xF (2+0)

**Table 19** Power supply - 2DIB041xF (2+0)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition      |
|---------------------------|-----------------|--------|------|------|------|------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                        |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.65 | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD2}$       |        |      | 1    | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.65 | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - DC input | $I_{DD2}$       |        |      | 1    | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 2.15 | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.1  | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 4.6  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 2.15 | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 8    | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 3.3  | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 14.5 | mA   | $DR = 40\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 5.6  | mA   | $DR = 40\text{ Mbps}$  |

#### 4 Thermal and electrical characteristics

##### 4.7.2.4 Power supply - 2DIB141xF (1+1)

**Table 20** Power supply - 2DIB141xF (1+1)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition                 |
|---------------------------|-----------------|--------|------|------|------|-----------------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                                   |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.4  | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.4  | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.4  | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.4  | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 1.7  | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.7  | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 3.5  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 3.5  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 5.8  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 5.8  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 9.6  | mA   | $DR = 40\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 10   | mA   | $DR = 40\text{ Mbps}$             |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.2.5 Dynamic characteristics

**Table 21** Dynamic characteristics

| Parameter                                                          | Symbol                | Values |      |      | Unit          | Note or condition                                                                                                           |
|--------------------------------------------------------------------|-----------------------|--------|------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------|
|                                                                    |                       | Min.   | Typ. | Max. |               |                                                                                                                             |
| INx to OUTx turn-on propagation delay                              | $t_{PD\text{on}}$     | 21     | 26   | 32   | ns            | From 1.4 V level of rising input to 1.4 V level of corresponding rising output                                              |
| INx to OUTx turn-off propagation delay                             | $t_{PD\text{off}}$    | 21     | 26   | 32   | ns            | From 1.4 V level of falling input to 1.4 V level of corresponding falling output                                            |
| Part-to-part propagation delays mismatch                           | $\Delta t_{PD,p-p}$   |        |      | 6    | ns            | <sup>1)</sup>                                                                                                               |
| Codirectional channel-to-channel propagation delay mismatch        | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns            | Within same sample, over operating temperature range, same-direction channels, switching in the same direction              |
| Opposite-directional channel-to-channel propagation delay mismatch | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns            | Within same sample, over operating temperature range, opposite-directional channels, switching with the same signal level.  |
| Pulse width distortion                                             | $PWD$                 |        |      | 3    | ns            | $ t_{PD\text{off}} - t_{PD\text{on}} $ <sup>2)</sup>                                                                        |
| Input pulse width that changes output state                        | $t_{pw,min}$          | 10     | 11.5 | 15   | ns            | Measured with full range of input signal $V_{IN} = V_{DDI}$ <sup>3)</sup>                                                   |
| Output signal rise time                                            | $t_{rise}$            |        |      | 3.5  | ns            | 10% to 90% rising output, $C_{LOAD} = 15 \text{ pF}$ <sup>4)</sup>                                                          |
| Output signal fall time                                            | $t_{fall}$            |        |      | 3.5  | ns            | 90% to 10% falling output, $C_{LOAD} = 15 \text{ pF}$ <sup>4)</sup>                                                         |
| Default output delay time from input power loss                    | $t_{DO}$              |        | 0.4  | 2.6  | $\mu\text{s}$ | Measured from $V_{DDX(UVLO\text{off})} = 2.55 \text{ V}$ . Power supply ramp rate = $1 \text{ V}/\mu\text{s}$ <sup>5)</sup> |
| Time from UVLO to valid output data                                | $t_{PU}$              |        |      | 3    | $\mu\text{s}$ | Power supply ramp rate = $1 \text{ V}/\mu\text{s}$ , $DR > 6.6 \text{ Mbps}$ <sup>4)</sup>                                  |

- 1) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
- 2) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
- 3)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$
- 4) Parameter not tested in production
- 5) Maximum value tested in production



## 4 Thermal and electrical characteristics

### 4.7.3 Electrical characteristics - 3.3 V supply

Typical values are given at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = V_{DD2} = 3.3\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range of  $V_{DD1} = V_{DD2} = 3.3\text{ V} \pm 10\%$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching characteristics are tested with  $C_{LOAD} = 15\text{ pF}$  and 50% duty-cycle input square wave, over operating range unless otherwise specified. Supply current values are specified considering that all channels are switching at the same data rate. Parameters are tested in production unless otherwise specified. Supply current values are tested in production only for data rates up to 1 Mbps.

#### 4.7.3.1 Logic inputs

**Table 22** Logic inputs

| Parameter                                       | Symbol       | Values |      |      | Unit             | Note or condition                 |
|-------------------------------------------------|--------------|--------|------|------|------------------|-----------------------------------|
|                                                 |              | Min.   | Typ. | Max. |                  |                                   |
| High-level input current                        | $I_{IH}$     |        |      | 10   | $\mu\text{A}$    | $V_{INX} = V_{DDI}$ <sup>1)</sup> |
| Low-level input current                         | $I_{IL}$     | -10    |      |      | $\mu\text{A}$    | $V_{INX} = 0\text{ V}$            |
| Input voltage threshold for LH transition (TTL) | $V_{I\_LH}$  | 1.4    |      | 1.9  | V                |                                   |
| Input voltage threshold for HL transition (TTL) | $V_{I\_HL}$  | 1.0    |      | 1.4  | V                |                                   |
| Input voltage threshold hysteresis (TTL)        | $V_{I\_HYS}$ | 0.38   |      |      | V                |                                   |
| Input pull-down resistor                        | $R_{IN}$     |        | 825  |      | $\text{k}\Omega$ | $V_{INX} = V_{DDI}$ <sup>1)</sup> |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

#### 4.7.3.2 Logic outputs

**Table 23** Logic outputs

| Parameter                 | Symbol   | Values          |      |      | Unit | Note or condition                    |
|---------------------------|----------|-----------------|------|------|------|--------------------------------------|
|                           |          | Min.            | Typ. | Max. |      |                                      |
| High-level output voltage | $V_{OH}$ | $V_{DDO} - 0.3$ |      |      | V    | $I_{OH} = 2\text{ mA}$ <sup>1)</sup> |
| Low-level output voltage  | $V_{OL}$ |                 |      | 0.3  | V    | $I_{OL} = -2\text{ mA}$              |

1)  $V_{DDO}$  - Output-side supply voltage. For output buffers on side 1 it is  $V_{DD1}$  and for output buffers on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.3.3 Power supply - 2DIB041xF (2+0)

**Table 24** Power supply - 2DIB041xF (2+0)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition      |
|---------------------------|-----------------|--------|------|------|------|------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                        |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.6  | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD2}$       |        |      | 1    | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.6  | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - DC input | $I_{DD2}$       |        |      | 1    | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 2.1  | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.1  | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 4.5  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 1.8  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 8    | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 2.5  | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 14.5 | mA   | $DR = 40\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 4.2  | mA   | $DR = 40\text{ Mbps}$  |

#### 4 Thermal and electrical characteristics

##### 4.7.3.4 Power supply - 2DIB141xF (1+1)

**Table 25** Power supply - 2DIB141xF (1+1)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition                 |
|---------------------------|-----------------|--------|------|------|------|-----------------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                                   |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.39 | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.39 | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.39 | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.39 | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 1.65 | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.65 | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 3.4  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 3.5  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 5.4  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 5.5  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 9.2  | mA   | $DR = 40\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 9.6  | mA   | $DR = 40\text{ Mbps}$             |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.3.5 Dynamic characteristics

**Table 26** Dynamic characteristics

| Parameter                                                          | Symbol                | Values |      |      | Unit          | Note or condition                                                                                                           |
|--------------------------------------------------------------------|-----------------------|--------|------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------|
|                                                                    |                       | Min.   | Typ. | Max. |               |                                                                                                                             |
| INx to OUTx turn-on propagation delay                              | $t_{PD\text{on}}$     | 21     | 26   | 32   | ns            | From 1.4 V level of rising input to 1.4 V level of corresponding rising output                                              |
| INx to OUTx turn-off propagation delay                             | $t_{PD\text{off}}$    | 21     | 26   | 32   | ns            | From 1.4 V level of falling input to 1.4 V level of corresponding falling output                                            |
| Part-to-part propagation delays mismatch                           | $\Delta t_{PD,p-p}$   |        |      | 6    | ns            | <sup>1)</sup>                                                                                                               |
| Codirectional channel-to-channel propagation delay mismatch        | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns            | Within same sample, over operating temperature range, same-direction channels, switching in the same direction              |
| Opposite-directional channel-to-channel propagation delay mismatch | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns            | Within same sample, over operating temperature range, opposite-directional channels, switching with the same signal level   |
| Pulse width distortion                                             | $PWD$                 |        |      | 3    | ns            | $ t_{PD\text{off}} - t_{PD\text{on}} $ <sup>2)</sup>                                                                        |
| Input pulse width that changes output state                        | $t_{pw,min}$          | 10     | 11.5 | 15   | ns            | Measured with full range of input signal $V_{IN} = V_{DDI}$ <sup>3)</sup>                                                   |
| Output signal rise time                                            | $t_{rise}$            |        |      | 3.5  | ns            | 10% to 90% rising output, $C_{LOAD} = 15 \text{ pF}$ <sup>4)</sup>                                                          |
| Output signal fall time                                            | $t_{fall}$            |        |      | 3.5  | ns            | 90% to 10% falling output, $C_{LOAD} = 15 \text{ pF}$ <sup>4)</sup>                                                         |
| Default output delay time from input power loss                    | $t_{DO}$              |        | 0.4  | 2.6  | $\mu\text{s}$ | Measured from $V_{DDX(UVLO\text{off})} = 2.55 \text{ V}$ . Power supply ramp rate = $1 \text{ V}/\mu\text{s}$ <sup>5)</sup> |
| Time from UVLO to valid output data                                | $t_{PU}$              |        |      | 3    | $\mu\text{s}$ | Power supply ramp rate = $1 \text{ V}/\mu\text{s}$ , $DR > 6.6 \text{ Mbps}$ <sup>4)</sup>                                  |

- 1) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
- 2) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
- 3)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$
- 4) Parameter not tested in production
- 5) Maximum value tested in production

## 4 Thermal and electrical characteristics

### 4.7.4 Electrical characteristics - 2.7 V supply

Typical values are given at  $T_A = 25^\circ\text{C}$  with  $V_{DD1} = V_{DD2} = 2.7\text{ V}$ . Minimum/maximum specifications apply over the entire recommended operation range of  $V_{DD1} = V_{DD2} = 2.7\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted. Switching characteristics are tested with  $C_{LOAD} = 15\text{ pF}$  and 50% duty-cycle input square wave, over operating range unless otherwise specified. Supply current values are specified considering that all channels are switching at the same data rate. Parameters are not tested in production unless otherwise specified.

#### 4.7.4.1 Logic inputs

**Table 27** Logic inputs

| Parameter                                       | Symbol       | Values |      |      | Unit          | Note or condition                    |
|-------------------------------------------------|--------------|--------|------|------|---------------|--------------------------------------|
|                                                 |              | Min.   | Typ. | Max. |               |                                      |
| High-level input current                        | $I_{IH}$     |        |      | 10   | $\mu\text{A}$ | $V_{INX} = V_{DDI}$ <sup>1) 2)</sup> |
| Low-level input current                         | $I_{IL}$     | -10    |      |      | $\mu\text{A}$ | $V_{INX} = 0\text{ V}$ <sup>2)</sup> |
| Input voltage threshold for LH transition (TTL) | $V_{I\_LH}$  | 1.4    |      | 1.9  | V             |                                      |
| Input voltage threshold for HL transition (TTL) | $V_{I\_HL}$  | 1.0    |      | 1.4  | V             |                                      |
| Input voltage threshold hysteresis (TTL)        | $V_{I\_HYS}$ | 0.38   |      |      | V             |                                      |
| Input pull-down resistor                        | $R_{IN}$     |        | 825  |      | k $\Omega$    | $V_{INX} = V_{DDI}$ <sup>1) 2)</sup> |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

2) Parameter tested in production

#### 4.7.4.2 Logic outputs

**Table 28** Logic outputs

| Parameter                 | Symbol   | Values          |      |      | Unit | Note or condition                    |
|---------------------------|----------|-----------------|------|------|------|--------------------------------------|
|                           |          | Min.            | Typ. | Max. |      |                                      |
| High-level output voltage | $V_{OH}$ | $V_{DDO} - 0.3$ |      |      | V    | $I_{OH} = 1\text{ mA}$ <sup>1)</sup> |
| Low-level output voltage  | $V_{OL}$ |                 |      | 0.3  | V    | $I_{OL} = -1\text{ mA}$              |

1)  $V_{DDO}$  - Output-side supply voltage. For output buffers on side 1 it is  $V_{DD1}$  and for output buffers on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.4.3 Power supply - 2DIB041xF (2+0)

**Table 29** Power supply - 2DIB041xF (2+0)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition      |
|---------------------------|-----------------|--------|------|------|------|------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                        |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.6  | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.0  | mA   | $V_{INx} = V_{DD1}$    |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.6  | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.0  | mA   | $V_{INx} = 0\text{ V}$ |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 2    | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.0  | mA   | $DR = 1\text{ Mbps}$   |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 4.5  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 1.8  | mA   | $DR = 10\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 8    | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 2.5  | mA   | $DR = 20\text{ Mbps}$  |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 14.5 | mA   | $DR = 40\text{ Mbps}$  |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 4    | mA   | $DR = 40\text{ Mbps}$  |

#### 4 Thermal and electrical characteristics

##### 4.7.4.4 Power supply - 2DIB141xF (1+1)

**Table 30** Power supply - 2DIB141xF (1+1)

| Parameter                 | Symbol          | Values |      |      | Unit | Note or condition                 |
|---------------------------|-----------------|--------|------|------|------|-----------------------------------|
|                           |                 | Min.   | Typ. | Max. |      |                                   |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.35 | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.35 | mA   | $V_{INx} = V_{DDI}$ <sup>1)</sup> |
| Supply current - DC input | $I_{DD1}$       |        |      | 1.35 | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - DC input | $I_{DD2}$       |        |      | 1.35 | mA   | $V_{INx} = 0\text{ V}$            |
| Supply current - AC input | $I_{DD1\_1Mb}$  |        |      | 1.55 | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD2\_1Mb}$  |        |      | 1.55 | mA   | $DR = 1\text{ Mbps}$              |
| Supply current - AC input | $I_{DD1\_10Mb}$ |        |      | 3.1  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_10Mb}$ |        |      | 3.2  | mA   | $DR = 10\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_20Mb}$ |        |      | 5.2  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_20Mb}$ |        |      | 5.4  | mA   | $DR = 20\text{ Mbps}$             |
| Supply current - AC input | $I_{DD1\_40Mb}$ |        |      | 8.8  | mA   | $DR = 40\text{ Mbps}$             |
| Supply current - AC input | $I_{DD2\_40Mb}$ |        |      | 9.4  | mA   | $DR = 40\text{ Mbps}$             |

1)  $V_{DDI}$  - Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$

#### 4 Thermal and electrical characteristics

##### 4.7.4.5 Dynamic characteristics

**Table 31** Dynamic characteristics

| Parameter                                                          | Symbol                | Values |      |      | Unit    | Note or condition                                                                                                                       |
|--------------------------------------------------------------------|-----------------------|--------|------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------|
|                                                                    |                       | Min.   | Typ. | Max. |         |                                                                                                                                         |
| INx to OUTx turn-on propagation delay                              | $t_{PDOn}$            | 21     | 26   | 32   | ns      | From 1.4 V level of rising input to 1.4 V level of corresponding rising output <sup>1)</sup>                                            |
| INx to OUTx turn-off propagation delay                             | $t_{PDOff}$           | 21     | 26   | 32   | ns      | From 1.4 V level of falling input to 1.4 V level of corresponding falling output <sup>1)</sup>                                          |
| Part-to-part propagation delays mismatch                           | $\Delta t_{PD,p-p}$   |        |      | 6    | ns      | <sup>2) 3)</sup>                                                                                                                        |
| Codirectional channel-to-channel propagation delay mismatch        | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns      | Within same sample, over operating temperature range, same-direction channels, switching in the same direction <sup>2)</sup>            |
| Opposite-directional channel-to-channel propagation delay mismatch | $\Delta t_{PD,Ch-Ch}$ |        |      | 3    | ns      | Within same sample, over operating temperature range, opposite-directional channels, switching with the same signal level <sup>2)</sup> |
| Pulse width distortion                                             | $PWD$                 |        |      | 3    | ns      | $ t_{PDOff} - t_{PDOn} $ <sup>2) 4)</sup>                                                                                               |
| Input pulse width that changes output state                        | $t_{pw,min}$          | 10     | 11.5 | 15   | ns      | Measured with the full range of input signal $V_{IN} = V_{DDI}$ <sup>2) 5)</sup>                                                        |
| Output signal rise time                                            | $t_{rise}$            |        |      | 3    | ns      | 10% to 90% rising output, $C_{LOAD} = 15$ pF                                                                                            |
| Output signal fall time                                            | $t_{fall}$            |        |      | 3    | ns      | 90% to 10% falling output, $C_{LOAD} = 15$ pF                                                                                           |
| Default output delay time from input power loss                    | $t_{DO}$              |        | 0.4  | 2.6  | $\mu s$ | Measured from $V_{DDX(UVLOoff)} = 2.55$ V. Power supply ramp rate = 1 V/ $\mu s$                                                        |
| Time from UVLO to valid output data                                | $t_{PU}$              |        |      | 3    | $\mu s$ | Power supply ramp rate = 1 V/ $\mu s$ , DR > 6.6 Mbps                                                                                   |

1) Parameter tested in production

2) Parameter tested in production

3) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature

4) Also known as pulse skew. The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range

5)  $V_{DDI}$  = Input-side supply voltage. For input channels on side 1 it is  $V_{DD1}$  and for input channels on side 2 it is  $V_{DD2}$



## 4 Thermal and electrical characteristics

### 4.8 Insulation and safety-related specifications

This digital isolator is suitable for the rated insulation only within the safety-limiting values. Compliance with these safety-limiting values must be ensured by means of suitable protective circuits.

#### 4.8.1 Insulation characteristics

| Parameter                                     | Symbol     | Value         | Unit | Note or condition                                                                                                  |
|-----------------------------------------------|------------|---------------|------|--------------------------------------------------------------------------------------------------------------------|
| External clearance                            | <i>CLR</i> | >4            | mm   | Shortest distance in air from any input pin to any output pin according to IEC 60664-1 <sup>1)</sup>               |
| External creepage                             | <i>CRP</i> | >4            | mm   | Shortest distance over package surface from any input pin to any output pin according to IEC 60664-1 <sup>1)</sup> |
| Comparative tracking index                    | <i>CTI</i> | >400          | V    | According to IEC 60112                                                                                             |
| Material group                                |            | II            |      | According to IEC 60112                                                                                             |
| Pollution degree                              |            | 2             |      | According to IEC 60664-1                                                                                           |
| Overvoltage category according to IEC 60664-1 | -          | I - IV        |      | Rated mains voltage $\leq 150 V_{rms}$                                                                             |
|                                               | -          | I - III       |      | Rated mains voltage $\leq 300 V_{rms}$                                                                             |
|                                               | -          | I - II        |      | Rated mains voltage $\leq 600 V_{rms}$                                                                             |
|                                               | -          | I             |      | Rated mains voltage $\leq 1000 V_{rms}$                                                                            |
| Climatic category                             |            | 40/125<br>/21 |      |                                                                                                                    |

#### Input-to-output isolation according to UL1577 Ed. 5 <sup>2)</sup>

|                                   |           |      |           |                                                                                                                               |
|-----------------------------------|-----------|------|-----------|-------------------------------------------------------------------------------------------------------------------------------|
| Input-to-output isolation voltage | $V_{ISO}$ | 3000 | $V_{rms}$ | $V_{TEST} = V_{ISO}$ for $t = 60$ s (qualification);<br>$V_{TEST} = 1.2 \times V_{ISO}$ for $t = 1$ s (100% productive tests) |
|-----------------------------------|-----------|------|-----------|-------------------------------------------------------------------------------------------------------------------------------|

#### Input-to-output isolation according to DIN VDE 0884-17, IEC 60747-17 <sup>3)</sup>

|                                            |            |      |          |                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------|------------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Maximum rated transient isolation voltage  | $V_{IOTM}$ | 4242 | $V_{pk}$ | $V_{TEST} = 1.2 \times V_{IOTM}$ for $t_{ini} = 1$ s                                                                                                                                                                                                                                                                                                        |
| Maximum impulse voltage                    | $V_{IMP}$  | 4242 | $V_{pk}$ | According to IEC 60664-1, IEC 60747-17                                                                                                                                                                                                                                                                                                                      |
| Maximum rated repetitive isolation voltage | $V_{IORM}$ | 1000 | $V_{pk}$ |                                                                                                                                                                                                                                                                                                                                                             |
| Apparent charge                            | $q_{PD}$   | <5   | pC       | Method (b1) (routine test and type test preconditioning)<br>$V_{PD(ini)} = 1.2 \times V_{IOTM}$ for $t_{ini} = 1$ s<br>$V_{PD(m)} > 1.65 \times V_{IORM}$ for $t_m = 1$ s <sup>4)</sup><br><br>Method (a) (type test, subgroup 1 final measurements)<br>$V_{PD(ini)} = V_{IOTM}$ for $t_{ini} = 60$ s<br>$V_{PD(m)} = 1.3 \times V_{IORM}$ for $t_m = 10$ s |

#### 4 Thermal and electrical characteristics

| Parameter                          | Symbol      | Value      | Unit     | Note or condition                                                              |
|------------------------------------|-------------|------------|----------|--------------------------------------------------------------------------------|
| Maximum surge isolation voltage    | $V_{IOSM}$  | 6000       | $V_{pk}$ | $V_{TEST} = 1.3 \times V_{IOSM}$ <sup>5)</sup>                                 |
| Isolation resistance <sup>7)</sup> | $R_{IO}$    | $>10^{12}$ | $\Omega$ | $V_{IO} = 500 V_{dc}$ for $t = 60 s$ , $T_A = 25^\circ C$ <sup>6)</sup>        |
|                                    |             | $>10^{11}$ | $\Omega$ | $V_{IO} = 500 V_{dc}$ for $t = 60 s$ , $T_A = 125^\circ C$ <sup>6)</sup>       |
|                                    | $R_{IO\_S}$ | $>10^9$    | $\Omega$ | $V_{IO} = 500 V_{dc}$ for $t = 60 s$ , $T_A = T_S = 150^\circ C$ <sup>6)</sup> |
| Isolation capacitance              | $C_{IO}$    | $<2$       | pF       | $f = 1 MHz$ <sup>6)</sup> <sup>7)</sup>                                        |

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standards. Care should be taken to keep the required creepage and clearance value on printed circuit board level.

2) See UL1577 certificate n. E311313.

3) Safety certification planned. The IEC 60747-17 and its German equivalent VDE 0884-17 is the successor of the component standard VDE 0884-11, which will expire in 2023.

4) The partial discharge voltage  $V_{PD(m)}$  applied during productive tests is greater ( $2110 V_{pk} > 1.65 \times V_{IORM}$ ) to include the  $F_4$  factor (1.1) that takes into account the maximum deviation of the mains supply voltage from its nominal value as specified by the end-equipment standards IEC 60664-1, IEC 62368-1 ( $V_{PD(m)} = F_1 \times F_2 \times F_4 \times V_{IORM} = 1.5 \times F_4 \times V_{IORM}$ ).

5) The surge test is performed in insulation oil to determine the intrinsic surge immunity of the insulation barrier.

6) The parameters apply to the product configured as a two terminals device with all terminals on side 1 connected together and all terminals on side 2 connected together.

7) Parameter not tested in production.

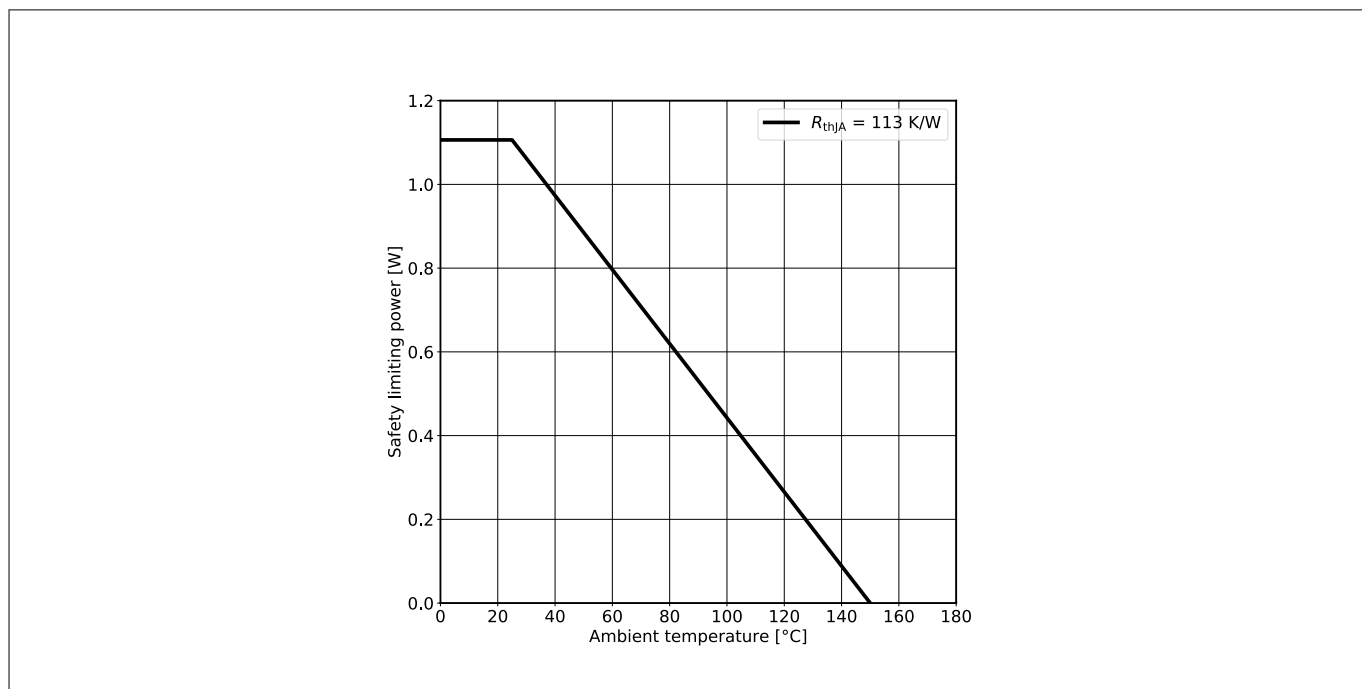
## 4 Thermal and electrical characteristics

### 4.8.2 Safety-limiting values

This digital isolator is suitable for the rated insulation only within the safety-limiting values. Compliance with these safety-limiting values must be ensured by means of suitable protective circuits.

| Parameter                          | Symbol      | Value | Unit | Note or condition                                                                                               |
|------------------------------------|-------------|-------|------|-----------------------------------------------------------------------------------------------------------------|
| Maximum ambient safety temperature | $T_S$       | 150   | °C   |                                                                                                                 |
| Safety power dissipation           | $P_S$       | 1.10  | W    | $R_{thJA} = 113 \text{ K/W}$ , $T_A = 25^\circ\text{C}$ , $T_J = 150^\circ\text{C}$                             |
| Safety supply current              | $I_{S,TOT}$ | 220   | mA   | $R_{thJA} = 113 \text{ K/W}$ , $T_A = 25^\circ\text{C}$ , $T_J = 150^\circ\text{C}$ , $V_{DDX} = 5.0 \text{ V}$ |

#### 4.8.2.1 Thermal derating curve



**Figure 22 Thermal derating curve**

## **5 Application and Implementation**

### **5.1 Detailed Description**

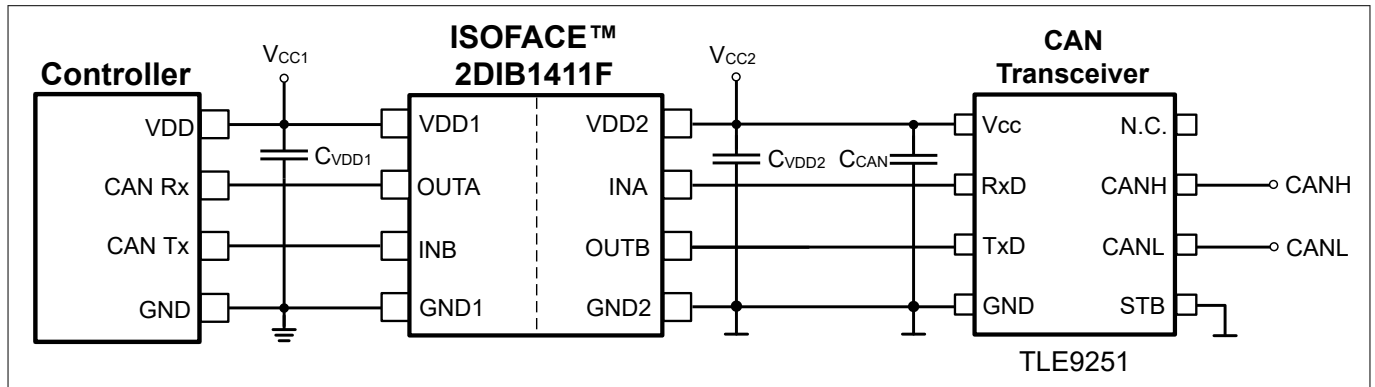
ISOFACE™ 2DIBx41xF is a family of high-performance digital isolators enabling robust data transmission over a SiO<sub>2</sub> isolation barrier. These devices have a very wide operating supply voltage range of 2.7 V to 6.5 V on both sides of the isolation barrier. Each side of the digital isolator can be independently supplied with any voltage between 2.7 V and 6.5 V irrespective of the supply voltage on the other side. For example, side 1 ( $V_{DD1}$ ) of the digital isolator could be supplied with 3.3 V and side 2 ( $V_{DD2}$ ) with 5 V. Therefore, these digital isolators in addition to providing safety isolation also act as logic-level translators in applications that are powered by different supply voltages.

The ISOFACE™ 2DIBx41xF family features fixed TTL input configurations for high noise immunity and signal integrity ensuring robust signal transmission in noisy environments. Only two external bypass capacitors (one on each side of the digital isolators) of 0.1  $\mu$ F are needed for proper functionality, thereby facilitating high-density PCB designs compared to optical isolators. An internal glitch filter on the inputs of each channel filters any signals below 10 ns, thereby preventing unwanted noise from corrupting the original data. With 3000  $V_{rms}$  isolation voltage ( $V_{ISO}$  according to UL1577), ISOFACE™ 2DIBx41xF digital isolators are highly suitable for isolating gate-drive PWM signals from microcontrollers or isolating a bi-directional communication interface such as Controller Area Network (CAN) or Universal Asynchronous Receiver Transmitter (UART).



## 5 Application and Implementation

### 5.2.2 Isolating communication interfaces



**Figure 24** Typical application - Functional isolation of Controller Area Network (CAN) communication

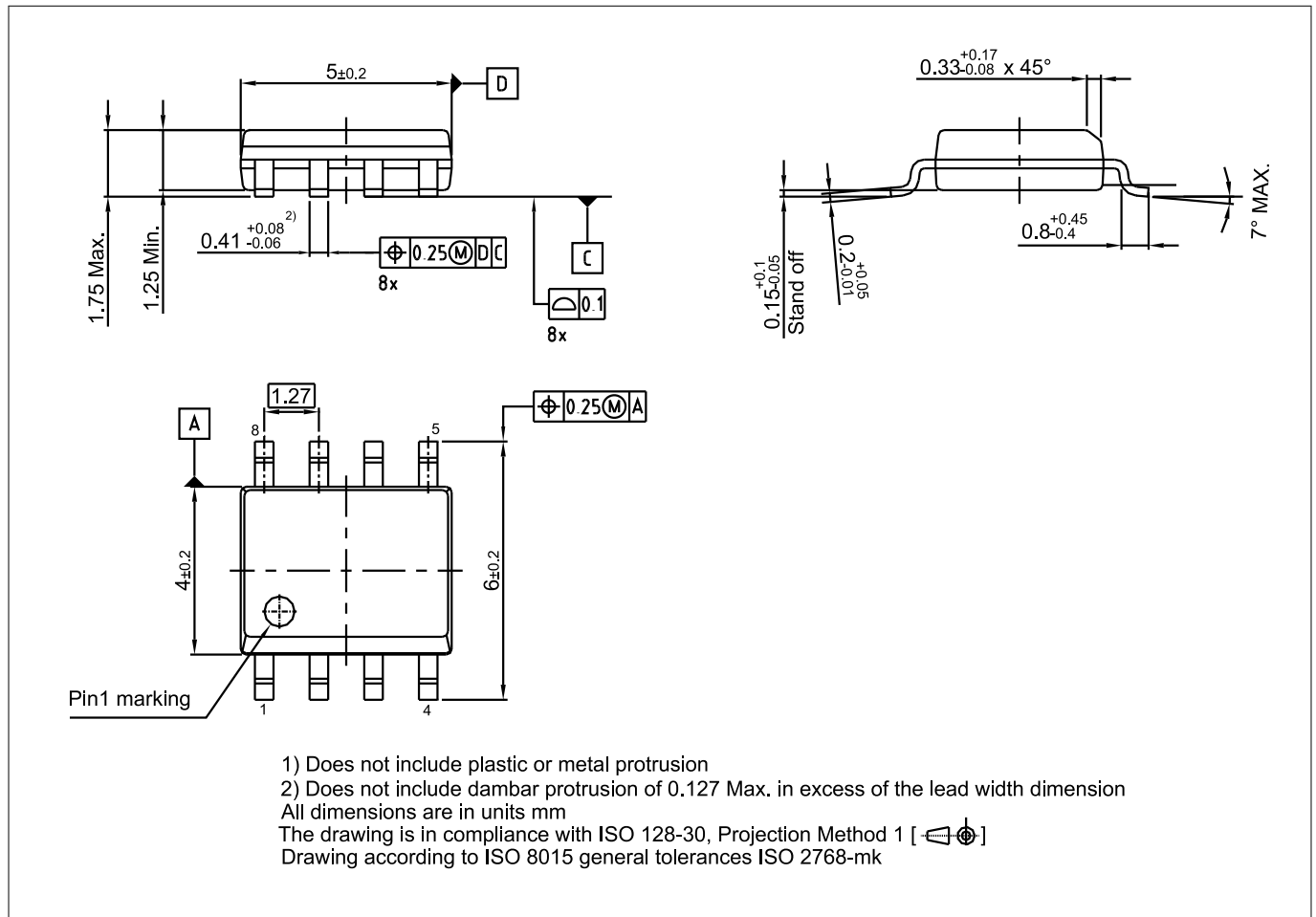
Figure 24 shows an example application where the ISOFACE™ 2DIB1411F is used to isolate a CAN communication interface. The digital isolator is used to isolate the TxD and RxD signals from the microcontroller to a high speed CAN FD transceiver like TLE 9251. Side 1 of the digital isolator is powered from the same supply ( $V_{CC1}$ ) as the microcontroller with either 3.3 V or 5 V, irrespective of the supply voltage on side 2 ( $V_{CC2}$ ), which is powered with the same supply as the CAN transceiver. With a maximum data rate of 40 Mbps and a very low pulse-width distortion (< 3 ns), the ISOFACE™ 2DIB1411F digital isolator ensures reliable communication in isolating high speed CAN FD transceivers. The variant with high as default output state is selected for this application since the default state of the CAN communication bus is logical high.

## 6 Package dimensions

### 6 Package dimensions

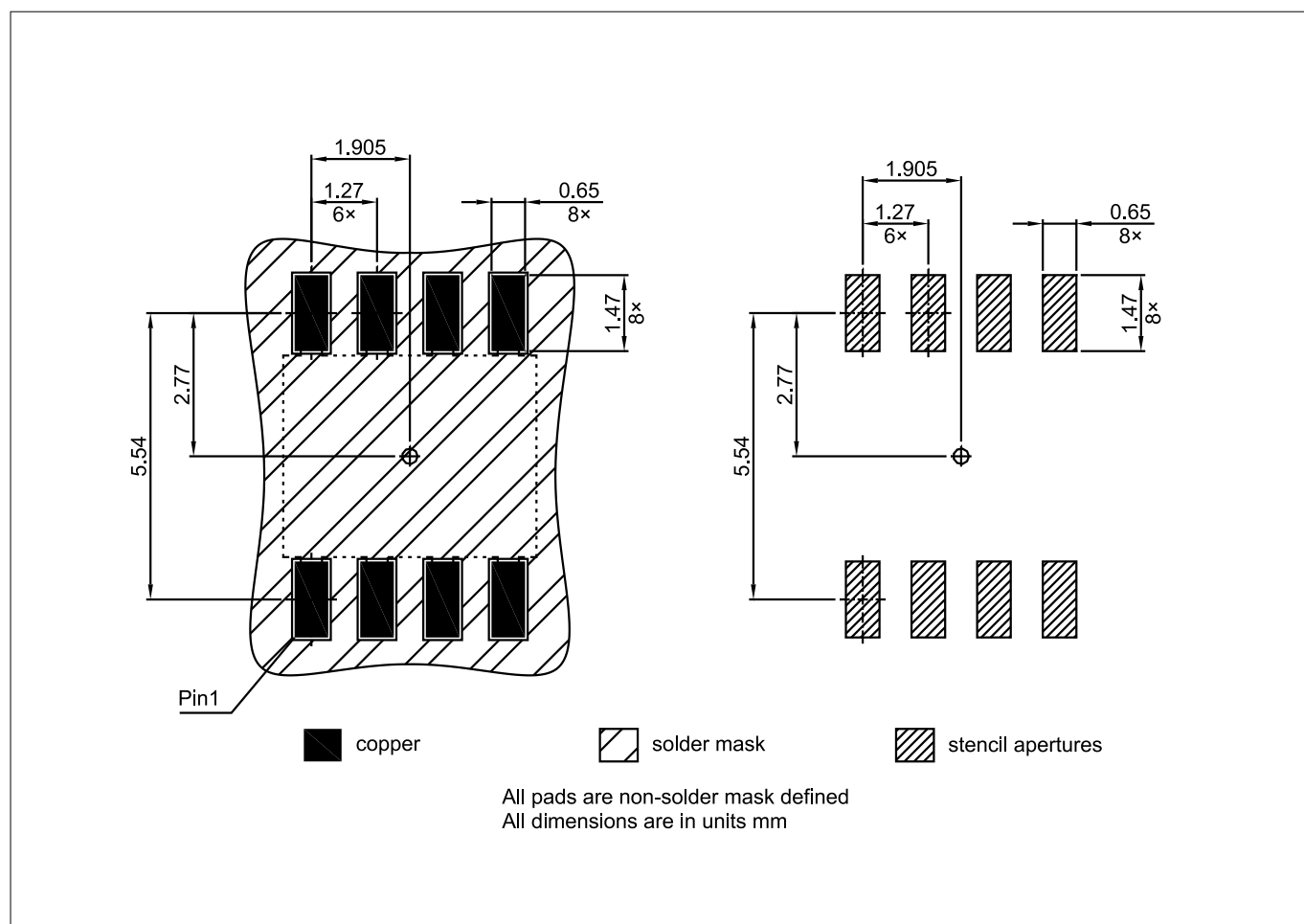
The package dimensions of dual-channel digital isolator are provided.

#### Package PG-DSO-8 narrow-body 150-mil



**Figure 25 PG-DSO-8 narrow-body 150-mil outline**

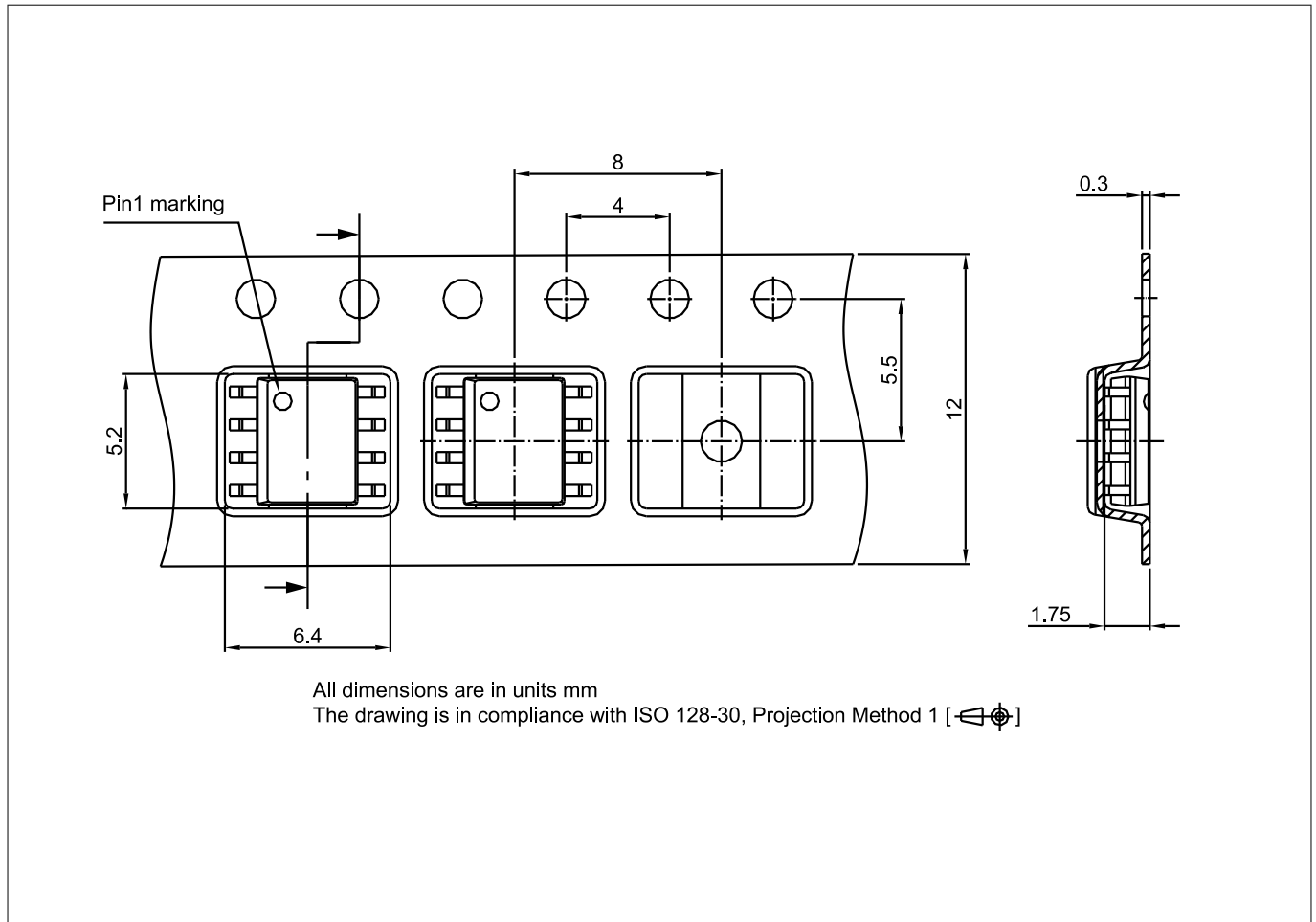
**6 Package dimensions**



**Figure 26 PG-DSO-8 narrow-body 150-mil footprint**



## 6 Package dimensions



**Figure 27** PG-DSO-8 narrow-body 150-mil packing

### Green product (RoHS-compliant)

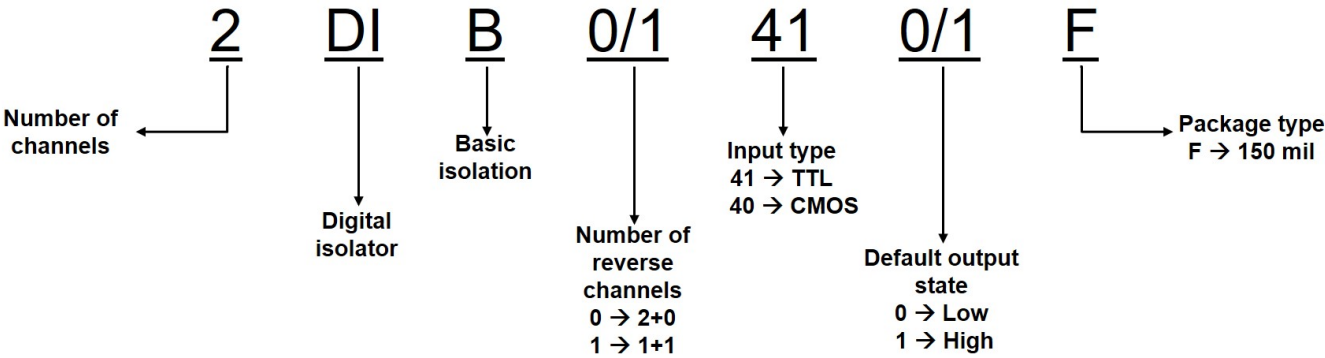
To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (i.e. they have Pb-free finish on leads and are suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Further information on packages:** <https://www.infineon.com/packages>

7 Ordering guide

7 Ordering guide

| Orderable part number (OPN) | Part number | Channel configuration     | Default output state | Input thresholds | Package marking |
|-----------------------------|-------------|---------------------------|----------------------|------------------|-----------------|
| 2DIB0410FXUMA1              | 2DIB0410F   | 2 forward 0 reverse (2+0) | Low                  | Fixed (TTL)      | 2B0410A         |
| 2DIB0411FXUMA1              | 2DIB0411F   |                           | High                 |                  | 2B0411A         |
| 2DIB1410FXUMA1              | 2DIB1410F   | 1 forward 1 reverse (1+1) | Low                  |                  | 2B1410A         |
| 2DIB1411FXUMA1              | 2DIB1411F   |                           | High                 |                  | 2B1411A         |



## 8 Revision history

### 8 Revision history

| Revision number | Major changes since previous revision                                   |
|-----------------|-------------------------------------------------------------------------|
| 2.0, 2024-07-25 | Corrected value of the Isolation resistance at high ambient temperature |
| 1.0, 2023-03-22 | Datasheet initial release                                               |

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