EiceDRIVER™ gate driver 1EDI3051AS

Single channel isolated IGBT/SiC-MOSFET driver

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AEC Qualified | RoHS | ISO 26262 compliant

Features

- Single channel isolated IGBT/SiC driver using coreless transformer technology
- For IGBTs/SiC-MOSFETs up to 1200 V
- Integrated SPI
- CMTI up to 150 V/ns up to 1000 V
- 8 kV basic insulation according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10
- Basic insulation according to UL 1577
- Integrated booster with up to 20 A peak current rail-to-rail split output
- Integrated flyback controller
- Dual monitoring/clamping for parallel power device driving
- Safety inputs for primary ASC trigger and PWM control
- Propagation delay 60 ns typical
- Internal and external active Miller clamp supports unipolar switching
- Integrated dual ADC for temperature or DC-Link voltage measurement
- Integrated safety features to support ASIL D on system level:
  - Redundant DESAT and OCP protection
  - Differential overcurrent protection with matched impedance inputs
  - Gate and output stage monitoring
  - LV/HV supply monitoring
  - Internal supervision
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL B
- Green Product (RoHS compliant)

Potential applications

- Traction inverters for HEV and EV
- High power DC/DC converter

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

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1 Description

The EiceDRIVER™ gate driver 1EDI3051AS is a high-voltage IGBT/SiC driver designed for automotive motor drives above 50 kW. The device is based on Infineon's Coreless Transformer (CT) technology, providing galvanic insulation between low voltage and high voltage domains. The device has been designed to support 600 V, 750 V and 1200 V IGBT/SiC-MOSFET technologies.

The device is connected to a 5 V logic on the low voltage (primary) side.

On the high voltage (secondary) side, the device is dimensioned to drive IGBTs/SiC-MOSFETs directly . Short propagation delays and controlled internal tolerances lead to a minimal distortion of the PWM signal.

The device features an output stage of minimum 20 A peak current. In addition, there is a dual Miller clamping stage with typically 5 A integrated, and on top it also supports an external Clamp transistor drive.

A large panel of safety-related functions have been implemented in the device in order to support functional safety requirements at system level (as per ISO 26262). These integrated features ease the implementation of transition to safe-state.

A flyback converter controller integrated to the primary side of the device supports the installation of the isolated supply domain.

Type	Package	Marking
1EDI3051AS	PG-DSO-36	1EDI3051AS

2 Block diagram

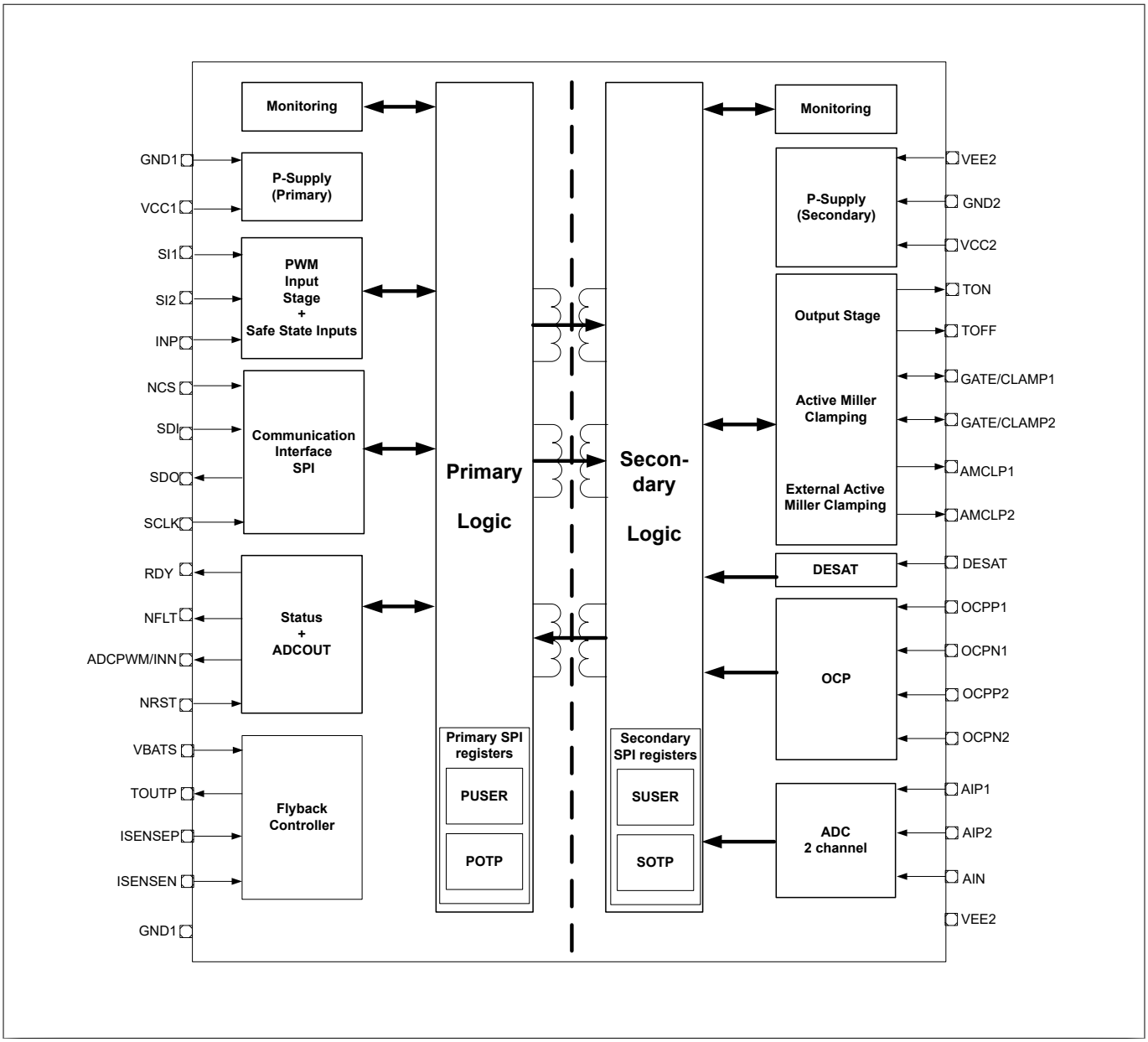

Figure 1 Block diagram

3 Pin configuration

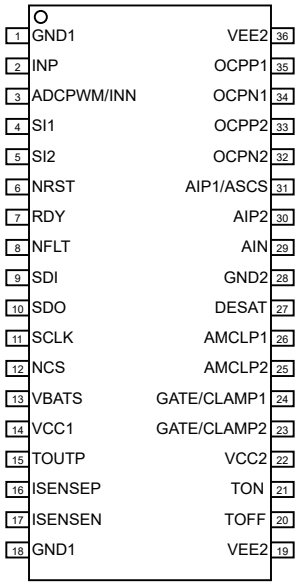

Figure 2 Pin assignment

3.1 Pin definitions and functions

Table 1 Pin definitions and functions

Pin #	Pin name	I/O	Function
1	GND1	Ground	Ground connection for the primary side.
2	INP	Input	The non-inverting PWM signal of the driver. An internal weak pull-down resistor to GND1 drives this input to low state in case the pin is floating.
3	INN/ ADCPWM	Input/ output	The inverting PWM signal is used for monitoring for shoot-through protection. An internal weak pull-up resistor to VCC1 drives this input to high state in case the pin is floating. This pin can be configured as ADCPWM signal for ADC data. In this case it is a push-pull output which is driving a PWM signal according to the data.
4	SI1	Input	The safe state input 1 sets PWM ON/OFF or triggers a primary ASC. Functionality corresponds to pin state of SI2. An internal weak pull-down resistance is disabling the device in case the pin is floating.
5	SI2	Input	The safe state input 2 sets PWM ON/OFF or primary ASC. Functionality corresponds to pin state of SI1. An internal weak pull-down resistance is disabling the device in case the pin is floating.
6	NRST	Input	The reset signal is used to clear the failure/fault events which triggered RDY or NFLT active low. The signal is clearing an error on rising edge. An internal pull-down resistance is driving this pin to low state in case the pin is floating.

(table continues...)

3 Pin configuration

Table 1 (continued) Pin definitions and functions

Pin #	Pin name	I/O	Function
7	RDY	Output	The ready open-drain signal is used to report failure events of Event Class B (like UVLO1, UVLO2, OVLO2, UVLO3, OVLO3, life sign lost, output stage error, gate monitoring error, etc.). As a result this pin is driven to low. This pin has to be connected externally to VCC1 with a pull-up resistance
8	NFLT	Output	The fault open-drain signal is used to report failure events triggered by DESAT or OCP protection. As a result the pin is driven to low. This pin has to be connected externally to VCC1 with a pull-up resistance
9	SDI	Input	The serial data signal is used for the SPI interface. An internal weak pull-down device to GND1 drives this pin to low state in case it is floating.
10	SDO	Output	Serial Data Output (push-pull) for the SPI interface.
11	SCLK	Input	The serial clock signal is used for the SPI interface. An internal weak pull-down device to GND1 drives this pin to low state in case it is floating.
12	NCS	Input	This pin is used as chip select signal for the SPI interface or as ADC data output selection (1 or 2). This signal is low active (chip select). An internal weak pull-up to VCC1 drives this pin to high state in case it is floating. The data of ADC is shown on ADCPWM according to the given signal (low = ADC 1, high = ADC 2).
13	VBATS	Input	This pin is used for battery voltage sensing for the flyback controller. Connect to GND1 with R_{VDBAT2} and to VBAT with R_{VDBAT1} when used. When not used connect to either VCC1 directly or with R_{VDBAT2} to GND1.
14	VCC1	Supply	5 V power supply for the primary side (referring to GND1).
15	TOUTP	Output	The gate drive signal is used for controlling the external NMOS of the flyback.
16	ISENSEP	Input	The positive current sense signal for the flyback controller must be connected to an external shunt. This signal is differential therefore it must be routed close to ISENSEN signal. A common-mode filter should be applied to the ISENSEN signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
17	ISENSEN	Input	The negative current sense signal is used as a reference for the flyback controller and must be connected to an external shunt. This signal is differential therefore it must be routed close to ISENSEP signal. A common-mode filter should be applied to the ISENSEP signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
18	GND1	Ground	Ground connection for the primary side.
19	VEE2	Supply	Negative power supply for the secondary side (referring to GND2).
20	TOFF	Input/ output	The transistor OFF signal switches the IGBT/SiC-MOSFET gate to VEE2 according to the PWM input.
21	TON	Input/ output	The transistor ON signal switches the IGBT/SiC-MOSFET gate to VCC2 according to the PWM input.
22	VCC2	Output	Positive power supply for the secondary side (referring to GND2).
23	GATE/ CLAMP2	Output	The gate monitoring 2 and internal active miller clamp 2 signal is monitoring the gate of the second IGBT/SiC-MOSFET and can detect different thresholds. This signal is clamping the gate to VEE2, if the clamping threshold is reached.

(table continues...)

Table 1 (continued) Pin definitions and functions

Pin #	Pin name	I/O	Function
24	GATE/ CLAMP1	Output	The gate monitoring 1 and internal active miller clamp 1 signal is monitoring the gate of the first IGBT/SiC-MOSFET and can detect different thresholds. This signal is clamping the gate to VEE2, if the clamping threshold is reached.
25	AMCLP2	Output	The external active Miller clamp 2 signal is driving the gate of an external active Miller clamping transistor (NMOS).
26	AMCLP1	Output	The external active Miller clamp 2 signal is driving the gate of an external active Miller clamping transistor (NMOS).
27	DESAT	Input	The DESAT protection signal monitors the voltage across the power switch. An internal current source to VCC2 drives this signal to high level in case it is floating.
28	GND2	Ground	Reference ground for the secondary side.
29	AIN	Analog Ground	The ADC common ground pin is the reference of the measurement of the ADC on AIP1/2.
30	AIP2	Input	The ADC2 signal can be used to monitor voltages or temperatures at the IGBT/SiC-MOSFET. An internal, configurable current source supplies external components.
31	AIP1/ASCS	Input	The ADC1 signal can be used to monitor voltages or temperatures at the IGBT/SiC-MOSFET. An internal, configurable current source supplies external components. This pin can be configured as a secondary side ASC pin. In this case it is used to switch the gate of the power switch on. This signal has higher priority as PWM and will overrule other inputs according to the rules of this specification.
32	OCPN2	Input	The negative overcurrent protection 2 signal is differential therefore it should be routed close to OCPP signal. A common-mode filter should be applied to the OCPP signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
33	OCPP2	Input	The positive overcurrent protection 2 signal is differential therefore it should be routed close to OCPN signal. A common-mode filter should be applied to the OCPN signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
34	OCPN1	Input	The negative overcurrent protection 1 signal is differential therefore it should be routed close to OCPP signal. A common-mode filter should be applied to the OCPP signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
35	OCPP1	Input	The positive overcurrent protection 1 signal is differential therefore it should be routed close to OCPN signal. A common-mode filter should be applied to the OCPN signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
36	VEE2	Supply	Negative power supply for the secondary side (referring to GND2).

4 General product characteristics

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	V_{VCC1_MAX}	-0.3	–	7	V	Referenced to GND1	PRQ-39
Positive power supply (secondary)	V_{VCC2_MAX}	-0.3	–	30	V	Referenced to GND2	PRQ-40
Negative power supply (secondary)	V_{VEE2_MAX}	-13	–	0.3	V	Referenced to GND2	PRQ-41
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2-VEE2\_MAX}$	–	–	40	V		PRQ-42
Maximum voltages on digital I/O pin on primary side (INP, NRST, RDY, SI1, SI2, ADCPWM, SDO, SDI, NCS ,SCLK, NFLT)	V_{INDx_MAX}	-0.3	–	V_{VCC1} + 0.3	V	Referenced to GND1	PRQ-479
AIPx maximum voltage	V_{AIPx_MAX}	-0.3	–	V_{CC2}+0.3	V		PRQ-45
AIN maximum voltage	V_{AIN_MAX}	-0.3	–	+0.3	V	referenced to GND2	PRQ-526
DESAT maximum voltage	V_{DESAT_MAX}	-0.7	–	V_{VCC2} + 0.3	V	Referenced to GND2, I_{DESAT} = 50 mA for 500 ns	PRQ-46
OCPPx maximum voltage	V_{OCPPx_MAX}	-2.8	–	2.8	V	Referenced to GND2	PRQ-47
OCPNx maximum voltage	V_{OCPNx_MAX}	-2.8	–	2.8	V	Referenced to GND2	PRQ-48
AMCLPx maximum voltage	V_{AMCLPx_MAX}	- 0.3	–	V_{AMCLP} + 2.8	V	Referenced to VEE2, $V_{AMCLPx\_MAX} \leq V_{VCC2}$ + 0.3 V	PRQ-883
GATE/CLAMPx maximum voltage	V_{GATEx_MAX}	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-49
TON/TOFF maximum voltage	$V_{TON-TOFF\_MAX}$	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-50

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate drive high maximum source current	$I_{TON\_H\_MAX}$	-20	–	–	A	t_{MAX} = 0.5 µs, non-repetitive	PRQ-51
Gate drive low maximum sink current	$I_{TOFF\_L\_MAX}$	–	–	20	A	t_{MAX} = 0.5 µs, non-repetitive	PRQ-52
AMCLPx low maximum sink current	$I_{AMCLPx\_low\_Max}$	–	–	3	A	t_{MAX} = 100 ns; non-repetitive; using external clamp transistor	PRQ-53
AMCLPx high maximum source current	$I_{AMCLPx\_high\_Max}$	-1.1	–	–	A	t_{MAX} = 100 ns; non-repetitive; using external clamp transistor	PRQ-64
CLAMPx low maximum output current	I_{CLAMPx_Max}	–	–	7.5	A	t_{MAX} = 1.5 µs; non-repetitive; internal clamping transistor used;	PRQ-58
Maximum current on output logic pins (ADCPWM, RDY, NFLT, SDO)	$\lvert I_{OUTx\_MAX} \rvert$	–	–	10	mA		PRQ-54
HBM robustness, all pins	$V_{ESD,HBM}$	-2	–	2	kV	Human Body Model "HBM" robustness: class2 according to AEC-Q100-002	PRQ-55
CDM robustness, all pins	$V_{ESD,CDM1}$	–	–	500	TC	Charged Device Model "CDM" robustness: class C2a according to AEC-Q100-011 Rev D. "TC" corresponds to "Test Condition" according to AEC-Q100-011	PRQ-808

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CDM robustness, corner pins (VEE2, GND1)	$V_{ESD,CDM2}$	–	–	750	TC	Charged Device Model "CDM" robustness: class C2a according to AEC-Q100-011 Rev D. "TC" corresponds to "Test Condition" according to AEC-Q100-011	PRQ-810
Storage junction temperature	T_{s_MAX}	-55	–	150	°C		PRQ-56
Junction temperature	T_{J_MAX}	-40	–	150	°C		PRQ-57
Maximum voltage on TOUTP pin on primary side	V_{TOUTP_MAX}	-0.3	–	V_{VCC1} + 0.3	V	Referenced to GND1	PRQ-60
TOUTP low maximum sink current	$I_{TOUTP\_L\_MAX}$	–	–	1.5	A	Referenced to GND1, t = 1.5 µs, non-repetitive, T_{amb}= 25°C	PRQ-65
TOUTP high maximum source current	$I_{TOUTP\_H\_MAX}$	-0.75	–	–	A	Referenced to GND1, t = 1.5 µs, non-repetitive, T_{amb}= 25°C	PRQ-548
ISENSEx maximum voltage	$V_{ISENSEx\_MAX}$	-2.5	–	2.5	V	Referenced to GND1	PRQ-226
VBATS maximum voltage	V_{VBATS_MAX}	-0.3	–	18	V	Referenced to GND1, R_{VDBAT2} should be connected.	PRQ-490

Note: Stresses above the limits listed in this table may cause permanent damage to the device (including galvanic isolation). Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

4.2 Functional range

Table 3 Functional range

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	V_{VCC1}	4.55	5	5.5	V	Referenced to GND1	PRQ-71
VCC1 ramp-up slew rate	t_{RP1}	–	–	2000	V/ms		PRQ-72
Positive power supply (secondary)	V_{VCC2}	14	15	21.5	V	Referenced to GND2,	PRQ-73
VCC2 ramp-up slew rate	t_{RP2}	0.65	–	1000	V/ms		PRQ-74
Negative power supply (secondary)	V_{VEE2}	-12	-5	0	V	Referenced to GND2	PRQ-75
VEE2 ramp-up slew rate	t_{RP3}	-0.1	–	-1000	V/ms		PRQ-76
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2- VEE2}$	–	–	25	V		PRQ-77
Operating temperature	*Tjunc*	-40	–	150	°C	Temperature at junction	PRQ-78
Common mode transient immunity	dV_{ISO}/dt	-150	–	150	kV/µs	@ 1000 V	PRQ-79
Voltages on digital I/O pin on primary side (INP, NRST, RDY, SI1, SI2, ADCPWM, SDI, SDO, NCS, SCLK, NFLT)	V_{INx}	0	–	V_{VCC1}	V	Referenced to GND1	PRQ-480
ISENSEx input voltage range	$V_{INISENSEx}$	-0.5	–	1.5	V	Referenced to GND1	PRQ-274
Voltage on VBATS	$V_{INVBATS}$	0	–	5.5	V	Referenced to GND1, R_{VDBAT2} should be connected.	PRQ-491
GATE/CLAMPx input voltage	$V_{GATE/CLAMPx}$	V_{VEE2}	–	V_{VCC2}	V	Referenced to GND2	PRQ-712
OCPPx input voltage range	V_{OCPPx_IN}	-1.1	–	2.1	V	Referenced to GND2	PRQ-524
OCPNx input voltage range	V_{OCPNx_IN}	-1.1	–	2.1	V	Referenced to GND2	PRQ-525
AIPx input voltage range	V_{AIPx_IN}	V_{GND2}	–	5.0	V		PRQ-528

(table continues...)

Table 3 (continued) Functional range

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ASC input voltage range	V_{ASC_IN}	V GND2	-	V CC2	V	ASCSDIS=0x0, AIP1DIS= 0x1.	PRQ-879

Note: Within the functional range, the IC operates as described in the circuit descriptions. Electrical characteristics stated within the following sections are specified within the conditions given in the electrical characteristics tables.

4.3 Thermal resistance

Table 4 Thermal resistance

T_J = -40°C to 150°C (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal Resistance Junction to Ambient (25 °C)	R_{THJA}	–	65	–	K/W	T_{amb} = 25 °C	PRQ-66
Thermal Resistance Junction to Ambient (125°C)	$R_{THJA,125}$	–	51	–	K/W	T_{AMB} = 125°C	PRQ-67
Thermal Resistance Junction to Case (bottom)	$R_{THJCBOT}$	–	27	–	K/W	T_{amb} = 25 °C	PRQ-68
Thermal Resistance Junction to Case (top)	$R_{THJCTOP}$	–	24	–	K/W	T_{amb} = 25 °C	PRQ-69
Ψ - Pseudo Thermal Resistance Junction to Case (top)	R_{PSIJT}	–	–	8	K/W	T_{amb} = 25 °C	PRQ-70
Thermal Resistance Junction to Board (25 °C)	$R_{THJBOARD}$		38.5		K/W	T_{amb} = 25 °C, power losses on secondary side ≤ 350 mW, power losses on primary side ≤ 100 mW	PRQ-611

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

4.4 Insulation characteristics

Table 5 Insulation characteristics for reinforced insulation in compliance with DIN EN IEC 60747-17 (VDE 0884-17):2021-10

Description	Symbol	Characteristic	Unit
Installation classification per IEC 60664-1, Table F.1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-IV I-III I-II	–
Climatic classification	–	40/125/21	–
Pollution degree (IEC 60664-1)	–	2	–
Minimum external clearance	CLR	> 8	mm
Minimum external creepage	CPG	> 8	mm
Minimum comparative tracking index	CTI	> 400	–
Maximum rated repetitive peak isolation voltage	V_{IORM}	1767	V_{peak}
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{peak}
Maximum impulse voltage, tested in air	V_{IMP}	8000	V_{peak}
Maximum surge isolation voltage for reinforced insulation, tested in oil Test voltage in subgroup #1 = 11 kV ≥ 1.3 x V_{IMP}, min. 10 kV	V_{IOSM}	11000	V_{peak}
Input to output test voltage, method b1) $V_{ini,b}$ = 1.2 x V_{IOTM}, $V_{pd(m)} \geq V_{IORM}$ x 1.875, 100% production test, $t_{ini,b} = t_m$= 1 s	q_{PD}	< 5	pC
Input to output test voltage, method a) $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)} \geq V_{IORM}$ x 1.6 , sample test, t_{ini} = 60 s, t_m = 60 s	q_{PD}	< 5	pC
Isolation resistance at 25 °C ≤ T_{amb} ≤ 125 °C, V_{io} = 500 V	R_{IO}	> 10^{12}	Ω
Isolation resistance at T_S = 150°C, V_{io} = 500 V	R_{IO}	> 10^9	Ω

Table 6 Insulation characteristics recognized according to UL 1577

Parameter	Symbol	Characteristic	Unit
Insulation withstand voltage / 1 min	V_{ISO}	5700	V (rms)
Insulation test voltage / 1 s	V_{ISO}	6000	V (rms)

4.5 Current consumption

Table 7 Current consumption

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Quiescent Current Primary (VCC1)	I_{QVCC1}	6	7	9	mA	Init_Mode, all primary I/Os open, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, TOUTP = 0 V, flyback controller off	PRQ-81
Quiescent Current Primary (VCC1) with INP = "high"	I_{QVCC1_ON}	8.5	11.75	15	mA	Normal_Mode, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, $I_{DESATCS1}$, I_{ADCCS1} configured, INP =5V	PRQ-894
Quiescent Current Secondary (VCC2)	I_{QVCC2}	6	12	18	mA	Ready_Mode, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, $I_{DESATCS1}$, I_{ADCCS1} configured	PRQ-83
Quiescent Current Secondary (VEE2)	I_{QVEE2}	-0.8	-1.5	-3	mA	Ready_Mode, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, $I_{DESATCS1}$, I_{ADCCS1} configured	PRQ-82

5 Operating modes

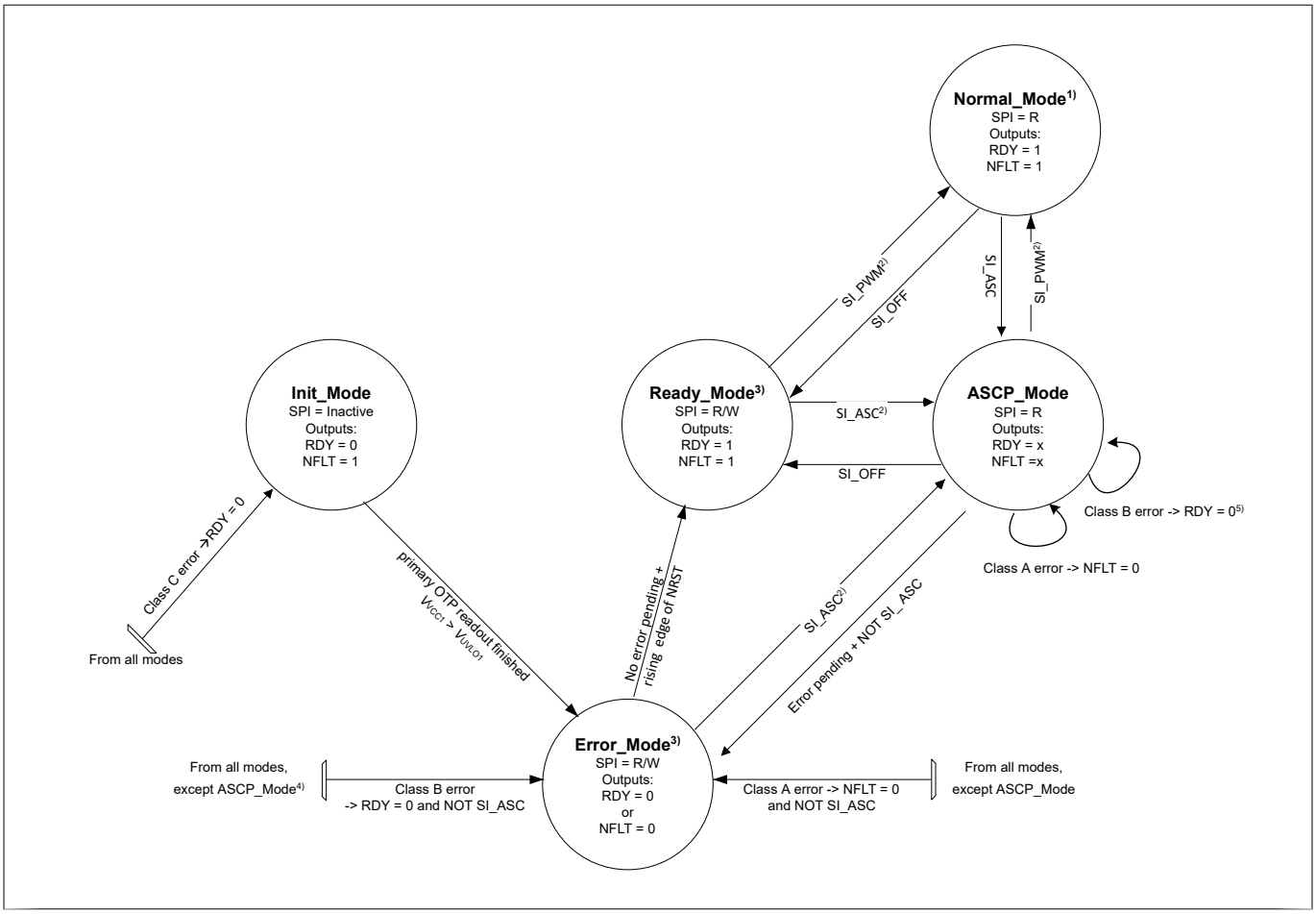

Figure 3 Operating mode diagram

Notes:

1. *PWM is enabled.*
2. *STATUSP.SPICES is cleared by the device. If configuration is in progress, the configuration, which is valid at this mode transition will be used.*
3. *Configuration via SPI only in Ready_Mode and Error_Mode, only if CTRL.SPICE = 1 and SI2 = 0.*
4. *Error reaction during ASC is set to "not ignored" for any bit field (ASCIGNOVLO2, ASCIGNUVLO2, ASCIGNOVLO3, ASCIGNUVLO3) in register SPSMER, when the corresponding error occurs.*
5. *Error reaction during ASC is set to "ignored" for any bit field ASCIGNOVLO2, ASCIGNUVLO2, ASCIGNOVLO3, ASCIGNUVLO3 in register SPSMER,when the corresponding error occurs.*

The device is operating in the following modes:

- Ready_Mode (PWM is disabled)
- Normal_Mode (PWM is enabled)
- Error_Mode (failure/fault event occurred)
- ASCP_Mode (TOUT = high(VCC2))

Init_Mode

In this start-up mode, the device is not operating. This mode is also entered, if an UVLO1 or a primary internal supervision error is occurring. If there is a partly supply on the device (e.g. VCC1 only) the device will enter Error_Mode and from there Ready_Mode can be accessed. Therefore supplies should rise within the specified slew rates to a valid voltage level according to given operating conditions.

Ready_Mode

In this mode the device is up and ready (no error event occurred). The device can be configured via the integrated SPI interface, if CTRL.SPICE is set to 1 and SI2 = 0. Diagnostic and status bits can also be read in Ready_Mode.

Normal_Mode

In this mode the device is enabled to switch PWM pattern inserted on the INP pin. A high level on SI1 and SI2 is needed for a mode transition from Ready_Mode.

Note: Normal_Mode can only be entered if no faults and errors are active.

Error_Mode

The device changes (from any other Mode, except ASCP_Mode) to Error_Mode, if a ready lost or DESAT/OCP event occurs. Also in this mode the device can be configured via the SPI interface, if CTRL.SPICE is set to 1 and SI2 = 0.

Note: In Error_Mode NFLT or RDY are low. Triggering events can be found in the description of RDY and NFLT.

ASCP_Mode

This mode is entered (from any mode, except Init_Mode), if a primary ASC is triggered via the safety input pins SI1/SI2. This mode is kept, even when an error occurs. The error will be notified on RDY or NFLT pins. The responsible logic device needs to trigger a mode change from ASCP_Mode via SI1/SI2 transition.

Events Class A

The following (exhaustive) list of errors are defined as Events Class A:

- DESAT
- OCP

After an event Class A the output stage initiates a safe turn-off sequence (soft or hard turn-off). The event is notified via an error bit in the corresponding register and the NFLT pin.

When an event Class A occurs, the device may change its operating mode depending on which mode is active when the event occurs:

- If it was in any Mode (except ASCP_Mode), it goes to Error_Mode
- If it was in ASCP_Mode, it stays in ASCP_Mode

In ASCP_Mode, any class A event is prioritized and will trigger the configured turn-off signal on secondary side. An ASCP signal via SI1/SI2 will only apply after a configurable delay.

Events Class B

The following (exhaustive) list of errors are defined as Events Class B:

- Output stage monitoring
- Gate monitoring
- OCPx pin open detection
- Secondary internal supervision
- Lifesign lost
- UVLO2

- OVLO2
- UVLO3
- OVLO3

After an Event Class B the output stage initiates a safe turn-off sequence or tri-state. The turn-off mode can be configured independently for some errors or is pre-defined and fixed for others. The event is notified via an error bit in the corresponding register and via the RDY pin.

When an Event Class B occurs, the device may change its operating mode depending on which mode is active when the event occurs:

- If it was in any Mode (except ASCP_Mode), it goes to Error_Mode
- If it was in ASCP_Mode, it stays in ASCP_Mode

In ASCP_Mode, supply related class B events are prioritized and will trigger the configured turn-off signal on secondary side, if the error reaction for corresponding UVLOx/OVLOx erros is set to "not ignored" in register SPSMER. An ASCP signal via SI1/SI2, while a corresponding class B event occurs, will only apply, if the error reaction for corresponding UVLOx/OVLOx errors is set to "ignored" in register SPSMER.

Events Class C

The following (exhaustive) list of events is comprised within the Event Class C:

- UVLO1
- Primary internal supervision

When an Event Class C occurs, the device will always go to Init_Mode.

6 Serial Peripheral Interface (SPI)

6.1 Functional description SPI

The product has a Serial Peripheral Interface (SPI) on the primary side to process 32 bit communication frames.

Note: The SPI can be used to change the settings (not mandatory) in the registers from default to customized ones. This needs to be done before entering the PWM switching mode (SI1 = 1, SI2 = 1). Status can be read always.

The SPI of the product has an interface which is peer-to-peer and bus (daisy chain) compatible.

Note:
The SPI of the product is capable to operate in a bus system where the pins SCLK and NCS of all slaves can be connected to the pins with the same function and where the SDO of the first slave is connected to the next slave until the final SDO is connected back to the master(Output to Input).

The device has a continuous parity protection mechanism for all its configuration bits, for 8 bits in a register 1 parity bit.

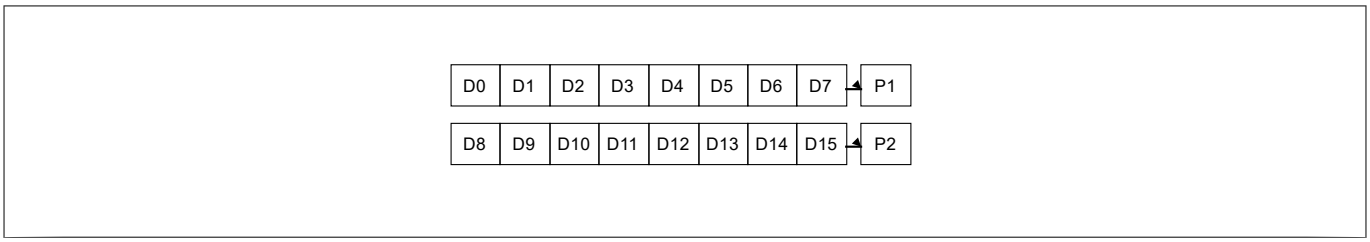

Figure 4 Bit protection diagram

The drawing below shows the setup using daisy chain configuration of the SPI.
To achieve a peer-to-peer communication the SDO pin of the slave is directly connected back to the master.

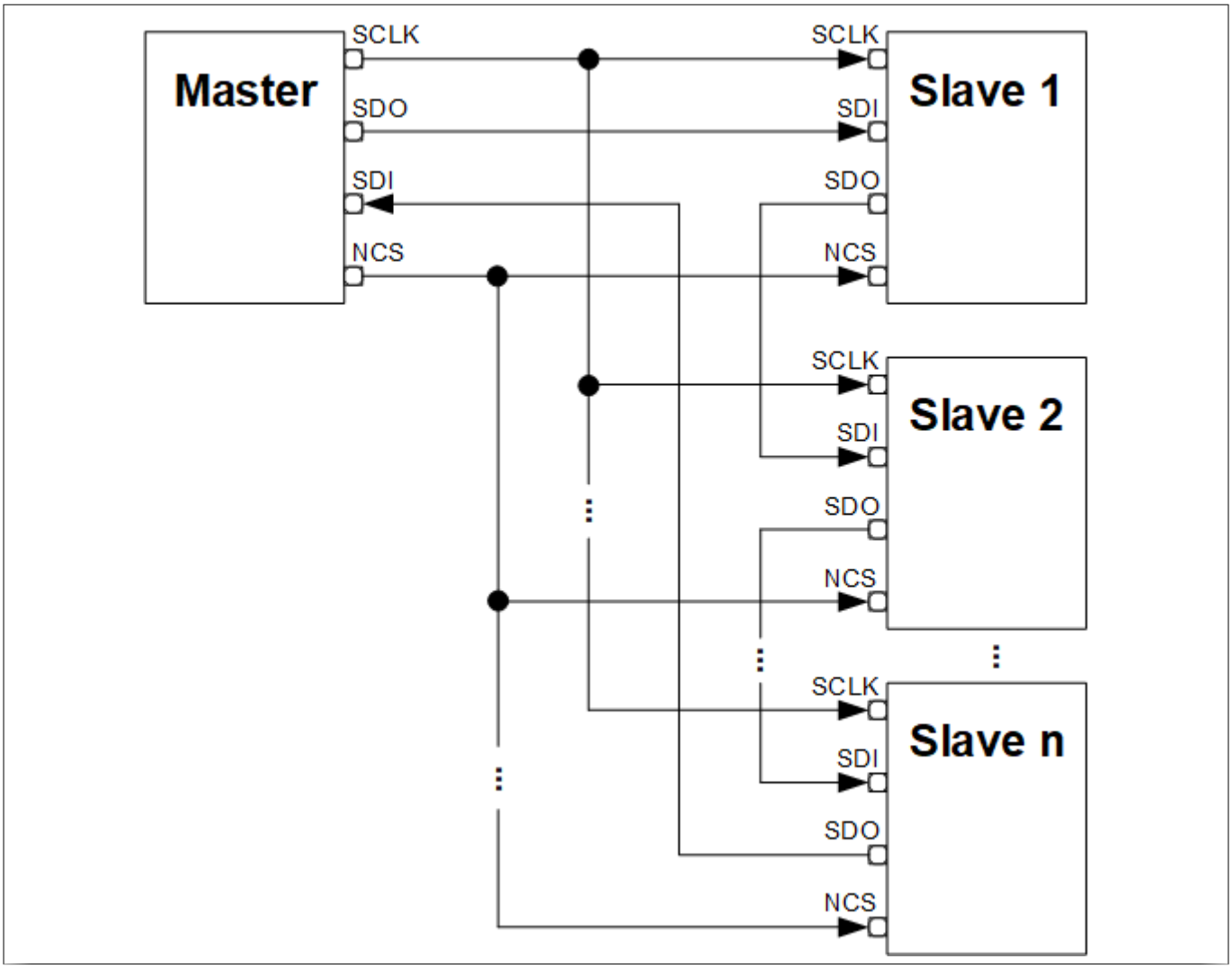

Figure 5 SPI daisy chain configuration

The 8 bit CRC is defined according to SAE-J1850 CRC8 standard.

The device implements a CRC8 check on incoming messages on the address and data inside the 32 bit SPI frame.

The device implements a CRC8 algorithm on outgoing messages on the status and data bits inside the 32 bit SPI frame.

The CRC mode can be selected via bit field PINPC.CRCMODE.

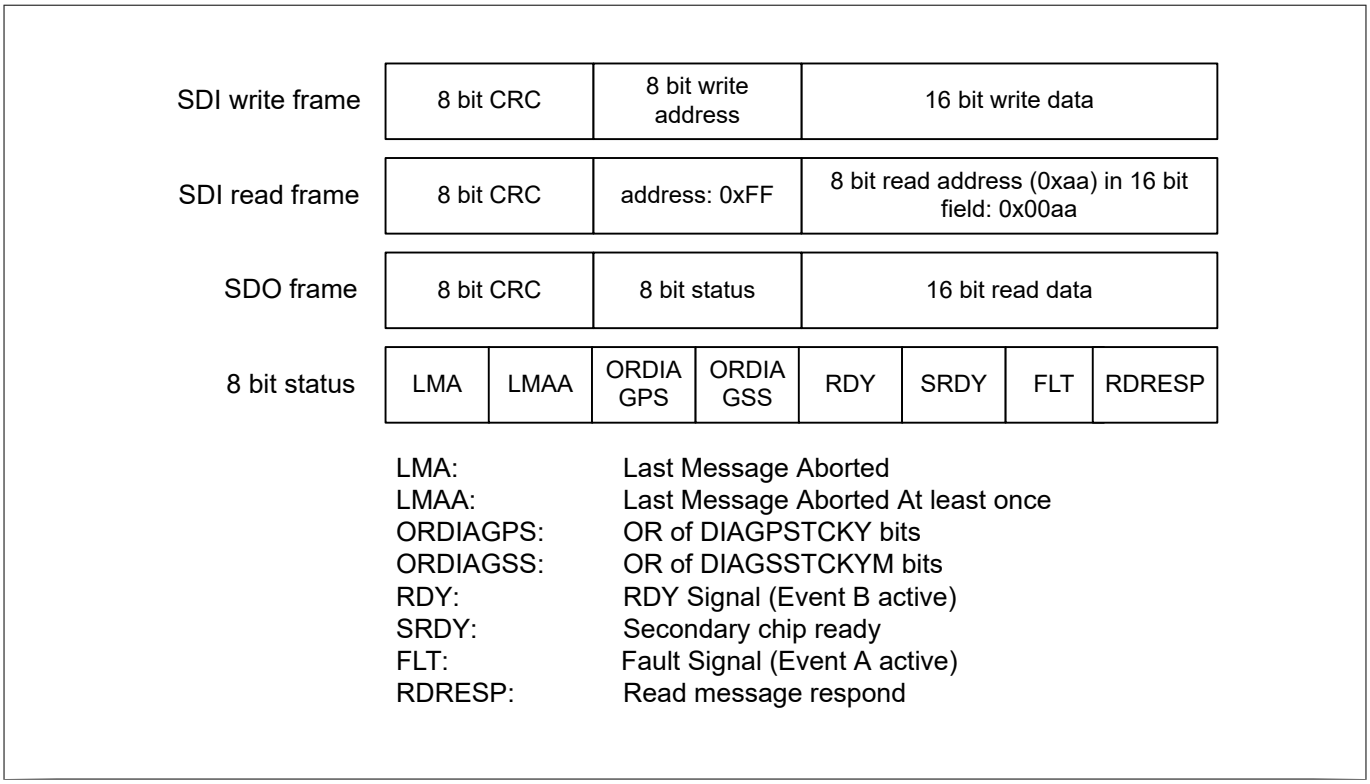

Figure 6 SPI frame overview

Note: The last valid status is shifted out with NCS activation.

The device has a hardware protection which ensures that an access on an address is only allowed on the address provided by the SPI message. In case of a failure or a detected wrong access the device will set the Last Message Aborted bit in the status bits of the belonging answer message.

The customer accessible SPI registers on the primary side are found in the register sets PUSER (primary status and diagnosis read-out) and POTP (primary configuration registers), the customer accessible SPI register on the secondary side are found in the register sets SUSER (secondary status and diagnosis read-out) and SOTP (secondary configuration registers).

All secondary side status and diagnosis bits in register SUSER.STATUSS and SUSER.DIAGS are mirrored to the primary side register PUSER.STATUSSMIR and PUSER.DIAGSMIR. Therefor the access time $t_{NCSinactive,prim}$ applies when accessing prim side registers only. The secondary side access timing $t_{NCSinactive,sec}$ applies only for configuration or read-out of bits in SOTP or SUSER registers.

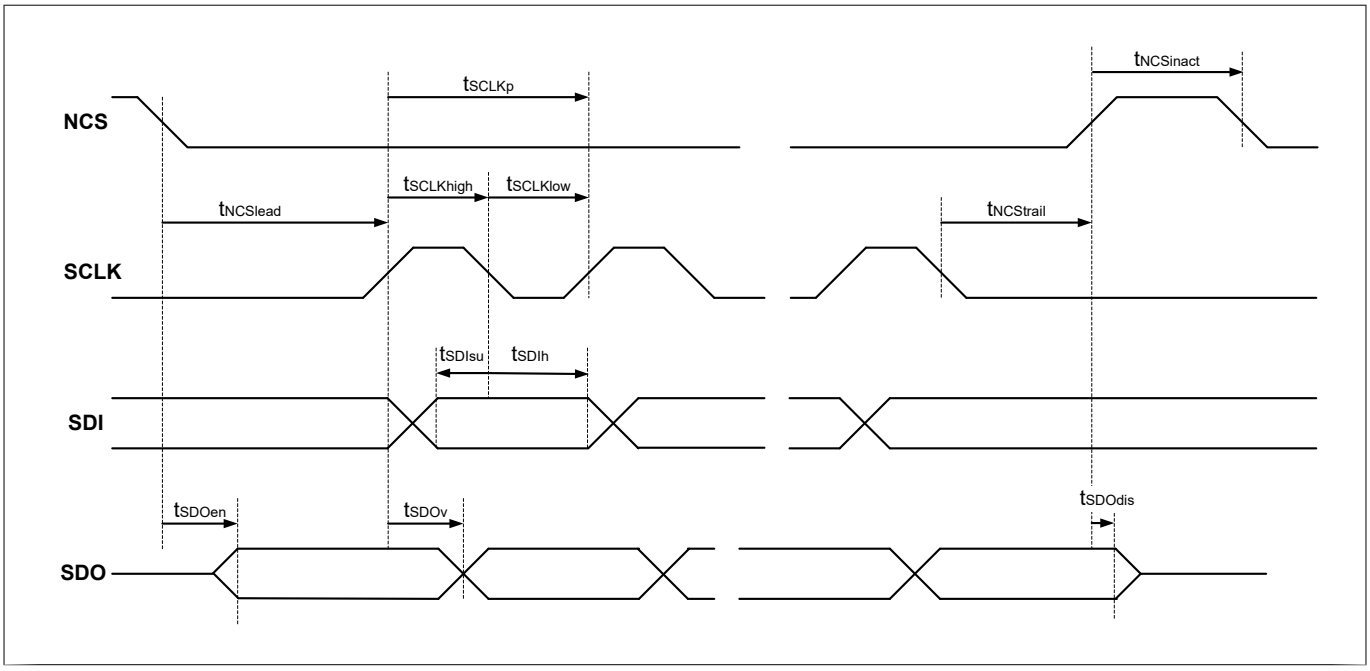

Figure 7 SPI timing diagram

Note:

- $t_{SCLKp} = 1 / f_{SCLK}$, $D_{SCLK} = t_{SCLKhigh} / t_{SCLKp} * 100$
- *The final timing depends on the filtering at concerned pins*
- *Rising edge of SCLK leads to SDO toggle*

The SPI timing ($t_{SDIholdx}$, $t_{SDIsetx}$) depend on the setting in bit field PINPC.SAMPDEL.

The device can be configured via SPI to change the settings versus the default values. This can be only done in Ready_Mode or Error_Mode, the SI2 pin must remain 0 all the time and the supply at VCC1 must be stable and in operating range. The registers for functions on the secondary will be updated when the VCC2 is in operating range, otherwise the automatic register content reply via SPI will trigger an LMA. For writing the configuration the CTRL.SPICE bit needs to be set to "high" first. This also enables the automatic register content reply via SPI, meaning after the device wrote the configuration to the register it will feedback the written content in the next SPI message (in case no error occurs).

Note: During configuration (SI2 = 0) the inputs on INP and INN are ignored. Rising edge on SI2 during configuration mode will trigger an clear of write enable bit in the status register.

For timings that are configurable via SPI the following formula applies for resulting timings:

$t_{output} = 1/f_{OSC,int} * HEX_{val}$

Table 8 Default register setting

Register setting	Register	Bit field	Default value SPI	Parameter	Value [typ]	Unit
POTP	PINPC	ASCDEL	0x0C (tASCdelay = 12 dec)	$t_{ASCdelay}$	4.8	µs
		SITOC	0x0 (HARDOFF = 0 dec)	SI1/SI2 turn-off	Hard-off	-

(table continues...)

Table 8 (continued) Default register setting

Register setting	Register	Bit field	Default value SPI	Parameter	Value [typ]	Unit
		ADCPWMINV1	0x0 (INVDIS = 0 dec)	ADCPWM1	Not inverted	-
		ADCPWMINV2	0x1 (INVEN = 1 dec)	ADCPWM2	Inverted	-
		ADCPWMPER	0x0 (tPeriod_ADC0 = 0 dec)	t_{Period_ADC0}	100	µs
		CRCMODE	0x0 (CRC24 = 0 dec)	CRC mode	CRC24	-
		SAMPDEL	0x2 (SAMPDEL2 = 2 dec)	$t_{SDIset2}$	-25	ns
POTP	FLYBACKC1	FLYSTART	0x1 (Start3 = 1 dec)	Flyback transformer	10	µH
		FLYMAXTUP	0x7 (TSOFTSTART1 = 7 dec)	$t_{flymaxtup}$	32	ms
		FLYLEBLK	0x1 (tIsenseBT1 = 1 dec)	$t_{ISenseBT1}$	200	ns
		FLYBENA	0x1 (EN = 1 dec)	Flyback	Enabled	-
POTP	FLYBACKC2	FLYFREQ	0x63 (not in enumeration: 99 dec)	$f_{SW\text{-}out}$	200	kHz
		FLYIPKL	0x2 (IPWMpk2 = 2 dec)	I_{PWMpk2}	425	mV
		FLYB2IPK	0x1 (EN = 1 dec)	Dual IPk value	Enabled	-
POTP	FLYBACKC3	FLYSCHK	0x1 (EN = 1 dec)	Self check timeout fail	Enabled	-
		FLYBOVEN	0x0 (DIS = 0 dec)	Flyback OV protection	Disabled	-
		FLYRCYC	0xF (15 dec)	FLYRCYC15	15	Cycles
		OCPINJFLT	0x0 (DIS = 0 dec)	OCP fault injection	Disabled	-
		FLYOUTTRI	0x0 (DIS = 0 dec)	Tristate in case of ISENSE trigger	Disabled	-

(table continues...)

Table 8 (continued) Default register setting

Register setting	Register	Bit field	Default value SPI	Parameter	Value [typ]	Unit
POTP	FLYBACKC4	FLYRSTT	0x0 (tDEADfly = 0 dec)	$t_{DEADfly0}$	1.6	ms
		FLYADACYC	0x2 (2 dec)	FLYFPOWERP2	2	Pulses
POTP	PVARIANT	INNSTPENAB	0x0 (INNDIS = 0 dec)	INN pin	Disabled	-
		ADCPWMENAB	0x0 (ADCPWMAIP1OR2 = 0 dec)	ADCPWM pin	ADC1 or ADC2	-
		DEADT	0x00 (tDEADx = 0 dec)	t_{DEAD}	0	ns
SOTP	SCPC	DESATVL	0x0 (VDESAT0 = 0 dec)	V_{DESAT0}	9	V
		DESATERR	0x1 (SOFTOFF = 1 dec)	DESAT error reaction	Soft-off	-
		DESATCS	0x1 (IDESATCS1 = 1 dec)	$I_{DESATCS0}$	500	µA
		OCPVL1	0x2 (VOCPD2 = 2 dec)	V_{OCPD2}	500	mV
		OCPVL2	0x1 (VOCPD1 = 1 dec)	V_{OCPD1}	900	mV
		OCPERR	0x1 (SOFTOFF = 1 dec)	OCP error reaction	Soft-off	-
		DESATOCPBT	0x1 (tDESATOCBT1 = 1 dec)	$t_{DESATOCPBT1}$	260	ns
		OCPBTDIS	0x0 (BTON = 0 dec)	OCP blanking time	Enabled	-
		DESATBTDIS	0x0 (BTON = 0 dec)	DESAT blanking time	Enabled	-
SOTP	SPSML	OVLO2VL	0x1 (VOVLO2HL1 = 1 dec)	V_{OVLO2H/L_1}	17/16.5	V

(table continues...)

Table 8 (continued) Default register setting

Register setting	Register	Bit field	Default value SPI	Parameter	Value [typ]	Unit
		UVLO2VL	0x0 (VUVLO2HL0 = 0 dec)	V_{UVLO2H/L_0}	10.3/10.0	V
		OVLO3VL	0x0 (VOVLO3HL0 = 0 dec)	V_{OVLO3H/L_0}	-2.9/-3.7	V
		UVLO3VL	0x0 (VUVLO3HL0 = 0 dec)	V_{UVLO3H/L_0}	-6.4/-7.2	V
		VCC2VL	0xe (VOVSL14 = 14 dec)	V_{OVSL14}	14	V
SOTP	SPSMER	OVLO2ERR	0x1 (SOFTOFF = 1 dec)	OVLO2 error reaction	Soft-off	-
		UVLO2ERR	0x1 (SOFTOFF = 1 dec)	UVLO2 error reaction	Soft-off	-
		OVLO3ERR	0x1 (IGNORED = 1 dec)	OVLO3 error reaction	Ignored	-
		UVLO3ERR	0x1 (IGNORED = 1 dec)	UVLO3 error reaction	Ignored	-
		ASCIGNOVLO2	0x0 (NOTIGNORED = 0 dec)	OVLO2 error reaction @ASCP	Not ignored	-
		ASCIGNUVLO2	0x0 (NOTIGNORED = 0 dec)	UVLO2 error reaction @ASCP	Not ignored	-
		ASCIGNOVLO3	0x0 (NOTIGNORED = 0 dec)	OVLO3 error reaction @ASCP	Not ignored	-
		ASCIGNUVLO3	0x0 (NOTIGNORED = 0 dec)	UVLO3 error reaction @ASCP	Not ignored	-
		ENAADAP	0x1 (EN =1 dec)	Flyback adaptive power mode	enabled	-
SOTP	STOFFC	STOFFPVL	0x0 (VPLT0 = 0 dec)	V_{PLT0}	4	V

(table continues...)

Table 8 (continued) Default register setting

Register setting	Register	Bit field	Default value SPI	Parameter	Value [typ]	Unit
		STOFFPT	0x0C (tTLTOffPLT = 12 dec)	$t_{TLTOffPLT}$	600	ns
		STOFFRC	0x00 (tSOFTOFF = 0 dec)	$t_{PLTRAMP}$	0	ns
SOTP	ADCSET	ADC1CS	0x1 (IADC1CS1 = 1 dec)	I_{ADCCS1}	200	µA
		ADC2CS	0x1 (IADC2CS1 = 1 dec)	I_{ADCCS1}	200	µA
		ADCSR	0x3 (fSAMPLE3 = 3 dec)	$f_{SAMPLE3}$	1.2	kHz
SOTP	GMOSMC	GMERR	0x0 (HARDOFF = 0 dec)	Gate mon error reaction	Hard-off	-
		GMBT	0x3 (tGMBTx3 = 3 dec)	t_{GMBTx3}	7.9	µs
		OSMBT	0x3 (tOUTMBTx3 = 3 dec)	$t_{OSMBTx1}$	1200	ns
		GATEISVCCDIS	0x0 (EN = 0 dec)	Send GATEISVCC bit	Enabled	-
SOTP	AMCLPC	IAMCDIS	0x0 (EN = 0 dec)	Internal active miller clamping	Enabled	-
		EAMCEN	0x0 (DIS = 0 dec)	External active miller clamping	Disabled	-
		AMCVL	0x2 (VCLAMPx2 = 2 dec)	V_{CLAMPx_2}	3	V
		EAMCLPDEL	0x0 (TAMCLPDELAY0 = 0 dec)	EAMCLP delay time	Disabled	-
SOTP	SVARIANT	ASCSDIS	0x1 (DIS = 1 dec)	ASCS pin	Disabled	-
		AIP1DIS	0x0 (EN = 0 dec)	AIP1 pin	Enabled	-

6.2 Electrical characteristics SPI

Table 9 Electrical characteristics SPI

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Baud rate	f_{SCLK}	0.25	–	3.75	MHz	possible speed depends on SPI setup;	PRQ-294
Baud rate in daisy chain	$f_{SCLK,daisy}$	0.25	–	3.75	MHz	Daisy chain operation	PRQ-832
SPI frame size	N_{bit}	32	–	512	bit	formula: N_{bit} = x * 32 bit, x is number of slaves,	PRQ-296
SDI, SCLK & NCS digital input low level	$V_{SPI,input(low)}$	0	–	1.2	V	Referenced to GND1	PRQ-457
SDI, SCLK & NCS digital input high level	$V_{SPI,input(high)}$	3.5	–	V_{VCC1}	V	Referenced to GND1	PRQ-458
SDI, SCLK input leakage current high	$I_{INLEAKH\_SPI}$	–	107	190	µA	V_{VCC1} at pin, V_{VCC1} = 5 V	PRQ-208
SDI, SCLK input leakage current low	$\lvert I_{INLEAKL\_SPI}\rvert$	–	0.3	10	µA	0 V at pin, V_{VCC1} = 5 V	PRQ-209
SDI, SCLK minimum slew rate	$V_{SPI,slew}$	0.13			V/ns		PRQ-866
NCS input leakage current high	$\lvert I_{INLEAKH\_NCS}\rvert$	–	7.3	17	µA	VCC1 at pin, V_{VCC1} = 5 V	PRQ-677
NCS input leakage current low	$\lvert I_{INLEAKL\_NCS}\rvert$	–	93	190	µA	0 V at pin, V_{VCC1} = 5 V	PRQ-676
Weak pull down resistance SDI & SCLK	R_{PDIN_SPI}	38	48	58	kΩ		PRQ-210
Weak pull up resistance NCS	R_{PUNCS}	38	48	58	kΩ		PRQ-675
SDO output low level	$V_{SDO,output(low)}$	–	0	0.5	V	V_{VCC1} ≥ 4.55 V; $\lvert I_{load}\rvert$ = 5 mA	PRQ-212
SDO output high level	$V_{SDO,output(high)}$	V_{VCC1} - 0.5	V_{VCC1}	–	V	V_{VCC1} ≥ 4.55 V; $\lvert I_{load}\rvert$ = 5 mA	PRQ-213
SCLK duty cycle	D_{SCLK}	45	–	55	%		PRQ-476
SDI setup time 0	$t_{SDIset0}$	25	–	–	ns		PRQ-297
SDI setup time 1	$t_{SDIset1}$	0	–	–	ns		PRQ-858
SDI setup time 2	$t_{SDIset2}$	-25	–	–	ns		PRQ-859

(table continues...)

Table 9 (continued) Electrical characteristics SPI

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SDI setup time 3	$t_{SDIset3}$	-50	–	–	ns		PRQ-861
SDI hold time 0	$t_{SDIhold0}$	70	–	–	ns		PRQ-298
SDI hold time 1	$t_{SDIhold}$	95	–	–	ns		PRQ-860
SDI hold time 2	$t_{SDIhold2}$	120	–	–	ns		PRQ-862
SDI hold time 3	$t_{SDIhold3}$	145	–	–	ns		PRQ-863
NCS lead time	$t_{NCSlead}$	400	–	–	ns		PRQ-302
NCS trail time	$t_{NCStrail}$	400	–	–	ns		PRQ-303
NCS inactive time primary side access	$t_{NCSinact,prim}$	5	–	–	µs		PRQ-304
NCS inactive time secondary side access	$t_{NCSinact,sec}$	17	–	–	µs		PRQ-750
SDO enable time	t_{SDOen}	–	–	250	ns	C_{LOAD} = 20 pF	PRQ-300
SDO disable time	t_{SDOdis}	–	–	500	ns	C_{LOAD} = 20 pF	PRQ-492
SDO valid time	t_{SDOv}	5	–	137	ns	C_{LOAD} = 20 pF	PRQ-301

6.3 Registers

6.3.1 Register address space - IFX1EDI3051AS

Table 10 Registers address space - IFX1EDI3051AS

Module	Base address	End address	Note
SPI	00000000_H	$000000FF_H$	User SPI (16 bit data width)
TSPIP	00000000_H	$0000007F_H$	Test SPI primary (8 bit data width)
TSPIS	00000000_H	$0000007F_H$	Test SPI secondary (8 bit data width)

6.3.2 Register overview - IFX1EDI3051AS (ascending offset address)

Table 11 Register overview - IFX1EDI3051AS (ascending offset address)

Short name	Long name	Offset address	Page number
PINPC	Input configuration register	000_H	34
FLYBACKC1	Flyback configuration register 1 - Start-up	001_H	35
FLYBACKC2	Flyback configuration register 2 - Normal Operation	002_H	36
FLYBACKC3	Flyback configuration register 3 - Error Handling	003_H	37
FLYBACKC4	Flyback configuration register 4 - Error Timing	004_H	38
PVARIANT	Primary Variant Configuration Register	005_H	39
CTRL	Control	020_H	51
ADC1R	ADC1 result register	021_H	51
ADC2R	ADC2 result register	022_H	52
STATUSP	Status register primary	023_H	52
DIAGP	Error diagnosis primary	024_H	53
DIAGPSTCKY	Error diagnosis primary sticky	025_H	53
DIAGSMIR	Error diagnosis secondary mirrored	026_H	54
DIAGSMIRSTCKY	Error diagnosis secondary mirrored sticky version	027_H	55
DIAGFLY	Error diagnosis flyback	028_H	55
DIAGFLYSTCKY	Error diagnosis flyback	029_H	56
STATUSSMIR	Status register secondary	$02A_H$	57
STATUSSMIRSTCKY	Status register secondary	$02B_H$	58
SCPC	Short circuit protection configuration register	040_H	43
SPSML	Secondary power supply monitoring level register	041_H	44
SPSMER	Secondary power supply monitoring error reaction register	042_H	46
STOFFC	Soft off configuration register	043_H	47
ADCSET	ADC1 and ADC2 additional settings	044_H	48
GMOSMC	Gate Monitoring and Output Stage Monitoring configuration register	045_H	48

(table continues...)

Table 11 (continued) Register overview - IFX1EDI3051AS (ascending offset address)

Short name	Long name	Offset address	Page number
AMCLPC	Active Miller Clamping configuration	046_H	49
SVARIANT	Secondary Variant Configuration Register	047_H	50
STATUSS	Status register secondary	060_H	39
DIAGS	Error diagnosis secondary	061_H	40
DIAGSSTCKY	Sticky bits secondary	062_H	41
SSCR	Secondary Supervision Control Register	063_H	41
SSRESP	Secondary Supervision Response	064_H	42
READADDR	Read address for next shift out	$0FF_H$	59

6.3.3 Register overview - POTP (ascending offset address)

Table 12 Register overview - POTP (ascending offset address)

Short name	Long name	Offset address	Page number
PINPC	Input configuration register	000_H	34
FLYBACKC1	Flyback configuration register 1 - Start-up	001_H	35
FLYBACKC2	Flyback configuration register 2 - Normal Operation	002_H	36
FLYBACKC3	Flyback configuration register 3 - Error Handling	003_H	37
FLYBACKC4	Flyback configuration register 4 - Error Timing	004_H	38
PVARIANT	Primary Variant Configuration Register	005_H	39

6.3.4 Register overview - SUSER (ascending offset address)

Table 13 Register overview - SUSER (ascending offset address)

Short name	Long name	Offset address	Page number
STATUSS	Status register secondary	060_H	39
DIAGS	Error diagnosis secondary	061_H	40
DIAGSSTCKY	Sticky bits secondary	062_H	41
SSCR	Secondary Supervision Control Register	063_H	41
SSRESP	Secondary Supervision Response	064_H	42

6.3.5 Register overview - SOTP (ascending offset address)

Table 14 Register overview - SOTP (ascending offset address)

Short name	Long name	Offset address	Page number
SCPC	Short circuit protection configuration register	040_H	43
SPSML	Secondary power supply monitoring level register	041_H	44

(table continues...)

Table 14 (continued) Register overview - SOTP (ascending offset address)

Short name	Long name	Offset address	Page number
SPSMER	Secondary power supply monitoring error reaction register	042_H	46
STOFFC	Soft off configuration register	043_H	47
ADCSET	ADC1 and ADC2 additional settings	044_H	48
GMOSMC	Gate Monitoring and Output Stage Monitoring configuration register	045_H	48
AMCLPC	Active Miller Clamping configuration	046_H	49
SVARIANT	Secondary Variant Configuration Register	047_H	50

6.3.6 Register overview - PUSER (ascending offset address)

Table 15 Register overview - PUSER (ascending offset address)

Short name	Long name	Offset address	Page number
CTRL	Control	020_H	51
ADC1R	ADC1 result register	021_H	51
ADC2R	ADC2 result register	022_H	52
STATUSP	Status register primary	023_H	52
DIAGP	Error diagnosis primary	024_H	53
DIAGPSTCKY	Error diagnosis primary sticky	025_H	53
DIAGSMIR	Error diagnosis secondary mirrored	026_H	54
DIAGSMIRSTCKY	Error diagnosis secondary mirrored sticky version	027_H	55
DIAGFLY	Error diagnosis flyback	028_H	55
DIAGFLYSTCKY	Error diagnosis flyback	029_H	56
STATUSSMIR	Status register secondary	$02A_H$	57
STATUSSMIRSTCKY	Status register secondary	$02B_H$	58

6.3.7 Register overview - READACCS (ascending offset address)

Table 16 Register overview - READACCS (ascending offset address)

Short name	Long name	Offset address	Page number
READADDR	Read address for next shift out	$0FF_H$	59

6.3.8 Input configuration register

PINPC Offset address: 000_H

Input configuration register Reset values see: Table 17

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMPDEL		CRCMODE		ADCPWMPER		ADC PWM INV2	ADC PWM INV1	Res	SITOC	ASCDEL					
rw		rw		rw		rw	rw	r	rw	rw					

Field	Bits	Type	Description
ASCDEL	5:0	rw	**ASC delay** $t_{ASCDELAY}$ = 400 ns * ASCDEL
SITOC	6	rw	**Safety inputs turn-off configuration** 0_B **HARDOFF**: Safety inputs hard turn-off 1_B **SOFTOFF**: TON/TOFF reaction soft turn off
ADCPWMINV1	8	rw	**invert PWM output for AIP1** 0_B **INVDIS**: ADC PWM normal output 1_B **INVEN**: ADC PWM inverted output
ADCPWMINV2	9	rw	**invert PWM output for AIP2** 0_B **INVDIS**: ADC PWM normal output 1_B **INVEN**: ADC PWM inverted output
ADCPWMPER	11:10	rw	**ADC PWM period selection** 00_B **tPeriod_ADC0**: ADC Data period selection 0 01_B **tPeriod_ADC1**: ADC Data period selection 1 10_B **tPeriod_ADC2**: ADC Data period selection 2 11_B **tPeriod_ADC3**: ADC Data period selection 3
CRCMODE	13:12	rw	**Select SPI CRC mode** 00_B **CRC24**: CRC24 mode 10_B **NO_CRC**: expect and send constant 0xF1 crc 11_B **IGN_CRC**: ignore inbound CRC , send j1850 CRC
SAMPDEL	15:14	rw	**Adjust SDI sample delay in relation to falling edge of SCLK** 00_B **SAMPDEL0**: no delay 01_B **SAMPDEL1**: delay sampling by 1 system clock cycle 10_B **SAMPDEL2**: delay sampling by 2 system clock cycles

Table 17 Reset values of PINPC

Reset type	Reset value	Note
Basic reset	$820C_H$	

6.3.9 Flyback configuration register 1 - Start-up

FLYBACKC1 Offset address: 001_H

Flyback configuration register 1 - Start-up Reset values see: Table 18

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLYBENA	**Res**	**FLYLEBLK**		**Res**				**FLYMAXTUP**			**Res**			**FLYSTART**	
rw	r	rw		r				rw			r			rw	

Field	Bits	Type	Description
FLYSTART	1:0	rw	**Set according to primary inductance of flyback transformer** 00_B **Start0**: 20 µH 01_B **Start1**: 10 µH 10_B **Start2**: 5 µH 11_B **Start3**: 3 µH
FLYMAXTUP	7:5	rw	**Max accepted soft startup time till lifesign or fault** 000_B **TSOFTSTART0**: TSOFTSTART0 001_B **TSOFTSTART1**: TSOFTSTART1 010_B **TSOFTSTART2**: TSOFTSTART2 011_B **TSOFTSTART3**: TSOFTSTART3 100_B **TSOFTSTART4**: TSOFTSTART4 101_B **TSOFTSTART5**: TSOFTSTART5 110_B **TSOFTSTART6**: TSOFTSTART6 111_B **TSOFTSTART7**: TSOFTSTART7
FLYLEBLK	13:12	rw	**Selection of leading edge blanking** 00_B **tIsenseBT0**: FBPWM blanking time 0 on ISENSEx 01_B **tIsenseBT1**: FBPWM blanking time 1 on ISENSEx 10_B **tIsenseBT2**: FBPWM blanking time 2 on ISENSEx 11_B **tIsenseBT3**: FBPWM blanking time 3 on ISENSEx
FLYBENA	15	rw	**Enable/disable flyback function** 0_B **DIS**: Disable flyback driver stage 1_B **EN**: Enable flyback driver stage

Table 18 Reset values of FLYBACKC1

Reset type	Reset value	Note
Basic reset	$9CFD_H$	

6.3.10 Flyback configuration register 2 - Normal Operation

FLYBACKC2 Offset address: 002_H

Flyback configuration register 2 - Normal Operation Reset values see: Table 19

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		**FLYB2IPK**	**Res**	**FLYIPKL**		**Res**		**FLYFREQ**							
r		rw	r	rw		r		rw							

Field	Bits	Type	Description
FLYFREQ	7:0	rw	**Frequency Selection** f_{SW-OUT} = 20 Mhz / (FLYFREQ + 1) FLYFREQ should be at least 0x24h.
FLYIPKL	11:10	rw	**LSB/MSB of target peak current (via sense shunt voltage)** 00_B **IPWMpk0**: PWM peak current 0 01_B **IPWMpk1**: PWM peak current 1 10_B **IPWMpk2**: PWM peak current 2 11_B **IPWMpk3**: PWM peak current 3
FLYB2IPK	13	rw	**Enable flyback with dual IPK-mode (lowP/low ripple, full power for TOUTP-PWM)** 0_B **DIS**: Disable dual IPK mode 1_B **EN**: Enable dual IPK mode

Table 19 Reset values of FLYBACKC2

Reset type	Reset value	Note
Basic reset	2863_H	

6.3.11 Flyback configuration register 3 - Error Handling

FLYBACKC3 Offset address: 003_H

Flyback configuration register 3 - Error Handling Reset values see: Table 20

15	14	13 12	11 10 9 8	7 6 5	4	3 2 1	0
FLYOUTTRI	**OCPINJFLT**	**Res**	**FLYRCYC**	**Res**	**FLYBOVEN**	**Res**	**FLYSCHK**
rw	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
FLYSCHK	0	rw	**Stop on self check timeout fail enable (check driving MOS and receive sense, to find target peak current trigger)** 0_B **DIS**: Disable self-check on Flyback 1_B **EN**: Enable self-check on Flyback
FLYBOVEN	4	rw	**Flyback fault FLYBOVER (via VBATS) considered in error handling** 0_B **DIS**: FLYBOVER not considered in error handling 1_B **EN**: FLYBOVER considered in error handling

(table continues...)

(continued)

Field	Bits	Type	Description
FLYRCYC	11:8	rw	**Number of restart cycles until fault** 0_H **FLYRCYC0**: no retry 1_H **FLYRCYC1**: 1 retry cycle 2_H **FLYRCYC2**: FLYRCYC2 3_H **FLYRCYC3**: FLYRCYC3 4_H **FLYRCYC4**: FLYRCYC4 5_H **FLYRCYC5**: FLYRCYC5 6_H **FLYRCYC6**: FLYRCYC6 7_H **FLYRCYC7**: FLYRCYC7 8_H **FLYRCYC8**: FLYRCYC8 9_H **FLYRCYC9**: FLYRCYC9 A_H **FLYRCYC10**: FLYRCYC10 B_H **FLYRCYC11**: FLYRCYC11 C_H **FLYRCYC12**: FLYRCYC12 D_H **FLYRCYC13**: FLYRCYC13 E_H **FLYRCYC14**: FLYRCYC14 F_H **FLYRCYC15**: FLYRCYC15
OCPINJFLT	14	rw	**inject flyback OCP error** 0_B **DIS**: no action 1_B **EN**: force flyback overcurrent error
FLYOUTTRI	15	rw	**when set drive flyback TOUTP PP stage to tristate if FLYTMONER gets set** this bit enables automatic tristate of TOUTP when isense at off is detected.(FLYTMONER gets set) 0_B **DIS**: No tristate 1_B **EN**: Tristate

Table 20 Reset values of FLYBACKC3

Reset type	Reset value	Note
Basic reset	$0F01_H$	

6.3.12 Flyback configuration register 4 - Error Timing

FLYBACKC4 Offset address: 004_H

Flyback configuration register 4 - Error Timing Reset values see: Table 21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				FLYADACYC				Res		FLYRSTT		Res			
r				rw				r		rw		r			

Field	Bits	Type	Description
FLYRSTT	5:4	rw	**Dead time between restart trials** $t_{DEADfly}$ = 1.6ms * (FLYRSTT + 1)

(table continues...)

(continued)

Field	Bits	Type	Description
FLYADACYC	11:8	rw	**number of full power pulses executed for adaptive power requests** value 0 means no FP pulse will be executed for adaptive request

Table 21 Reset values of FLYBACKC4

Reset type	Reset value	Note
Basic reset	$020F_H$	

6.3.13 Primary Variant Configuration Register

PVARIANT Offset address: 005_H

Primary Variant Configuration Register Reset values see: Table 22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			**DEADT**					**ADCPWMENAB**			**INNSTPENAB**	**Res**			
r			rw					rw			rw	r			

Field	Bits	Type	Description
INNSTPENAB	4	rw	**Enable INN input and STP protection** 0_B **INNDIS**: INN pin not used for shoot-through protection 1_B **INNEN**: INN pin functionality enabled
ADCPWMENAB	7:5	rw	**Enable ADCPWM output** 000_B **ADCPWMAIP1OR2**: ADCPWMENAB is output AIP1/AIP2 selection by NCS_ADCSEL pin 001_B **ADCPWMAIP1**: ADCPWMENAB is output, showing AIP1 010_B **ADCPWMAIP2**: ADCPWMENAB is output, showing AIP2 011_B **ADCPWMAIP1AND2**: ADCPWMENAB is output, showing AIP1/ AIP2 interleaved 100_B **TRISTATE**: ADCPWMENAB not used, output tristated
DEADT	12:8	rw	**Dead time configuration** $\mathbf{t_{DEAD}}$ = ((jitter) +DEADT+1)*(1/fOSC,int) jitter = 0 or 1

Table 22 Reset values of PVARIANT

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.14 Status register secondary

STATUSS Offset address: 060_H

Status register secondary Reset values see: Table 23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0								Res	GATEISVCC	VALOCP2	VALOCP1	VALOCPN2	VALOCPP2	VALOCPN1	VALOCPP1
r								r	r	r	r	r	r	r	r

Field	Bits	Type	Description
VALOCPP1	0	r	**Digital level currently seen on OCPP1 pin**
VALOCPN1	1	r	**Digital level currently seen on OCPN1 pin**
VALOCPP2	2	r	**Digital level currently seen on OCPP2 pin**
VALOCPN2	3	r	**Digital level currently seen on OCPN2 pin**
VALOCP1	4	r	**OCP1 value**
VALOCP2	5	r	**OCP2 value**
GATEISVCC	6	r	**both gates are VCC**
RES0	15:8	r	

Table 23 Reset values of STATUSS

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.15 Error diagnosis secondary

DIAGS Offset address: 061_H

Error diagnosis secondary Reset values see: Table 24

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0					OCPPOD	OCPER	DESATER	OSMER	GMONER	OVLO3ER	UVLO3ER	OVLO2ER	UVLO2ER	Res	
r					r	r	r	r	r	r	r	r	r	r	

Field	Bits	Type	Description
UVLO2ER	2	r	**UVLO2 error (VCC2)**
OVLO2ER	3	r	**OVLO2 error (VCC2)**
UVLO3ER	4	r	**UVLO3 error (VEE2)**
OVLO3ER	5	r	**OVLO3 error (VEE2)**
GMONER	6	r	**Gate monitoring error**
OSMER	7	r	**Output stage monitoring error**
DESATER	8	r	**Desat error**
OCPER	9	r	**any of both OCPs indicates an error**
OCPPOD	10	r	**OCP pin open detection**
RES0	15:11	r	

Table 24 Reset values of DIAGS

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.16 Sticky bits secondary

DIAGSSTCKY Offset address: 062_H

Sticky bits secondary Reset values see: Table 25

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0					OCPPODS	OCPERS	DESATERS	OSMERS	GMONERS	OVLO3ERS	UVLO3ERS	OVLO2ERS	UVLO2ERS	SIRSTS	SPORSTS
r					r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
SPORSTS	0	r	**Secondary power on reset sticky**
SIRSTS	1	r	**Secondary internal reset sticky**
UVLO2ERS	2	r	**UVLO2 error (VCC2) sticky**
OVLO2ERS	3	r	**OVLO2 error (VCC2) sticky**
UVLO3ERS	4	r	**UVLO3 error (VEE2) sticky**
OVLO3ERS	5	r	**OVLO3 error (VEE2) sticky**
GMONERS	6	r	**Gate monitoring error sticky**
OSMERS	7	r	**Output stage monitoring error sticky**
DESATERS	8	r	**Desat error sticky**
OCPERS	9	r	**OCP error sticky**
OCPPODS	10	r	**OCP pin open detection sticky**
RES0	15:11	r	

Table 25 Reset values of DIAGSSTCKY

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.17 Secondary Supervision Control Register

SSCR Offset address: 063_H

Secondary Supervision Control Register Reset values see: Table 26

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0										SVENABLE	DESATSVTRIG	OCP2SVOPDIS	OCP1SVOPDIS	OCP2SVTRIG	OCP1SVTRIG
r										rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
OCP1SVTRIG	0	rw	**Select OCP supervision and trigger OCP1** 0_B **OFF**: OCP1 supervision disabled 1_B **ON**: OCP1 supervision enabled and OCP1 triggered
OCP2SVTRIG	1	rw	**Select OCP supervision and trigger OCP2** 0_B **OFF**: OCP2 supervision disabled 1_B **ON**: OCP2 supervision enabled and OCP2 triggered
OCP1SVOPDIS	2	rw	**OCP1 Open Detect Disable at OCP1 supervision** 0_B **EN**: OCP1 open error is enabled during supervision 1_B **DIS**: OCP1 open error is disabled during supervision
OCP2SVOPDIS	3	rw	**OCP2 Open Detect Disable at OCP2 supervision** 0_B **EN**: OCP2 open error is enabled during supervision 1_B **DIS**: OCP2 open error is disabled during supervision
DESATSVTRIG	4	rw	**Select Desat supervision and trigger Desat** 0_B **OFF**: DESAT supervision disabled 1_B **ON**: DESAT supervision enabled
SVENABLE	5	rw	**Enable supervision mode** 0_B **DIS**: supervision mode disabled 1_B **EN**: supervision mode enabled
RES0	15:6	r	

Table 26 Reset values of SSCR

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.18 Secondary Supervision Response

SSRESP Offset address: 064_H

Secondary Supervision Response Reset values see: Table 27

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0			**DESATCNT**												
r			r												

Field	Bits	Type	Description
DESATCNT	12:0	r	**Read Desat trigger time** measured time: DESATNCT*25ns
RES0	15:13	r	

Table 27 Reset values of SSRESP

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.19 Short circuit protection configuration register

SCPC Offset address: 040_H

Short circuit protection configuration register Reset values see: Table 28

15	14	13 12 11	10	9 8	7 6	5 4	3	2 1 0
DESATBTDIS	**OCPBTDIS**	**DESATOCPBT**	**OCPERR**	**OCPVL2**	**OCPVL1**	**DESATCS**	**DESATERR**	**DESATVL**
rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DESATVL	2:0	rw	**DESAT threshold voltage level** 000_B **VDESAT0**: DESAT reference level 0 001_B **VDESAT1**: DESAT reference level 1 010_B **VDESAT2**: DESAT reference level 2 011_B **VDESAT3**: DESAT reference level 3 100_B **VDESAT4**: DESAT reference level 4 101_B **VDESAT5**: DESAT reference level 5 110_B **VDESAT6**: DESAT reference level 6 111_B **VDESAT7**: DESAT reference level 7
DESATERR	3	rw	**DESAT error reaction** 0_B **HARDOFF**: DESAT reaction hard turn-off 1_B **SOFTOFF**: TON/TOFF reaction soft turn off
DESATCS	5:4	rw	**DESAT current source setting** 00_B **IDESATCS0**: DESAT current source 0 01_B **IDESATCS1**: DESAT current source 1 10_B **IDESATCS2**: DESAT current source 2 11_B **IDESATCS3**: DESAT current source 3
OCPVL1	7:6	rw	**OCP1 threshold voltage level** 00_B **VOCPD0**: Overcurrent error detection threshold 0 01_B **VOCPD1**: Overcurrent error detection threshold 1 10_B **VOCPD2**: Overcurrent error detection threshold 2 11_B **VOCPD3**: Overcurrent error detection threshold 3
OCPVL2	9:8	rw	**OCP2 threshold voltage level** 00_B **VOCPD0**: Overcurrent error detection threshold 0 01_B **VOCPD1**: Overcurrent error detection threshold 1 10_B **VOCPD2**: Overcurrent error detection threshold 2 11_B **VOCPD3**: Overcurrent error detection threshold 3
OCPERR	10	rw	**OCP error reaction** 0_B **HARDOFF**: OCP reaction hard turn-off 1_B **SOFTOFF**: TON/TOFF reaction soft turn off

(table continues...)

(continued)

Field	Bits	Type	Description
DESATOCPBT	13:11	rw	**DESAT/OCP blanking time selection** 000_B **tDESATOCPBT0**: … 111_B **tDESATOCPBT7**:
OCPBTDIS	14	rw	**OCP blanking time disable** 0_B **BTON**: Enable blanking time 1_B **BTOFF**: Disable Blanking time
DESATBTDIS	15	rw	**DESAT blanking time disable** 0_B **BTON**: Enable blanking time 1_B **BTOFF**: Disable Blanking time

Table 28 Reset values of SCPC

Reset type	Reset value	Note
Basic reset	$0D98_H$	

6.3.20 Secondary power supply monitoring level register

SPSML Offset address: 041_H

Secondary power supply monitoring level register Reset values see: Table 29

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCC2VL				**UVLO3VL**		**OVLO3VL**		**UVLO2VL**				**OVLO2VL**			
rw				rw		rw		rw				rw			

Field	Bits	Type	Description
OVLO2VL	3:0	rw	**VCC2 over voltage protection threshold selection** **V_{OVLO2H} , V_{OVLO2L}** 0_H **VOVLO2HL0**: OVLO2 threshold high/low 0 1_H **VOVLO2HL1**: OVLO2 threshold high/low 1 2_H **VOVLO2HL2**: OVLO2 threshold high/low 2 3_H **VOVLO2HL3**: OVLO2 threshold high/low 3 4_H **VOVLO2HL4**: OVLO2 threshold high/low 4 5_H **VOVLO2HL5**: OVLO2 threshold high/low 5 6_H **VOVLO2HL6**: OVLO2 threshold high/low 6 7_H **VOVLO2HL7**: OVLO2 threshold high/low 7 8_H **VOVLO2HL8**: OVLO2 threshold high/low 8

(table continues...)

(continued)

Field	Bits	Type	Description
UVLO2VL	7:4	rw	**VCC2 under voltage protection threshold selection** V_{UVLO2H} , V_{UVLO2L} 0_H **VUVLO2HL0**: UVLO2 threshold high/low 0 1_H **VUVLO2HL1**: UVLO2 threshold high/low 1 2_H **VUVLO2HL2**: UVLO2 threshold high/low 2 3_H **VUVLO2HL3**: UVLO2 threshold high/low 3 4_H **VUVLO2HL4**: UVLO2 threshold high/low 4 5_H **VUVLO2HL5**: UVLO2 threshold high/low 5 6_H **VUVLO2HL6**: UVLO2 threshold high/low 6 7_H **VUVLO2HL7**: UVLO2 threshold high/low 7 8_H **VUVLO2HL8**: UVLO2 threshold high/low 8
OVLO3VL	9:8	rw	**VEE2 over voltage protection threshold selection** V_{OVLO3H} , V_{OVLO3L} 00_B **VOVLO3HL0**: OVLO3 threshold high/low 0 01_B **VOVLO3HL1**: OVLO3 threshold high/low 1 10_B **VOVLO3HL2**: OVLO3 threshold high/low 2
UVLO3VL	11:10	rw	**VEE2 under voltage protection threshold selection** V_{UVLO3H} , V_{UVLO3L} 00_B **VUVLO3HL0**: UVLO3 threshold high/low 0 01_B **VUVLO3HL1**: UVLO3 threshold high/low 1 10_B **VUVLO3HL2**: UVLO3 threshold high/low 2
VCC2VL	15:12	rw	**Flyback VCC2 target voltage setting** 0_H **VOVSL0**: Output voltage set level 0 1_H **VOVSL1**: Output voltage set level 1 2_H **VOVSL2**: Output voltage set level 2 3_H **VOVSL3**: Output voltage set level 3 4_H **VOVSL4**: Output voltage set level 4 5_H **VOVSL5**: Output voltage set level 5 6_H **VOVSL6**: Output voltage set level 6 7_H **VOVSL7**: Output voltage set level 7 8_H **VOVSL8**: Output voltage set level 8 9_H **VOVSL9**: Output voltage set level 9 A_H **VOVSL10**: Output voltage set level 10 B_H **VOVSL11**: Output voltage set level 11 C_H **VOVSL12**: Output voltage set level 12 D_H **VOVSL13**: Output voltage set level 13 E_H **VOVSL14**: Output voltage set level 14 F_H **VOVSL15**: Output voltage set level 15

Table 29 Reset values of SPSML

Reset type	Reset value	Note
Basic reset	$E001_H$	

6.3.21 Secondary power supply monitoring error reaction register

SPSMER

Secondary power supply monitoring error reaction register

Offset address: 042_H

Reset values see: Table 30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			ENADAP	ASCIGNUVLO3	ASCIGNOVLO3	ASCIGNUVLO2	ASCIGNOVLO2	Res	UVLO3ERR	Res	OVLO3ERR	UVLO2ERR		OVLO2ERR	
r			rw	rw	rw	rw	rw	r	rw	r	rw	rw		rw	

Field	Bits	Type	Description
OVLO2ERR	1:0	rw	**VCC2 over voltage protection error reaction** 00_B **HARDOFF**: TON/TOFF reaction hard turn off 01_B **SOFTOFF**: TON/TOFF reaction soft turn off
UVLO2ERR	3:2	rw	**VCC2 under voltage protection error reaction** 00_B **HARDOFF**: TON/TOFF reaction hard turn off 01_B **SOFTOFF**: TON/TOFF reaction soft turn off
OVLO3ERR	4	rw	**VEE2 over voltage protection error reaction** 0_B **HARDOFF**: TON/TOFF reaction hard turn off 1_B **IGNORED**: No TON/TOFF Reaction, send VEE=ok over CT, but DIAG flags set correctly
UVLO3ERR	6	rw	**VEE2 under voltage protection error reaction** 0_B **HARDOFF**: TON/TOFF reaction hard turn off 1_B **IGNORED**: No TON/TOFF Reaction, send VEE=ok over CT, but DIAG flags set correctly
ASCIGNOVLO2	8	rw	**VCC2 over voltage protection ignored during ASC (no TON/TOFF reaction)** 0_B **NOTIGNORED**: 1_B **IGNORED**:
ASCIGNUVLO2	9	rw	**VCC2 under voltage protection ignored during ASC (no TON/TOFF reaction)** 0_B **NOTIGNORED**: 1_B **IGNORED**:
ASCIGNOVLO3	10	rw	**VEE2 over voltage protection ignored during ASC (no TON/TOFF reaction)** 0_B **NOTIGNORED**: 1_B **IGNORED**:
ASCIGNUVLO3	11	rw	**VEE2 under voltage protection ignored during ASC (no TON/TOFF reaction)** 0_B **NOTIGNORED**: 1_B **IGNORED**:

(table continues...)

(continued)

Field	Bits	Type	Description
ENAADAP	12	rw	**Enable adaptive flyback power feature** 0_B **DIS**: disable feature 1_B **EN**: enable adaptive power feature

Table 30 Reset values of SPSMER

Reset type	Reset value	Note
Basic reset	1055_H	

6.3.22 Soft off configuration register

STOFFC Offset address: 043_H

Soft off configuration register Reset values see: Table 31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STOFFRC						**STOFFPT**						**STOFFPVL**			
rw						rw						rw			

Field	Bits	Type	Description
STOFFPVL	3:0	rw	**Soft off plateau voltage level** V_{PLTx} 0_H **VPLT0**: Plateau voltage 0 1_H **VPLT1**: Plateau voltage 1 2_H **VPLT2**: Plateau voltage 2 3_H **VPLT3**: Plateau voltage 3 4_H **VPLT4**: Plateau voltage 4 5_H **VPLT5**: Plateau voltage 5 6_H **VPLT6**: Plateau voltage 6 7_H **VPLT7**: Plateau voltage 7 8_H **VPLT8**: Plateau voltage 8 9_H **VPLT9**: Plateau voltage 9 A_H **VPLT10**: Plateau voltage 10 B_H **VPLT11**: Plateau voltage 11 C_H **VPLT12**: Plateau voltage 12
STOFFPT	9:4	rw	**Soft off plateau time** $t_{TLTOffPLT}$ = STOFFPT * 50 ns ; value 0 sets this to 64*50ns
STOFFRC	15:10	rw	**Soft off ramp down configuration** $t_{SOFTOFF}$: STOFFRC*25 ns

Table 31 Reset values of STOFFC

Reset type	Reset value	Note
Basic reset	$00C0_H$	

6.3.23 ADC1 and ADC2 additional settings

ADCSET Offset address: 044_H

ADC1 and ADC2 additional settings Reset values see: Table 32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res												ADC2CS		ADC1CS	
r												rw		rw	

Field	Bits	Type	Description
ADC1CS	1:0	rw	**ADC1 current source setting** 00_B **IADCREF0**: ADC1 current source 0 01_B **IADCREF1**: ADC1 current source 1 10_B **IADCREF2**: ADC1 current source 2 11_B **IADCREF3**: ADC1 current source 3
ADC2CS	3:2	rw	**ADC2 current source setting** 00_B **IADCREF0**: ADC2 current source 0 01_B **IADCREF1**: ADC2 current source 1 10_B **IADCREF2**: ADC2 current source 2 11_B **IADCREF3**: ADC2 current source 3

Table 32 Reset values of ADCSET

Reset type	Reset value	Note
Basic reset	$00B5_H$	

6.3.24 Gate Monitoring and Output Stage Monitoring configuration register

GMOSMC Offset address: 045_H

Gate Monitoring and Output Stage Monitoring configuration register Reset values see: Table 33

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res										GATEISVCCDIS		OSMBT		GMBT	GMERR
r										rw		rw		rw	rw

Field	Bits	Type	Description
GMERR	0	rw	**Gate monitoring error reaction** 0_B **HARDOFF**: 1_B **SOFTOFF**:

(table continues...)

(continued)

Field	Bits	Type	Description
GMBT	2:1	rw	**Gate monitoring blanking time selection** t_{GMBTs} , t_{GMBTd} 00_B **tGMBTx0**: Disable gate monitoring 01_B **tGMBTx1**: Dynamic/static gate monitoring blanking time 1 10_B **tGMBTx2**: Dynamic/static gate monitoring blanking time 2 11_B **tGMBTx3**: Dynamic/static gate monitoring blanking time 3
OSMBT	4:3	rw	**Output stage monitoring blanking time selection** **$t_{OUTMBTs}$, $t_{OUTMBTd}$** 00_B **tOUTMBTx0**: Output stage monitoring disabled 01_B **tOUTMBTx1**: Dynamic/static output stage monitoring blanking time 1 10_B **tOUTMBTx2**: Dynamic/static output stage monitoring blanking time 2 11_B **tOUTMBTx3**: Dynamic/static output stage monitoring blanking time 3
GATEISVCCDIS	5	rw	**Disable sending over GATEISVCC information to prim side** 0_B **EN**: GATEISVCC information is sent 1_B **DIS**: GATEISVCC information is not sent

Table 33 Reset values of GMOSMC

Reset type	Reset value	Note
Basic reset	$001E_H$	

6.3.25 Active Miller Clamping configuration

AMCLPC Offset address: 046_H

Active Miller Clamping configuration Reset values see: Table 34

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res									**EAMCLPDEL**			**AMCVL**		**EAM CEN**	**IAMC DIS**
r									rw			rw		rw	rw

Field	Bits	Type	Description
IAMCDIS	0	rw	**Internal active miller clamping disable(GATE_CLAMPx not used for active clamping)** 0_B **EN**: Internal active miller clamping enabled 1_B **DIS**: Internal active miller clamping disabled
EAMCEN	1	rw	**External active miller clamping enable (AMCLPx pins used for active clamping)** 0_B **DIS**: External active miller clamping disabled 1_B **EN**: External active miller clamping enabled

(table continues...)

(continued)

Field	Bits	Type	Description
AMCVL	3:2	rw	**Active miller clamping threshold voltage level selection** 00_B **VCLAMPx0**: Clamp threshold voltage 0 01_B **VCLAMPx1**: Clamp threshold voltage 1 10_B **VCLAMPx2**: Clamp threshold voltage 2
EAMCLPDEL	6:4	rw	**External active miller clamping delay time of TON/TOFF** 000_B **TEAMCLPDELAY0**: AMCLP Propagation delay 0 001_B **TEAMCLPDELAY1**: AMCLP Propagation delay 1 010_B **TEAMCLPDELAY2**: AMCLP Propagation delay 2 011_B **TEAMCLPDELAY3**: AMCLP Propagation delay 3 100_B **TEAMCLPDELAY4**: AMCLP Propagation delay 4 101_B **TEAMCLPDELAY5**: AMCLP Propagation delay 5 110_B **TEAMCLPDELAY6**: AMCLP Propagation delay 6 111_B **TEAMCLPDELAY7**: AMCLP Propagation delay 7

Table 34 Reset values of AMCLPC

Reset type	Reset value	Note
Basic reset	0008_H	

6.3.26 Secondary Variant Configuration Register

SVARIANT Offset address: 047_H

Secondary Variant Configuration Register Reset values see: Table 35

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						AIP1 DIS	ASCS DIS	Res							
r						rw	rw	r							

Field	Bits	Type	Description
ASCSDIS	8	rw	**ASCS disable** 0_B **EN**: ASCS active 1_B **DIS**: ASCS disabled
AIP1DIS	9	rw	**This bit disables AIP1 and clamps to LOW. No CT transmissions of ADC1 when disabled.** 0_B **EN**: AIP1 active 1_B **DIS**: AIP1 disabled

Table 35 Reset values of SVARIANT

Reset type	Reset value	Note
Basic reset	0100_H	

6.3.27 Control

CTRL Offset address: 020_H

Control Reset values see: Table 36

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1							SPICE	RES0						CLRS	CLRP
r							w	r						w	w

Field	Bits	Type	Description
CLRP	0	w	**Clear primary sticky bits** 0_B **KEEP**: Keep primary sticky bits 1_B **CLRP**: Clear primary sticky bits
CLRS	1	w	**Clear secondary sticky bits** 0_B **KEEP**: Keep secondary sticky bits 1_B **CLRS**: Clear secondary sticky bits
RES0	7:2	r	**reserved**
SPICE	8	w	**SPI configuration enable** 0_B **DIS**: SPI configuration disabled 1_B **EN**: SPI configuration enabled
RES1	15:9	r	**reserved**

Table 36 Reset values of CTRL

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.28 ADC1 result register

ADC1R Offset address: 021_H

ADC1 result register Reset values see: Table 37

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0				ADC1RES											
r				r											

Field	Bits	Type	Description
ADC1RES	11:0	r	**ADC1 result**
RES0	15:12	r	

Table 37 Reset values of ADC1R

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.29 ADC2 result register

ADC2R Offset address: 022_H

ADC2 result register Reset values see: Table 38

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0				ADC2RES											
r				r											

Field	Bits	Type	Description
ADC2RES	11:0	r	**ADC2 result**
RES0	15:12	r	

Table 38 Reset values of ADC2R

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.30 Status register primary

STATUSP Offset address: 023_H

Status register primary Reset values see: Table 39

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0			Res	OPM			SPICES	CRCERRS	FLT	SRDY	RDY	ORDIAGSS	ORDIAGPS	LMAA	LMA
r			r	r			r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
LMA	0	r	**Last Message Aborted**
LMAA	1	r	**Last Message Aborted At least once**
ORDIAGPS	2	r	**OR of DIAGPSTCKY bits, except pin levels**
ORDIAGSS	3	r	**OR of DIAGSSTCKYM**
RDY	4	r	**RDY value (value driven to RDY pin)**
SRDY	5	r	**Secondary chip ready** 0x0 A fault from the secondary has been reported or communication has been lost 0x1 No faults reported from the secondary side and the communication has been established
FLT	6	r	**Fault value (inverted value driven to NFLT pin)**
CRCERRS	7	r	**sticky CRC error flag**
SPICES	8	r	**SPI configuration enable status (allows POTP/SOTP accesses when mode successfully entered)**

(table continues...)

(continued)

Field	Bits	Type	Description
OPM	11:9	r	**Operating mode** 000_B **Init_Mode**: Init Mode 001_B **Ready_Mode**: Ready Mode 010_B **Normal_Mode**: Normal Mode 011_B **ASCP_Mode**: ASCP Mode 100_B **Error_Mode**: Error Mode
RES0	15:13	r	

Table 39 Reset values of STATUSP

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.31 Error diagnosis primary

DIAGP Offset address: 024_H

Error diagnosis primary Reset values see: Table 40

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALINP	**VALINN**	**VALSI1**	**VALSI2**	**VALNRST**	**RES0**						**KPSERR**	**PLSL**	**PLS**	**Res**	
r	r	r	r	r	r						r	r	r	r	

Field	Bits	Type	Description
PLS	2	r	**Life sign aquired and not lost**
PLSL	3	r	**Life sign lost**
KPSERR	4	r	**keep state error**
RES0	10:5	r	
VALNRST	11	r	**Level currently seen on NRST pin**
VALSI2	12	r	**Level currently seen on SI2 pin**
VALSI1	13	r	**Level currently seen on SI1 pin**
VALINN	14	r	**Level currently seen on INN pin**
VALINP	15	r	**Level currently seen on INP pin**

Table 40 Reset values of DIAGP

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.32 Error diagnosis primary sticky

DIAGPSTCKY Offset address: 025_H

Error diagnosis primary sticky Reset values see: Table 41

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0											KPSERRS	PLSLS	PLSS	PIRSTS	PPORSTS
r											r	r	r	r	r

Field	Bits	Type	Description
PPORSTS	0	r	**Primary power on reset sticky - set on event occurrence**
PIRSTS	1	r	**Primary internal reset sticky - set on event occurrence**
PLSS	2	r	**Life sign sticky - set on event occurrence**
PLSLS	3	r	**Life sign lost sticky - set on event occurrence**
KPSERRS	4	r	**keep state error sticky - set on event occurrence**
RES0	15:5	r	

Table 41 Reset values of DIAGPSTCKY

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.33 Error diagnosis secondary mirrored

DIAGSMIR Offset address: 026_H

Error diagnosis secondary mirrored Reset values see: Table 42

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0					OCPPODM	OCPERM	DESATERM	OSMERM	GMONERM	OVLO3ERM	UVLO3ERM	OVLO2ERM	UVLO2ERM	Res	
r					r	r	r	r	r	r	r	r	r	r	

Field	Bits	Type	Description
UVLO2ERM	2	r	**UVLO2 error (VCC2) (mirrored)**
OVLO2ERM	3	r	**OVLO2 error (VCC2) (mirrored)**
UVLO3ERM	4	r	**UVLO3 error (VEE2) (mirrored)**
OVLO3ERM	5	r	**OVLO3 error (VEE2) (mirrored)**
GMONERM	6	r	**Gate monitoring error (mirrored)**
OSMERM	7	r	**Output stage monitoring error (mirrored)**
DESATERM	8	r	**Desat error (mirrored)**
OCPERM	9	r	**OCP error (mirrored)**
OCPPODM	10	r	**OCP pin open detection (mirrored)**
RES0	15:11	r	

Table 42 Reset values of DIAGSMIR

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.34 Error diagnosis secondary mirrored sticky version

DIAGSMIRSTCKY Offset address: 027_H

Error diagnosis secondary mirrored sticky version Reset values see: Table 43

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0					OCPPODMS	OCPERMS	DESATERMS	OSMERMS	GMONERMS	OVLO3ERMS	UVLO3ERMS	OVLO2ERMS	UVLO2ERMS	SIRSTSMS	SPORSTMS
r					r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
SPORSTMS	0	r	**Secondary power on reset sticky**
SIRSTSMS	1	r	**Secondary internal reset sticky**
UVLO2ERMS	2	r	**VCC2 UVLO2 error sticky**
OVLO2ERMS	3	r	**VCC2 OVLO2 error sticky**
UVLO3ERMS	4	r	**VEE2 UVLO3 error sticky**
OVLO3ERMS	5	r	**VEE2 OVLO3 error sticky**
GMONERMS	6	r	**Gate monitoring error sticky**
OSMERMS	7	r	**Output stage monitoring error sticky**
DESATERMS	8	r	**Desat error sticky**
OCPERMS	9	r	**OCP error sticky**
OCPPODMS	10	r	**OCP pin open detection sticky**
RES0	15:11	r	

Table 43 Reset values of DIAGSMIRSTCKY

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.35 Error diagnosis flyback

DIAGFLY Offset address: 028_H

Error diagnosis flyback Reset values see: Table 44

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLYBFSM				FLYRERR	FLYSTUP	FLYMLOW	FLYMFUL	FLYBACT	FLYBOVLOER	FLYBOPNER	FLYBOPPER	FLYTMONER	FLYBOCER	FLYMAXTER	FLYBSCHKER
undef				r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FLYBSCHKER	0	r	**Flyback error in self-check (driving MOS until sense reacts)**
FLYMAXTER	1	r	**Flyback Start-up Time (FLYMAXTUP) exceeded**
FLYBOCER	2	r	**Flyback overcurrent error (ISENSEP-N >> IPK+50%)**
FLYTMONER	3	r	**Flyback external MOSFET monitoring error (ISENSEP-N triggered at off, ext. MOS shorted)**
FLYBOPPER	4	r	**Flyback open pin error (ISENSEP)**
FLYBOPNER	5	r	**Flyback open pin error (ISENSEN)**
FLYBOVLOER	6	r	**Flyback OVLO error (VBATS)**
FLYBACT	7	r	**Flyback is active and not in FAULT or ERROR recovery procedure**
FLYMFUL	8	r	**Flyback mode 'fullpower' active**
FLYMLOW	9	r	**Flyback mode 'lowpower' active**
FLYSTUP	10	r	**Flyback currently in one of startup phase IIa/b/c**
FLYRERR	11	r	**Flyback currently in error handling loop (error occured, FLYRCYC not reached)) – remains high if retries did not succeed**
FLYBFSM	15:12	undef	**State machine States** 0_H **RESET**: Flyback is disabled 1_H **SELF_CHECK_HI_LO**: SELF_CHECK_HI/LO 2_H **SOFT_CHARGE_A**: Burst mode and no life-sign is received 3_H **SOFT_CHARGE_B**: Secondary life-sign is received and VCC2 is ramping (VCC2<9V) 4_H **SOFT_CHARGE_C**: VCC2 is ramping (VCC2>9V) to UVLO 5_H **WAIT_LIFESIGN**: Waiting for life-sign (200us) 8_H **PWM_CHARGE_FULL_PWR**: PWM_CHARGE (full power) 9_H **PWM_CHARGE_LOW_PWR**: PWM_CHARGE (low power) C_H **PWM_SKIP**: PWM_SKIP D_H **CLR_ERR_DEAD_TIME**: CLR_ERR/DEAD_TIME F_H **FAULT**: Unrecoverable error is detected, and the Flyback is shutdown.

Table 44 Reset values of DIAGFLY

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.36 Error diagnosis flyback

DIAGFLYSTCKY Offset address: 029_H

Error diagnosis flyback Reset values see: Table 45

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				FLYRERRS	FLYSTUPS	FLYMLOWS	FLYMFULS	FLYBACTS	FLYBOVLOERS	FLYBOPNERS	FLYBOPPERS	FLYTMONERS	FLYBOCERS	FLYMAXTERS	FLYBSCHKERS
r				r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FLYBSCHKERS	0	r	**Flyback error in self-check (driving MOS until sense reacts)**
FLYMAXTERS	1	r	**Flyback Start-up Time (FLYMAXTUP) exceeded**
FLYBOCERS	2	r	**Flyback overcurrent error (ISENSEP-N >> IPK+50%)**
FLYTMONERS	3	r	**Flyback external MOSFET monitoring error (ISENSEP-N triggered at off, ext. MOS shorted)**
FLYBOPPERS	4	r	**Flyback open pin error (ISENSEP)**
FLYBOPNERS	5	r	**Flyback open pin error (ISENSEN)**
FLYBOVLOERS	6	r	**Flyback OVLO error (VBATS)**
FLYBACTS	7	r	**Flyback active; '1' = AND (FLYBENA=1, no error,no lifesign loss)**
FLYMFULS	8	r	**Flyback mode 'fullpower' active**
FLYMLOWS	9	r	**Flyback mode 'lowpower' active**
FLYSTUPS	10	r	**Flyback currently in startup mode, waiting for lifesign**
FLYRERRS	11	r	**Flyback currently in error handling loop (error occured, FLYRCYC not reached)**

Table 45 Reset values of DIAGFLYSTCKY

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.37 Status register secondary

STATUSSMIR Offset address: $02A_H$

Status register secondary Reset values see: Table 46

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0									GATEISVCCMIR	VALOCP2MIR	VALOCP1MIR	VALOCPN2MIR	VALOCPP2MIR	VALOCPN1MIR	VALOCPP1MIR
r									r	r	r	r	r	r	r

Field	Bits	Type	Description
VALOCPP1MIR	0	r	**Digital level currently seen on OCPP1 pin mirrored form SUSER.STATUSS**
VALOCPN1MIR	1	r	**Digital level currently seen on OCPN1 pin mirrored form SUSER.STATUSS**

(table continues...)

(continued)

Field	Bits	Type	Description
VALOCPP2MIR	2	r	**Digital level currently seen on OCPP2 pin mirrored form SUSER.STATUSS**
VALOCPN2MIR	3	r	**Digital level currently seen on OCPN2 pin mirrored form SUSER.STATUSS**
VALOCP1MIR	4	r	**OCP1 value mirrored form SUSER.STATUSS**
VALOCP2MIR	5	r	**OCP2 value mirrored form SUSER.STATUSS**
GATEISVCCMIR	6	r	**Gate is VCC mirrored**
RES0	15:7	r	

Table 46 Reset values of STATUSSMIR

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.38 Status register secondary

STATUSSMIRSTCKY Offset address: $02B_H$

Status register secondary Reset values see: Table 47

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0									GATEISVCCMIRS	VALOCP2MIRS	VALOCP1MIRS	VALOCPN2MIRS	VALOCPP2MIRS	VALOCPN1MIRS	VALOCPP1MIRS
r									r	r	r	r	r	r	r

Field	Bits	Type	Description
VALOCPP1MIRS	0	r	**Sticky Digital level currently seen on OCPP1 pin mirrored form SUSER.STATUSS**
VALOCPN1MIRS	1	r	**Sticky Digital level currently seen on OCPN1 pin mirrored form SUSER.STATUSS**
VALOCPP2MIRS	2	r	**Sticky Digital level currently seen on OCPP2 pin mirrored form SUSER.STATUSS**
VALOCPN2MIRS	3	r	**Sticky Digital level currently seen on OCPN2 pin mirrored form SUSER.STATUSS**
VALOCP1MIRS	4	r	**Sticky OCP1 value mirrored form SUSER.STATUSS**
VALOCP2MIRS	5	r	**Sticky OCP2 value mirrored form SUSER.STATUSS**
GATEISVCCMIRS	6	r	**Gate is VCC mirrored**
RES0	15:7	r	

Table 47 Reset values of STATUSSMIRSTCKY

Reset type	Reset value	Note
Basic reset	0000_H	

6.3.39 Read address for next shift out

READADDR Offset address: $0FF_H$

Read address for next shift out Reset values see: Table 48

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR															
w															

Field	Bits	Type	Description
ADDR	15:0	w	

Table 48 Reset values of READADDR

Reset type	Reset value	Note
Basic reset	0000_H	

7 Switching characteristics

7.1 Functional description switching

The turn ON propagation delay is defined from rising edge of PWM input signal to rising edge of TON, the turn OFF propagation delay is defined from falling edge of PWM input signal to falling edge of TOFF. The specified propagation delays include an additional delay caused by the configured EAMCLP delay (configurable via SPI).

$t_{PD,total} = t_{PDON/OFF} + t_{EAMCLPDELAYx}$

Note: The propagation delay timings in this chapter refer to $t_{EAMCLPDELAY0}$. $t_{PD,total}$ will be extended by the delay times described in the EAMCLP chapter, as stated in the formula above.

7.2 Electrical characteristics switching

Table 49 Electrical characteristics switching

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level output peak current	I_{OUTH}	–	–	- 15	A	INP = V_{VCC1}, SI1 = SI2 = $V_{VCC1,}$ TON = rising edge to V_{VCC2}, CLAMP/ GATE = $V_{VEE2,}$ V_{VCC2} = 15 V, V_{VEE2} = -5 V, C_{LOAD}= 250 nF	PRQ-88
Low level output peak current	I_{OUTL}	15	–	–	A	INP = V_{GND1}, SI1 = SI2 = $V_{VCC1,}$ TOFF = falling edge to V_{VEE2}, CLAMP/ GATE = $V_{VCC2,}$ VCC2 = 15 V, VEE2 = -5 V, C_{LOAD}= 250 nF	PRQ-89
Propagation delay - On	t_{PDON}	40	60	120	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no load (C_{LOAD} <=100 pF), no gate resistance, no AMCLPx activated	PRQ-90

(table continues...)

Table 49 (continued) Electrical characteristics switching

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Propagation delay - Off	t_{PDOFF}	40	60	120	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP falling edge at $V_{digital,input(low)}$, Stop: TOFF falling edge at V_{VCC2} - 1.5 V, no load (C_{LOAD} <=100 pF), no gate resistance, no AMCLPx activated	PRQ-91
Propagation delay distortion	$t_{Prop,dis}$	-20	–	20	ns	t_{PDON} - t_{PDOFF}, t_{PDON} & t_{PDOFF} measured @ same T_{JUNC}	PRQ-92
Rise time 90 %	t_{Rise1}	–	–	45	ns	no C_{LOAD}, R_{LOAD} = 1.69 Ω, V_{VCC2} = 15 V, V_{VEE2} = -5 V, V_{TON} = V_{VEE2} + 1.5 V to V_{TON} = V_{VCC2} - 1.5 V	PRQ-95
Rise time 70 %	t_{Rise2}	–	–	35	ns	no C_{LOAD}, R_{LOAD} = 1.69 Ω, V_{VCC2} = 15 V, V_{VEE2} = -5 V, V_{TON} = V_{VEE2} + 1.5 V to V_{TON} = V_{VCC2} - 3 V	PRQ-96
Fall time	t_{Fall}	–	–	45	ns	No C_{LOAD}, R_{LOAD} = 1.69 Ω, V_{VCC2} = 15 V, V_{VEE2} = -5 V, V_{TOFF} = V_{VCC2} - 1.5 V to V_{TOFF} = V_{VEE2} + 1.5 V	PRQ-97
TON RDSON High-side P&N	$R_{DSON-OSHP}$	0.44	–	1.1	Ω	Voltage drop V_{VCC2} - V_{TON} < 1 V	PRQ-98
TOUT RDSON High-side	$R_{DSON-OSHN}$	–	0.35	–	Ω	N-MOS, tolerances according to $R_{DSON-OSLN}$	PRQ-683
TOFF RDSON Low-side	$R_{DSON-OSLN}$	0.15	–	0.37	Ω	Voltage drop V_{TOFF} - V_{VEE2} < 1 V	PRQ-99
Switching frequency	f_{SW}	–	–	450	kHz	V_{VCC2} = 18 V, V_{VEE2} = -5 V, $C_{total,TON/TOFF}$ = 15 nF, R_{gon1} + R_{gon2} = 6 Ω, T_{AMB} = 90°C	PRQ-743
Internal OSC frequency	$f_{OSC,int}$	38	40	42	MHz		PRQ-813

8 RDY

8.1 Functional description RDY

The RDY pin reports whether the device is ready.

Note: Please refer to signal event activation table for a detailed overview over the events triggering a not ready.

The RDY pin has a passive clamping.

Note: Passive clamping keeps RDY = 0 in case of no supply.

Table 50 RDY signal event activation list

Event	SPI Diagnosis	TON/TOFF	Configurable	SPI config register	SI1, SI2
UVLO1L threshold triggered	DIAGP	turn-off	no	-	Not active
OVLO2H threshold triggered	DIAGS	configurable	Voltage levels, error reaction	SPSML, SPSMER	Active
UVLO2L threshold triggered	DIAGS	configurable	Voltage levels, error reaction	SPSML, SPSMER	Active
OVLO3L threshold triggered	DIAS	configurable	Voltage levels, error reaction	SPSML, SPSMER	Active
UVLO3H threshold triggered	DIAGS	configurable	Voltage levels, error reaction	SPSML, SPSMER	Active
Gate1 monitoring error	DIAGS	configurable	Blanking time, error reaction	GMOSMC	Not active
Gate2 monitoring error	DIAGS	configurable	Blanking time, error reaction	GMOSMC	Not active
Output stage monitoring error	DIAGS	tri-state	Blanking time	GMOSMC	Not active
STP keep state time out error	DIAGP	turn-off	no	-	Not active
Prim. internal supervision error	DIAGP	turn-off	no	-	Not active
Sec. internal supervision error	DIAGS	turn-off	no	-	Not active

Note:

- *In case of OVLO2/3, UVLO2/3 error SI1 and SI2 inputs remain active, but priority can be configured in bit fields SPSMER.ASCIGNxVLOx*
- *All events listed above lead to an low condition on RDY pin. Last Message aborted can be caused by transmit or processing errors*
- *For OVLO2, UVLO2, OVLO3, UVLO3: RDY state changes status due to primary ASC trigger of SI1/SI2*
- *If flyback is only VCC2/VEE2 supply: In case of UVLO1 or flyback fault RDY will not go "high" at start-up and in operation RDY goes "low" after crossing of UVLO2 threshold*
- *At floating VCC1 the passive clamping of RDY applies*

8.2 Electrical characteristics RDY

Table 51 Electrical characteristics RDY

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDY open drain output low level	$V_{RDY(low)}$	0.05	0.3	0.5	V	$V_{VCC1} \geq 4.55$ V; I_{load} = 5 mA	PRQ-103
RDY output low passive clamping	$V_{RDYCLAMP}$	0.25	0.5	1	V	$I_{RDYCLAMP}$ = 500 µA; V_{CC1} = floating	PRQ-104
Time from rising Edge NRST to RDY = high	$t_{NRST2RDY}$	50	–	200	ns	No error detected, Start: NRST rising edge 50 %, stop point = RDY rises edge 0.5 V with 2.5 k pull-up, VCC1 = typ.	PRQ-201

9 Fault

9.1 Functional description fault

The device has an active low fault pin (NFLT) to report DESAT and OCP short circuit events (Event class A).

If the device switches off the output stage due to a DESAT or OCP event, it goes to Error_Mode and signal the event on pin NFLT with NFLT = 0 within t_{NFLT_DESAT} or t_{NFLT_OCP}.

The fault signal stays available until a reset event takes place.

Note: All events are cleared with the rising edge on NRST.

Table 52 NFLT signal event activation list

Event	SPI Diagnosis	TON/TOFF	Configurable	SPI config register	SI1, SI2
OCP threshold triggered	DIAGS	turn-off	Voltage levels, error reaction	SCPC	Not active
DESAT threshold triggered	DIAGS	turn-off	Voltage levels, current source, error reaction	SCPC	Not active

Note: All events listed above lead to an low condition on NFLT pin. Last Message aborted can be caused by transmit or processing errors.

9.2 Electrical characteristics fault

Table 53 Electrical characteristics fault

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP event detection to NFLT activation	t_{NFLT_OCP}	–	1.2	4.3	µs	$V_{OCP\_Overdrive}$= +/-200 mV, slew rate = 100 mV/ns; NFLT = 90%, R_{PU_NFLT} = 1 kΩ;	PRQ-110
DESAT event detection to NFLT activation	t_{NFLT_DESAT}	–	1.5	4.5	µs	$V_{DESAT\_Overdrive}$= +/-200 mV, slew rate = 10 V/µs; NFLT = 90%, R_{PU_NFLT} = 1 kΩ;	PRQ-111
NFLT open drain output low level	V_{NFLT}	0.05	0.3	0.5	V	V_{VCC1} ≥ 4.55 V; I_{NFLT} = 5 mA	PRQ-112

10 DESAT (Collector/Drain Monitoring)

10.1 Functional description DESAT

The device monitors the IGBT voltage (V_{CE}) or SiC voltage (V_{DS}) when TON = high(VCC2). If the selected reference level (V_{DESATx}) is reached, it issues a turn-off within $t_{DESAT2OFFx}$ (Event Class A generated), then changes into Error_Mode and signals a NFLT low in t_{NFLT_DESAT}.

The DESAT pin has an internal clamping which clamps DESAT to V_{DESATL} in case TON/TOFF = low (VEE2), TON/TOFF = $V_{SOffPLT}$ or tristate. The clamp is released after the DESAT blanking time is exceeded.

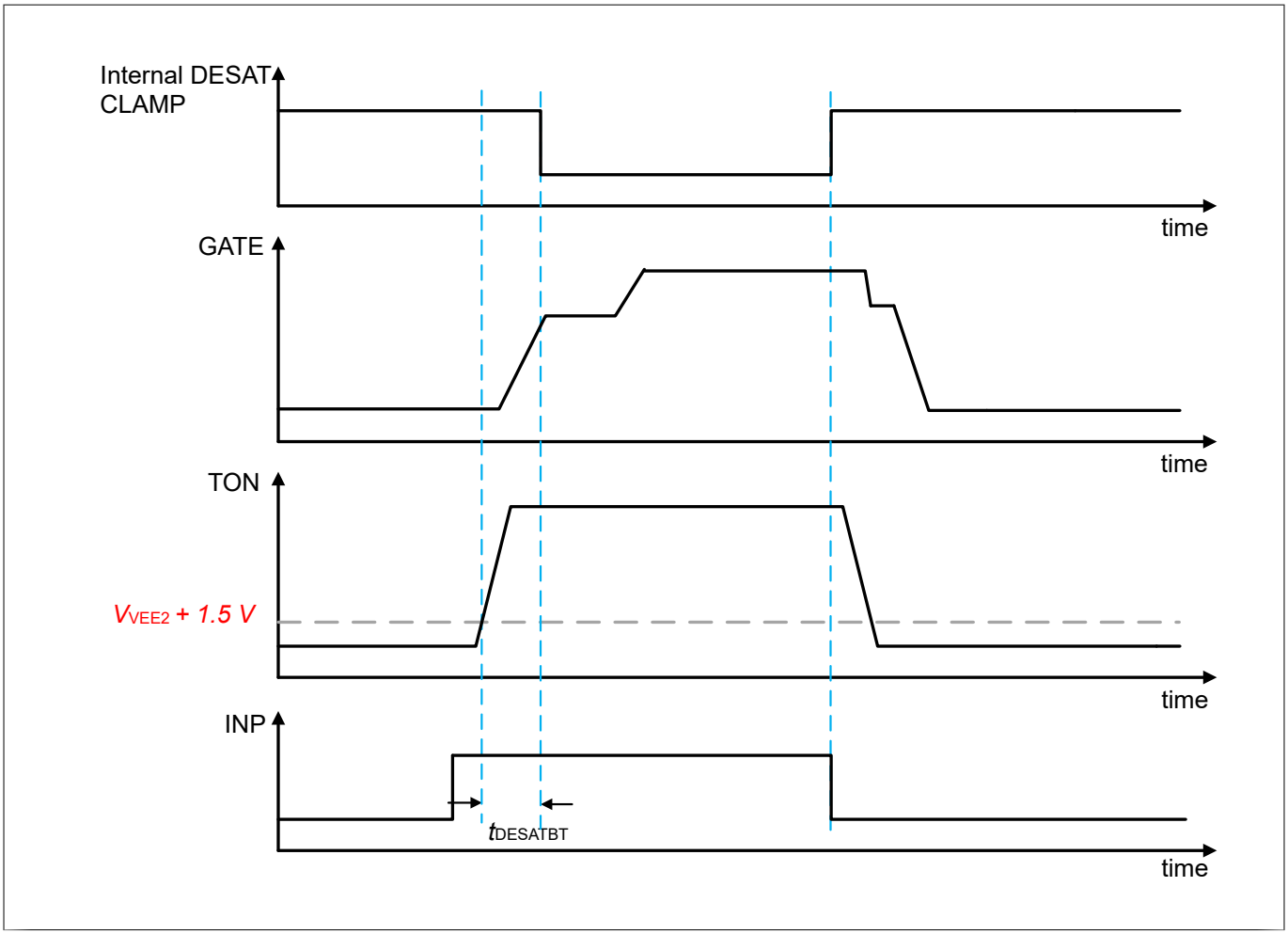

Figure 8 DESAT clamping and blanking timing diagram

The DESAT blanking time can be configured via bit field SCPC.DESATOCPBT.

Note: DESAT and OCP blanking time are configured in the same bit field.

The current source level is configurable via bit SCPC.DESATCS.

The DESAT blanking time can be disabled via SCPC.DESATBTDIS

Note: This bit disables the DESAT blanking time independent on the blanking time setting and the OCP blanking time disable function.

The DESAT threshold level is configurable via bit SCPC.DESATVL.

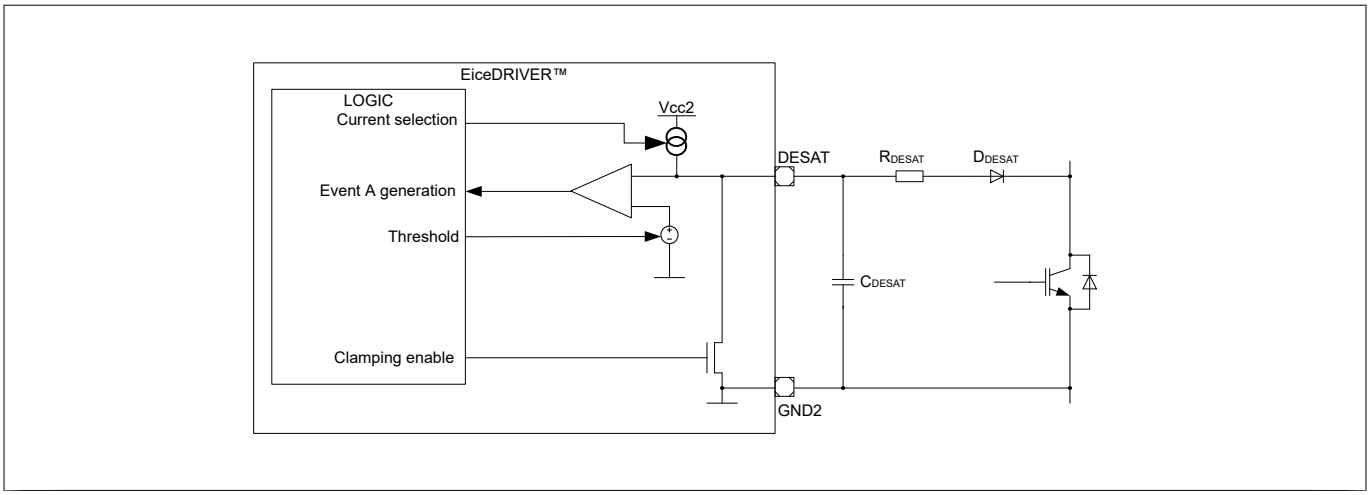

Figure 9 DESAT diagram of principle

The safe turn-off behavior for DESAT (Event Class A) can be configured via bit SCPC.DESATERR.

The device allows different configuration in terms of turn-off behavior. Due to this possibility also the timings differ from each other depending on the configuration of the turn-off.

Two timings are specified to give an overview of the different modes and the influence of it.

In the figure below the two level turn off is shown and the corresponding turn-off time from event to output reaction $t_{DESAT2OFF1}$.

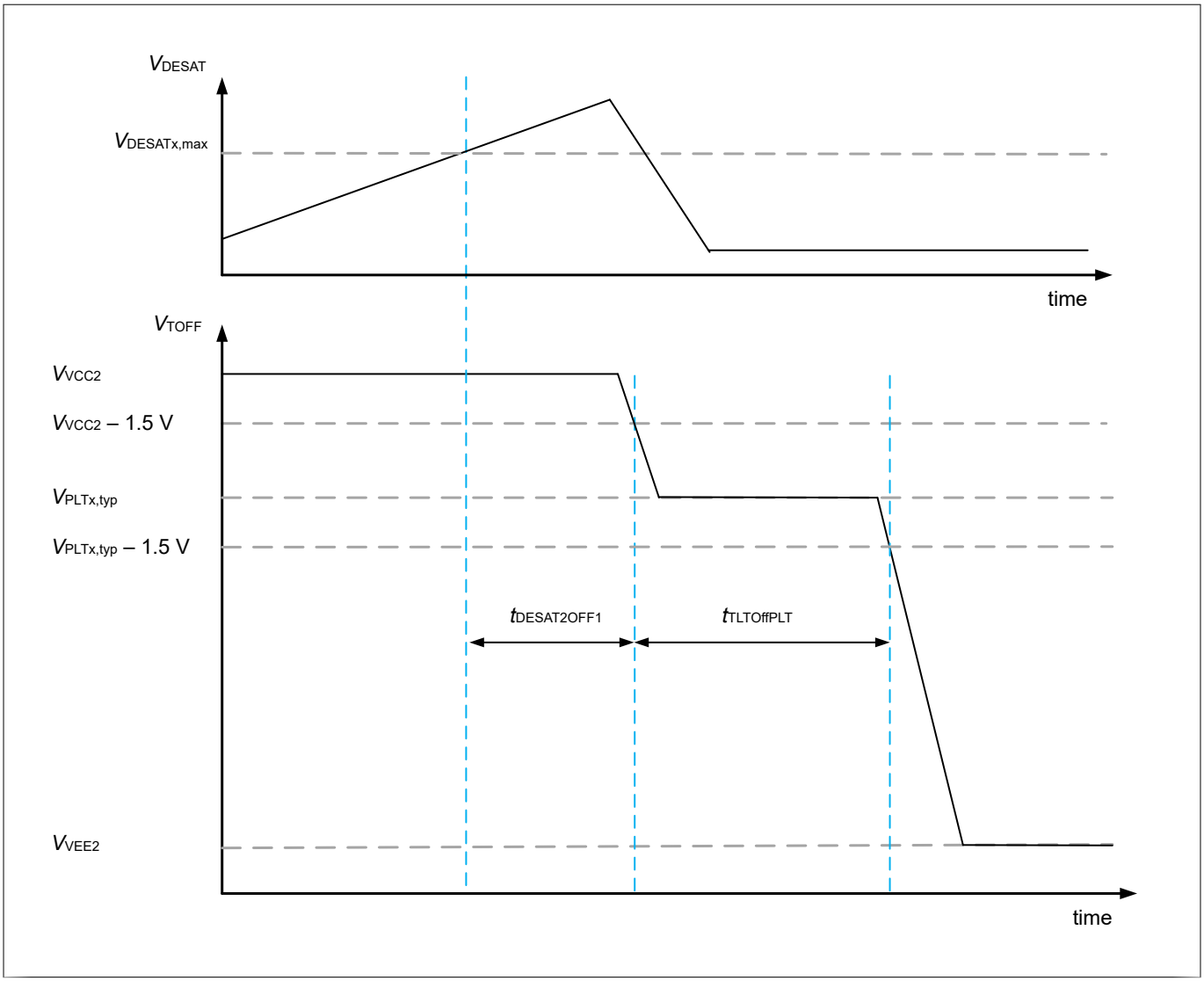

Figure 10 DESAT timing diagram for two-level-turn-off switching

In the next diagram the hard turn off is shown and the corresponding turn-off time from event to output reaction $t_{DESAT2OFF2}$.

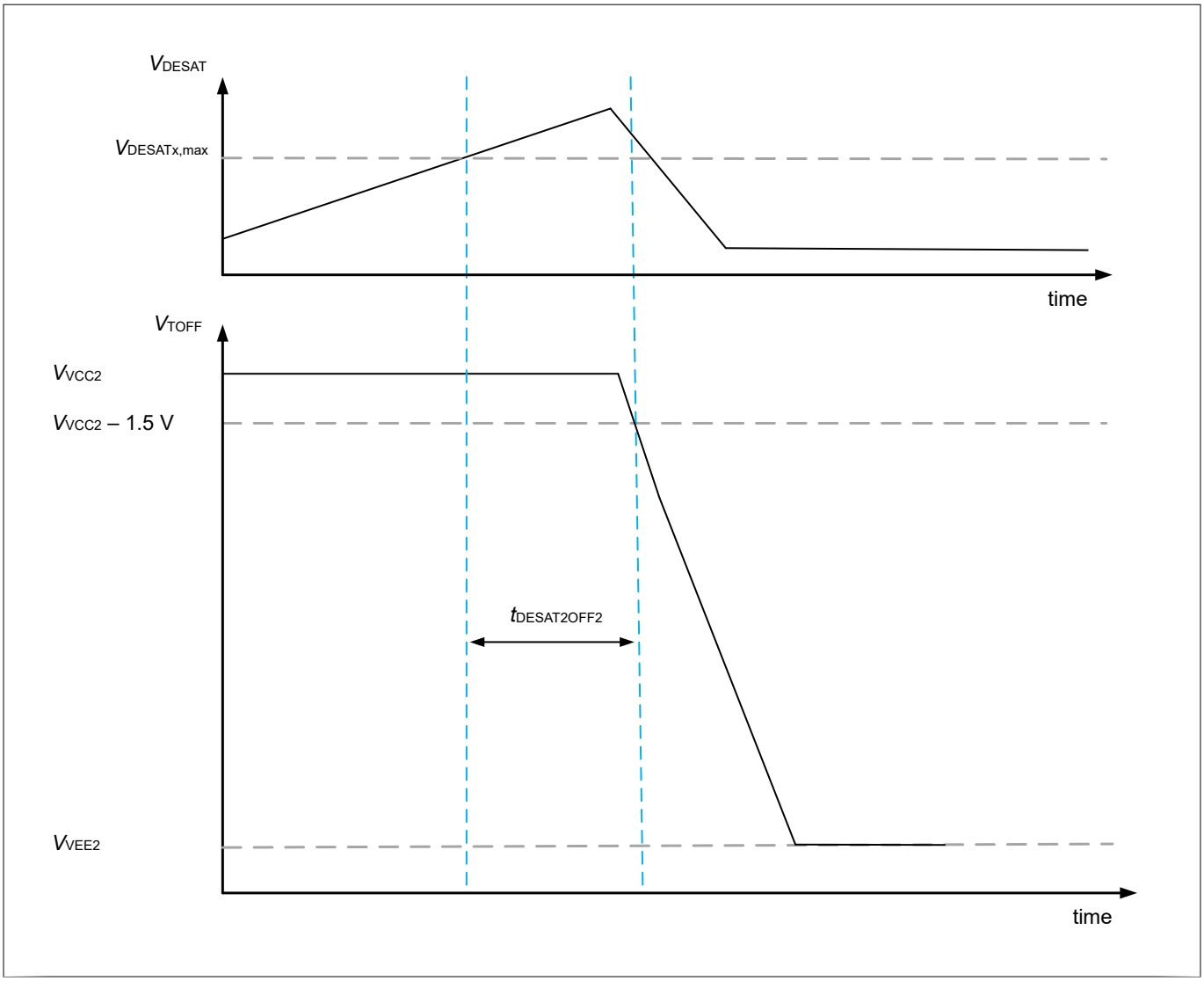

Figure 11 DESAT timing diagram for hard turn off switching

The device has an integrated DESAT self test to check the correct functionality of DESAT.

The DESAT self test can be triggered via bit field SSCR.DESATSVTRIG. The device will issue an artificial DESAT event, which will be notified on the NFLT pin and in the SPI diagnosis. A timer will count from DESAT self test event trigger to DESAT event recognition. This timing is available in bit field SSRESP.DESATCNT. The device is set to error_mode as a "real" DESAT error would. Therefore the bit field SSCR.DESATSVTRIG needs to be unset and the NRST pin needs to be triggered for OPM mode transition.

10.2 Electrical characteristics DESAT

Table 54 Electrical characteristics DESAT

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT reference level 0	V_{DESAT0}	8.7	9	9.3	V	VCC2 = typ., VEE2 = typ.	PRQ-121
DESAT reference level 1	V_{DESAT1}	8.2	8.5	8.7	V	VCC2 = typ., VEE2 = typ.	PRQ-227
DESAT reference level 2	V_{DESAT2}	7.7	8	8.3	V	VCC2 = typ., VEE2 = typ.	PRQ-123
DESAT reference level 3	V_{DESAT3}	7.2	7.5	7.8	V	VCC2 = typ., VEE2 = typ.	PRQ-122
DESAT reference level 4	V_{DESAT4}	6.7	7	7.3	V	VCC2 = typ., VEE2 = typ.	PRQ-124
DESAT reference level 5	V_{DESAT5}	6.2	6.5	6.8	V	VCC2 = typ., VEE2 = typ.	PRQ-125
DESAT reference level 6	V_{DESAT6}	5.7	6	6.3	V	VCC2 = typ., VEE2 = typ.	PRQ-126
DESAT reference level 7	V_{DESAT7}	5.2	5.5	5.8	V	VCC2 = typ., VEE2 = typ.	PRQ-228
DESAT current source 0	$I_{DESATCS0}$	0.1	1	10	µA	DESAT clamping = off, DESAT current source = off, VCC2 = 15 V, VCC1 = 5 V, VEE2 = -5 V, INP = V_{VCC1}, INN = V_{GND1}, DESAT = 9 V,	PRQ-231
DESAT current source 1	$I_{DESATCS1}$	-550	-500	-450	µA	DESAT ≤ V_{DESAT0}, referenced to GND2	PRQ-127
DESAT current source 2	$I_{DESATCS2}$	-1100	-1000	-900	µA	DESAT ≤ V_{DESAT0}, referenced to GND2	PRQ-229
DESAT current source 3	$I_{DESATCS3}$	-1650	-1500	-1350	µA	DESAT ≤ V_{DESAT0}, referenced to GND2	PRQ-230
DESAT low voltage	V_{DESATL}	10	50	100	mV	Referenced to GND2, DESAT clamping enabled, I_{sink} = 5 mA.	PRQ-128
DESAT detection & reaction time 1	$t_{DESAT2OFF1}$	–	140	195	ns	$V_{DESAT\_Overdrive}$= +/-2 V, Slew rate @ DESAT = 10 V/µs, TOFF = V_{VCC2} - 1.5 V, $C_{LOAD\_TON/TOFF}$ = $R_{LOAD\_TON/TOFF}$ = no load, TLTOFF = enabled	PRQ-129
DESAT detection & reaction time 2	$t_{DESAT2OFF2}$	–	120	170	ns	$V_{DESAT\_Overdrive}$= +/-2 V, Slew rate @ DESAT = 10 V/µs; TOFF = V_{VCC2} - 1.5 V, TON/TOFF no load, TLTOFF = disabled	PRQ-272

(table continues...)

Table 54 (continued) Electrical characteristics DESAT

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT negative transient current	$I_{DESATNTC}$	-50	–	–	mA	$t_{DESATNTC}$ = 500 ns, TON = $V_{VEE2,}$ TOFF = $V_{VEE2,,}$ DESAT clamping = on, $f_{s,max}$ = 60 kHz	PRQ-232
DESAT blanking time 0	$t_{DESATOCPBT0}$	138	160	180	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-716
DESAT blanking time 1	$t_{DESATOCPBT1}$	236	260	284	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-717
DESAT blanking time 2	$t_{DESATOCPBT2}$	332	360	393	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-718
DESAT blanking time 3	$t_{DESATOCPBT3}$	427	460	493	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-719

(table continues...)

Table 54 (continued) Electrical characteristics DESAT

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT blanking time 4	$t_{DESATOCPBT4}$	522	560	598	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-720
DESAT blanking time 5	$t_{DESATOCPBT5}$	620	660	705	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-721
DESAT blanking time 6	$t_{DESATOCPBT6}$	715	760	807	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-722
DESAT blanking time 7	$t_{DESATOCPBT7}$	805	860	915	ns	From TON = V_{VEE2} + 1.5 V to release of clamping (DESAT pin voltage rising above 0.5 V, with internal current source, no external C_{LOAD}) , $I_{DESATCS1}$ selected	PRQ-723

11 Overcurrent protection (OCP)

11.1 Functional description OCP

The device monitors the voltage difference between OCPPx and OCPNx when TON = high (VCC2). If the corresponding reference level (V_{OCPDx}) is reached, it issues a turn-off (Event Class A generated) within $t_{OCP2OFFx}$, then changes into Error_Mode and signals a NFLT low in t_{NFLT_OCP}.

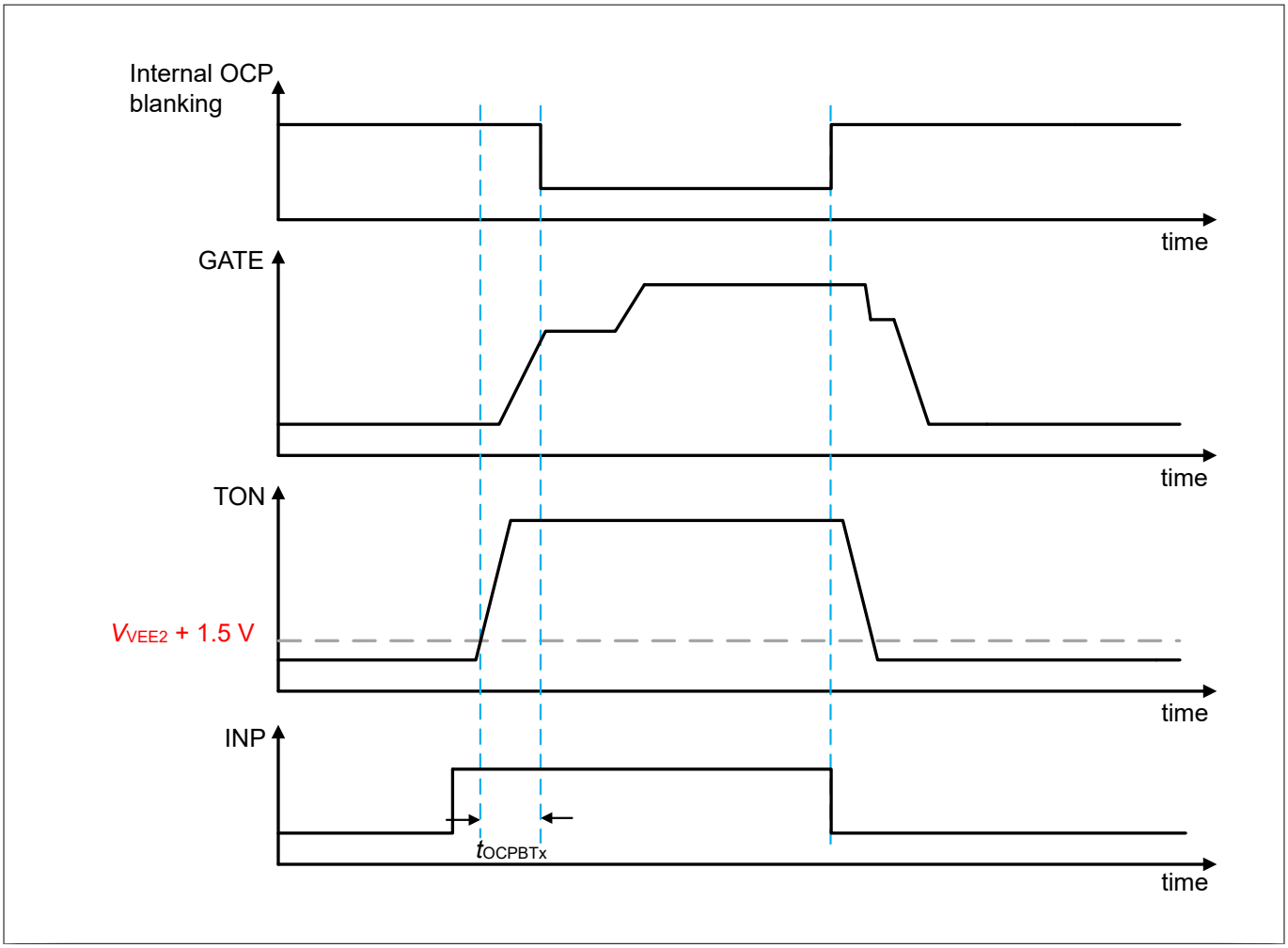

Figure 12 OCP blanking timing

The OCP blanking time can be configured via bit field SCPC.DESATOCPBT.

Note: DESAT and OCP blanking time are configured in the same bit field.

The OCP blanking time can be disabled via bit field SCPC.OCPBTDIS, this means that the blanking time is 0.

Note: This bit disables the OCP blanking time independent on the blanking time setting and the DESAT blanking time disable function.

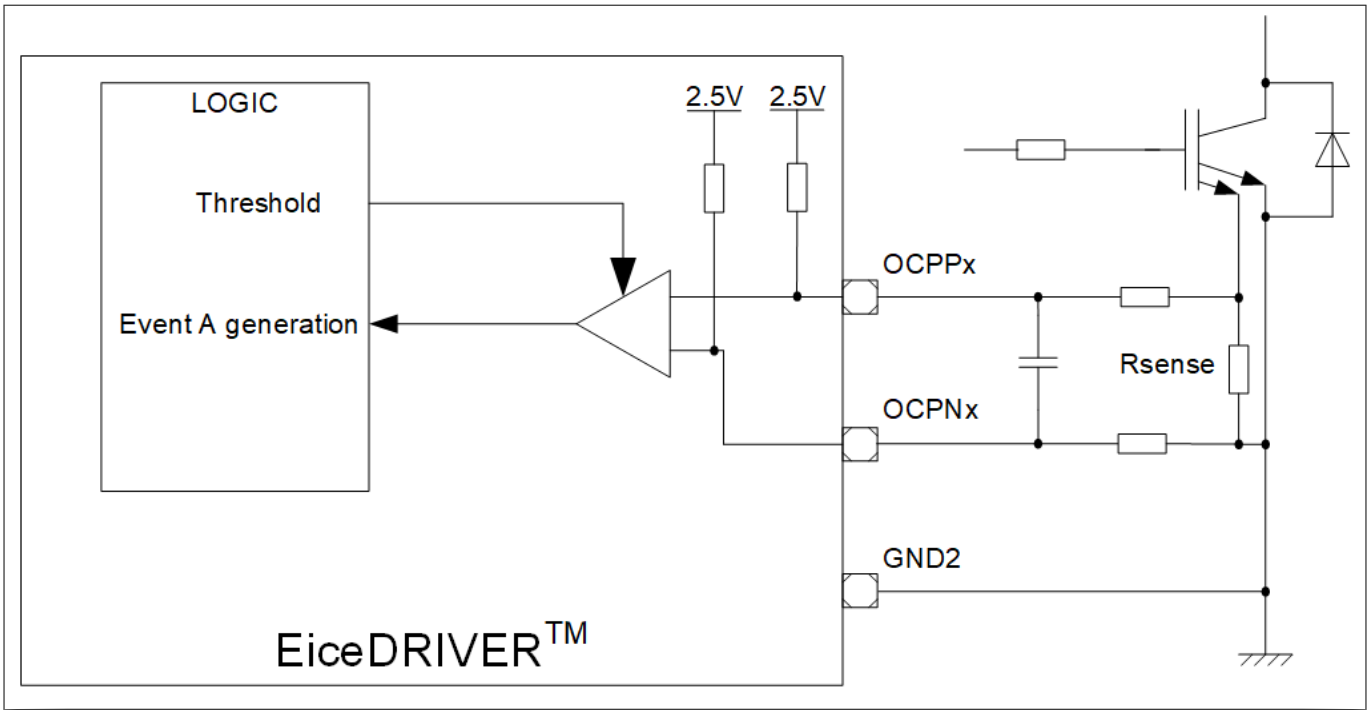

Figure 13 OCP diagram of principle

The OCP threshold level is configurable separately for OCP1 and OPC2 via bit fields SCPC.OCPVL1 and SCPC.OCPVL2.

The safe turn-off behavior for OCP (Event class A) can be configured via bit SCPC.OCPERR.

The device allows different configuration in terms of turn-off behavior. Due to this possibility also the timings differ from each other depending on the configuration of the turn-off.

Two timings are specified to give an overview of the different modes and the influence of it.

In the figure below the two level turn off is shown and the corresponding turn-off time from event to output reaction $t_{OCP2OFF1}$.

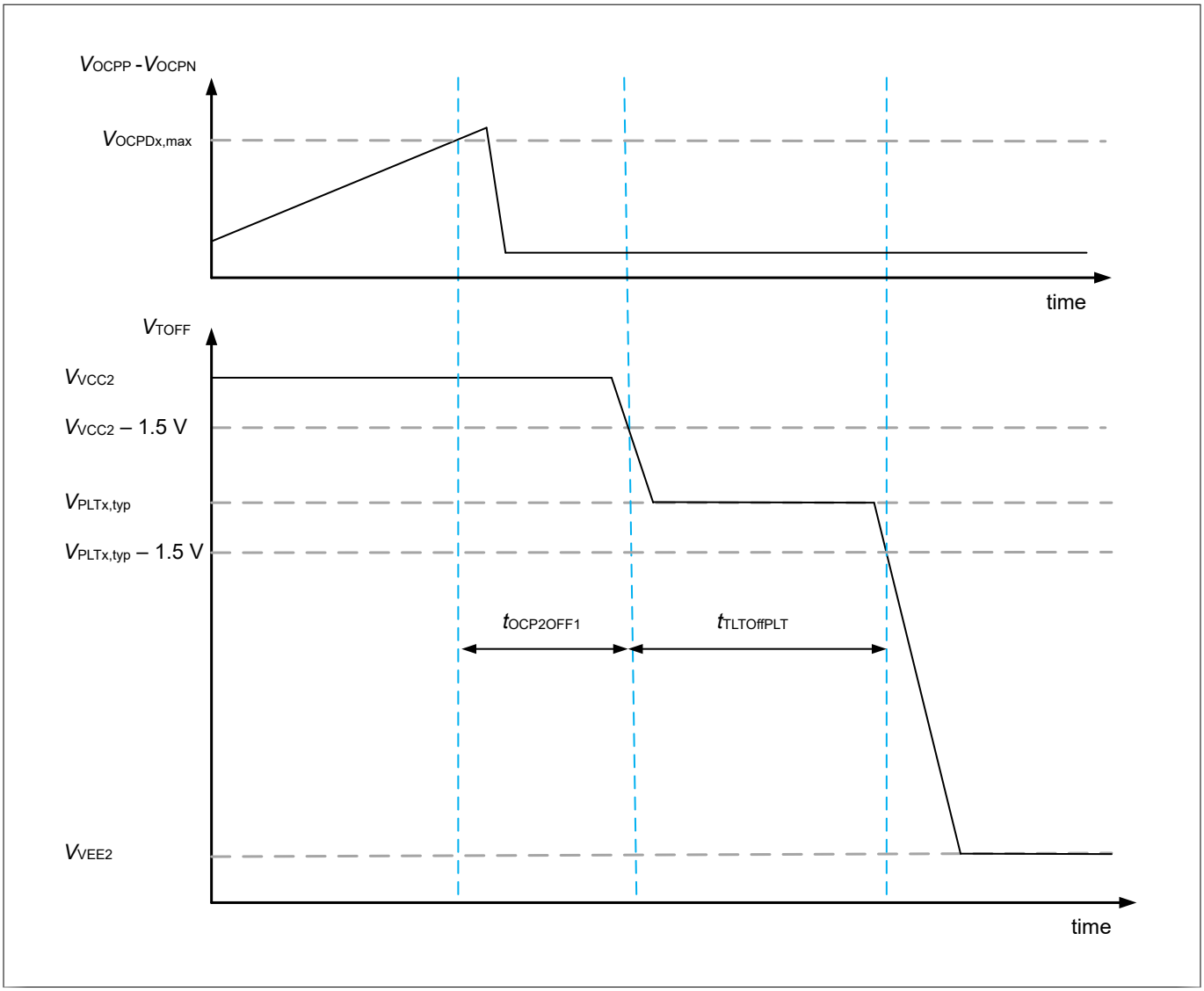

Figure 14 OCP timing diagram for two-level-turn-off switching

In the next diagram the hard turn off is shown and the corresponding turn-off time from event to output reaction $t_{OCP2OFF2}$.

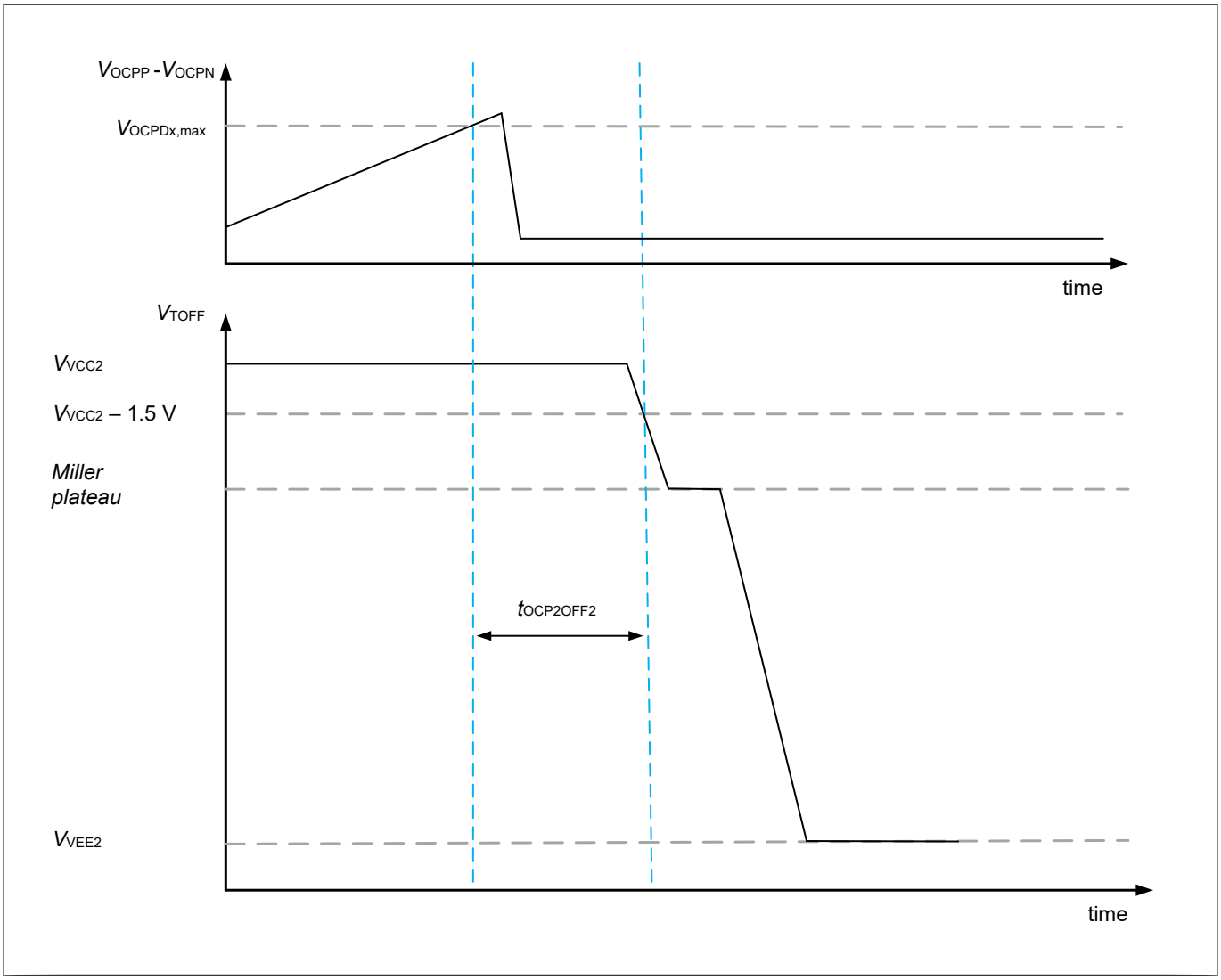

Figure 15 OCP timing diagram for hard turn off switching

The device has an integrated OCP self test to check the correct functionality of OCPx.

The OCPx self test for OCP1 or OCP2 can be triggered via bit field SSCR.OCP1SVTRIG or SSCR.OCP2SVTRIG. The device will issue an artificial OCP event, which will be notified on the NFLT pin and in the SPI diagnosis. Additionally an OCP pin open detection error will be triggered and notified on RDY pin and in the SPI diagnosis. The device is set to error_mode as a "real" OCP error would. Therefore the bit field SSCR.OCPxSVTRIG needs to be unset and the NRST pin needs to be triggered for OPM mode transition.

Note:

- *OCP1 and OCP2 self test needs to be triggered separately*

The additional OCP open pin detection error and RDY pin notification by an OCPx self test trigger can be disabled via bit fields SSCR.OCP1SVOPDIS or SSCR.OCP2SVOPDIS.

11.2 Electrical characteristics OCP

Table 55 Electrical characteristics OCP

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent error detection threshold 0	V_{OCPD0}	670	700	731	mV	V_{OCPPx} - V_{OCPNx}	PRQ-132
Overcurrent error detection threshold 1	V_{OCPD1}	864	900	935	mV	V_{OCPPx} - V_{OCPNx}	PRQ-133
Overcurrent error detection threshold 2	V_{OCPD2}	475	500	528	mV	V_{OCPPx} - V_{OCPNx}	PRQ-187
Overcurrent error detection threshold 3	V_{OCPD3}	573	600	630	mV	V_{OCPPx} - V_{OCPNx}	PRQ-188
OCPPx & OCPNx pull-up resistance	R_{PUOCP2}	25	–	100	kΩ		PRQ-134
OCP detection & reaction time 1	$t_{OCP2OFF1}$	–	120	170	ns	$V_{OCPx\_Overdrive}$= 600 mV, slew rate = 100 mV/ns, TOFF = V_{VCC2} - 1.5 V, after blanking time is elapsed, $C_{LOAD\_TON/TOFF}$ = $R_{LOAD\_TON/TOFF}$ = no load, TLTOFF = enabled	PRQ-271
OCP detection & reaction time 2	$t_{OCP2OFF2}$	–	100	150	ns	$V_{OCPx\_Overdrive}$= 600 mV, slew rate = 100 mV/ns, TOFF = V_{VCC2} - 1.5 V, after blanking time is elapsed, $C_{LOAD\_TON/TOFF}$ = $R_{LOAD\_TON/TOFF}$ = no load, TLTOFF = disabled	PRQ-136
OCP blanking time 0	$t_{DESATOCPBT0}$	138	160	180	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-724
OCP blanking time 1	$t_{DESATOCPBT1}$	236	260	284	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-725

(table continues...)

Table 55 (continued) Electrical characteristics OCP

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP blanking time 2	$t_{DESATOCPBT2}$	332	360	393	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-726
OCP blanking time 3	$t_{DESATOCPBT3}$	427	460	493	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-727
OCP blanking time 4	$t_{DESATOCPBT4}$	522	560	598	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-728
OCP blanking time 5	$t_{DESATOCPBT5}$	620	660	705	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-729
OCP blanking time 6	$t_{DESATOCPBT6}$	715	760	807	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-730
OCP blanking time 7	$t_{DESATOCPBT7}$	805	860	915	ns	From V_{TON} = V_{VEE2} + 1.5 V to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns	PRQ-731

12 Power supply voltage monitoring

12.1 Functional description power supply voltage monitoring

The device is equipped with an undervoltage lockout for the Input chip (VCC1) and Output chip (VCC2 & VEE2) in order to ensure correct switching of the IGBT/SiC.

The device is equipped with an overvoltage lockout for the secondary supply VCC2 and VEE2 in order to prevent damage of the IGBT/SiC.

The device turns off the IGBTs/SiC and ignores signals at SI1, SI2 and INP (go into Init_Mode) if the power supply VCC1 drops below V_{UVLO1L}. It returns to Ready_Mode, if the voltage at VCC1 is above V_{UVLO1H} and the device received a rising edge at NRST.

Note: In Error_Mode, RDY changes to 0.

The undervoltage lockout level for VCC2 (UVLO2) can be configured in bit SPSML.UVLO2VL.

The undervoltage lockout error reaction for VCC2 (UVLO2) can be configured in bit SPSMER.UVLO2ERR.

Note:

- *The UVLO2 function can't be disabled, but ignored (only warning created).*

The device turns off the IGBTs/SiC within $t_{UVLO22OFF}$ and ignores signals at INP (go into Error_Mode and set UVLO2ER) within t_{PS2RDY} if the power supply VCC2 drops below V_{UVLO2L_x}. It returns to Ready_Mode (UVLO2ER cleared) if the voltage at VCC2 is above V_{UVLO2H_x} and the device received a rising edge at NRST.

Note:

- *In Error_Mode, RDY changes to 0*
- *Exception: Primary ASC via SI1/SI2 --> TON = high (VCC2)*

The overvoltage lockout level for VCC2 (OVLO2) can be configured in bit SPSML.OVLO2VL.

The overvoltage lockout error reaction for VCC2 (OVLO2) can be configured in bit SPSMER.OVLO2ERR.

The device turns off the IGBTs/SiC within $t_{OVLO22OFF}$ and ignores signals at INP (go into Error_Mode and set OVLO2ER) within t_{PS2RDY} if the power supply V_{VCC2} rises above V_{OVLO2H_x}. It returns to Ready_Mode and clear OVLO2ER if the voltage V_{VCC2} is below V_{OVLO2L_x} and the device received a rising edge at NRST.

Note:

- *In Error_Mode, RDY changes to 0*
- *Exception: Primary ASC via SI1/SI2 --> TON = high (VCC2)*

The undervoltage lockout level for VEE2 (UVLO3) can be configured in bit SPSML.UVLO3VL.

The undervoltage lockout error reaction for VEE2 (UVLO3) can be configured in bit SPSMER.UVLO3ERR.

Note:

- *The UVLO3 function can't be disabled, but ignored (only warning created)*

The device turns off the IGBTs/SiC within $t_{UVLO32OFF}$ and ignores signals at INP (go into Error_Mode and set UVLO3ER) within t_{PS2RDY} if the power supply VEE2 drops below V_{UVLO3L_x}. It returns to Ready_Mode (clear UVLO3ER) if the voltage at VEE2 is above V_{UVLO3H_x} and the device received a rising edge at NRST.

Note:

- *In Error_Mode, RDY changes to 0*
- *Exception: Primary ASC via SI1/SI2 --> TON = high (VCC2)*

The device keeps the signal at the output TON/TOFF as before and sets the error bit UVLO3ER in the status register, if the power supply VEE2 drops below V_{UVLO3L_x}. Signals at SI1, SI2 and INP are not ignored and device

is not turning into Error_Mode within t_{PS2RDY}. The error must be cleared by SPI message after the external failure condition is gone.

Note:
Error is sticky until it is cleared by SPI message or NRST rising edge.

The overvoltage lockout level for VEE2 (OVLO3) can be configured in bit SPSML.OVLO3VL.

The overvoltage lockout function for VEE2 (OVLO3) can be configured in the register SPSMER.OVLO3ERR.

Note

- *Note: The OVLO3 function can't be disabled, but ignored (only warning created)*

The device turns off the IGBTs/SiC within $t_{OVLO22OFF}$ and ignores signals at INP (go into Error_Mode and set OVLO3ER) within t_{PS2RDY} if the power supply voltage V_{VEE2} at VEE2 rises above V_{OVLO3H_x}. It returns to Ready_Mode (clear OVLO3ER) if the voltage V_{VEE2} is below V_{OVLO3L_x} and the device received a rising edge at NRST.

Note:

- *In Error_Mode, RDY changes to 0*
- *Exception: Primary ASC via SI1/SI2 --> TON = high (VCC2)*

The device keep the signal at the output TON/TOFF as before and sets the error bit OVLO3ER in the status register, if the power supply voltage V_{VEE2} at VEE2 rises above V_{OVLO3H_x}. Signals at SI1, SI2 and INP are not ignored and device is not turning into Error_Mode within t_{PS2RDY}. The error must be cleared by SPI message (OVLO3ER) after the external failure condition is gone.

Note:
In Error_Mode, RDY changes to 0.

The UVLO/OVLO on VCC2 and VEE2 is ignored during an ASC trigger, if bit fields SPSMER.ASCIGNUVLO2/3 or SPSMER.ASCIGNOVLO2/3 is set to 1.

Note: If the ASC request is triggered during an UVLO2/OVLO2 detection or reaction event that happened either before or concurrently with the ASC trigger, then the output (TON/TOFF) may have the state "Low" (VEE) even after the ASC is triggered, in which case the ASC command has to be re-triggered in order to activate ASC.

12.2 Electrical characteristics power supply voltage monitoring

Table 56 Electrical characteristics power supply voltage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO1 threshold low	V_{UVLO1L}	4.09	4.23	4.36	V	@ VCC1, referenced to GND1	PRQ-162
UVLO1 threshold high	V_{UVLO1H}	4.18	4.32	4.45	V	@ VCC1, referenced to GND1	PRQ-163
UVLO1 detection & reaction time	$t_{UVLO12OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-183
UVLO2 detection & reaction time	$t_{UVLO22OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-184
OVLO2 detection & reaction time	$t_{OVLO22OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-185
Power Supply Monitoring detection and notification time	t_{PS2RDY}	–	2.5	4.5	µs	VCC2 = 15 V, VEE2 = -5 V	PRQ-186
Power up timing: Time from UVLO1 release to device operable	t_{PUprim}	–	200	800	µs	Secondary chip running	PRQ-199
Power up timing: Time from UVLO2 release to device operable	t_{PUsec}	–	200	800	µs	Primary chip running	PRQ-200
OVLO3 threshold high 0	V_{OVLO3H_0}	-3.1	-2.9	-2.75	V	VEE2 to GND2; configurable via SPI	PRQ-751
OVLO3 threshold low 0	V_{OVLO3L_0}	-3.95	-3.7	-3.5	V	VEE2 to GND2; configurable via SPI	PRQ-752
OVLO3 threshold high 1	V_{OVLO3H_1}	-4.6	-4.15	-3.7	V	VEE2 to GND2; configurable via SPI	PRQ-753
OVLO3 threshold low 1	V_{OVLO3L_1}	-4.95	-4.7	-4.5	V	VEE2 to GND2; configurable via SPI	PRQ-754
OVLO3 threshold high 2	V_{OVLO3H_2}	-6.1	-5.8	-5.55	V	VEE2 to GND2; configurable via SPI	PRQ-755
OVLO3 threshold low 2	V_{OVLO3L_2}	-6.9	-6.6	-6.3	V	VEE2 to GND2; configurable via SPI	PRQ-756
UVLO3 threshold high 0	V_{UVLO3H_0}	-6.9	-6.4	-6.15	V	VEE2 to GND2; configurable via SPI	PRQ-757
UVLO3 threshold low 0	V_{UVLO3L_0}	-7.65	-7.2	-6.9	V	VEE2 to GND2; configurable via SPI	PRQ-758

(table continues...)

Table 56 (continued) Electrical characteristics power supply voltage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO3 threshold high 1	V_{UVLO3H_1}	-9.85	-9.5	-9.1	V	VEE2 to GND2; configurable via SPI	PRQ-759
UVLO3 threshold low 1	V_{UVLO3L_1}	-10.75	-10.3	-9.9	V	VEE2 to GND2; configurable via SPI	PRQ-760
UVLO3 threshold high 2	V_{UVLO3H_2}	-12.1	-11.6	-11.2	V	VEE2 to GND2; configurable via SPI	PRQ-761
UVLO3 threshold low 2	V_{UVLO3L_2}	-12.95	-12.45	-12.0	V	VEE2 to GND2; configurable via SPI	PRQ-762
OVLO3 detection & reaction time	$t_{OVLO32OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-429
UVLO3 detection & reaction time	$t_{UVLO32OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-428
OVLO2 threshold high 0	V_{OVLO2H_0}	15.5	16.0	16.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-763
OVLO2 threshold low 0	V_{OVLO2L_0}	15.0	15.5	16.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-764
OVLO2 threshold high 1	V_{OVLO2H_1}	16.5	17	17.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-765
OVLO2 threshold low 1	V_{OVLO2L_1}	16	16.5	17	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-766
OVLO2 threshold high 2	V_{OVLO2H_2}	17.4	18.0	18.6	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-767
OVLO2 threshold low 2	V_{OVLO2L_2}	16.9	17.5	18.1	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-768
OVLO2 threshold high 3	V_{OVLO2H_3}	18.4	19	19.6	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-769
OVLO2 threshold low 3	V_{OVLO2L_3}	17.8	18.4	19.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-770

(table continues...)

Table 56 (continued) Electrical characteristics power supply voltage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OVLO2 threshold high 4	V_{OVLO2H_4}	19.4	20.0	20.6	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-771
OVLO2 threshold low 4	V_{OVLO2L_4}	18.8	19.4	20.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-772
OVLO2 threshold high 5	V_{OVLO2H_5}	20.4	21.0	21.6	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-773
OVLO2 threshold low 5	V_{OVLO2L_5}	19.75	20.1	20.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-774
OVLO2 threshold high 6	V_{OVLO2H_6}	21.3	22.0	22.7	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-775
OVLO2 threshold low 6	V_{OVLO2L_6}	20.6	21.3	22.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-776
OVLO2 threshold high 7	V_{OVLO2H_7}	22.3	23.0	23.7	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-777
OVLO2 threshold low 7	V_{OVLO2L_7}	21.6	22.3	23.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-778
OVLO2 threshold high 8	V_{OVLO2H_8}	23.3	24.0	24.7	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-779
OVLO2 threshold low 8	V_{OVLO2L_8}	22.6	23.3	24.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-780
UVLO2 threshold high 0	V_{UVLO2H_0}	10.0	10.3	10.6	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-781
UVLO2 threshold low 0	V_{UVLO2L_0}	9.65	9.9	10.25	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-782

(table continues...)

Table 56 (continued) Electrical characteristics power supply voltage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO2 threshold high 1	V_{UVLO2H_1}	10.9	11.3	11.7	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-783
UVLO2 threshold low 1	V_{UVLO2L_1}	10.6	11.0	11.3	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-784
UVLO2 threshold high 2	V_{UVLO2H_2}	12.0	12.4	12.8	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-785
UVLO2 threshold low 2	V_{UVLO2L_2}	11.6	12.0	12.4	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-786
UVLO2 threshold high 3	V_{UVLO2H_3}	13.0	13.4	13.8	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-787
UVLO2 threshold low 3	V_{UVLO2L_3}	12.6	13.0	13.4	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-788
UVLO2 threshold high 4	V_{UVLO2H_4}	14.0	14.4	14.8	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-789
UVLO2 threshold low 4	V_{UVLO2L_4}	13.55	14.0	14.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-790
UVLO2 threshold high 5	V_{UVLO2H_5}	15.0	15.5	16.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-791
UVLO2 threshold low 5	V_{UVLO2L_5}	14.5	15.0	15.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-792
UVLO2 threshold high 6	V_{UVLO2H_6}	16.0	16.5	17.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-793
UVLO2 threshold low 6	V_{UVLO2L_6}	15.5	16.0	16.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-794

(table continues...)

Table 56 (continued) Electrical characteristics power supply voltage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO2 threshold high 7	V_{UVLO2H_7}	17.0	17.5	18.0	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-795
UVLO2 threshold low 7	V_{UVLO2L_7}	16.5	17.0	17.5	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-796
UVLO2 threshold high 8	V_{UVLO2H_8}	17.9	18.5	19.1	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-797
UVLO2 threshold low 8	V_{UVLO2L_8}	17.4	18.0	18.6	V	@ VCC2; referenced to GND2; configurable via SPI	PRQ-798
UVLO1 hysteresis	$V_{UVLO1HYS}$			3	%	Related to V_{UVLO1H}	PRQ-873
UVLO2 hysteresis	$V_{UVLO2HYS}$			3.04	%	Related to $V_{UVLO2H,x}$, valid for all UVLO2,x settings	PRQ-869
OVLO2 hysteresis	$V_{OVLO2HYS}$			3.04	%	Related to $V_{OVLO2H,x}$, valid for all OVLO2,x settings	PRQ-870
UVLO3 hysteresis	$V_{UVLO3HYS}$			3.04	%	Related to $V_{UVLO3H,x}$, valid for all UVLO3,x settings	PRQ-872
OVLO3 hysteresis	$V_{OVLO3HYS}$			3.04	%	Related to $V_{OVLO3H,x}$, valid for all OVLO3,x settings	PRQ-871

13 Shoot-through protection (STP)

13.1 Functional description STP

The device has a Shoot-Through Protection (STP) function to prevent both high-side and low-side switches to be activated simultaneously.

The shoot-through protection can be enabled by activating INN input on INN/ADCPWM pin via bit field PVARIANT.INNSTPENAB.

Note: The ADCPWM function needs to be disable via register PVARIANT.ADCPWMEN = 0x04

Note: In case INP is shorted to INN and both are activated simultaneously, the output stage might be switched to "high".

If one of the drivers is in ON state, the driver's counterpart PWM input is inhibited, preventing it to turn on.

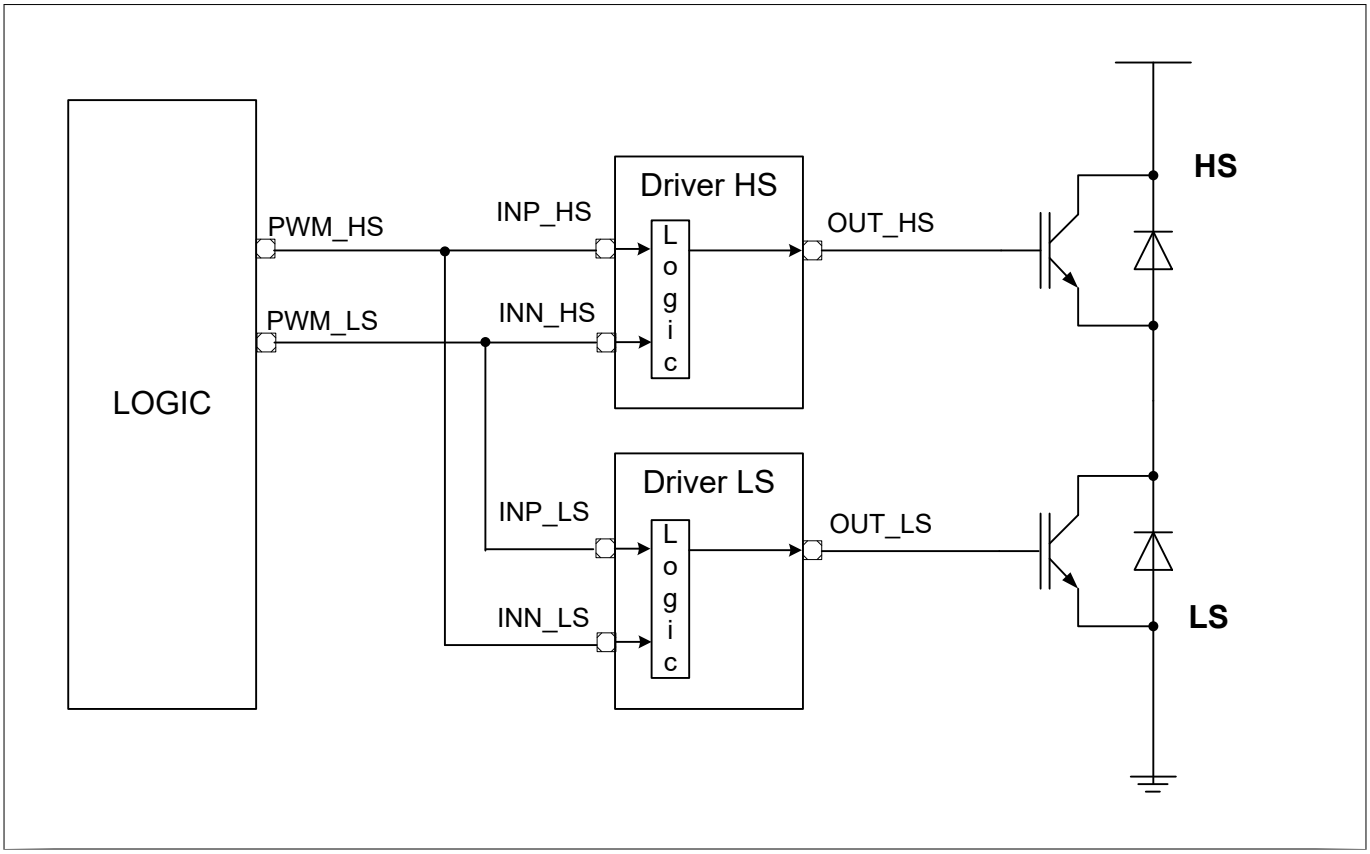

Figure 16 Shoot-through protection application diagram

The device follows the shoot-through protection timing diagram shown below:

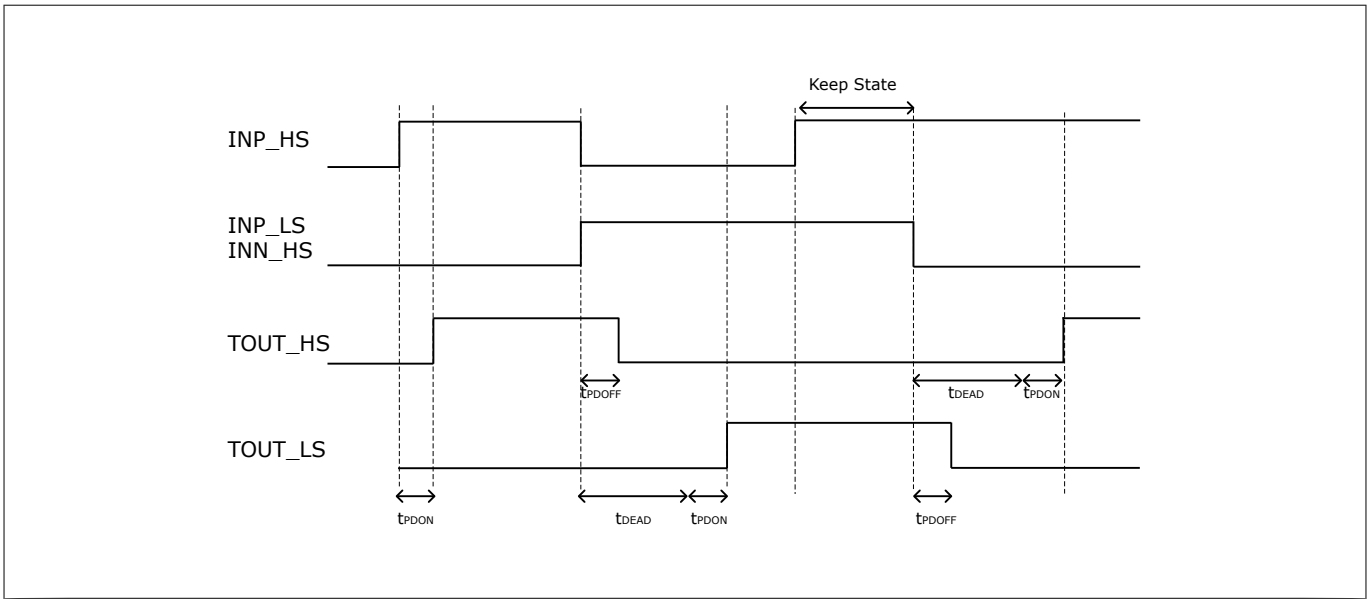

Figure 17 Shoot-through protection timing diagram

Note: This diagram shows INN assertion during INP = "high". The same behavior is achieved if INP is asserted during INN = "high".

The shoot-through protection dead time can be configured via bit field PVARIANT.DEADT.

If the maximum keep state time $t_{keepstate,max}$ is exceeded a turn-off (TOFF = low (VEE2)) is triggered, bit DIAGP.KPSERR is set and RDY is set to low.

13.2 Electrical characteristics STP

Table 57 Electrical characteristics STP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Dead time for shoot-through protection	t_{DEAD}	50	–	900	ns	Minimum setting of DEADT = 1.	PRQ-638
Keep state time limit	$t_{keepstate}$		2	2.21	µs		PRQ-656

14 External TON/TOFF control

14.1 Functional description external TON/TOFF control

PWM signal refers to INP signal

The device has two safety input pins SI1 and SI2 that define different safe states. Possible input combinations and their safe state are shown in the following table.

Table 58 Safety input states

Safety input state	SI1*	SI2	TON/TOFF	Exception
SI_OFF (soft or hard-off)	0	0	Low (VEE2)	Init_Mode, Error_Mode
SI_ASCP	0	1	High (VCC2)	See table "Driver status at failure events/ conditions during ASCP"
SI_OFF (soft or hard-off)	1	0	Low (VEE2)	Init_Mode, Error_Mode
SI_PWM	1	1	PWM	Init_Mode, Error_Mode

*: 0 means a lower voltage than $V_{digital,input(low)}$ is applied on SI1 or SI2, 1 means a higher voltage than $V_{digital,input(high)}$ is applied on SI1 or SI2

The turn-off behavior of the SI1/2 turn-OFF transition (soft or hard OFF) can be configured via bit field PINPC.SITOC.

The PWM signal is valid only if safety inputs are set to PWM state. The PWM signal is ignored by the primary ASC function, if INP was already high before an SI1/SI2 transition, or until $t_{CTdelay}$ if exceed in certain transitions. A primary ASC trigger applies after a configurable delay time $t_{ASCdelay}$ (via bit PINPC.ASCDEL) to avoid a potential shoot-through caused by slow soft turn-off ramps. Different turn-off behavior of the output stage can be configured (hard turn-off or soft turn-off) for safety input triggered turn-offs. This configuration can be done in the primary input configuration register. All mode transitions at a configured hard turn-off are shown in the following diagram.

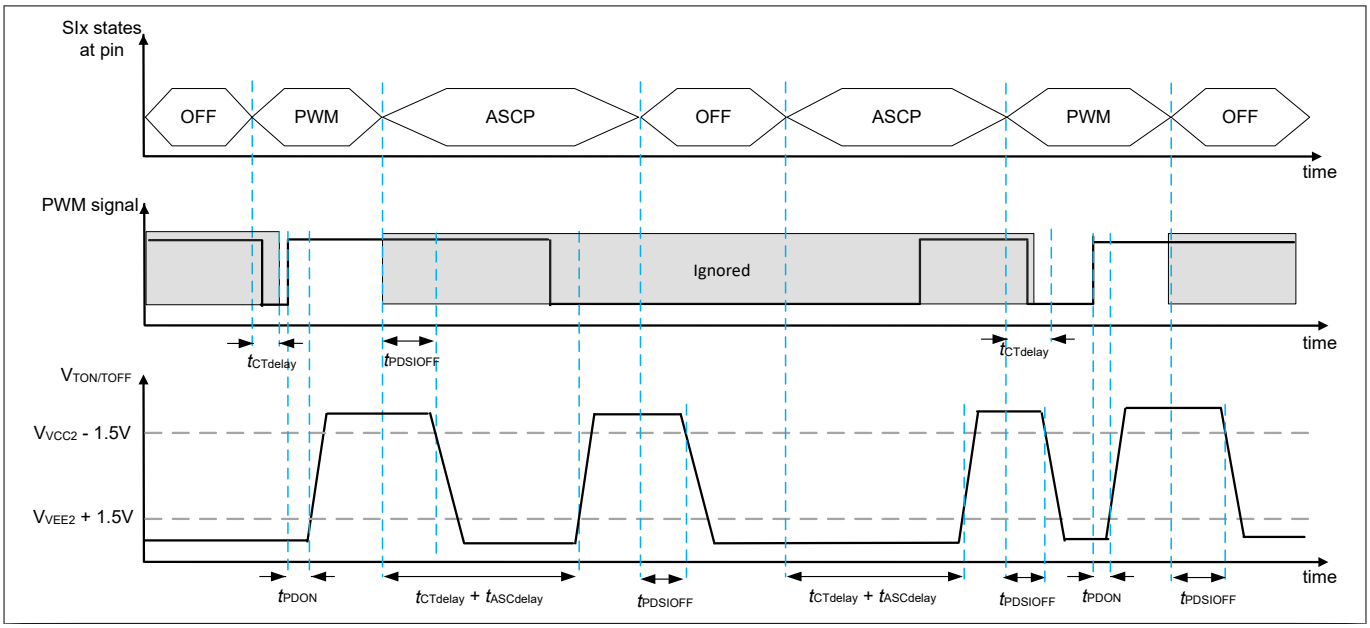

Figure 18 Safety input states transition diagram with hard turn-off

All mode transitions at a configured soft turn-off are shown in the following diagram.

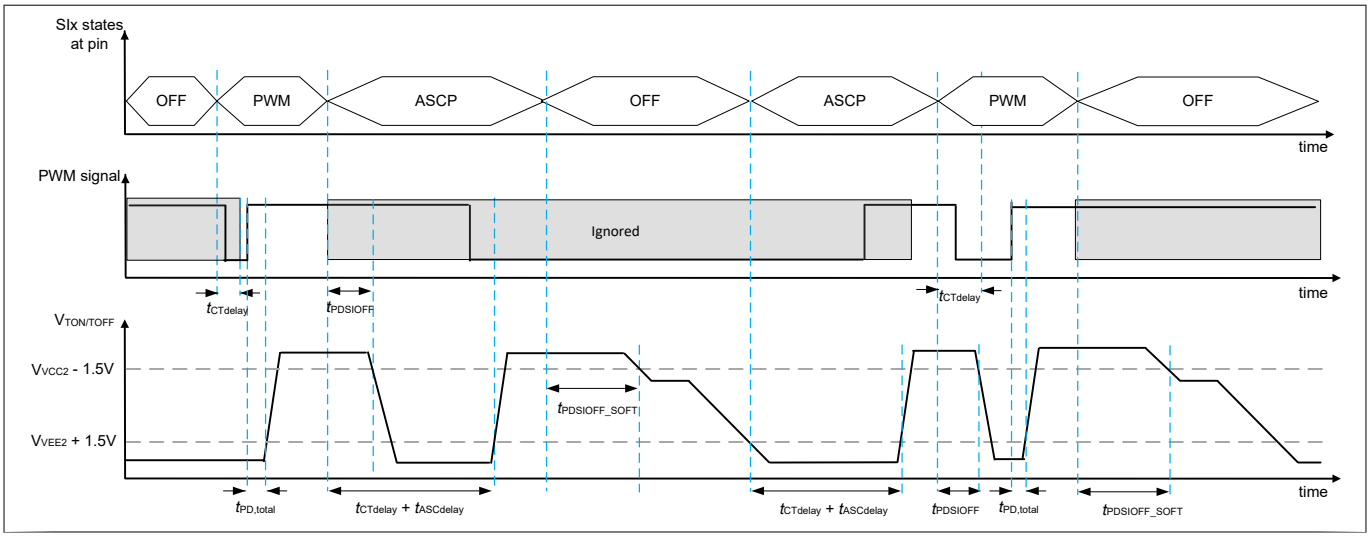

Figure 19 Safety input states transition diagram with soft turn-off

In order to receive a valid mode change via SI1/SI2 transition, the according high/low levels need to be applied for a minimum of $t_{ASCdelay} + t_{CTdelay}$.

For valid safety mode transitions (OFF, PWM, ASCP) the second required SI1/SI2 signal change from "high" to "low" or vice versa needs to be applied before a defined filter time $t_{SIfilter}$ is elapsed, as shown in the diagram below. A second change in Si1/SI2 must be stable for $t_{SIfilter}$ in order to apply a valid SI1/SI2 transition.

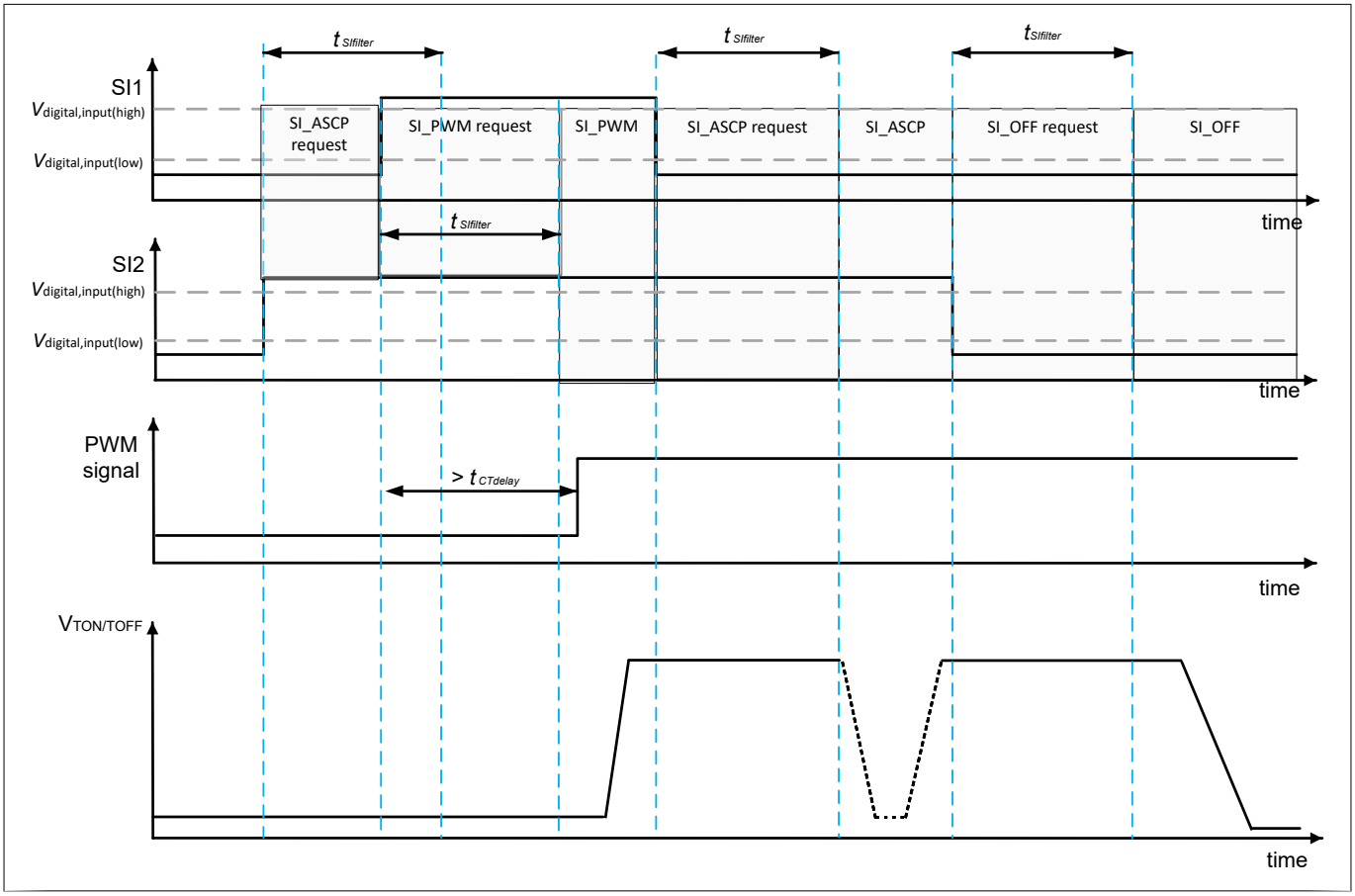

Figure 20 SI1/SI2 filter time for mode transitions

If a transition from (hard or soft) turn-off to PWM is triggered via SI1 and SI2 the following conditions apply:

1. PWM signal is blanked for $t_{CTdelay}$ and is valid with the next rising edge on PWM signal
2. The device is switching TON = high (VCC2) in t_{PDON} (AMCLPC.EAMCEN = 0) according to PWM signal

If a transition from PWM to ASCP is triggered via SI1 and SI2 the following conditions apply:

1. PWM signal is ignored after mode transition
2. If TON = high (VCC2): The device is switching TOFF = low (VEE2) after $t_{PDSIOFF}$
3. The device is switching TON = high (VCC2) after $t_{CTdelay} + t_{ASCdelay}$
4. RDY is switching to high, if device was in Error_Mode and NRST rising edge is triggered

If a transition from ASCP to (hard or soft) turn-off is triggered via SI1 and SI2 the following conditions apply:

1. PWM signal is ignored after mode transition
2. The device is switching TOFF = low (VEE2) in $t_{PDSIOFF}$, if a hard-off is configured
3. The device is switching TOFF = low (VEE2) in $t_{PDSIOFF\_SOFT}$, if a soft-off is configured

If a transition from (safe or hard) turn-off to ASCP is triggered via SI1 and SI2 the following conditions apply:

1. PWM signal is ignored after mode transition
2. The device is switching TON = high (VCC2) after $t_{CTdelay} + t_{ASCdelay}$
3. RDY is switching to high, if device was in Error_Mode and NRST rising edge is triggered

If a transition from ASCP to PWM is triggered via SI1 and SI2 the following conditions apply:

1. PWM signal is blanked for $t_{CTdelay}$ and is valid with the next rising edge on PWM signal
2. The device is switching according to PWM signal. From TOFF = low (VEE2) to TON = high (VCC2) in t_{PDON} (AMCLPC.EAMCEN = 0). If TON = high (VCC2), The device is switching TOFF = low (VEE2) after $t_{PDSIOFF}$.

If a transition from PWM to (soft or hard) turn-off is triggered via SI1 and SI2 the following conditions apply:

1. PWM signal is ignored after mode transition
2. The device is switching TOFF = low (VEE2) in $t_{PDSIOFF}$, if hard-off is configured
3. The device is switching TOFF = low (VEE2) in $t_{PDSIOFF\_SOFT}$ if soft-off is configured

The safety inputs of the HS and LS driver are cross connected, as follows. In that way, if a primary ASC is triggered, the opposite driver is turning off. Hence a shoot-through is avoided.

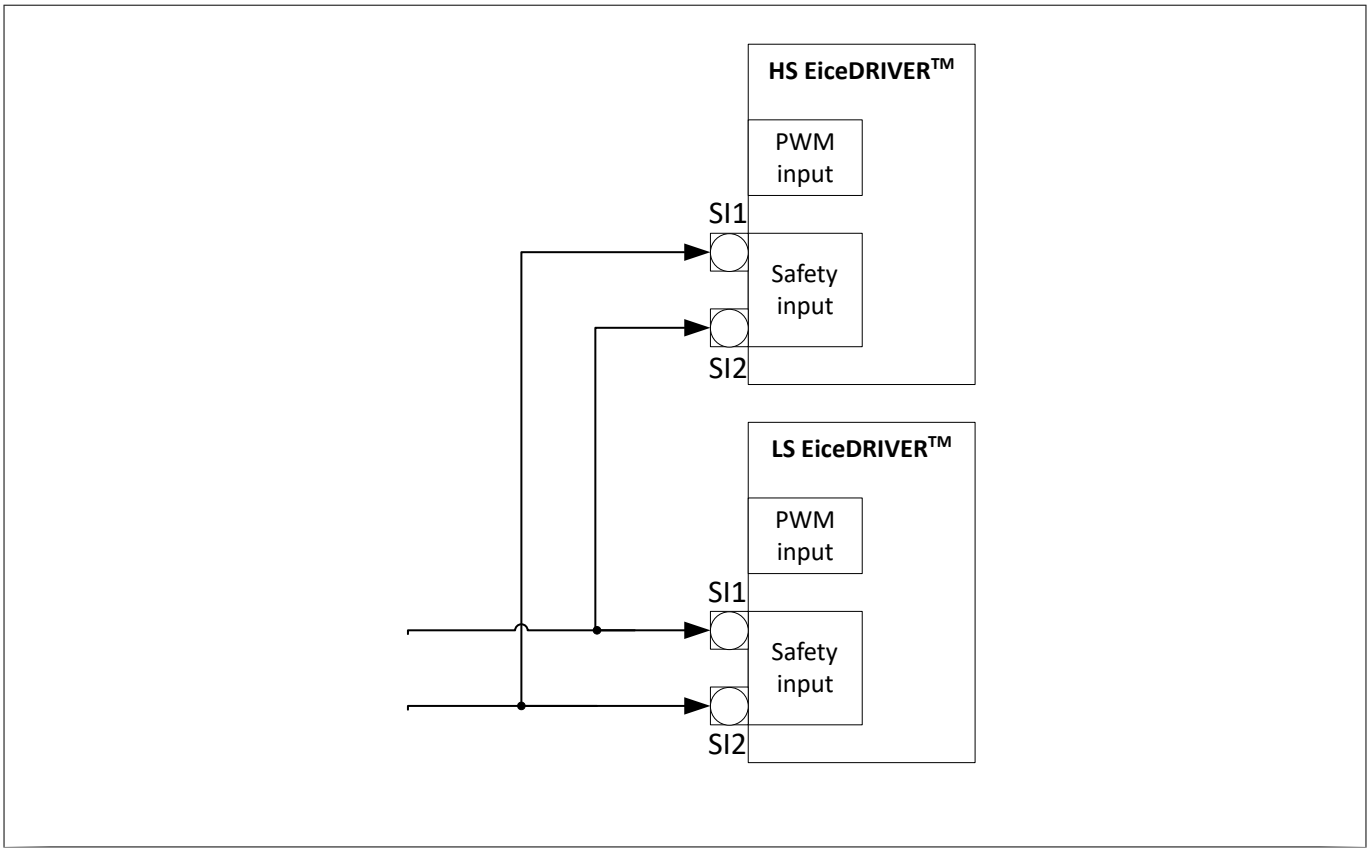

Figure 21 Cross connection of safety inputs in a half bridge configuration

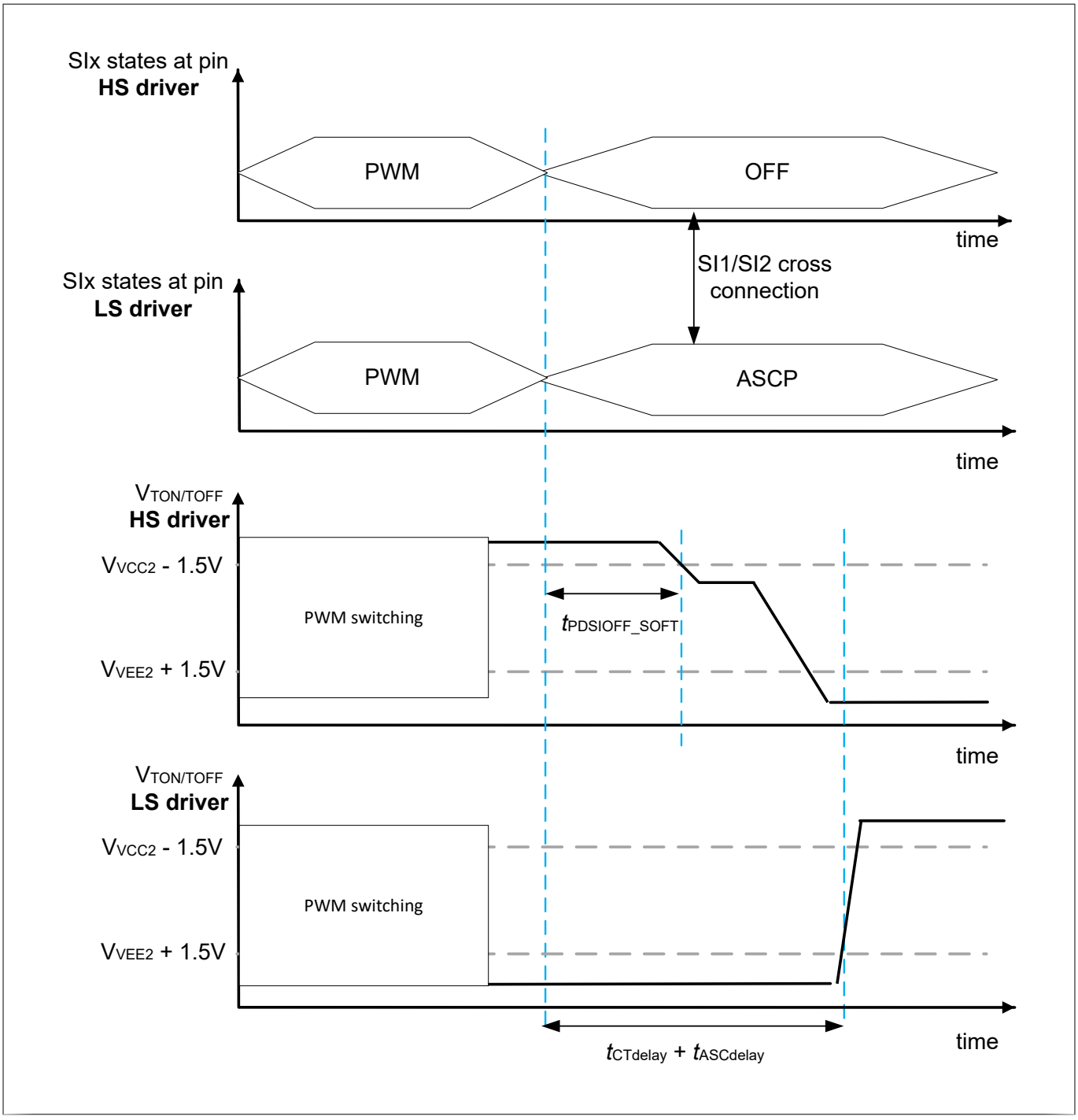

Figure 22 Timing diagram of an application scenario with SI1/SI2 cross connection.

A transition from any turn-off to ASCP can lead to a potential shoot-through across the half bridge, if the driver turns ON before the opposite driver is completely turned OFF. Thus $t_{ASCdelay}$ has to be programmed at least 100 ns longer than $t_{SOFTOFF}$ + $t_{TLTOffPLT}$ to prevent a shoot-through. This scenario is shown in the diagram below.

To avoid the triggering of an active short circuit with unknown configuration an ASCP signal needs to be triggered earliest 500 us after power-up to make sure the OTP read-out is finished in INIT_Mode.

The device sets bitfield STATUSS.GATEISVCC if both GATE/CLAMPx pins are "high" (VCC2).

Note:

- *The transfer of bitfield STATUSS.GATEISVCC can be disabled via bitfield GMOSMC.GATEISVCCDIS*
- The mirrored bit field STATUSSMIR.GATEISVCCMIR needs to be used for user read-out

The device implements an ASCS function which is driving "TON = high (VCC2)" to the IGBT/MOSFET in all modes, if requested via AIP/ASC pin.

Note:
- *The ASCS behavior for certain conditions/errors is stated in the Table Driver status at failure events/conditions during ASCS*
- *ASCS has a higher priority than a primary side triggered soft off (via SI1/SI2)*

Table 59 Driver status at failure events/conditions during ASCP

Condition/error	TON, if the device is in ASCP mode
Primary chip is not ready	TON = low (VEE2)
UVLO2/3, OVLO2/3 error event	TON = high (VCC2)[1)]
DESAT or OCP error event	Configured turn-off
Gate monitoring error event	Configured turn-off
Output stage monitoring error event	Tristate
Sec. internal supervision error event (OCPx pin open)	TON = high (VCC2)
Sec. internal supervision error event (PMU supervision error, parity)	TON = low (VEE2)

1) Only if SPSMER.ASCIGNOVLO2, SPSMER.ASCIGNUVLO2, SPSMER.ASCIGNOVLO3, SPSMER.ASCIGNUVLO3 = 1. Otherwise TON = low (VEE2)

Table 60 Driver status at failure events/conditions during ASCS

Condition/error	TON, if ASCS = high
Primary chip is not ready	TON = high (VCC2)
STP error event	TON = high (VCC2)
UVLO3, OVLO2/3 error event	TON = high (VCC2)[1)]
UVLO2 Error Event	TON = high (VCC2 ≥ $V_{ASCSOFF}$)[1)]
DESAT or OCP error event	Configured turn-off
Gate monitoring error event	Configured turn-off
Output stage monitoring error event	Tristate
Sec. internal supervision error event (OCPx pin open)	TON = high (VCC2)
Sec. internal supervision error event (PMU supervision error, parity)	TON = low (VEE2)

1) Only if SPSMER.ASCIGNOVLO2, SPSMER.ASCIGNUVLO2, SPSMER.ASCIGNOVLO3, SPSMER.ASCIGNUVLO3 = 1. Otherwise TON = low (VEE2)

If a DESAT or OCP error occurs while a valid ASC signal still applies, the device will set TON/TOFF = low (VEE2) according to the configured turn-off behavior and stay in this conditions until the following conditions are fulfilled:

- Error disappears
- $t_{latchend}$ is elapsed
- ASCP/S trigger is removed and re-applied

If a UVLO2/3 or OVLO2/3 error occurs and SPSMER.ASCIGNOVLO2, SPSMER.ASCIGNUVLO2, SPSMER.ASCIGNOVLO3, SPSMER.ASCIGNUVLO3 = 0 is set while a valid ASC signal applies, the device will set

TON/TOFF = low (VEE2) according to the configured turn-off behavior and stay in this conditions until the following conditions are fulfilled:

- Error disappears
- $t_{latchend}$ is elapsed
- ASCP/S trigger is removed and re-applied

Additionally, TON/TOFF stays ON, when additionally to theses bits OVLO3ERR, UVLO3ERR is set to IGNORED.

The ADC function on AIP1 needs to be disabled via SVARIANT.AIP1DIS, if ASCS pin is used.

14.2 Electrical characteristics external TON/TOFF control

Table 61 Electrical characteristics external TON/TOFF control

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Primary digital input low level	$V_{digital,input(low)}$	0	–	1.5	V	Referenced to GND1	PRQ-516
Primary digital input high level	$V_{digital,input(high)}$	3.5	–	V_{VCC1}	V	Referenced to GND1	PRQ-517
INP high/low duration	t_{INPPD}	250	–	–	ns	V_{VCC1}= 5 V,V_{VCC2}= 15 V,V_{VEE2}= -5 V, 50% to 50%	PRQ-191
SI1, SI2 & INP input leakage current high	$I_{INLEAKH1}$	–	115	135	µA	VCC1 at pin, V_{VCC1} = 5 V	PRQ-193
SI1, SI2 & INP input leakage current low	$I_{INLEAKL1}$	–	0.3	10	µA	0 V at pin, V_{VCC1} = 5 V	PRQ-194
Propagation delay SI1/SI2 to hard turn-off	$t_{PDSIOFF}$	0.65	1	1.2	µs	V_{VCC1} = typ., V_{VCC2} = typ., V_{VEE2} = typ., TON/TOFF = high (VCC2), SI1 = low, SI2 = high, Start: SI2 falling edge at $V_{digital,input(low)}$, Stop: TOFF = falling edge at V_{VCC2} - 1.5 V, no C_{LOAD}, no R_{LOAD} , external Miller clamping disabled, no Soft turn-off enabled, includes $t_{SIfilter}$	PRQ-94

(table continues...)

Table 61 (continued) Electrical characteristics external TON/TOFF control

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Propagation delay SI1/SI2 to soft turn-off	$t_{PDSIOFF\_SOFT}$	1.3	–	4.8	µs	V_{VCC1} = typ., V_{VCC2} = typ., V_{VEE2} = typ., TON/TOFF = high (VCC2), SI1 = low, SI2 = high, INP = high, INN = GND1, Start: SI2 falling edge at $V_{digital,input(low)}$, Stop: TOFF = falling edge at V_{VCC2} - 1.5 V referring to VEE2, no C_{LOAD}, R_{LOAD} = 1.69 Ω, external Miller clamping disabled, soft-off enabled	PRQ-531
ASCP delay for turn-on	$t_{ASCdelay}$	0	–	27	µs	SI1 = 0, start: SI2 = $V_{digital,input(low)}$, stop: TON/TOFF = VEE2 + 1.5 V, range is based on the programmed value.	PRQ-604
SI1/SI2 filter time	$t_{SIfilter}$	550	670	737	ns		PRQ-745
SI1/SI2 communication delay	$t_{CTdelay}$	4.0	4.5	5.0	µs		PRQ-685
Weak pull down resistance SI1, SI2 & INP	R_{PDIN1}	40	48	60	kΩ		PRQ-197
Reactivation time after error event during ASC	$t_{latchend}$			21	µs		PRQ-851

15 Reset

15.1 Functional description reset

The device has an reset active on rising-edge NRST pin.

All errors which are related to signal NFLT & RDY are only reset at a rising edge of NRST signal.

Note: If a failure signal is still alive the reset will not be processed.

15.2 Electrical characteristics reset

Table 62 Electrical characteristics reset

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum low pulse time at NRST	t_{NRST}	10	–	–	µs	
NRST input leakage current high	$I_{INLEAKH2}$	–	115	145	µA	VCC1 at pin, V_{VCC1} = 5 V
NRST input leakage current low	$\|I_{INLEAKL2}\|$	–	0.3	10	µA	0 V at pin, V_{VCC1} = 5 V
Weak pull down resistance NRST	R_{PDIN_NRST}	38	48	58	kΩ	
NRST input low level	$V_{NRST,input(low)}$	V_{GND1}	–	1.5	V	Referenced to GND1
NRST input high level	$V_{NRST,input(high)}$	3.5	–	V_{VCC1}	V	Referenced to GND1

16 ADC

16.1 Functional description ADC

The device has a Sigma-Delta ADC with 2 multiplexed channels which is converting its input voltage into digital value.

Note: The converted values can be read out via ADCPWM signal or SPI (ADC1R and ADC2R).

The ADCx result output on ADCPWM pin can be activated via bit field PVARIANT.ADCPWMENAB.

Note: This means that the shoot-through protection function is disabled.

The ADC PWM output signal can be inverted independently for each ADC channel via SPI in bit PINPC.ADCPWMINVx.

The NCS pin is used for selecting which result of the two multiplexed ADC channels on the secondary side is shown on the PWM signal of ADCPWM pin on the primary side. To switch between AIP1 PWM result and AIP2 PWM result the signal on NCS pin must be hold stable for the time $t_{ADCSEL(min)}$ after reaching threshold $V_{SPI,input(high)}$ until the rising edge of the AIP2 PWM signal. Accordingly it is switching in t_{ADCSEL}, if threshold $V_{SPI,input(low)}$ on NCS is hold until rising edge of AIP1 PWM. Inverting one or both of the ADC PWM signal will lead to the inverted behavior shown below.

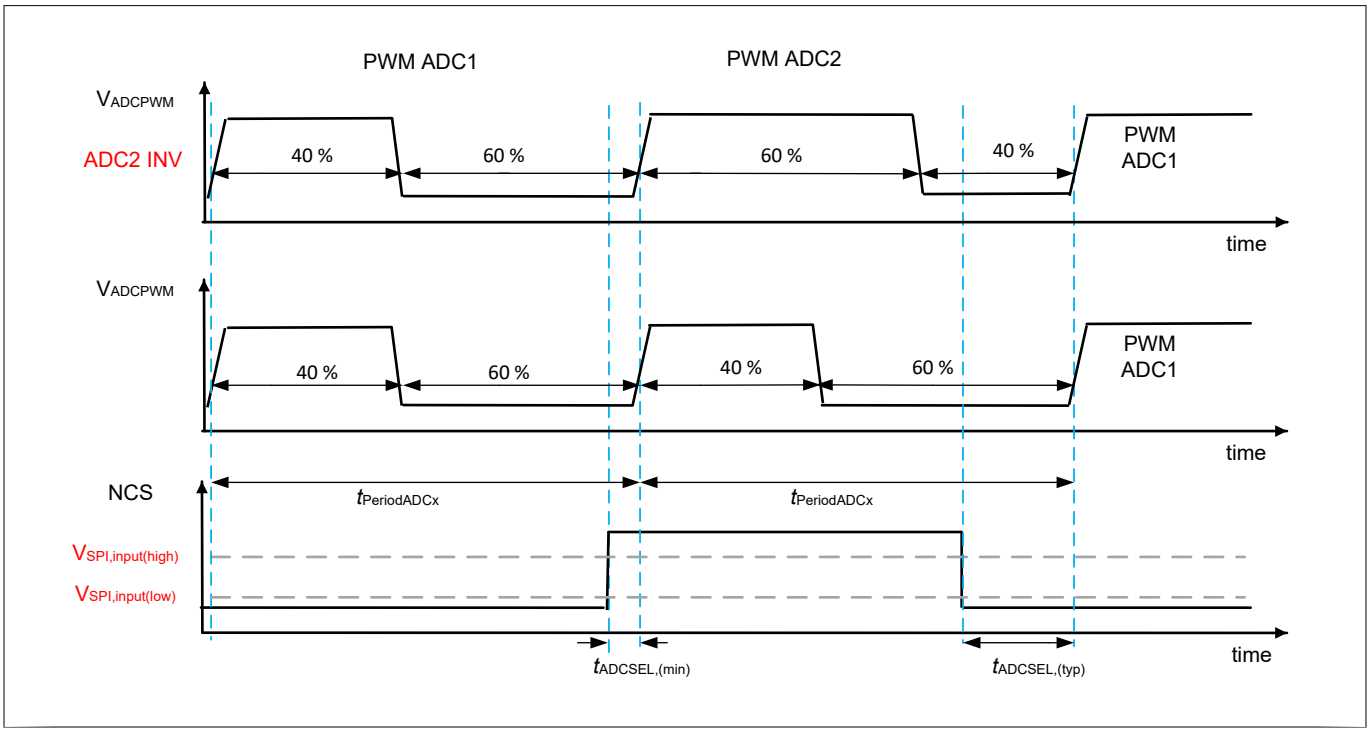

Figure 23 ADC selection timing diagram with ADC2 inverted and not inverted

Note:

- *ADC PWM duty pattern will always be finalized before switching to the other channel, therefore the timing can extend to the full ADC DATA period*
- *The NCS pin belongs to the SPI interface and is used additional also for the ADC toggling, therefore any toggle before $t_{ADCSEL,(min)}$ is ignored*
- *If NCS is used for toggling ADC it is recommended to not use SPI at the same time, as the ADC result will be interferred*

Additionally the SPI configuration in bit field PVARIANT.ADCPWMENAB can be used to change between ADC results (ADC1 or ADC2) to be shown on ADCPWM.

The ADC data rate $t_{PeriodADC}$ can be set in bit PINPC.ADCPWMPER, there are 4 different periods available and the default value is 1000 µs.

Note: The period for ADC1 and ADC2 are always identical. It is not possible to have different period timings for the ADCs.

The duty cycle can be calculated via the formula $D = V_{AIP\text{-}AIN} / 4.82 * 100$. Minimum and maximum values are limited as shown in corresponding diagram. If the configuration is changed to inverted values the upper and lower limits are changed accordingly.

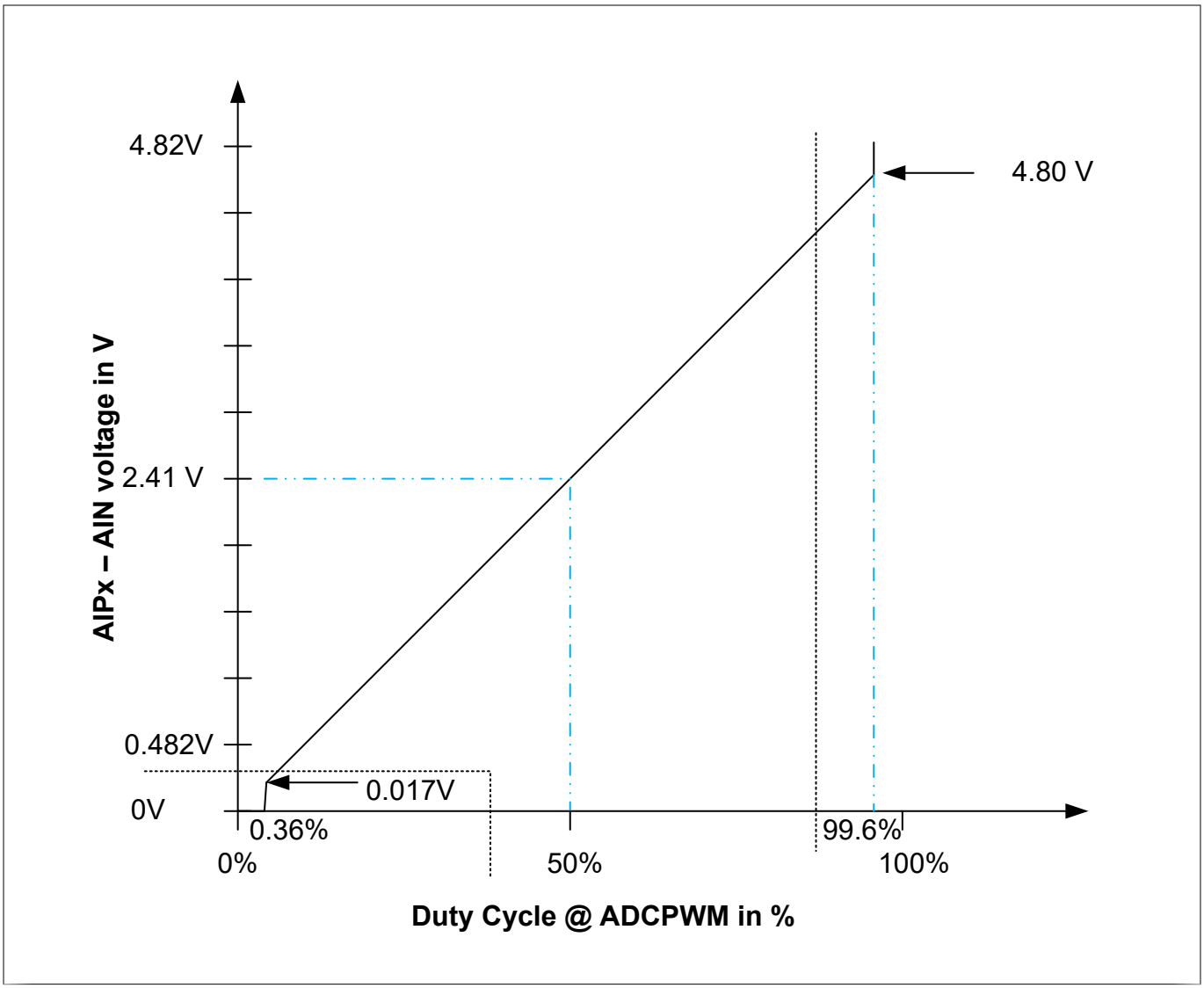

Figure 24 ADC input voltage to PWM duty cycle output diagram

The ADC sample rate can be configured via bit ADCSET.ADCSR.

Note:

- *By changing the frequency also the resolution will change accordingly*
- *The sample rate will be changed for both ADCx by the same bit*

The internal ADC current source of ADC1 and ADC2 can be configured via bit ADCSET.ADC1CS and ADCSET.ADC2CS. Setting these bit fields to 0 means disabling the current source.

The integrated ADC is designed for three typical application use cases:

- IGBT/SiC temperature measurement via diodes

- IGBT/SiC temperature measurement via NTC
- Main inverter DC-Link voltage measurement via resistor divider

The ADC offset error is calibrated on 2 V, which represents the hot temperature range of common temperature diodes in power modules. Hence measurement accuracy for temperature measurement applications is improved.

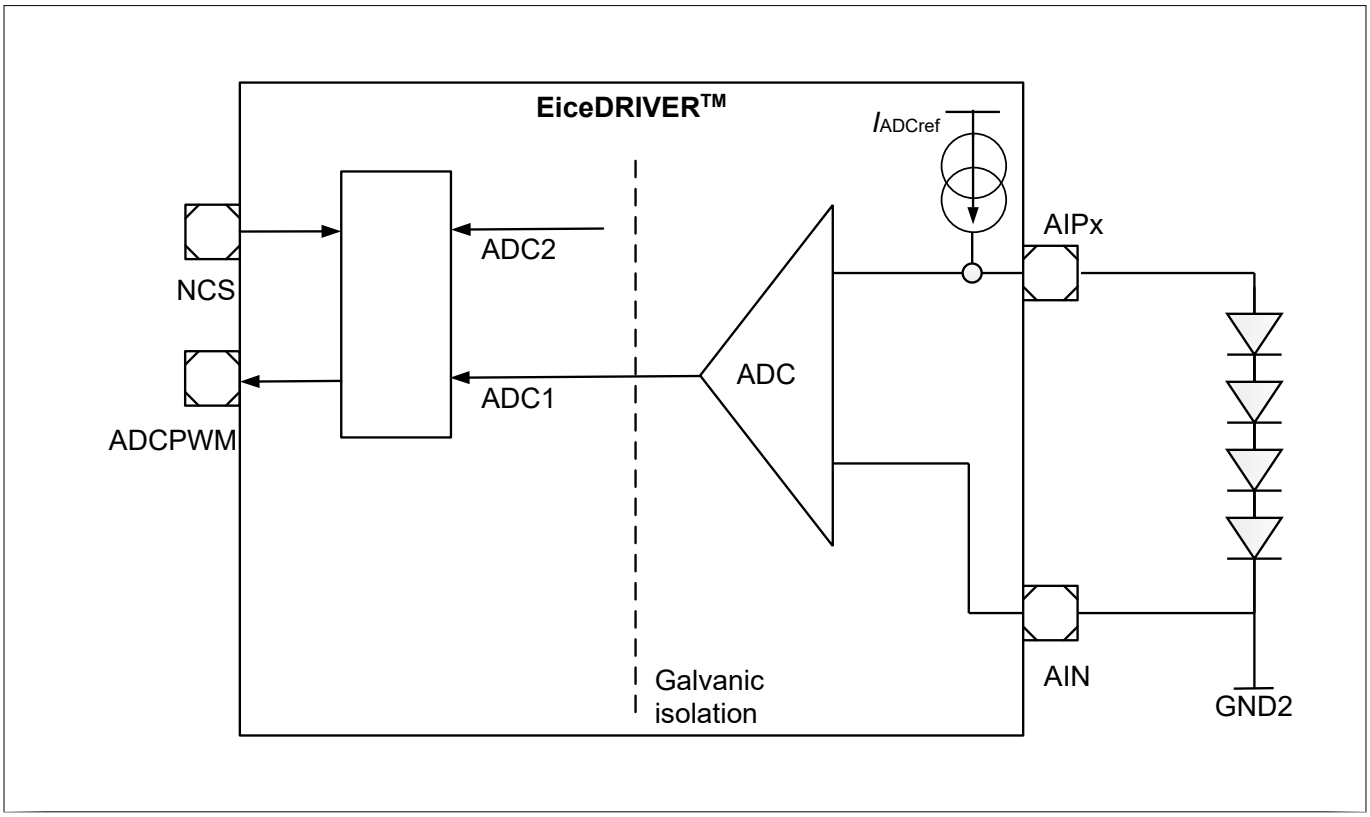

Figure 25 Temperature measurement diagram

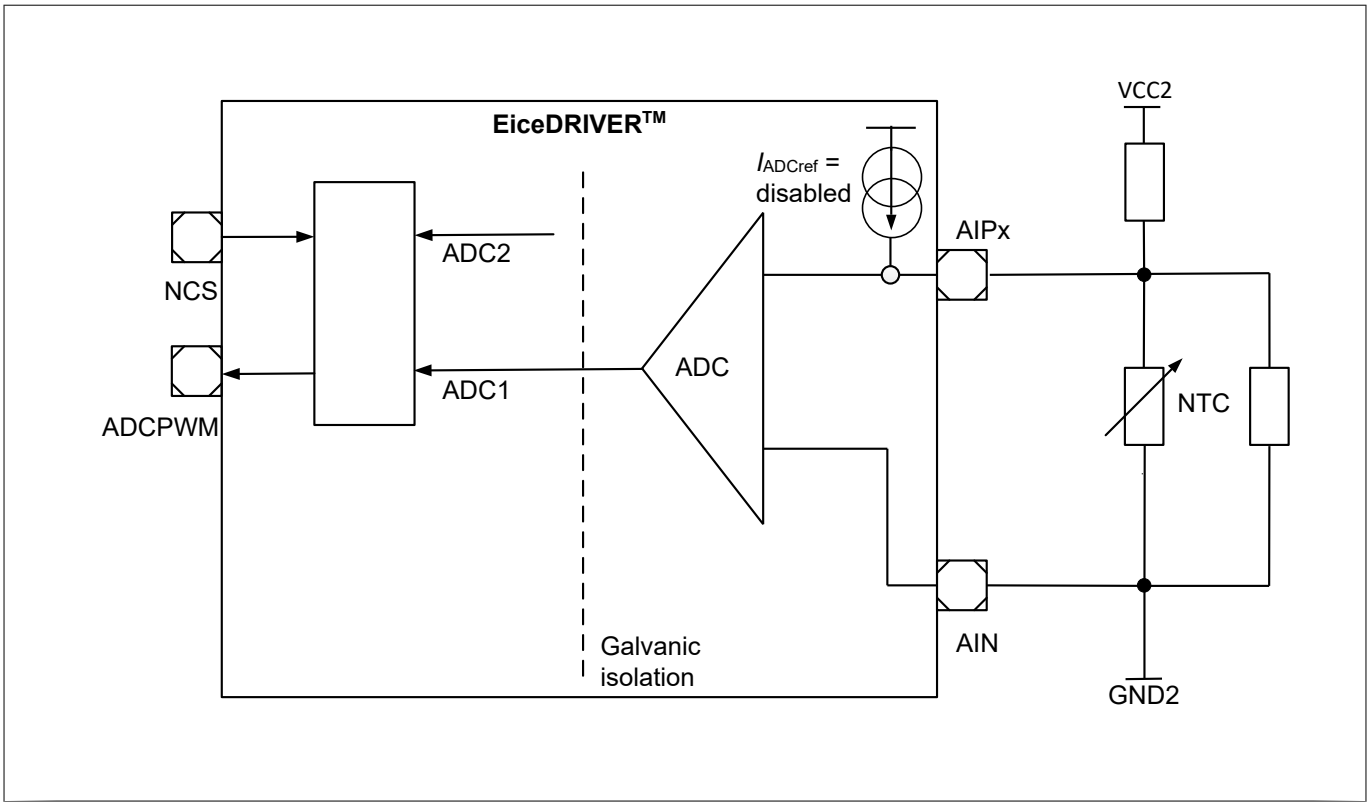

Figure 26 Temperature measurement diagram via NTC

Note:

- *ADC current source has to be disabled via SPI*

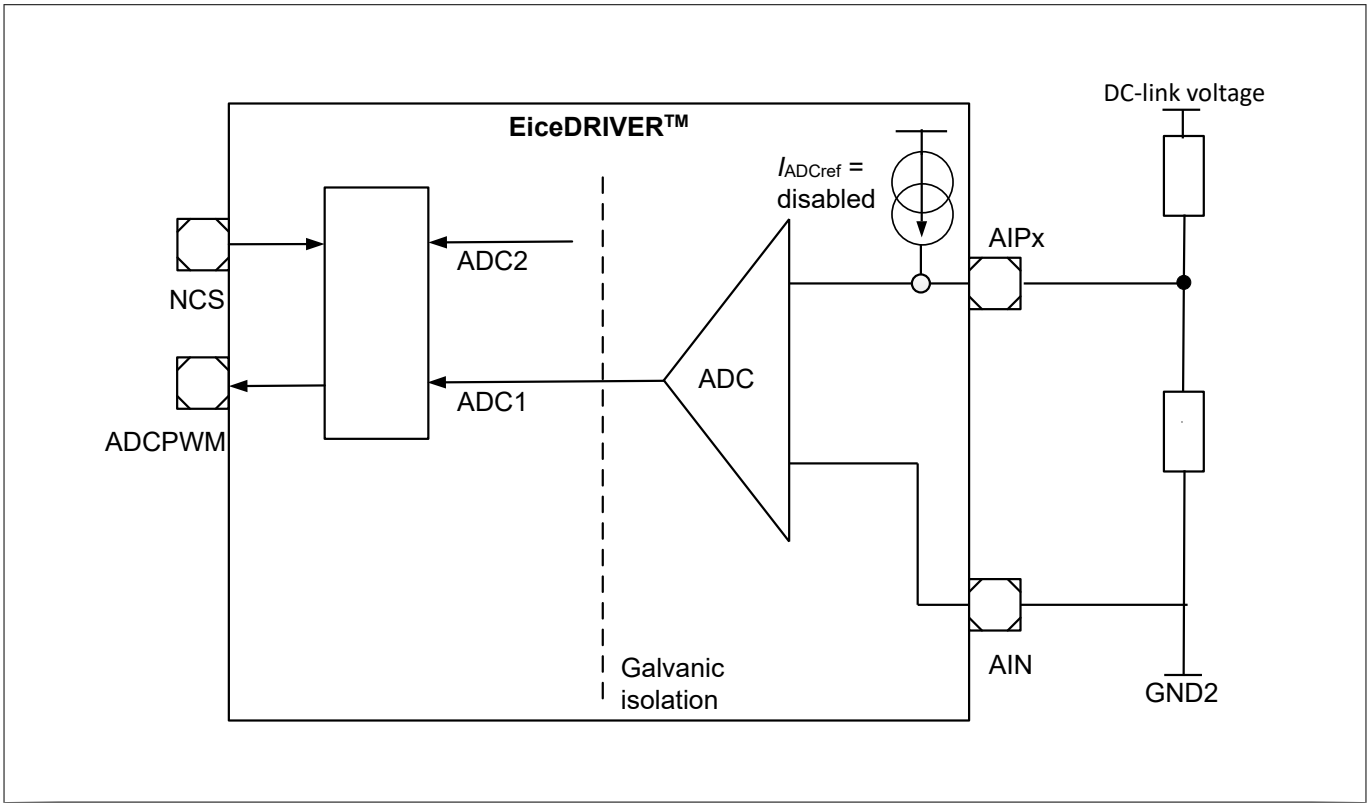

Figure 27 DC-link measurement diagram via resistor divider

16 ADC

Note: ADC current source has to be disabled via SPI

16.2 Electrical characteristics ADC

Table 63 Electrical characteristics ADC

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC resolution	ADC_{res}	-	12	-	bit		PRQ-215
Ideal ADC input voltage full scale	V_{AIP}	–	4.82	–	V		PRQ-216
ADC Gain Error	ER_{GAIN}	- 1.5	–	+ 1.5	%FS	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...4.4 V	PRQ-217
ADC Offset Error	ER_{OFF}	-0.25	–	+0.25	%FS	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...4.4 V, calibrated on 2 V	PRQ-218
ADC INL	INL	–	0.024	0.073	%FS	valid for 12 bits	PRQ-219
ADC DNL	DNL	–	0.007	0.025	%FS	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...4.4 V; valid for 12 bit	PRQ-220
ADC total error 0.4V ≤ VAIP-AIN ≤ 2.4V	TE	-20	0	20	mV	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...2.4 V	PRQ-494
ADC total error 2.4V ≤ VAIP-AIN ≤ 2.7V	TE	-50	0	50	mV	Valid for Input range V_{AIPx} - V_{AIN} = 2.4 V...2.7 V	PRQ-495
ADC total error 2.7V ≤ VAIP-AIN ≤ 4.8V	TE	-70	0	70	mV	Valid for Input range V_{AIPx} - V_{AIN} = 2.7 V...4.8 V	PRQ-496
ADC reference current 0	$I_{ADCref0}$	-3	–	3	µA	ADC current source turned-off	PRQ-612
ADC reference current 1 @hot	$I_{ADCref1}$	-205	-200	-195	µA	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...4.4 V, +25 °C ≤ T_{amb} ≤ +125 °C	PRQ-222
ADC reference current 1 @cold	$I_{ADCref1,cold}$	-206	-195	-186	µA	Valid for Input range V_{AIPx} - V_{GND2} = 0.4 V...4.4 V, -40 °C ≤ T_{amb} < +25 °C	PRQ-686
ADC reference current 2	$I_{ADCref2}$	-416	-400	-378	µA	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...4.4 V	PRQ-614
ADC reference current 3	$I_{ADCref3}$	-828	-800	-758	µA	Valid for Input range V_{AIPx} - V_{AIN} = 0.4 V...4.4 V	PRQ-613

(table continues...)

Table 63 (continued) Electrical characteristics ADC

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC sample rate	$f_{SAMPLE3}$	1.14	1.2	1.26	kHz	12 bit	PRQ-680
ADCSEL timing	t_{ADCSEL}	1.1	4	–	µs	during min. value NCS pin needs to be stable until rising edge of next ADCPWM, ADC period will be finished before switching to other channel	PRQ-467
ADCPWM duty cycle range	D_{ADC}	0.36	–	99.6	%		PRQ-460
ADCPWM period 0	t_{Period_ADC0}	97.2	102.4	107.5	µs		PRQ-461
ADCPWM period 1	t_{Period_ADC1}	194.5	204.8	215	µs		PRQ-463
ADCPWM period 2	t_{Period_ADC2}	389.1	409.6	430	µs		PRQ-464
ADCPWM period 3	t_{Period_ADC3}	778.2	819.2	860.2	µs		PRQ-465
Data Update time 0	$t_{ADC\_Update0}$	750	-	1900	µs	at t_{Period_ADC0}	PRQ-885
Data Update time 1	$t_{ADC\_Update1}$	750	-	2000	µs	at t_{Period_ADC1}	PRQ-887
Data Update time 2	$t_{ADC\_Update2}$	750	-	2200	µs	at t_{Period_ADC2}	PRQ-886
Data Update time 3	$t_{ADC\_Update3}$	750	-	2600	µs	at t_{Period_ADC3}	PRQ-888
ADCPWM output low level	$V_{ADCPWM, (low)}$	–	0	0.5	V	V_{VCC1} = typ., $\|I_{load}\|$ = 5 mA	PRQ-633
ADCPWM output high level	$V_{ADCPWM, (high)}$	V_{VCC1}-0.5	V_{VCC1}	–	V	Referenced to VCC1, $V_{VCC1} \geq 3.0$ V, $\|I_{load}\|$ = 5 mA	PRQ-634

17 Flyback controller

17.1 Functional description flyback controller

The device has a flyback controller integrated to enable the supply of the secondary side output chip.

The flyback controller regulation loop is based on hysteretic control principle based on VCC2 voltage on secondary side. The regulation and feedback loop is done internally in the device via the coreless transformer. Two thresholds ($V_{FBth,high}$ and $V_{FBth,low}$) define the operating mode that the flyback is entering.

The flyback controller has three operating modes:

1. Skip_Mode
2. Low_Power_Mode
3. Full_Power_Mode with adaptive response

The system parameters (C_{VCC2}, L_{prim}, V_{BAT} voltage range, I_{pk}) need to be adapted to operate the flyback controller in Low_Power_Mode for a stable operation to achieve highest accuracy on VCC2. The Skip_Mode and Full_Power_Mode are used to maintain specified accuracy parameters in unstable operation (C_{VCC2} deviation, V_{BAT} range exceeded…).

Principle of operation

The flyback controller generates VCC2 in two conditions:

1. VCC2 in DC operation
2. VCC2 during TON/TOFF switching

VCC2 in DC operation During DC operation the flyback modes Skip_Mode and Low_Power_Mode would be used. If VCC2 exceeds $V_{FBth,high}$ the Skip_Mode is entered and PWM at TOUTP is stopped. Once VCC2 voltage drops below $V_{FBth,high}$ the Low_Power_Mode is entered and the primary side is re-establishing the VCC2 voltage after $t_{FBdelay,DC}$ with the 1st PWM-cycle at TOUTP.

VCC2 during TON/TOFF switching If the application parameters are tuned according to the 1EDI305xAS application note the flyback controller will operate in Low_Power_Mode all the time. Low_Power_Mode operation means that the flyback controller never reaches the integrated flyback thresholds $V_{FBth,high/low}$. If stable operation is left or switching events on TON/TOFF lead to high VCC2 voltage drops a Full_Power_Mode with adaptive response is integrated to re-stablish the VCC2 voltage in a fast manner. This mode is entered if $V_{FBth,low}$ is undershot. Adaptive response means that several full power pulses (configurable via SPI) are followed by low power pulses. This approach allows fast response on VCC2 and a smooth reaching of the target level to avoid VCC2 over-shoots.

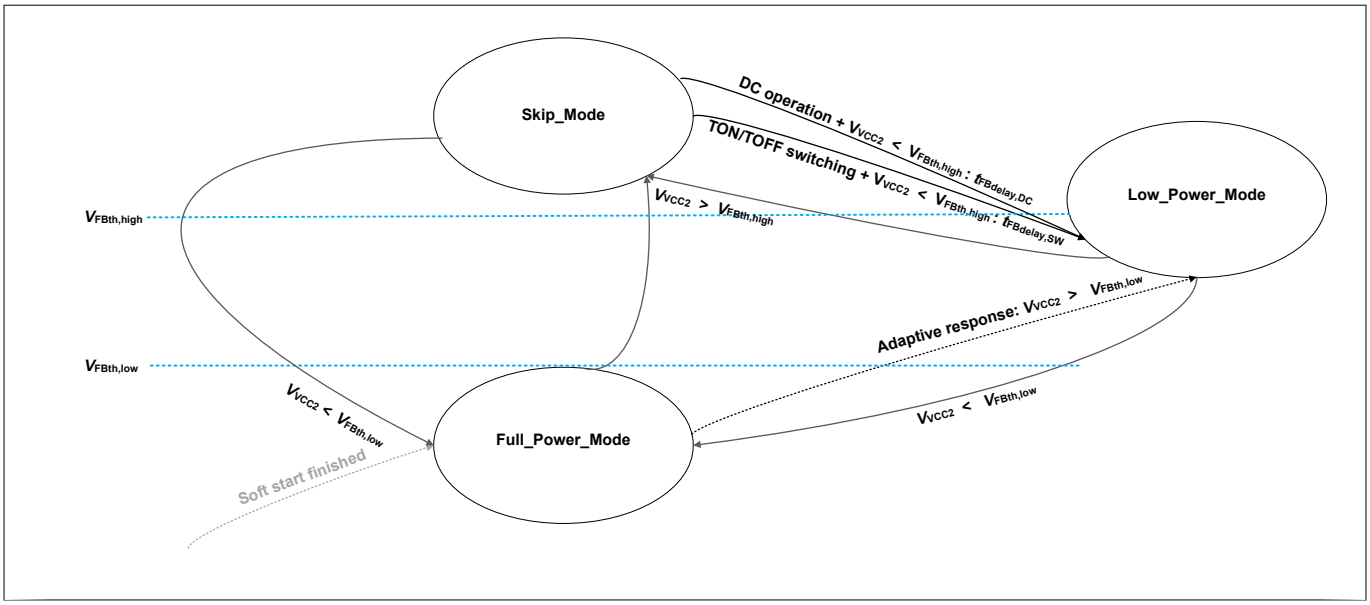

Figure 28 Flyback operating mode

The number of full power pulses before transition to low power pulses during adaptive response can be configured in bit field FLYBACKC4.FLYADACYC.

In DC operation, if $V_{FBth,high}$ is undershot, the flyback controller goes from Skip_Mode to Low_Power_Mode after a delay time of $t_{FBdelay,DC}$.

In TON/TOFF switching operation, if $V_{FBth,high}$ is undershot, the flyback controller goes from Skip_Mode to Low_Power_Mode after a delay time of $t_{FBdelay,SW}$.

The flyback controller can be disabled via bit FLYBACKC1.FLYBENA.External connection when disabled can be as following: TOUTp open, ISENSEx open, VBATS connected to VCC1 or GND1 via at least $R_{VDBAT2,min.}$.

The flyback controller has a differential overcurrent detection input.

If the overcurrent level of $V_{ISENSETH,(max)}$ on ISENSEx pin is triggered, the output TOUTP is switched to GND1 and the bit DIAGFLY.FLYBOCER is set within $t_{ISENSE2OFF}$. The device tries to reestablish the secondary supply for the number of retry cycles defined in FLYBACKC3.FLYRCYC. When the number of retry cycles elapsed, TOUTP switching activity will stop and DIAGFLY.FLYBFSM will be set to FAULT. Finally RDY is set to low when the secondary supply voltages cross UVLO2/OVLO3.. In this condition TOUT (secondary chip output pin) will be pulled low as long as VCC2 voltage allows, then enter a passive pull down mode.

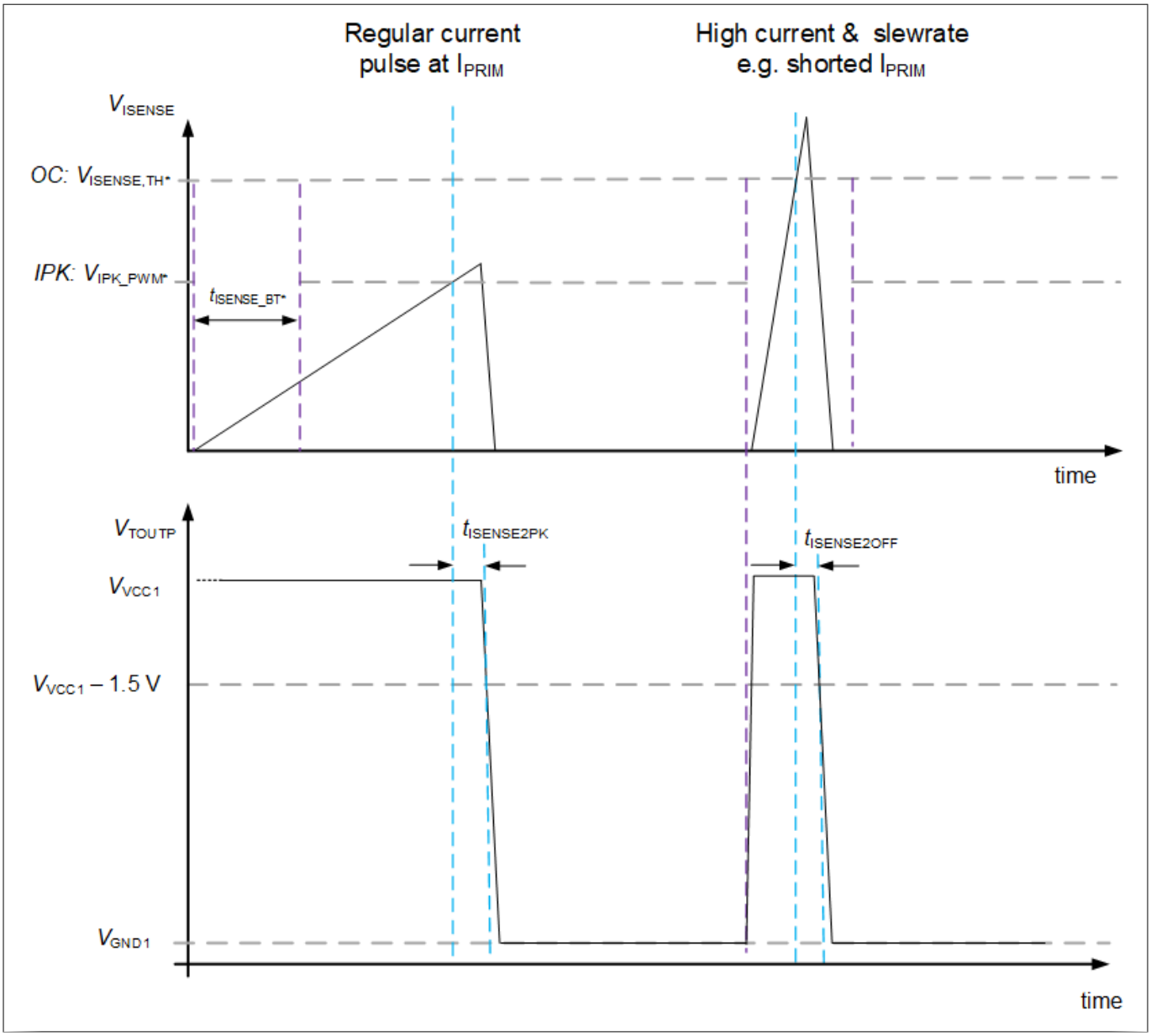

Figure 29 Flyback controller overcurrent timing diagram

Note: In this case the ASCP_Mode cannot be entered.

The output voltage VCC2 can be configured via bit SPSML.VCC2VL.

Note:

The OVLOx and UVLOx settings may need to be adjusted accordingly.

The negative VEE2 voltage must be realized through the turn ratios of the transformer and a middle point connection for GND2.

The flyback controller has an output to drive an external N-channel MosFET.

Note: A gate resistance is expected to limit the TOUTP max output current and damp possible gate loop ringing. Values defined in the EC section.

The flyback controller implements an OVLO detection by sensing the voltage on the VBATS pin. An OVLO event is detected when FLYBACKC3.FLYBOVEN is set and when the voltage on VBATS rises above $V_{OVLOFBH}$. In case of an OVLO event the output TOUTP is switched to GND1 within $t_{OVLO2OFF}$. The flyback controller then tries

to reestablish the secondary supply for the number of retry cycles defined in FLYBACKC3.FLYRCYC. When the number of retry cycles elapsed, TOUTP switching activity will stop and DIAGFLY.FLYBFSM will be set to FAULT. Finally RDY is set to low when the secondary supply voltages crosses UVLO2/OVLO3.

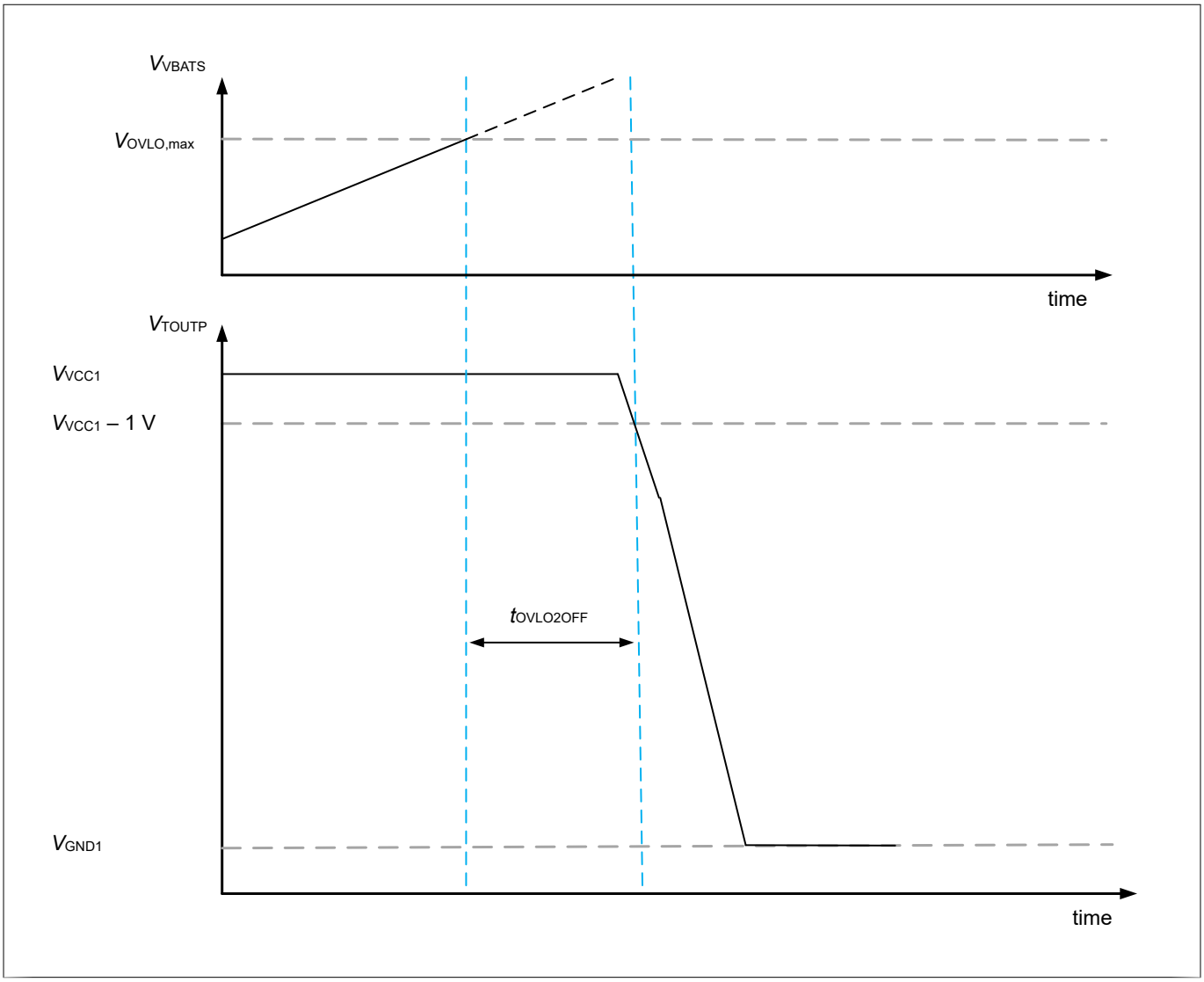

Figure 30 Flyback controller OVLO function

Flyback related errors are shown in the status register PUSER.DIAGFLY.

17.2 Electrical characteristics flyback controller

Table 64 Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output Voltage Set Level 0	V_{OVSL0}	–	15	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-240
Output Voltage Set Level 1	V_{OVSL1}	–	15.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-279
Output Voltage Set Level 2	V_{OVSL2}	–	16	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-280
Output Voltage Set Level 3	V_{OVSL3}	–	16.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-281
Output Voltage Set Level 4	V_{OVSL4}	–	17	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-282
Output Voltage Set Level 5	V_{OVSL5}	–	17.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-283
Output Voltage Set Level 6	V_{OVSL6}	–	18	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-284

(table continues...)

Table 64 (continued) Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output Voltage Set Level 7	V_{OVSL7}	–	18.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-285
Output Voltage Set Level 8	V_{OVSL8}	–	19	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-286
Output Voltage Set Level 9	V_{OVSL9}	–	19.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-287
Output Voltage Set Level 10	V_{OVSL10}	–	20	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-288
Output Voltage Set Level 11	V_{OVSL11}	–	20.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-289
Output Voltage Set Level 12	V_{OVSL12}	–	21	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-290
Output Voltage Set Level 13	V_{OVSL13}	–	21.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-291
Output Voltage Set Level 14	V_{OVSL14}	–	14	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-292

(table continues...)

Table 64 (continued) Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output Voltage Set Level 15	V_{OVSL15}	–	14.5	–	V	@ VCC2; referenced to GND2; DC characteristic, no ripple or transient included	PRQ-293
DC output voltage accuracy on VCC2	V_{FBVCC2}	-2	–	2	%	No transient or ripple included, stable input voltage, load current (DC) = I_{QVCC2} + I_{QVEE2} + 43 mA, Ready Mode	PRQ-881
Flyback threshold, high	$V_{FBth,high}$	98.7	101	102.7	%	Related to V_{OVSLx}	PRQ-837
Flyback threshold, low	$V_{FBth,low}$	97	99	101	%	Related to V_{OVSLx}	PRQ-838
Flyback threshold hysteresis	$V_{FBth,hyst}$	1		2.6	%	Deviation of $V_{FBth,high}$ vs $V_{FBth,low}$	PRQ-839
Flyback feedback delay time (DC operation)	$t_{FBdelay,DC}$	10	14	18.5	µs	f_{SW-OUT} = 250 kHz, From $V_{VCC2} > V_{FBth,high(max)}$ to $V_{FBth,low} < V_{VCC2} < V_{FBth,high}$ until $V_{TOUTP} \geq$ 1.5 V	PRQ-845
Flyback feedback delay time (TON/TOFF switching)	$t_{FBdelay,SW}$	2.9	6	11.1	µs	f_{SW-OUT} = 250 kHz, TON/TOFF switching, From $V_{VCC2} > V_{FBth,high(max)}$ to $V_{FBth,low} < V_{VCC2} < V_{FBth,high}$ until $V_{TOUTP} \geq$ 1.5 V	PRQ-846
VBATS input leakage current	$\lvert I_{LEAK-VBATS} \rvert$	–	0.3	2	µA	V_{VCC1} = 5 V, V_{VBATS} = 1.2 V	PRQ-277
Flyback controller switching frequency range	f_{SW-OUT}	100	200	550	kHz	At TOUTP pin, frequency selected via SPI	PRQ-243
Overcurrent threshold 0 on ISENSEx	$V_{ISENSETH0}$	380	430	480	mV	@ISENSEP, referenced to ISENSEN	PRQ-589
Overcurrent threshold 1 on ISENSEx	$V_{ISENSETH1}$	475	535	595	mV	@ISENSEP, referenced to ISENSEN	PRQ-590

(table continues...)

Table 64 (continued) Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent threshold 2 on ISENSEx	$V_{ISENSETH2}$	575	645	715	mV	@ISENSEP, referenced to ISENSEN	PRQ-591
Overcurrent threshold 3 on ISENSEx	$V_{ISENSETH3}$	760	850	940	mV	@ISENSEP, referenced to ISENSEN	PRQ-471
FBPWM peak current 0 on ISENSEx	I_{PWMpk0}	290	325	345	mV		PRQ-585
FBPWM peak current 1 on ISENSEx	I_{PWMpk1}	345	370	400	mV		PRQ-586
FBPWM peak current 2 on ISENSEx	I_{PWMpk2}	395	420	450	mV		PRQ-587
FBPWM peak current 3 on ISENSEx	I_{PWMpk3}	495	525	560	mV		PRQ-588
FBPWM blanking time 0 on ISENSEx	$t_{IsenseBT0}$		100		ns		PRQ-578
FBPWM blanking time 1 on ISENSEx	$t_{IsenseBT1}$		200		ns		PRQ-579
FBPWM blanking time 2 on ISENSEx	$t_{IsenseBT2}$		300		ns		PRQ-584
FBPWM blanking time 3 on ISENSEx	$t_{IsenseBT3}$		400		ns		PRQ-580
ISENSEx detection & reaction time	$t_{ISENSE2OFF}$	–	250	300	ns	After blanking time is elapsed, no C_{LOAD} and no resistive load on TON/TOFF, slewrate=10 V/µs, Overdrive=+/-100 mV	PRQ-263
Flyback soft start time-out 0	$t_{SoftStart0}$	3.72	4	4.28	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-657

(table continues...)

Table 64 (continued) Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Flyback soft start time-out 1	$t_{SoftStart1}$	7.44	8	8.56	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-658
Flyback soft start time-out 2	$t_{SoftStart2}$	11.16	12	12.84	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-659
Flyback soft start time-out 3	$t_{SoftStart3}$	14.88	16	17.12	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-660
Flyback soft start time-out 4	$t_{SoftStart4}$	18.6	20	21.4	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-833

(table continues...)

Table 64 (continued) Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Flyback soft start time-out 5	$t_{SoftStart5}$	22.32	24	25.68	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-834
Flyback soft start time-out 6	$t_{SoftStart6}$	26.04	28	29.96	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-835
Flyback soft start time-out 7	$t_{SoftStart7}$	29.76	32	34.24	ms	Applied in the following intervals: End of self check until life sign established when VCC2 >= 6V for more than 400µs, Life sign established until VCC2 >= 9V, VCC2 >= 9V until VCC2 >= VUVLO2Hx	PRQ-836
Soft start overshoot on VCC2	$V_{VCC2STARTO}$	–	–	1	V	Overshoot during ramp-up on VCC2	PRQ-425
Dead time between restart trials	$t_{DEADfly}$	1.52	–	6.72	ms	Start: Trigger of error event (e.g. VBAT OVLO) Stop: V_{TOUTP} = V_{VCC1} - 1.5 V. Min. & Max. values are the programming range.	PRQ-841
Vbats OVLOFB threshold high	$V_{OVLOFBH}$	1.1	1.2	1.32	V	@ VBATS pin, referenced to GND1	PRQ-447
Vbats OVLOFB threshold low	$V_{OVLOFBL}$	1.03	1.15	1.25	V	@ VBATS pin, referenced to GND1	PRQ-448

(table continues...)

Table 64 (continued) Electrical characteristics flyback controller

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Flyback OVLO detection&reaction time	$t_{OVLO2OFF}$	–	–	3	µs		PRQ-891
TOUTPLN-RDSON	$R_{DSON-TOUTPLN}$	0.75	–	3.5	Ω	I_{TOUTP} = 20mA, pulsed	PRQ-551
TOUTPHP-RDSON	$R_{DSON-TOUTPHP}$	2.5	–	9.5	Ω	I_{TOUTP} = 20mA, pulsed	PRQ-552

18 Turn-off modes

18.1 Functional description turn-off modes

The device issues two different turn-off modes:

1. Safe turn-off as turn-off reaction to error events. Can be configured as:
   - Hard turn-off
   - Tri-State (for OSM only)
   - Soft turn-off:
     - Two-level turn-off
     - Fast soft turn-off ramp down
     - Regular soft-off ramp down
2. Regular turn-off as PWM switching turn-off

In case of tristate the tristate impedance $I_{TRISTATE}$ and the following conditions apply for the device: TON = open, TOFF = open (weak pull down), GATE1/2 = open, AMCLP 1/2 = OFF (VEE2).

The device has a two-level turn-off mode. The plateau voltage V_{PLTx} and the plateau length $t_{TLTOffPLT}$ can be configured via bits STOFFC.STOFFPVL and STOFFC.STOFFPT.

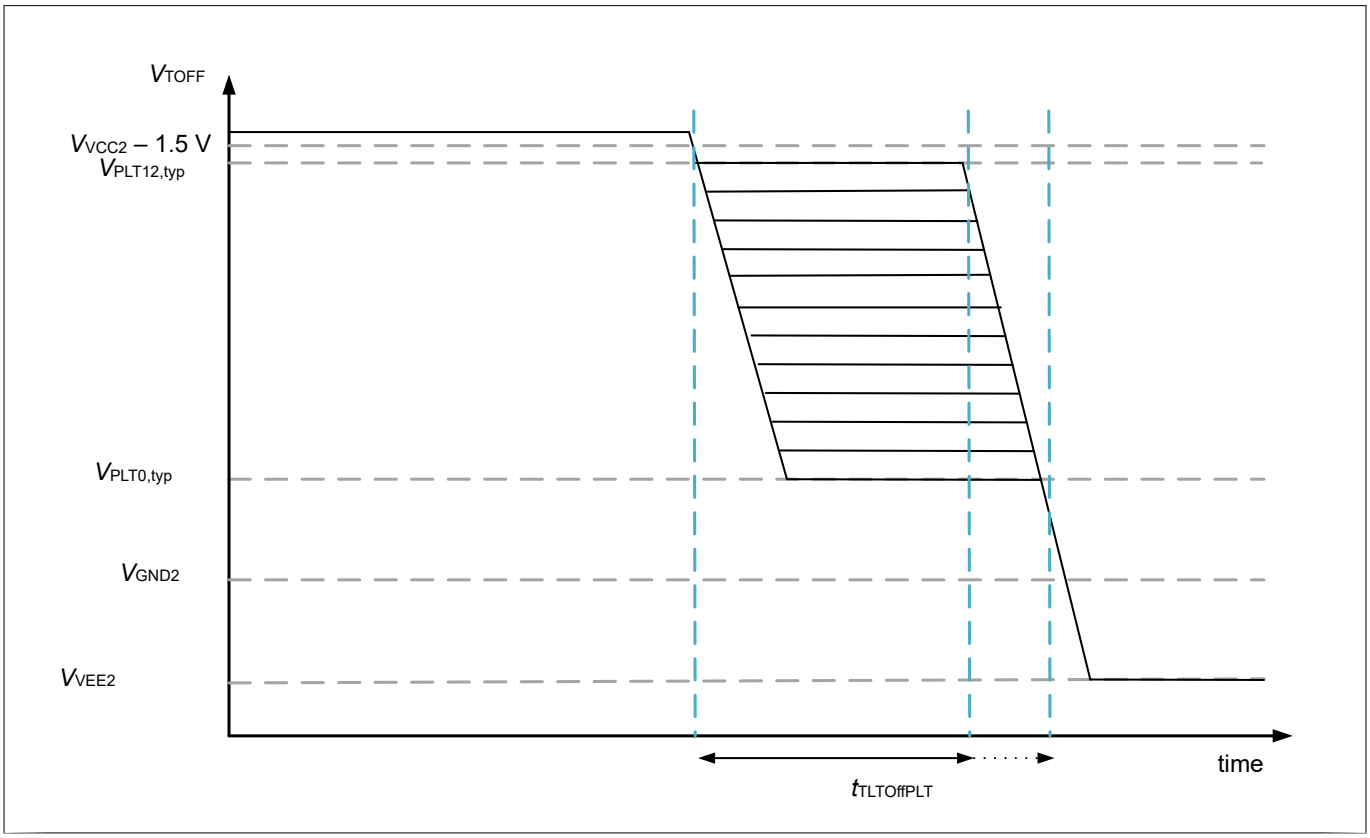

Figure 31 Two level turn-off timing diagram

Note: The ramp down function has to be disabled via bit STOFFC.STOFFRC to achieve a two-level turn-off behavior

A fast soft-off can be configured by choosing the lowest two-level turn-off plateau voltage V_{PLT0} and setting the plateau length according to following calculation $t_{TLTOffPLT} \geq (VCC2 - 4\ V) * 1/SR_{FSOFF}$. The device slew rate SR_{FSOFF} is fixed and defines the duration of t_{FSOFF} in dependency of VCC2.

Note: A positive margin of a few 100 ns on $t_{TLTOffPLT}$ should be considered to reach the target value (non-linearity of the slew rate).

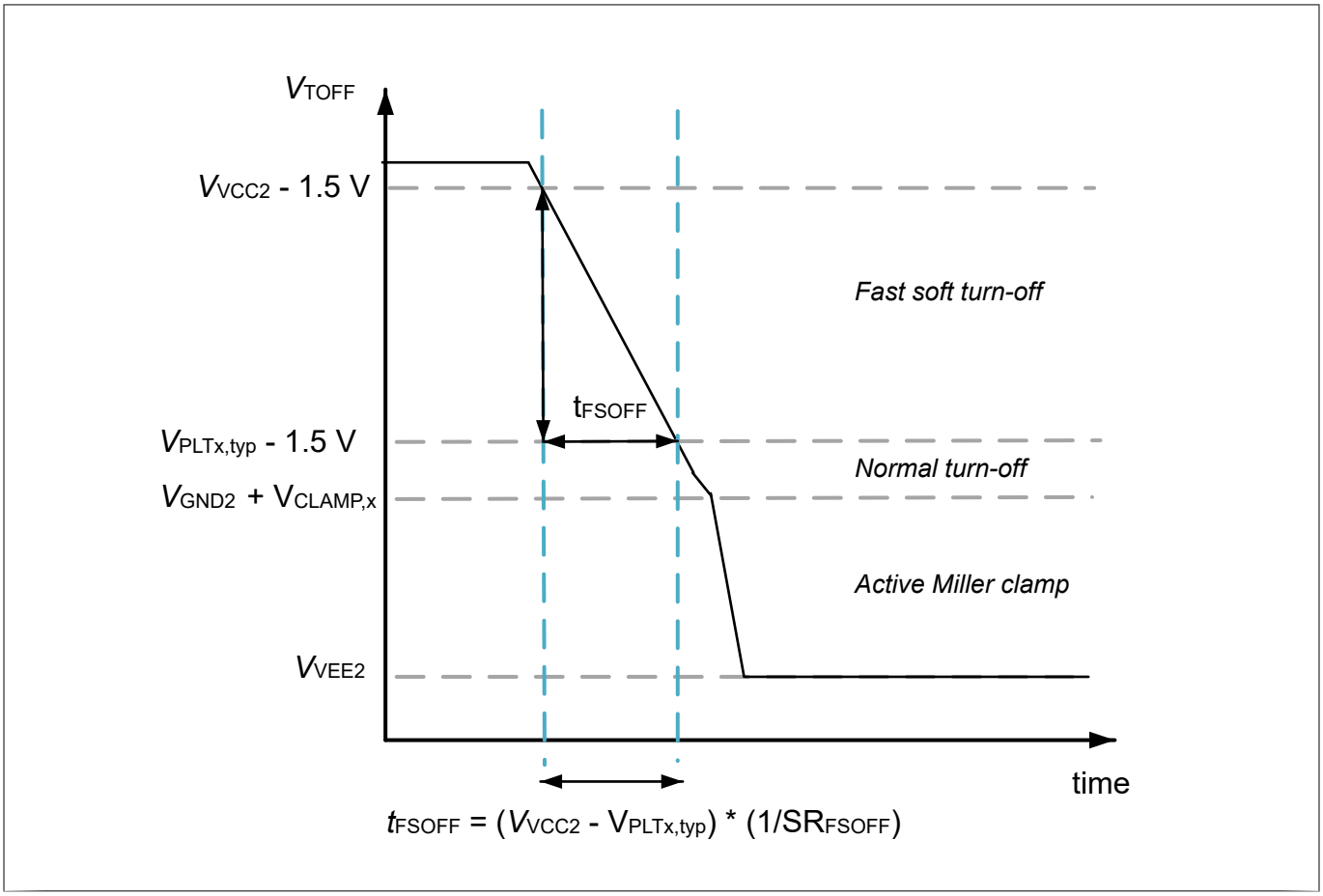

Figure 32 Fast soft turn-off timing diagram

The duration length for the regular soft turn-off ramp down starts after a chosen two-level turn-off plateau V_{PLTx} and is configurable in bit STOFFC.STOFFRC.

The regular soft turn-off extends the turn-off timing by a ramp-down from a start plateau $V_{PLTx,initial}$. The initial plateau voltage and length is configured according to a two-level turn-off. The length of the following regular soft-off ramp is defined by the chosen initial plateau voltage and the configured step length $t_{PLTRAMP}$, calculated according to below formula. If the initial plateau is not wanted, the timing of the $t_{TLTOffPLT}$ has to be configured to a similar or smaller value than $t_{PLTRAMP}$.

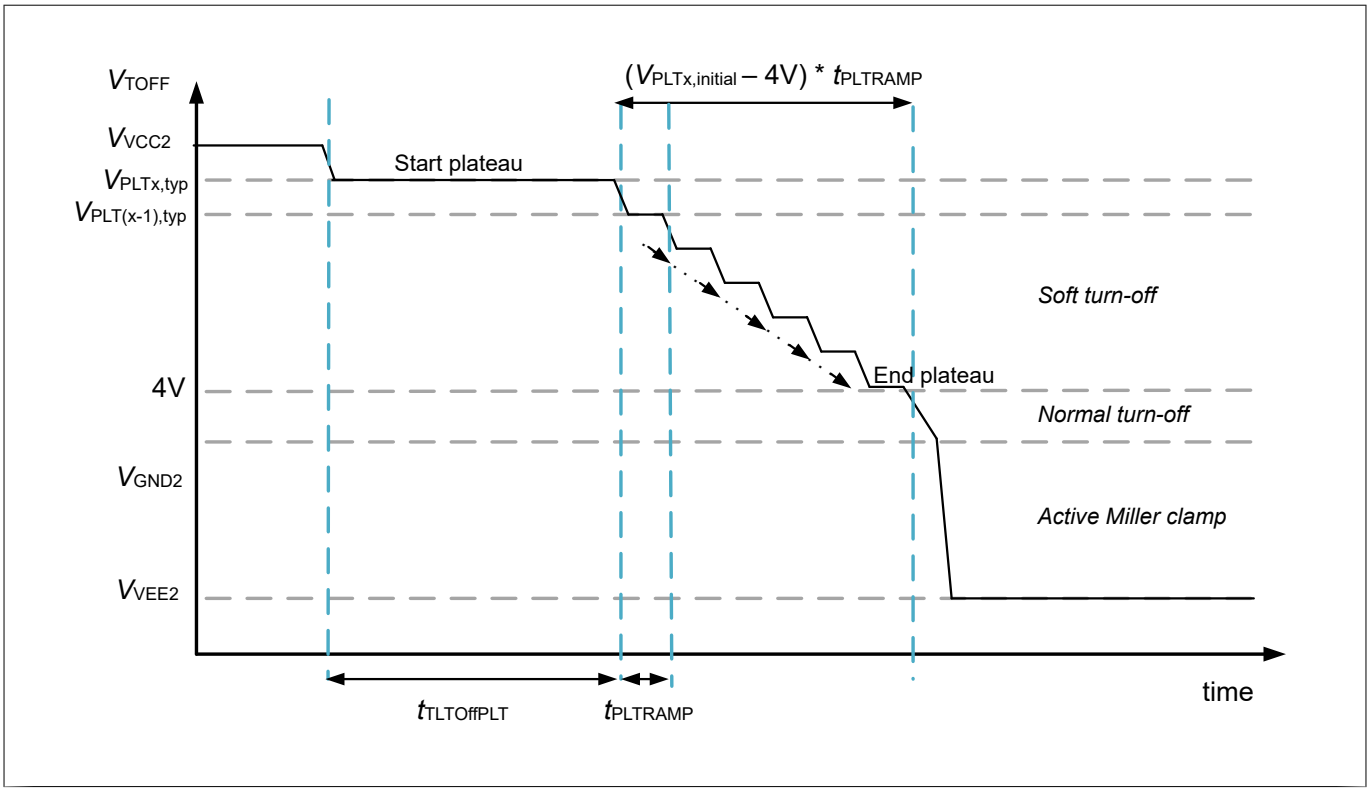

Figure 33 Regular soft turn-off timing diagram

Note:
- *The timing might change depending on the different gate charge that are used*
- *The initial plateau helps to reduce immediately the current on the power switch and should be selected to fit to the external power switch*

18.2 Electrical characteristics turn-off modes

Table 65 Electrical characteristics turn-off modes

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Two-level turn-off plateau time	$t_{TLTOffPLT}$	70	–	3387	ns	V_{VCC2} - 0.5 V to V_{PLTx} - 0.5 V, belongs to 6 bit value, jitter included	PRQ-451
Plateau voltage 0	V_{PLT0}	3.76	4	4.24	V	$V_{VCC2} \geq V_{PLT0}$ + 2 V, C_{LOAD} = 1 nF	PRQ-430
Plateau voltage 1	V_{PLT1}	4.7	5	5.3	V	$V_{VCC2} \geq V_{PLT1}$ + 2 V, C_{LOAD} = 1 nF	PRQ-431
Plateau voltage 2	V_{PLT2}	5.64	6	6.36	V	$V_{VCC2} \geq V_{PLT2}$ + 2 V, C_{LOAD} = 1 nF	PRQ-432

(table continues...)

Table 65 (continued) Electrical characteristics turn-off modes

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Plateau voltage 3	V_{PLT3}	6.58	7	7.42	V	$V_{VCC2} \geq V_{PLT3}$ + 2 V, C_{LOAD} = 1 nF	PRQ-433
Plateau voltage 4	V_{PLT4}	7.52	8	8.48	V	$V_{VCC2} \geq V_{PLT4}$ + 2 V, C_{LOAD} = 1 nF	PRQ-434
Plateau voltage 5	V_{PLT5}	8.46	9	9.54	V	$V_{VCC2} \geq V_{PLT5}$ + 2 V, C_{LOAD} = 1 nF	PRQ-435
Plateau voltage 6	V_{PLT6}	9.4	10	10.6	V	$V_{VCC2} \geq V_{PLT6}$ + 2 V, C_{LOAD} = 1 nF	PRQ-436
Plateau voltage 7	V_{PLT7}	10.34	11	11.66	V	$V_{VCC2} \geq V_{PLT7}$ + 2 V, C_{LOAD} = 1 nF	PRQ-437
Plateau voltage 8	V_{PLT8}	11.28	12	12.72	V	$V_{VCC2} \geq V_{PLT8}$ + 2 V, C_{LOAD} = 1 nF	PRQ-438
Plateau voltage 9	V_{PLT9}	12.22	13	13.78	V	$V_{VCC2} \geq V_{PLT9}$ + 2 V, C_{LOAD} = 1 nF	PRQ-439
Plateau voltage 10	V_{PLT10}	13.16	14	14.84	V	$V_{VCC2} \geq V_{PLT10}$ + 2 V, C_{LOAD} = 1 nF	PRQ-440
Plateau voltage 11	V_{PLT11}	14.1	15	15.9	V	$V_{VCC2} \geq V_{PLT11}$ + 2 V, C_{LOAD} = 1 nF	PRQ-441
Plateau voltage 12	V_{PLT12}	15.04	16	16.96	V	$V_{VCC2} \geq V_{PLT12}$ + 2 V, C_{LOAD} = 1 nF	PRQ-442
Regular soft-off step duration	$t_{PLTRAMP}$	20	–	1680	ns	Start: V_{PLTx} - 0.5 V, Stop: $V_{PLT(x-1)}$ - 0.5 V, belongs to 6 bit value, 0x0 = disabled	PRQ-116
Fast soft turn-off slew rate	SR_{FSOFF}	-0.020	-0.015	-0.0105	V/ns	VCC1 = typ., V_{VCC2} = 20 V, VEE2 = typ., C_{LOAD} = 1 nF, R_{LOAD} = 1.69 Ω, Start: V_{VCC2} - 1.5 V, Stop: $V_{PLT,x}$ + 1.5 V	PRQ-739
Tristate impedance TON	$I_{TRISTATE}$			2	mA		PRQ-674

19 Gate monitoring

19.1 Functional description gate monitoring

The device monitors in the time frame of t_{GMBT} (dynamic or static) the gate signal V_{GATE} at pin GATE/CLAMPx to ensure the signal from TON reaches GATE properly. If monitoring conditions are violated, the device issues a behavior according to configuration in less than $t_{GM\text{-}DaR}$ and if enabled/configured changes to Error_Mode in less than t_{RDY_GM}.

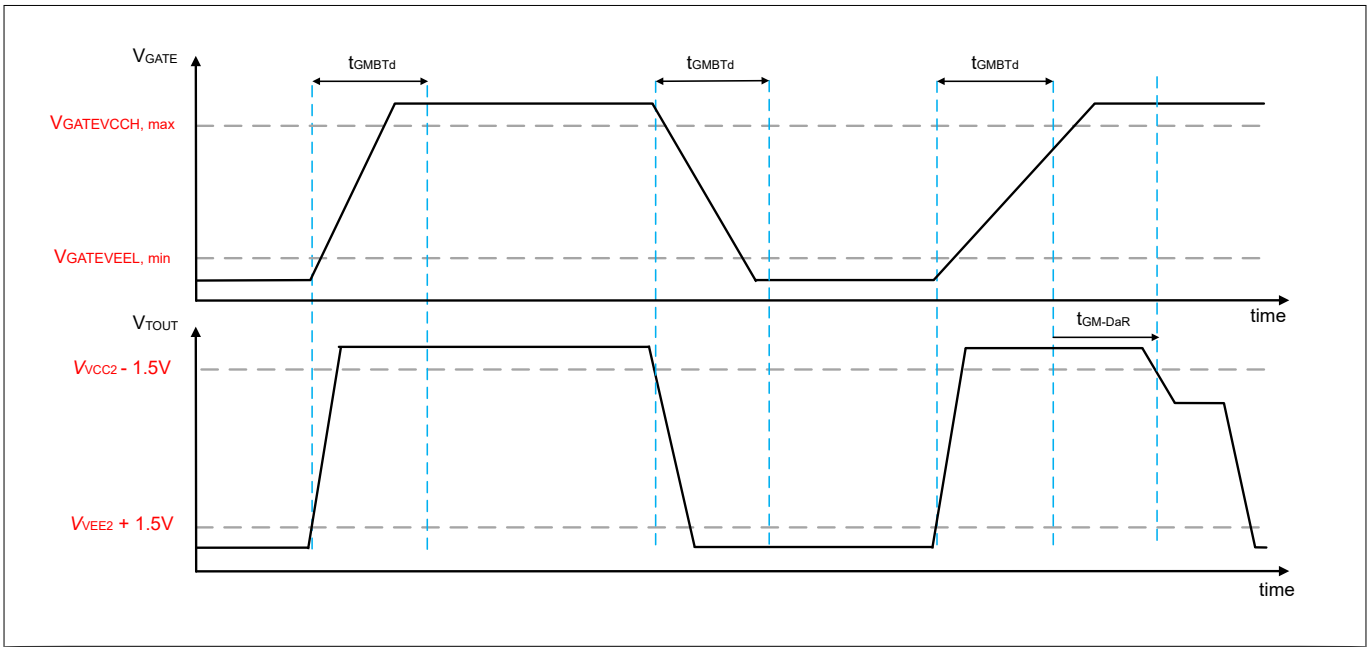

Figure 34 Dynamic gate monitoring timing diagram

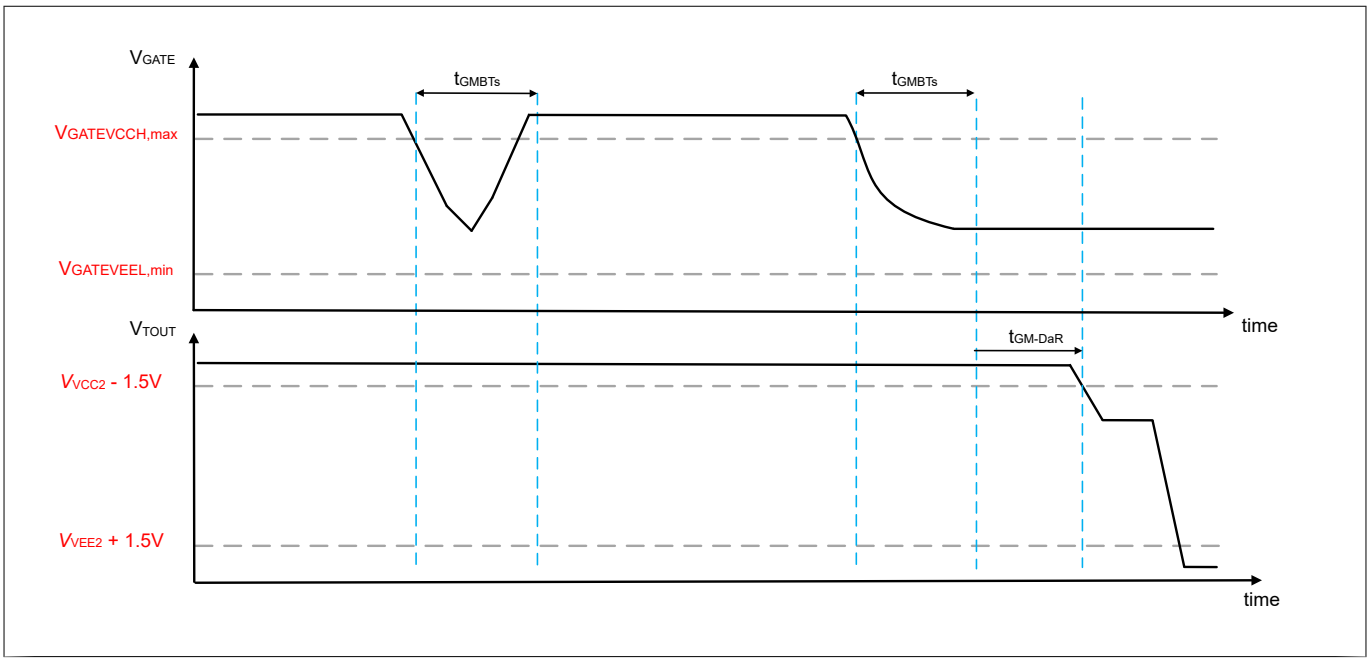

Figure 35 Static gate monitoring timing diagram

The gate monitoring blanking time (dynamic and static) can be configured via bit field GMOSMC.xGMBT.

The gate monitoring error reaction can be configured via bit field GMOSMC.GMERR.

19.2 Electric characteristics gate monitoring

Table 66 Electric characteristics gate monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring detection and reaction time	t_{GM-DaR}	200	350	560	ns	VCC2 = typ., VEE2 = typ.	PRQ-335
Gate monitoring detection and notification time	t_{RDY_GM}	–	1.5	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-336
Dynamic gate monitoring blanking time 1	t_{GMBTd1}	1.34	1.6	1.86	µs	VEE2 = typ., VCC2 = typ.	PRQ-338
Dynamic gate monitoring blanking time 2	t_{GMBTd2}	3.24	3.6	3.96	µs	VEE2 = typ., VCC2 = typ.	PRQ-340
Dynamic gate monitoring blanking time 3	t_{GMBTd3}	6.99	7.6	8.21	µs	VEE2 = typ., VCC2 = typ.	PRQ-342
Static gate monitoring blanking time 1	t_{GMBTs1}	1.75	1.9	2.05	µs	VEE2 = typ., VCC2 = typ.	PRQ-344
Static gate monitoring blanking time 2	t_{GMBTs2}	3.60	3.9	4.20	µs	VEE2 = typ., VCC2 = typ.	PRQ-346
Static gate monitoring blanking time 3	t_{GMBTs3}	7.40	7.9	8.40	µs	VEE2 = typ., VCC2 = typ.	PRQ-348
Gate monitoring VCC2 voltage threshold high level	$V_{GATEVCCH}$	V_{VCC2} - 2.3	V_{VCC2} - 2.1	V_{VCC2} - 1.9	V	t_{GMBT} is active	PRQ-349
Gate monitoring VCC2 voltage threshold low level	$V_{GATEVCCL}$	V_{VCC2} - 3.2	V_{VCC2} - 3	V_{VCC2} - 2.8	V	t_{GMBT} is active	PRQ-350
Gate monitoring VEE2 voltage threshold high level	$V_{GATEVEEH}$	2.8	3.0	3.2	V	t_{GMBT} is active, related to VEE2	PRQ-822
Gate monitoring VEE2 voltage threshold low level	$V_{GATEVEEL}$	1.9	2.1	2.3	V	t_{GMBT} is active, related to VEE2	PRQ-823

20 Output stage monitoring

20.1 Functional description output stage monitoring

The device output stage monitors whether the output signal of it is according to the given PWM or ASC input signal in $t_{OUTMBTx}$, otherwise it is issuing tri-state for the output stage in less than $t_{OUTM\text{-}DaR}$ and the device changes to Error_Mode in less than t_{RDY_OSM}.

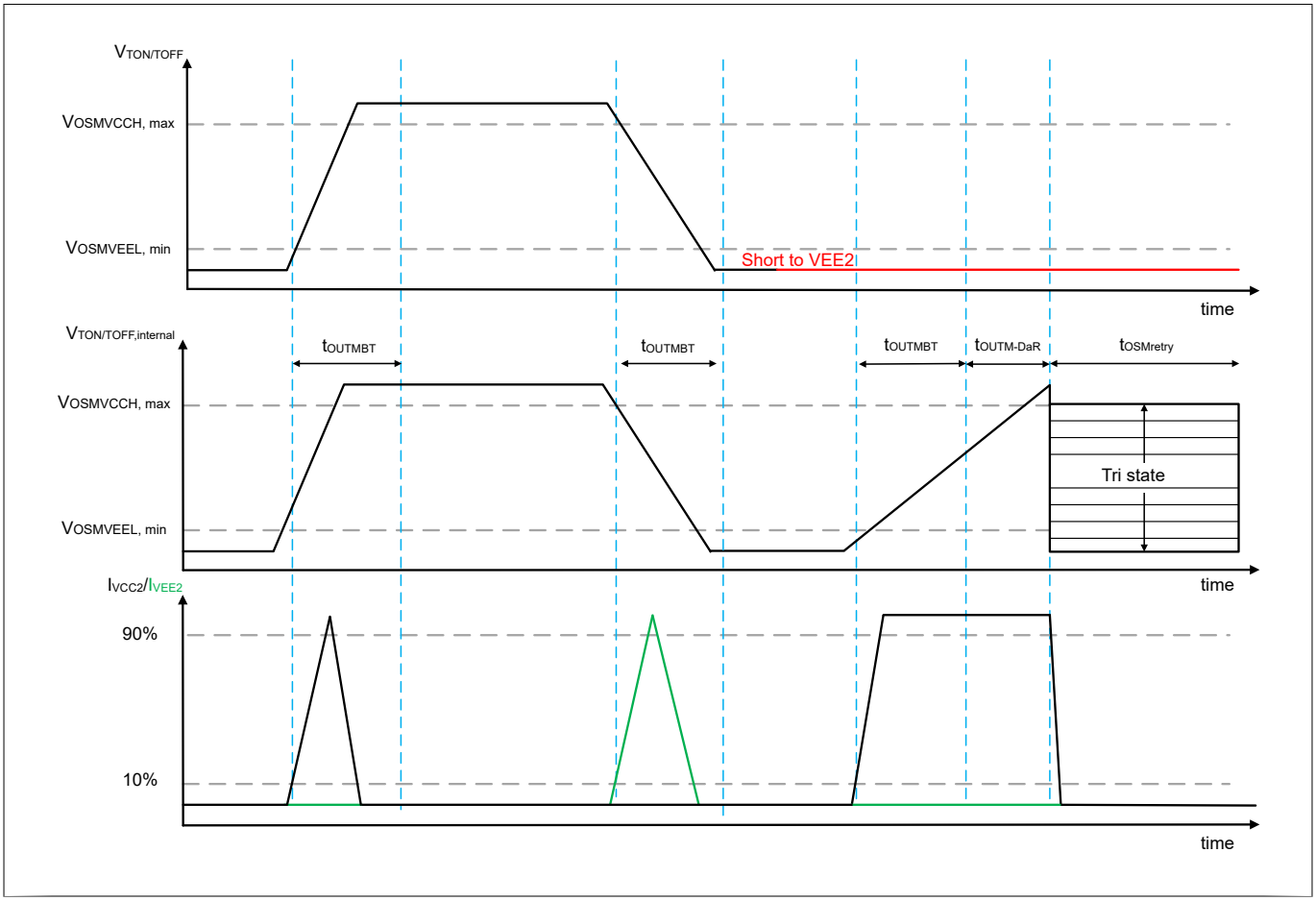

Figure 36 Dynamic output stage monitoring working principle

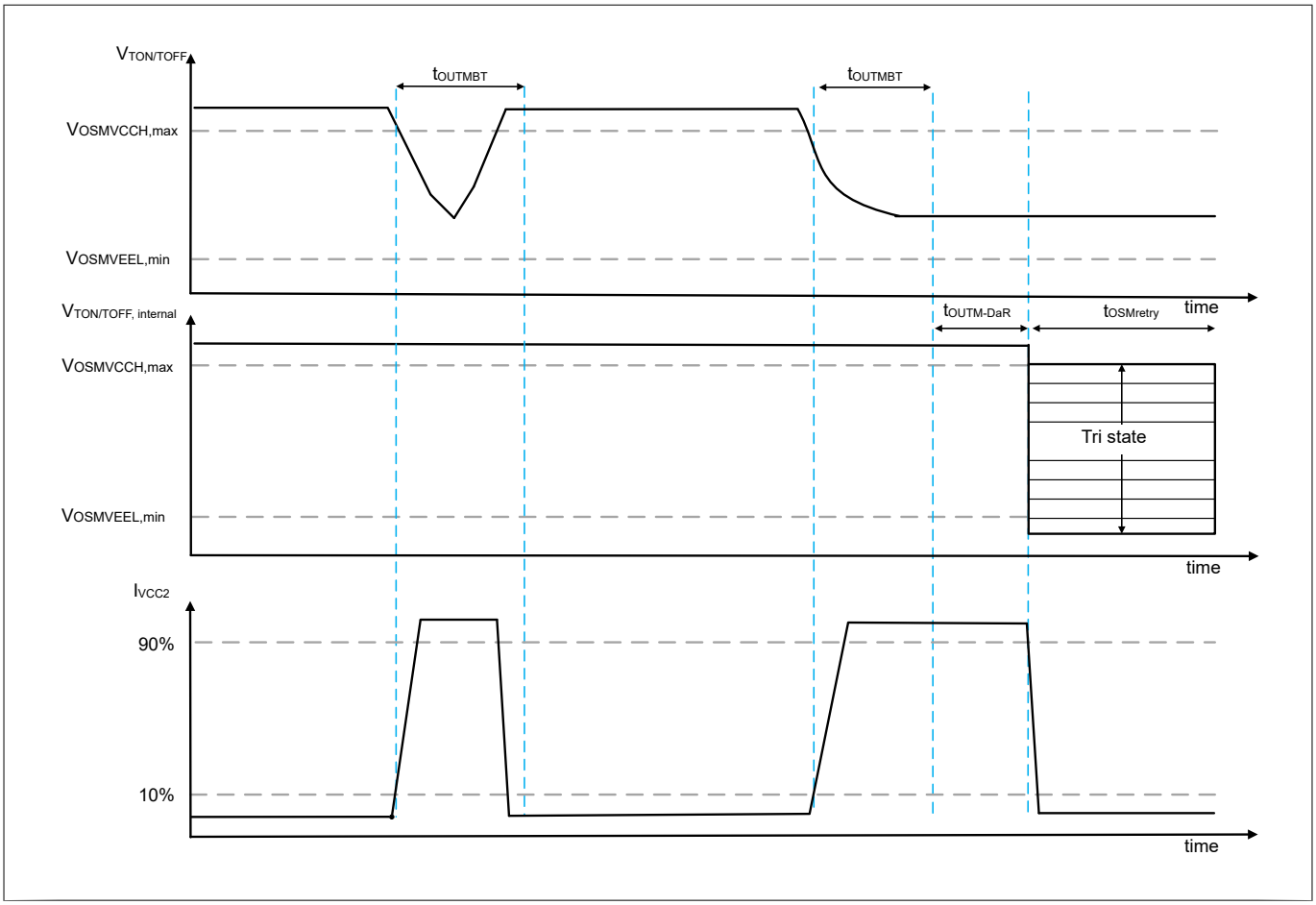

Figure 37 Static output stage monitoring working principle

Note:

- *The passive clamping at TOFF is working*
- *The blanking time starting point is defined by I_{VCC2}. $V_{TON/OFF,internal}$ is the internal TON/TOFF voltage generated by the device, based on the SI1/SI2 and PWM inputs. $V_{TON/TOFF}$ shows the actual voltage von pin TON/TOFF*
- *The OSM function monitors the path from SI1/SI2, PWM inputs ($V_{TON/TOFF, internal}$) to TON/TOFF pins ($V_{TON/TOFF}$)*

The output stage monitoring blanking time (dynamic and static) can be configured via bits GMOSMC.xOSMBT.

When the timing $t_{OSMretry}$ is exceeded after an output stage monitoring error was triggered, the tri-state of TON/TOFF is released and the device switches the output stage to the last commanded state in order to check if the error is still present. If yes, then the output stage monitoring error will be triggered again, otherwise the device will operate according to its input state.

20.2 Electric characteristics output stage monitoring

Table 67 Electric characteristics output stage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output stage monitoring detection and reaction time	$t_{OUTM-DaR}$	200	350	500	ns	VCC2 = 15 V, VEE2 = -5 V	PRQ-354
Output stage monitoring detection and notification time	t_{RDY_OSM}	–	1.5	2.5	µs	VCC2 = 15 V; VEE2 = -5 V;	PRQ-355
Output stage monitoring retry time	$t_{OSMretry}$	195	205	215	µs		PRQ-884
Output stage monitoring blanking time 1	$t_{OUTMBT1}$	200	400	600	ns	VEE2 = -5 V; VCC2 = 15 V;	PRQ-356
Output stage monitoring blanking time 2	$t_{OUTMBT2}$	600	800	1000	ns	VEE2 = -5 V; VCC2 = 15 V;	PRQ-357
Output stage monitoring blanking time 3	$t_{OUTMBT3}$	1000	1200	1400	ns	VEE2 = -5 V; VCC2 = 15 V;	PRQ-358
Output stage monitoring VCC2 voltage threshold high level	$V_{OSMVCCH}$	V_{VCC2} - 2.3	V_{VCC2} - 2.1	V_{VCC2} - 1.9	V	t_{OUTBT} is active	PRQ-362
Output stage monitoring VCC2 voltage threshold low level	$V_{OSMVCCL}$	V_{VCC2} - 3.2	V_{VCC2} - 3	V_{VCC2} - 2.8	V	t_{OUTBT} is active	PRQ-363
Output stage monitoring VEE2 voltage threshold high level	$V_{OSMVEEH}$	V_{VEE2} + 2.8	V_{VEE2} + 3	V_{VEE2} + 3.2	V	t_{OUTBT} is active	PRQ-364
Output stage monitoring VEE2 voltage threshold low level	$V_{OSMVEEL}$	V_{VEE2} + 1.9	V_{VEE2} + 2.1	V_{VEE2} + 2.3	V	t_{OUTBT} is active	PRQ-365

21 Passive gate clamping

21.1 Functional description passive gate clamping

If the secondary chip is not supplied via VCC2, the pin GATE/CLAMPx is passively clamped to VEE2.

21.2 Electrical characteristics passive gate clamping

Table 68 Electrical characteristics passive gate clamping

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GATE passive clamping voltage (ICLAMP = 10 mA)	V_{PCLPGx}	–	–	V_{VEE2} + 2 V	V	Secondary chip not supplied (VCC2 floating, VEE2 = 0 V), I_{Clamp} = 10 mA	PRQ-521

22 Internal supervision

22.1 Functional description internal supervision

The device has primary and secondary internal supervision. The specific functions are summarized in the table below:

Table 69 Primary and secondary internal supervision

Supervision	Function	Reaction of output stage
Primary	Parity bit protection	TON/TOFF = low (VEE2)
	PMU supervision	TON/TOFF = low (VEE2)
Secondary	OCP pin open detection	TON/TOFF = low (VEE2)
	Parity bit protection	TON/TOFF = low (VEE2)
	PMU supervision	TON/TOFF = low (VEE2)

Note: The output stage is turned-off at least for the duration of the internal supervision error event.

If an internal supervision error is triggered the device will switch TON/TOFF to low (VEE2) and notifies the primary side via RDY pin.

22.2 Electrical characteristics internal supervision

Table 70 Electrical characteristics internal supervision

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP pin open detection voltage	$V_{OCPxOPEN}$	2.2	2.45	2.7	V		PRQ-684
Primary internal supervision detection and notification time	t_{RDY_PINTSV}	–	1.5	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-867
Secondary internal supervision detection and notification time	t_{RDY_SINTSV}	–	35	38	µs	VCC2 = typ., VEE2 = typ.	PRQ-868

23 Active Miller Clamp

In a half bridge configuration the switched off IGBT/SiC tends to dynamically turn ON during the turn-on phase of the opposite IGBT/SiC. An active miller clamp allows sinking the miller current across a low impedance path in this high dV/dt situation. Therefore, in many applications the use of a negative supply voltage can be avoided. The device implements internal (via pin GATE/CLAMPx) and external active miller clamping (via pin AMCLPx).

23.1 External Active Miller Clamp (EAMCLP)

23.1.1 Functional description external Active Miller Clamp

The AMCLPx output can be used to drive an external clamping MOSFET as shown in the following application example.

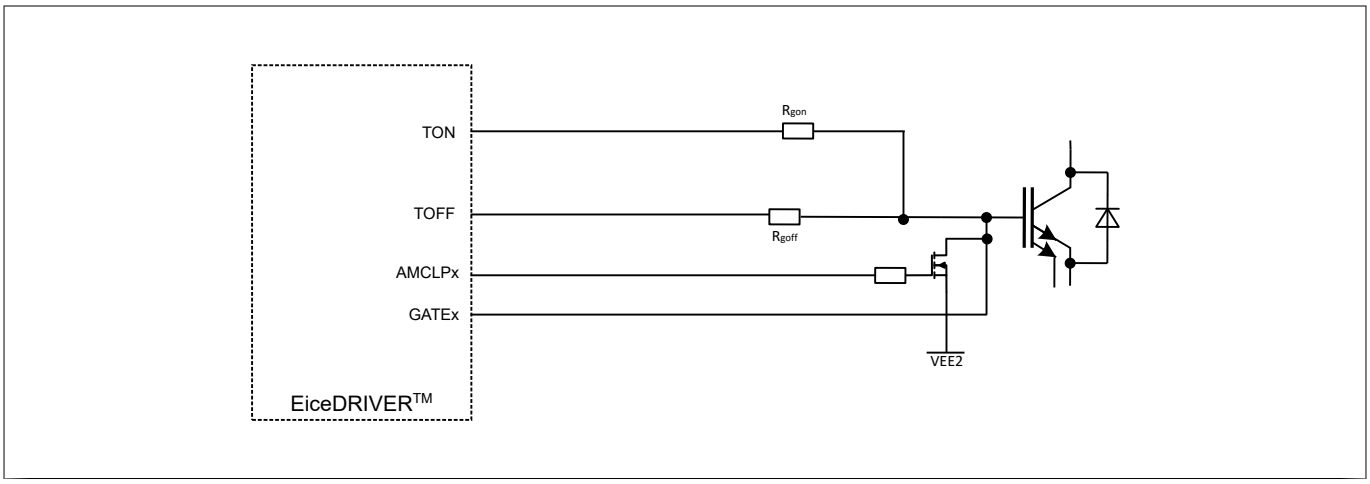

Figure 38 External active miller clamp example schematic

The external active miller clamping can be enabled/disabled via bit field AMCLPC.EAMCEN.

Note: IAMCLP has to be disabled via bit field AMCLPC.IAMCDIS, if external active miller clamping is used.

The EAMCLP propagation delay $t_{EAMCLPDELAYx}$ can be configured via bit field AMLCPC.EAMCLPDEL.

Note: This timing can be disabled, if external active miller clamp is disabled via SPI.

Note: Proper timing setting of the delays should be considered to avoid overlapping between output stage and ECLAMP.

Configuring $t_{EAMCLPDELAY0}$ means no additional delay at TON/TOFF compared to t_{pdon}.

The AMCLPx output is activated, if the gate voltage V_{GATE} decreases below the configured V_{CLAMPx_x} during turn-off.

Note: There are two output pins for this function dedicated for each gate of the parallel power switch (AMCLP1 & AMCLP2).

The AMCLPx output is deactivated before TON is activated when INP signal goes above $V_{digital,input(high)}$.

Note: There are two output pins for this function dedicated for each gate sensing input (AMCLP1 & AMCLP2).

The turn-on propagation delay t_{PDON} is extended by the configured time $t_{EAMCLPDELAYx}$, if EAMCLP is used.

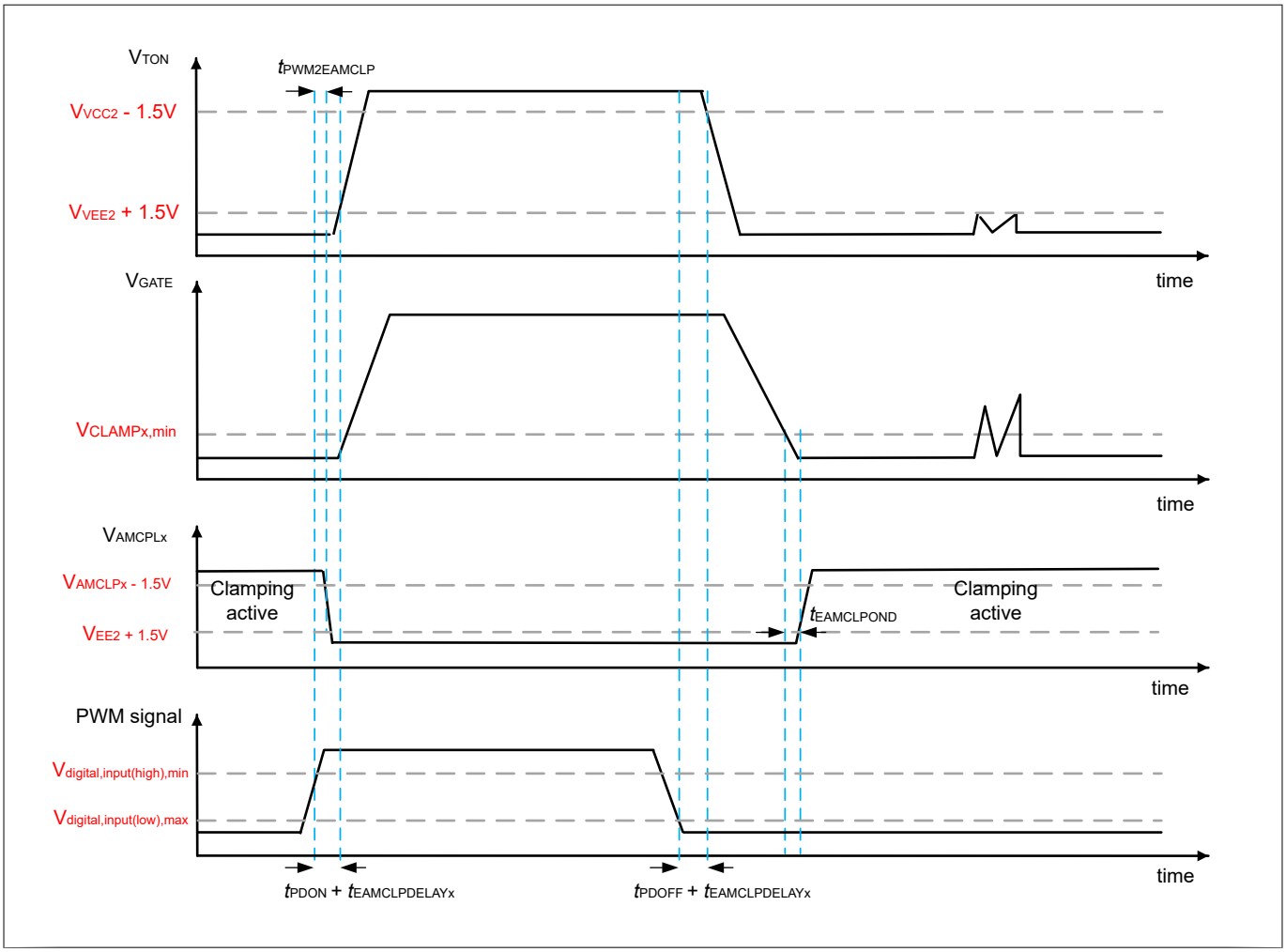

Figure 39 AMCLPx timing diagram

Note:

- *The turn-off propagation delay t_{PDOFF} is extended by the configured EAMCLP propagation delay $t_{EAMCLPDELAYx}$ to avoid distortion between turn-on and turn-off propagation delay.*
- *The start and stop timing indication in this diagram for turn-on and turn-off propagation delay are also valid if EAMCLP is disabled: $t_{EAMCLPDELAYx} = 0$.*

The clamping threshold level V_{CLAMPx_x} (when the clamping is activated) is configurable via bit AMCLPC.AMCVL. This threshold is valid for both: external and internal active miller clamping.

23.1.2 Electrical characteristics external Active Miller Clamp

Table 71 Electrical characteristics external Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level output voltage AMCLPx	V_{AMCLP}	10	12	14	V	Referenced to VEE2	PRQ-687
High level output peak current	I_{AMCLPH}	-0.4	-0.7	-	A	$V_{INP} = V_{GND1}$, $V_{SI1} = V_{SI2} = V_{VCC1}$, $V_{TOFF} = V_{VEE2}$, $V_{CLAMP/GATE} = V_{VEE2}$, V_{VCC2} = 15 V, V_{VEE2} = -5 V, $V_{AMCLP} = V_{VEE2} + 8V$, t_{max} = 100ns	PRQ-875
Low level RDSON	$R_{DSON\_AMCLPLx}$	-	1.5	3	Ω	$V_{INP} = V_{GND1}$, $V_{SI1} = V_{SI2} = V_{VCC1}$, $V_{TOFF} = V_{VEE2}$, TON = V_{VEE2}, $V_{CLAMP/GATE} = V_{VEE2}$, V_{VCC2} = 15 V, V_{VEE2} = -5 V, $V_{AMCLP} = V_{VEE2}$ + 0.2V	PRQ-880
EAMCLP rise time	$t_{Rise-AMCLPx}$	–	–	25	ns	C_{LOAD} = 1 nF, R_{LOAD} = 4.7 Ω, Start: AMCLPx rising edge at $V_{AMCLPx} = V_{VEE2}$ + 1.5 V, Stop: AMCLPx rising edge at $V_{AMCLPx} = V_{EAMCLPx,min}$ - 1.5 V, VEE2 = typ., VCC2 = typ., VCC1 = typ.	PRQ-694
EAMCLP fall time	$t_{Fall-AMCLP}$	–	–	15	ns	C_{LOAD} = 1 nF, R_{LOAD} = 4.7 Ω, Start: AMCLPx at falling edge at $V_{AMCLPx} = V_{EAMCLPx,max}$ - 1.5 V, Stop: AMCLPx falling edge at $V_{AMCLPx} = V_{VEE2}$ + 1.5 V, VCC2 = typ., VCC1 = typ., VEE2 = typ.	PRQ-695

(table continues...)

Table 71 (continued) Electrical characteristics external Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
EAMCLP activation time	$t_{EAMCLPOND}$	40	120	200	ns	Start: GATE/CLAMPx falling edge at V_{CLAMPx} = typ., Stop: AMCLPx rising edge at $V_{AMCLPx} = V_{VEE2}$ + 1.5 V, R_{LOAD} = 4.7 Ω, C_{LOAD} = 1 nF, VCC1 = typ., VCC2 = typ., VEE2 = typ.	PRQ-696
EAMCLP deactivation time	$t_{PWM2EAMCLP}$	30	50	110	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., C_{LOAD} = 1 nF, R_{LOAD} = 4.7 Ω, start is INP rising edge at $V_{digital,input(high)}$, stop is $V_{AMCLP,x} = V_{VEE2}$ + 1.5 V	PRQ-744
EAMCLP propagation delay 1	$t_{EAMCLPDELAY1}$	52	70	80	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-623
EAMCLP propagation delay 2	$t_{EAMCLPDELAY2}$	50	58	65	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-624
EAMCLP propagation delay 3	$t_{EAMCLPDELAY3}$	43	51	58	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-625

(table continues...)

Table 71 (continued) Electrical characteristics external Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
EAMCLP propagation delay 4	$t_{EAMCLPDELAY4}$	37	45	52	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-626
EAMCLP propagation delay 5	$t_{EAMCLPDELAY5}$	30	36	42	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-627
EAMCLP propagation delay 6	$t_{EAMCLPDELAY6}$	22	28	34	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-628
EAMCLP propagation delay 7	$t_{EAMCLPDELAY7}$	15	21	26	ns	$t_{EAMCLPDELAYx} = t_{PD,total} - t_{PDON/OFF,}$ VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no C_{LOAD}, no R_{LOAD}	PRQ-629
Clamp threshold voltage 0	V_{CLAMPx_0}	0.763	0.8	0.860	V	Related to GND2	PRQ-706
Clamp threshold voltage 1	V_{CLAMPx_1}	2	2.1	2.2	V	Related to GND2	PRQ-707
Clamp threshold voltage 2	V_{CLAMPx_2}	2.88	3	3.12	V	Related to GND2	PRQ-708

23.2 Internal Active Miller Clamp (IAMCLP)

23.2.1 Functional description internal Active Miller Clamp

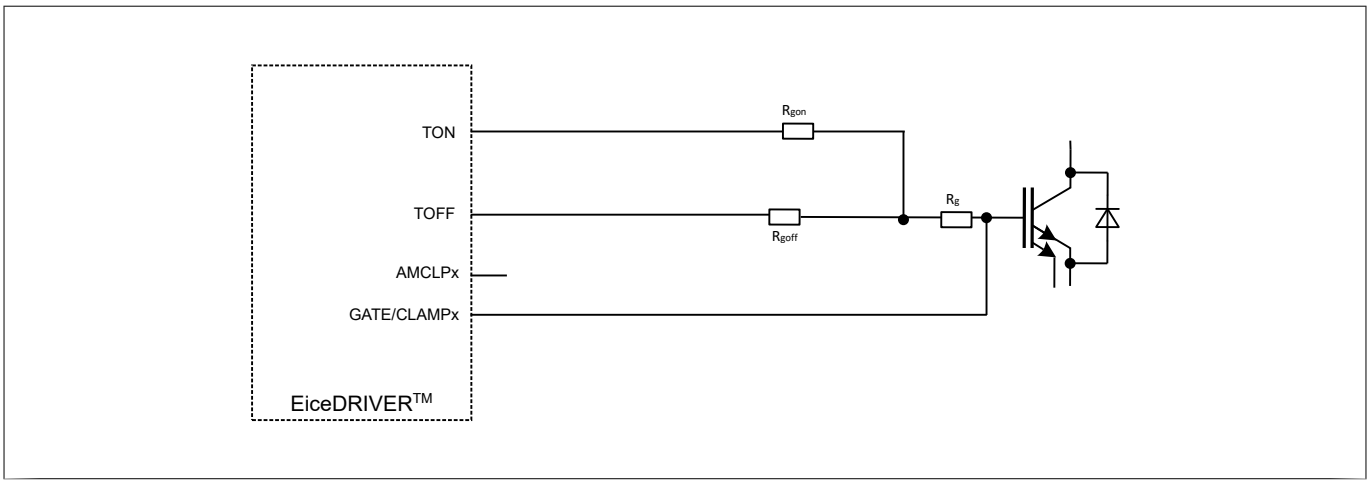

Figure 40 Internal active miller clamping example circuit

The internal active miller clamping can be enabled/disabled via bit field AMCLPC.IAMCDIS.

Note: EAMCLP has to be disabled via bit field AMCLPC.EAMCEN, if internal active miller clamping is used.

The GATE/CLAMPx output is activated, if the gate voltage V_{GATE} decreases below the configured V_{CLAMPx_x} during turn-off.

Note: There are two output pins for this function dedicated for each gate of the parallel power switch (GATE/CLAMP1 & GATE/CLAMP2).

The GATE/CLAMPx output is deactivated before TON is activated when INP signal goes above $V_{digital,input(high)}$.

Note: There are two output pins for this function dedicated for each gate sensing input (GATE/CLAMP1 & GATE/CLAMP2).

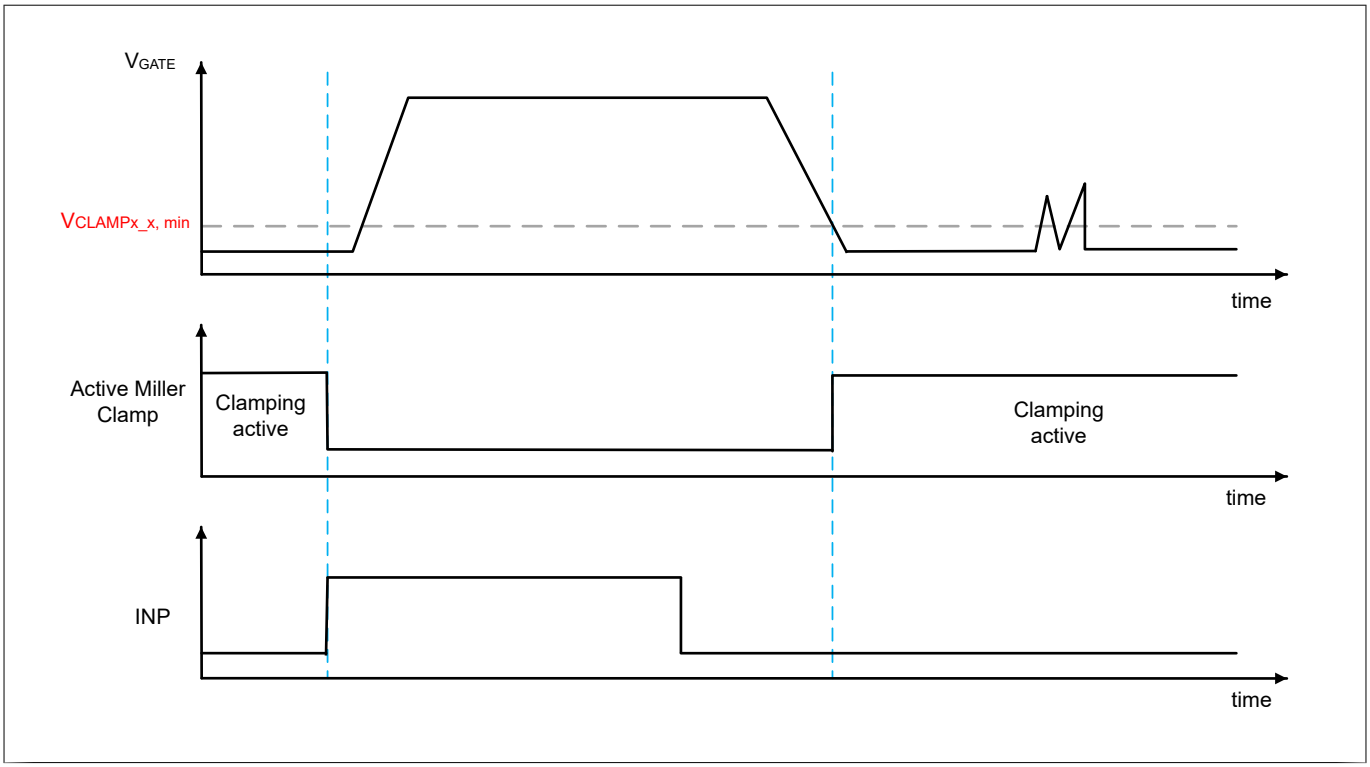

Figure 41 Internal active miller clamp timing diagram.

The clamping threshold V_{CLAMPx_x} (when the clamping is active) is configurable via bit AMCLPC.AMCVL. This threshold is valid for both: external and internal active miller clamping

23.2.2 Electrical characteristics internal Active Miller Clamp

Table 72 Electrical characteristics Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2}, and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level clamp peak current	$I_{CLAMPLx}$	3	5	–	A	INP = V_{GND1}, INN = V_{GND1}, SI1 = SI2 = V_{VCC1}, TOFF = falling edge to V_{VEE2}, CLAMP/ GATEx = $V_{CLAMPx\_2,(min)}$, VCC2 = 15 V, VEE2 = -5 V, C_{LOAD}= 1 µF	PRQ-149
CLAMPx RDSON	$R_{DSON-CLAMPx}$	0.23	–	0.6	Ω		PRQ-152

24 Application information

The following figure describes how the IC is used in its environment.

Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

- Please contact Infineon for additional supportive documentation.
- For further information you may contact http://www.infineon.com/

Note: This figure is a simplified example of an application circuit. The function must be verified in the application.

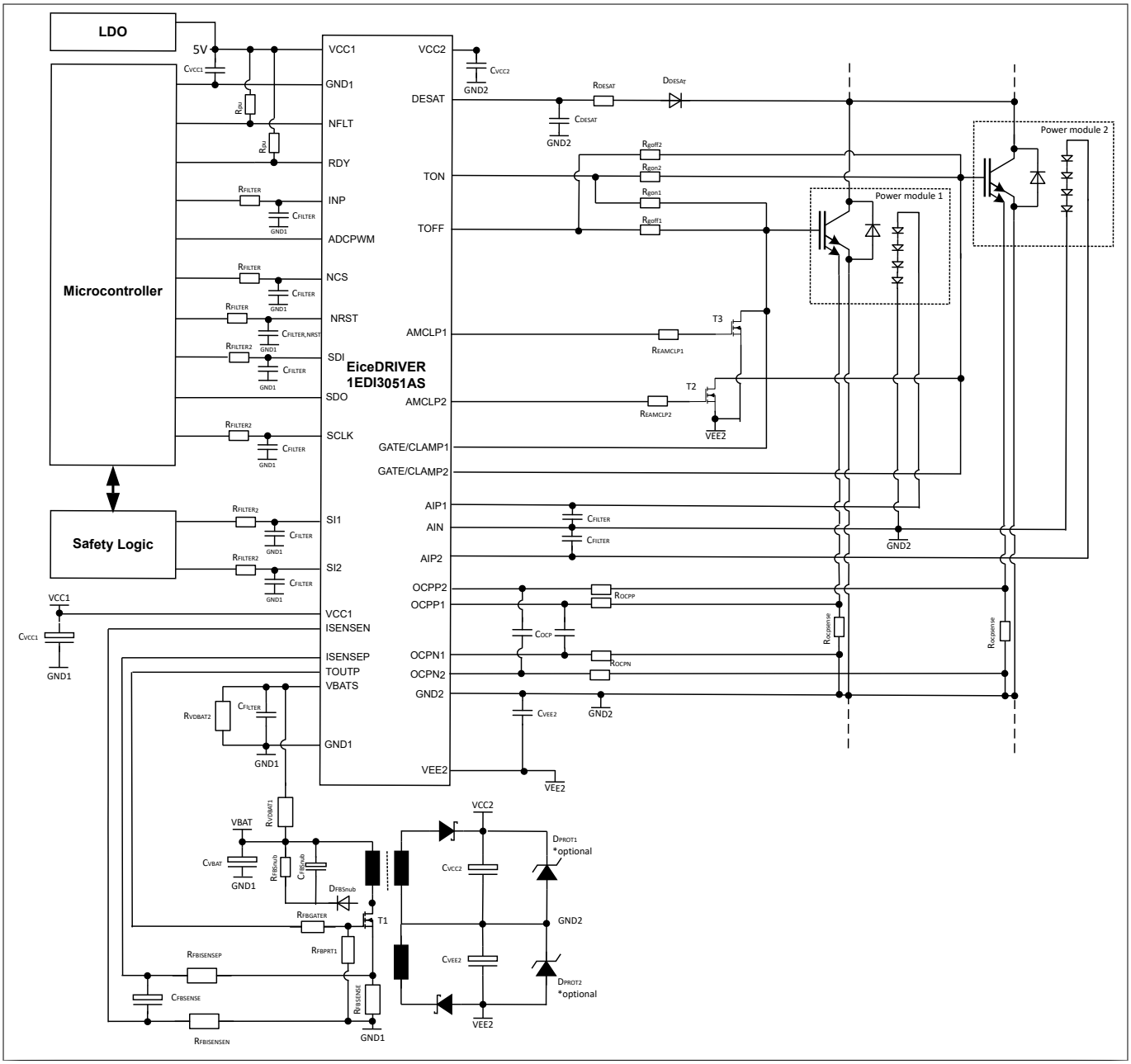

Figure 42 Simplified application example

24.1 Application schematic component values

Table 73 Application schematic component values

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Decoupling capacitance (between VCC1 and GND1)	C_{VCC1}	1	2.3	–	µF	Total capacitance refers to 2.2 µF capacitance + 0.1 µF close to the device. Max value depends on t_{RP1}.	PRQ-499
Decoupling capacitance (between VCC2 and GND2)	C_{VCC2}	4.7	11	20	µF	Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Values depend on external C_{LOAD}.	PRQ-500
Decoupling capacitance (between VEE2 and GND2)	C_{VEE2}	4.7	11	20	µF	Total capacitance refers to 10 µF capacitance + 1 µF close to the device.	PRQ-501
Output voltage ripple on VCC2 at constant load	$V_{VCC2RIPP}$	–	–	0.4	V	Peak to peak ripple during stable load condition, depends on application: $I_{LoadVCC2}$ = 120mA, V_{BAT} = 13V, C_{VCC2} = 11µF, L_{prim} = 5µH, f_s = 250kHz, V_{VCC2} = 18V, V_{VEE2} = -4V	PRQ-423
Output voltage ripple on VEE2 at constant load	$V_{VEE2RIPP}$	–	–	0.2	V	Peak to peak ripple during stable load condition, depends on application: $I_{LoadVEE2}$ = 120mA, V_{BAT} = 13V, C_{VEE2} = 22µF, L_{prim} = 5µH, f_s = 250kHz, V_{VCC2} = 18V, V_{VEE2} = -4V	PRQ-424
Pull-up resistance	R_{pu}	1.1	10	47	kΩ	Min value depends on I_{OUTx_MAX}.	PRQ-502
Filter resistance	R_{Filter}	–	1	–	kΩ	Value must fit to application	PRQ-503
Filter resistance 2	$R_{Filter2}$	-	100	-	Ω	Value must fit to application	PRQ-644
Filter capacitance	C_{Filter}	–	47	–	pF	Value must fit to application	PRQ-504

(table continues...)

Table 73 (continued) Application schematic component values

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Filter capacitance NRST	$C_{Filter,NRST}$	-	100	-	pF	Value must fit to application	PRQ-645
DESAT diode	D_{Desat}	600	1200	–	V	ultra fast diode recommended (e.g. 75ns)	PRQ-550
DESAT resistance	R_{Desat}	1	2.2	–	kΩ	Depends on maximum current and on V_{DESATx} selection.	PRQ-505
DESAT filter capacitance	C_{Desat}	10	100	–	pF	Depends on required response time and selected settings by SPI. Too large capacity may equals disabling DESAT function.	PRQ-506
OCP sense resistor	$R_{OCPSense}$	–	0.47	–	Ω	Value depends on IGBT/SiC specification, voltage rating and threshold selection of OCP pin has to be considered.	PRQ-507
OCPP filter resistance	R_{OCPP}	–	10	–	Ω	Depends on required response time. Consider internal pull-up.	PRQ-508
OCPP filter capacitance	C_{OCP}	–	10	–	pF	Depends on required response time	PRQ-509
OCPN resistance	R_{OCPN}	–	10	–	Ω	Should match to OCPP filter resistor. Consider internal pull-up.	PRQ-510
TON resistance ON	R_{gON}	1.1	2.35	–	Ω	Min resistor value required according to max output current in functional range (considered 14 V unipolar on VCC2). Max value limited by gate monitoring feature.	PRQ-511

(table continues...)

Table 73 (continued) Application schematic component values

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TOFF resistance OFF	R_{gOFF}	1.1	2.35	–	Ω	Min resistor value required according to max output current in functional range (considered 14 V VCC2 unipolar). Max value limited by gate monitoring feature.	PRQ-512
Flyback MOSFET protection resistance	R_{FBPRT1}	–	10	–	kΩ		PRQ-651
Flyback MOSFET gate resistance	$R_{FBGATER}$	4.7	–	–	Ω		PRQ-650
Flyback Transistor	T1	–	BSL606SN	–			PRQ-514
VBATS divider resistance 1	R_{VDBAT1}	-	220	-	kΩ	resistance on VBATS to battery (transformer input) voltage;	PRQ-472
VBATS divider resistance 2	R_{VDBAT2}	1	10	-	kΩ	resistance on VBATS to GND1 (primary / battery ground);	PRQ-473
VBAT capacitance	C_{VBAT}	-	10	-	µF	Value must fit to application	PRQ-643
ISENSEP filter resistance	$R_{FBISENSEP}$	-	10	-	Ω	Value must fit to application	PRQ-646
ISENSEN filter resistance	$R_{FBISENSEN}$	-	10	-	Ω	Value must fit to application	PRQ-647
ISENSEx shunt resistance	$R_{FBSENSE}$	-	200	-	mΩ	Shunt resistance tolerance should be 2% or lower	PRQ-648
ISENSEx filter capacitance	$C_{FBSENSE}$	-	10	-	nF	Value must fit to application	PRQ-649
Flyback snubber resistance	R_{FBSnub}	-	2.1	-	kΩ	Value must fit to application	PRQ-653
Flyback snubber capacitance	C_{FBSnub}	-	47	-	nF	Value must fit to application	PRQ-652
Flyback snubber diode	D_{FBSnub}		US1B-E3				PRQ-654
AMCLP Transistor	T2, T3	–	BSL306N	–			PRQ-515

(table continues...)

Table 73 (continued) Application schematic component values

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
EAMCLP gate resistance 1	$R_{EAMCLP1}$	4.7	10	-	Ω	Switching characteristics depend on application conditions	PRQ-892
EAMCLP gate resistance 2	$R_{EAMCLP2}$	4.7	10	-	Ω	Switching characteristics depend on application conditions	PRQ-893

25 Package information

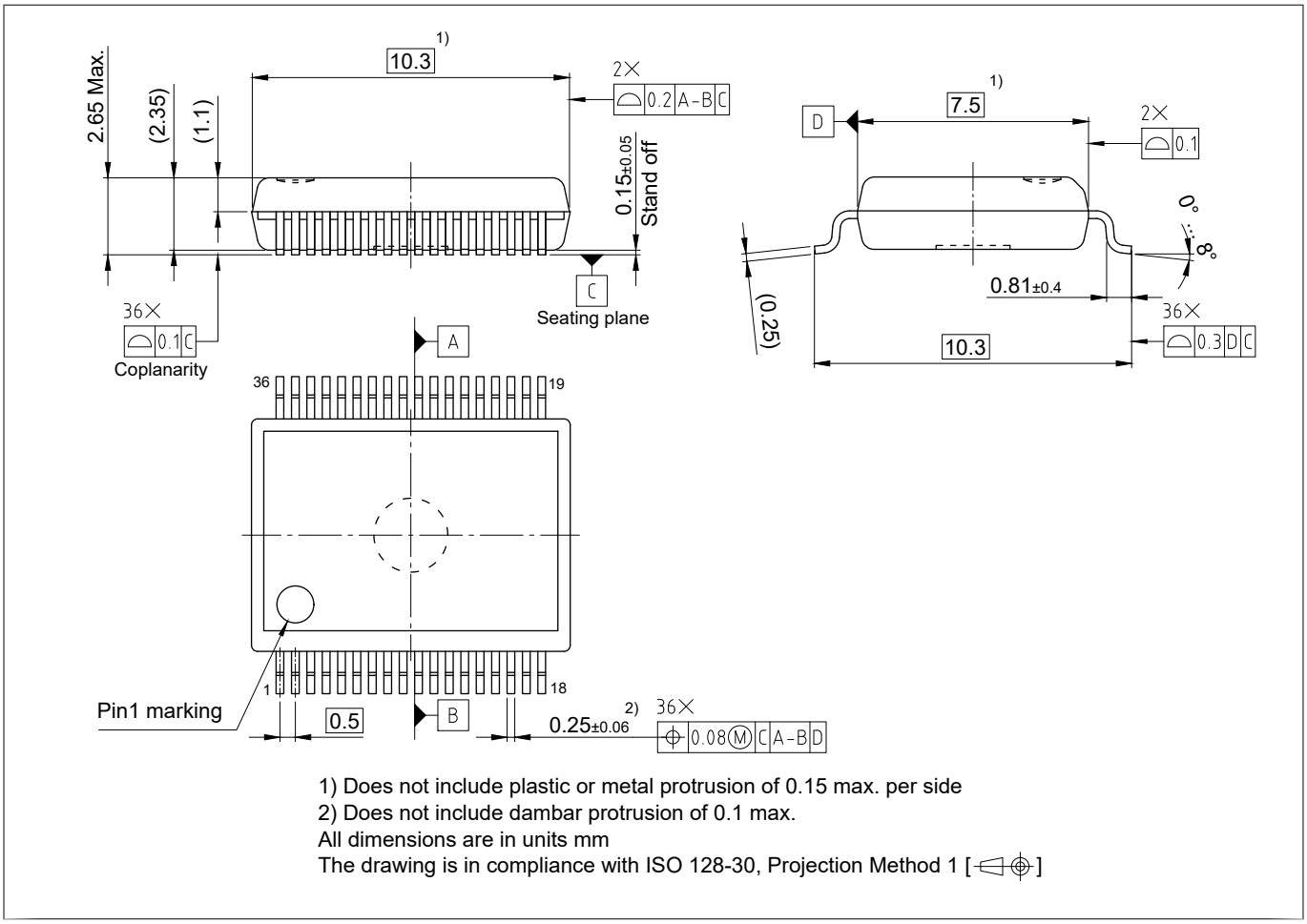

Figure 43 PG-DSO-36

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

26 Revision history

Revision	Date	Changes
1.0	2023-05-15	Datasheet Created

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