EiceDRIVER™ gate driver 1EDI3023AS

Single channel isolated IGBT driver

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AEC Qualified | RoHS | ISO 26262 compliant

Features

- Single channel isolated IGBT driver using coreless transformer technology
- For IGBTs up to 1200 V
- CMTI up to 150 V/ns at 1000 V
- Reinforced insulation 8 kV peak according to DIN EN IEC 60747-17 (VDE 0884-17) : 2021-10
- 5.7 kV rms insulation according to UL 1577
- Min. 12 A peak current rail-to-rail output
- Propagation delay 60 ns typical
- Typ. 10 A integrated Active Miller Clamp supports unipolar switching
- Integrated ADC for DC-link measurements
- Integrated safety features to support ASIL B(D):
  - Redundant DESAT and OCP protection
  - Gate and output stage monitoring
  - Shoot-through protection
  - Primary/secondary supply monitoring
  - Internal supervision
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL B
- Green Product (RoHS compliant)

Potential applications

- Traction inverters for HEV and EV
- Auxiliary inverters for HEV and EV
- High power DC/DC converters

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The EiceDRIVER™ gate driver 1EDI3023AS is a high-voltage IGBT driver designed for automotive motor drives above 5 kW. The device is based on Infineon's coreless transformer (CT) technology, providing galvanic insulation between low voltage and high voltage domains. The device has been designed to support 400 V, 600 V and 1200 V IGBT technologies.

Description

The device features a high output stage of minimum 12 A peak current. A comprehensive feature set allows advanced protection of the device and the power switch, as well as optimized driver performance and robustness.

The device can be connected on the low voltage side (“primary” side) to 5 V and 3.3 V logic.

On the high voltage side (secondary side), the device is dimensioned to drive the gate of IGBTs directly. Short propagation delays and controlled internal tolerances lead to a minimal distortion of the PWM signal. In addition, there is a Miller clamping stage with minimum 12 A integrated, which allows unipolar supply of the IGBT.

The device features an integrated ADC for DC link measurement and a detailed error diagnosis via a PWM signal.

A large panel of safety related functions supports functional safety requirements at system level as per ISO 26262. Besides, these integrated features ease the implementation of a transition to safe-state.

Type	Package	Marking
1EDI3023AS	PG-DSO-20	1EDI3023AS

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1 Block diagram

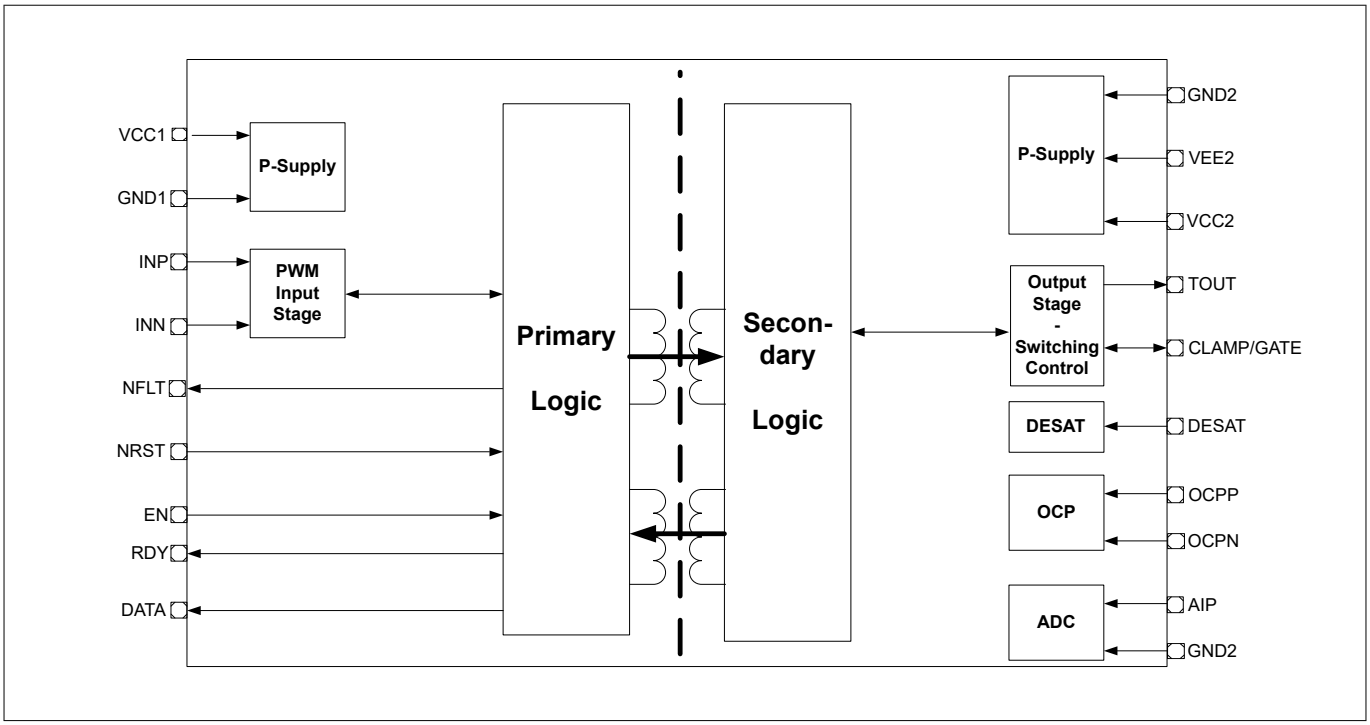


Figure 1 Block diagram

2 Pin configuration

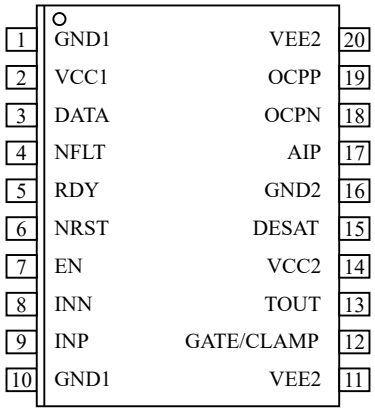


Figure 2 Pin assignment

2.1 Pin definitions and functions

Table 1 Pin definition and functions

Pin #	Pin name	I/O	Voltage class	Function
1	GND1	Ground	Primary ground	Ground connection for the primary side.
2	VCC1	Supply	Primary supply	5 V/3.3 V power supply for the primary side (referring to GND1).
3	DATA	Output	5 V primary	The data pin is used for ADC or diagnosis data. This pin is a push-pull output which is driving a PWM signal according to the data.
4	NFLT	Output	5 V primary	The fault open-drain signal is used to report failure events triggered by DESAT or OCP protection. As a result the pin is driven to low. This pin has to be connected externally to VCC1 with a pull-up resistance.
5	RDY	Output	5 V primary	The ready open-drain signal is used to report failure events like UVLO1, UVLO2, OVLO2, Life Sign Lost, Output Stage Error, Gate Monitoring Error, etc. As a result this pin is driven to low. This pin has to be connected externally to VCC1 with a pull-up resistance.
6	NRST	Input	5 V primary	The reset signal is used to clear the failure/fault events which triggered RDY or NFLT active low. The signal is clearing an error on rising edge. An internal pull-down resistance is driving this pin to low state in case the pin is floating.

(table continues...)

Table 1 (continued) Pin definition and functions

Pin #	Pin name	I/O	Voltage class	Function
7	EN	Input	5 V primary	The enable signal allows the logic on the primary side to enable or disable the device. The logic levels are according to the used power supply. An internal weak pull-down resistance is disabling the device in case the pin is floating.
8	INN	Input	5 V primary	The inverting PWM signal is used for monitoring for shoot through protection. An internal weak pull-up resistor to VCC1 drives this input to high state in case the pin is floating.
9	INP	Input	5 V primary	The non-inverting PWM signal of the driver. An internal weak pull-down resistor to GND1 drives this input to low state in case the pin is floating.
10	GND1	Ground	Primary ground	Ground connection for the primary side.
11	VEE2	Supply	Secondary supply	Negative power supply for the secondary side (referring to GND2).
12	GATE/ CLAMP	Input/ Output	15 V secondary	The gate monitoring and clamp signal is monitoring the gate of the power switch and clamping the gate to VEE2 if the threshold VCLAMP is reached.
13	TOUT	Output	15 V secondary	The transistor drive voltage signal switches the power switch gate to VCC2 or VEE2, according to the PWM input.
14	VCC2	Supply	Secondary supply	Positive power supply for the secondary side (referring to GND2).
15	DESAT	Input	15 V secondary	The desaturation protection signal monitors the voltage across the power switch. An internal current source to VCC2 drives this signal to high level in case it is floating.
16	GND2	Ground	Secondary ground	Reference ground for the secondary side.
17	AIP	Input	5 V secondary	The ADC function can be used to monitor the DC-link voltage. The internal current source is disabled.
18	OCPN	Input	5 V secondary	The negative over current protection signal is differential therefore it should be always close to OCPP signal. A common-mode filter should be applied to the OCPP signal.
19	OCPP	Input	5 V secondary	The positive over current protection signal is differential therefore it should be always close to OCPN signal. A common-mode filter should be applied to the OCPN signal. An internal weak pull-up resistor drives this input to high state in case the pin is floating.
20	VEE2	Supply	Secondary supply	Negative power supply for the secondary side (referring to GND2).

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	V_{VCC1_MAX}	-0.3	–	7	V	Referenced to GND1	PRQ-560
Positive power supply (secondary)	V_{VCC2_MAX}	-0.3	–	30	V	Referenced to GND2	PRQ-561
Negative power supply (secondary)	V_{VEE2_MAX}	-13	–	0.3	V	Referenced to GND2	PRQ-562
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2-VEE2\_MAX}$	–	–	40	V		PRQ-563
Voltages on any I/O pin on primary side (INP, INN, NRST, DATA, RDY, NFLT, EN)	V_{INx_MAX}	-0.3	–	V_{VCC1} + 0.3	V	Referenced to GND1	PRQ-564
AIP voltage	V_{AIP_MAX}	-0.3	–	V_{VCC2} + 0.3	V		PRQ-789
DESAT voltage	V_{DESAT_MAX}	-0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-566
OCPP	V_{OCPP_MAX}	-2.8	–	2.8	V	Referenced to GND2	PRQ-788
OCPN	V_{OCPN_MAX}	-2.8	–	2.8	V	Referenced to GND2	PRQ-831
Maximum Clamp/gate voltage	$V_{Clamp/Gate\_MAX}$	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-567
TOUT voltage	V_{OUT_MAX}	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-568

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TOUT high output maximum current	I_{OUTH_MAX}	-15	–	–	A	t_{MAX} = 1.5 µs, non-repetitive	PRQ-569
TOUT low output maximum current	I_{OUTL_MAX}	–	–	15	A	t_{MAX} = 1.5 µs, non-repetitive	PRQ-570
Gate/Clamp low maximum output current	$I_{Gate/Clamp\_Max}$	–	–	15	A	t_{MAX} = 1.5 µs, non-repetitive	PRQ-848
Current on output logic pins (DATA, RDY, NFLT)	$\|I_{OUTx\_MAX}\|$	–	–	10	mA		PRQ-572
ESD immunity	V_{ESD_HBM}	-2	–	2	kV	HBM according to AEC Q100-002, CDM according to AEC Q100-011	PRQ-573
Storage temperature	T_{s_MAX}	-55	–	150	°C		PRQ-575
Junction temperature	T_{J_MAX}	-40	–	150	°C		PRQ-790

3.2 Functional range

Table 3 Functional range

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	V_{VCC1}	3	–	5.5	V	Referenced to GND1	PRQ-579
VCC1 ramp-up slew-rate	t_{RP1}	–	–	2000	V/ms		PRQ-797

(table continues...)

Table 3 (continued) Functional range

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply IGBT (secondary)	V_{VCC2}	14.5	15	17.7	V	Referenced to GND2	PRQ-580
VCC2 ramp-up slew-rate	t_{RP2}	–	–	1000	V/ms		PRQ-798
Negative power supply (secondary)	V_{VEE2}	-11.5	-5	0	V	Referenced to GND2	PRQ-581
VEE2 ramp-up slew-rate	t_{RP3}	-1000	–	–	V/ms		PRQ-799
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2-VEE2}$	–	–	25	V		PRQ-582
Junction temperature	T_J	-40	–	150	°C		PRQ-588
Common mode transient immunity	dV_{ISO}/dt	-150	–	150	kV/µs	For voltages up to 1000 V	PRQ-589
Voltages on any I/O pin on primary side (INP, INN, NRST, DATA, RDY, NFLT)	V_{INx}	0	–	V_{VCC1}	V	Referenced to GND1	PRQ-583

3.3 Thermal characteristics

The thermal capability of the device is depending on the used power module. The following formula and parameters can be used to calculate the maximum switching frequency for a dedicated power module:

$$f_{SW} = \frac{P_{SW} \cdot \left(R_{DSON-OSLN} + R_g\right)}{\left(V_{VCC2} - V_{VEE2}\right)^2 \cdot C_{Gate} \cdot R_{DSON-OSLN}}$$

Figure 3 Formula to calculate the maximum switching frequency in application

Where the maximum switching losses are $P_{SW} = P_{DIS2} - P_{IDLE\_sec}$, R_g is the external gate resistor, C_{Gate} is the maximum gate charge of the power switch, and $R_{DSON-OSLN}$ is the internal gate resistor.

***Note**: This formula is only valid if ON/OFF resistors have the same value.*

3.3.1 Thermal characteristics parameters

Table 4 Thermal characteristics parameters

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power Dissipation - Primary Chip	P_{DIS1}	–	40	–	mW	T_{AMB} = 25°C, V_{VCC1} = 5 V, PWM duty cycle = 50%, Normal_Mode, no C_{LOAD}, no R_{LOAD} on TOUT, average value (peak current neglected)	PRQ-946
Power Dissipation - Secondary Chip	P_{DIS2}	–	300	–	mW	T_{AMB} = 25°C, V_{VCC2} = typ., V_{VEE2} = typ., PWM duty cycle = 50%, Normal_Mode, no C_{LOAD}, no R_{LOAD} on TOUT, average value (peak current neglected)	PRQ-947
Switching frequency	f_{SW}	–	25	430	kHz	V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_{Gate} = 9 nF, R_g = 6 Ω, T_{AMB} = 25°C	PRQ-839
Thermal Resistance Junction to Ambient (25°C)	R_{THJA}	–	85	–	K/W	T_{amb} = 25°C	PRQ-932
Thermal Resistance Junction to Ambient (125°C)	$R_{THJA,125}$	–	71	–	K/W	T_{AMB} = 125°C	PRQ-975
Thermal Resistance Junction to Case (bottom)	$R_{THJCBOT}$	–	60	–	K/W	T_{amb} = 25°C	PRQ-933
Thermal Resistance Junction to Case (top)	$R_{THJCTOP}$	–	52	–	K/W	T_{amb} = 25°C	PRQ-934
Thermal Resistance Junction to Board (25°C)	$R_{THJBOARD}$	–	45.4	–	K/W	T_{amb} = 25°C, power losses on secondary side ≤ 500 mW, power losses on primary side ≤ 50 mW	PRQ-1031

(table continues...)

Table 4 (continued) Thermal characteristics parameters

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Ψ - Pseudo Thermal Resistance Junction to Case (top)	R_{PSIJT}	–	21	–	K/W	T_{amb} = 25°C	PRQ-935

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.*

3.4 Insulation characteristics

Table 5 Insulation characteristics for reinforced insulation in compliance with DIN EN IEC 60747-17 (VDE 0884-17):2021-10

Description	Symbol	Characteristic	Unit
Installation classification per IEC 60664-1, Table F.1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-IV I-III I-II	–
Climatic classification	–	40/125/21	–
Pollution degree (IEC 60664-1)	–	2	–
Minimum external clearance	CLR	> 8	mm
Minimum external creepage	CPG	> 8	mm
Minimum comparative tracking index	CTI	> 400	–
Maximum rated repetitive peak isolation voltage	V_{IORM}	1767	V_{peak}
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{peak}
Maximum impulse voltage, tested in air	V_{IMP}	8000	V_{peak}
Maximum surge isolation voltage for reinforced insulation, tested in oil Test voltage in subgroup #1 = 11 kV ≥ 1.3 x V_{IMP}, min. 10 kV	V_{IOSM}	11000	V_{peak}
Input to output test voltage, method b1) $V_{ini,b}$ = 1.2 x V_{IOTM}, $V_{pd(m)} \geq V_{IORM}$ x 1.875, 100% production test, $t_{ini,b} = t_m$ = 1 s	q_{PD}	< 5	pC
Input to output test voltage, method a) $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)} \geq V_{IORM}$ x 1.6 , sample test, t_{ini} = 60 s, t_m = 60 s	q_{PD}	< 5	pC

(table continues...)

Table 5 (continued) Insulation characteristics for reinforced insulation in compliance with DIN EN IEC 60747-17 (VDE 0884-17):2021-10

Description	Symbol	Characteristic	Unit
Isolation resistance at 25 °C ≤ T_{amb} ≤ 125 °C, V_{io} = 500 V	R_{IO}	> 10^{12}	Ω
Isolation resistance at T_S = 150°C, V_{io} = 500 V	R_{IO}	> 10^9	Ω

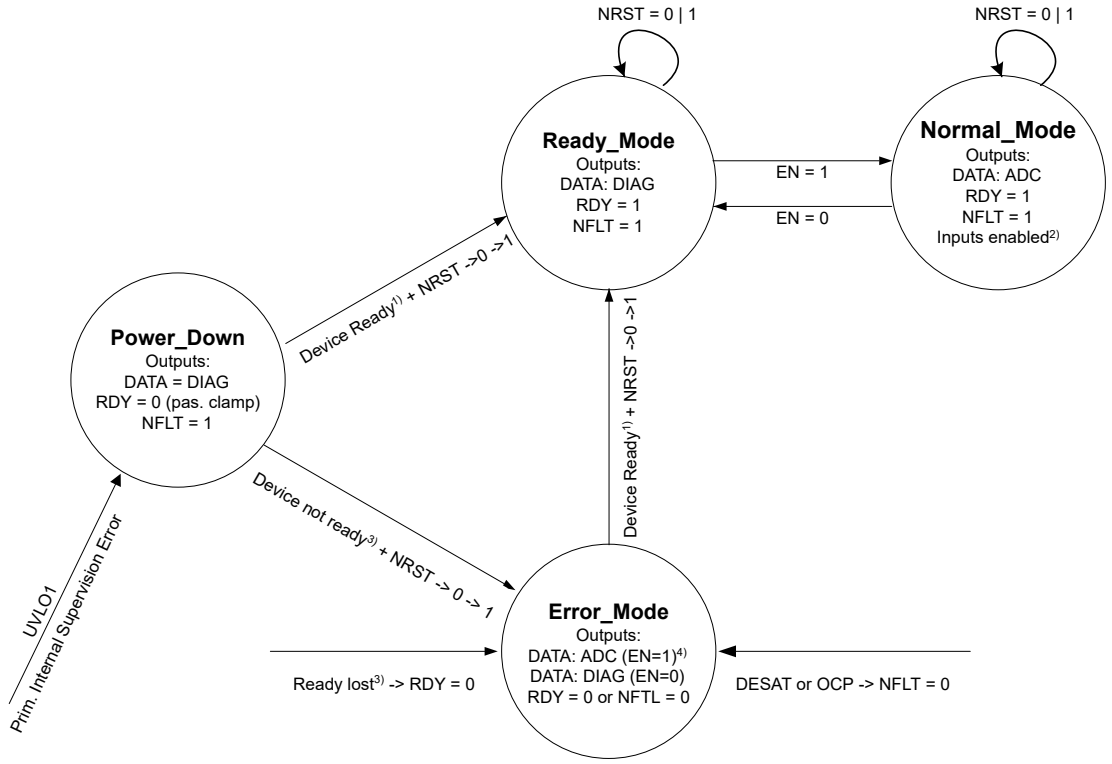
Table 6 Insulation characteristics recognized according to UL 1577

Parameter	Symbol	Characteristic	Unit
Insulation withstand voltage / 1 min	V_{ISO}	5700	V (rms)
Insulation test voltage / 1 s	V_{ISO}	6000	V (rms)

***Note**: The insulation characteristics only apply when the device is operated within the safety limits given by the absolute maximum ratings.*

4 Operating modes

4.1 Operating modes diagram



1) Device ready: no OSM Error, no Gate Monitoring Error, no OVLO2, no UVLO2, no open pin at OCPx, no Prim. or Sec. Internal Supervision Error, OTP read ok

2) INP & INN are enabled

3) Device not ready: OSM Error, Gate Monitoring Error, OVLO2, UVLO2, OCPx open pin, Sec. Internal Supervision Error, OTP read error

4) At life sign loss ADC signal at DATA pin output is static 0

Figure 4 Operating modes state diagram

***Note**:*
- *Life sign lost will be detected only if communication has been established once.*
- *External pull-up required on RDY and NFLT (open drain output)*

4.2 Operating modes description

The device has the following modes which it can operate in:
- Ready_Mode (not enabled)
- Error_Mode (Failure/Fault event occurred)
- Normal_Mode (Device enabled)

Reset

If the NRST signal is low the device keeps its operating mode (no influence on PWM). Further the rising edge on NRST signal will reset the failure/fault event memory.

Power Down and Start up

The device is in Power_Down_Mode at start-up or if an UVLO1 error occurs. In both cases it will not operate. If the device is partly supplied (e.g. VCC1 only) the device will enter Error_Mode. Therefore supplies should rise within the specified slew rates to a valid voltage level according to given operating conditions. Afterwards a rising edge on NRST will bring the device into Ready_Mode (no Failure or Fault Event occurred).

Mode Transitions

Once in Ready_Mode the change to Normal_Mode can be done with setting EN signal to "high level" (voltage level differs with VCC1 level), changing it to "low level" is also the returning into Ready_Mode. The transition into Error_Mode can only be done with the according events which are:

- OCP event
- DESAT event
- UVLO2 event
- OVLO2 event
- Sec. Internal Supervision Error
- Output Stage Monitor Error
- Gate Monitoring Error
- OCPx pin open
- OTP read error

Error_Mode

In Error_Mode a "low level" on signal EN will issue diagnosis information on the DATA pin. This diagnosis information states details about the failure root cause. A "high level" on signal EN issues the ADC information, identical to Normal_Mode.

A rising edge on NRST and no failure or fault active will transition the device back to Ready_Mode (or to Normal_Mode if signal EN is set). In Ready_Mode diagnosis information is available on the DATA pin. See also the operating modes diagram for further information.

4.3 Single failure events in Normal_Mode

Table 7 Single failure events in Normal_Mode

Failure Event	Output stage reaction	Resulting pin status changes
DESAT when TOUT = high (VCC2)	Safe turn-off	NFLT = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OCP when TOUT = high (VCC2)	Safe turn-off	NFLT = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
Gate monitoring error	Safe turn-off when TOUT = high (VCC2)	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OSM error	Tri-state	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
UVLO2	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OVLO2	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
UVLO1	Normal switch-off	RDY = 0; DATA = 0
Prim. internal supervision error	Normal switch-off	RDY = 0; DATA = 0
Sec. internal supervision error	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)
OCPx pin open	Normal switch-off	RDY = 0; DATA: ADC (EN = 1), DATA: DIAG (EN = 0)

5 Power supply

5.1 Bipolar and unipolar supplies

The device is designed to support two different supply configurations, bipolar supply and unipolar supply.

***Note**: In bipolar supply the driver is typically supplied with a positive voltage of 15 V at VCC2 and a negative voltage of -5 V at VEE2 (referenced to GND2). The negative supply prevents a dynamic turn on due to the additional charge which is generated from the input capacitance current of the power switch times the negative supply voltage. GATE/CLAMP has to be connected to the gate of the power switch in all power supply configurations.*

5.2 Electrical characteristics power supply

Table 8 Electrical characteristics power supply

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Quiescent Current Input Chip (VCC1)	I_{QVCC1}	3	5	–	mA	Ready_Mode, all primary I/Os without impact on Ready_Mode open, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-937
Operating Current VCC1 (TOUT = high (VCC2))	I_{QPVCC1_ON}	–	10	12.7	mA	Normal_Mode, INN = 0, INP = 1, EN = 1, NRST = 1, outputs open,V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-938
Operating Current VCC1 (TOUT = low (VEE2))	I_{OPVCC1_OFF}	–	5.5	7	mA	Normal_Mode, INN = 0, INP = 0, EN = 1, NRST = 1, outputs open, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-939
Operating Current VCC2 (TOUT = high (VCC2))	I_{OPVCC2_ON}	–	11	13	mA	Normal_Mode, INN = 0, INP = 1, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other pins open	PRQ-1036
Operating Current VCC2 (TOUT = low (VEE2))	I_{OPVCC2_OFF}	6	11	13	mA	Normal_Mode, INN = 0, INP = 0, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other pins open	PRQ-1037
Operating Current VEE2 (TOUT = high (VCC2))	I_{OPVEE2_ON}	–	1.5	2	mA	Normal_Mode, INN = 0, INP = 1, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other pins open	PRQ-944

(table continues...)

Table 8 (continued) Electrical characteristics power supply

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Operating Current VEE2 (TOUT = low (VEE2))	I_{OPVEE2_OFF}	0.5	1.5	2	mA	Normal_Mode, INN = 0, INP = 0, EN = 1, NRST = 1, primary outputs open, OCPx = 0, DESAT = 0, Gate shorted to TOUT, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other pins open	PRQ-945

6 Switching characteristics

6.1 Functional description switching

The voltage on pin TOUT ranges from V_{VEE2} to V_{VCC2} (referenced to GND2).

The device supports short propagation delay for On and Off switching of t_{PDON} and t_{PDOFF}.

6.2 Electrical characteristics switching

Table 9 Electrical characteristics switching

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High level output peak current	I_{OUTH}			- 12	A	INP = V_{VCC1}, INN = V_{GND1}, EN = V_{VCC1}, TOUT = V_{VCC2}, CLAMP/GATE = V_{VEE2}, V_{VCC2} = 15 V, V_{VEE2} = -5 V, C_{LOAD}= 200 nF	PRQ-662
Low level output peak current	I_{OUTL}	12			A	INP = V_{GND1}, INN = V_{GND1}, EN = V_{VCC1}, TOUT = V_{VEE2}, CLAMP/GATE = V_{VCC2}, V_{VCC2} = 15 V, V_{VEE2} = -5 V, C_{LOAD}= 200 nF	PRQ-663
Propagation delay - On	t_{PDON}	40	60	120	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TOUT rising edge at V_{VEE2} + 1.5 V, no load, no gate resistance	PRQ-770
Propagation delay - Off	t_{PDOFF}	40	60	120	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP falling edge at $V_{digital,input(low)}$, Stop: TOUT falling edge at V_{VCC2} - 1.5 V, no load, no gate resistance	PRQ-851
Propagation delay distortion	$t_{Prop,dis}$	-20	–	20	ns	t_{PDON} - t_{PDOFF}, t_{PDON} & t_{PDOFF} measured @ same T_{JUNC}	PRQ-803
Propagation delay EN to turn-on (INP = high)	t_{PDENON}	10	60	120	ns	V_{VCC1} = typ.; V_{VCC2} = typ., V_{VEE2} = typ., INP = high, INN = GND1, TOUT = V_{VEE2} + 1.5 V, referring to VEE2 (rising edge)	PRQ-968
Propagation delay EN to turn-off (INP = high)	$t_{PDENOFF}$	10	60	120	ns	V_{VCC1} = typ., V_{VCC2} = typ., V_{VEE2} = typ., INP = high, INN = GND1, TOUT = V_{VCC2} - 1.5 V referring to VEE2 (falling edge)	PRQ-967
TOUT rise time 90 %	t_{Rise1}	–	–	55	ns	no C_{LOAD}, no R_{LOAD}, V_{VCC2} = typ., V_{VEE2} = typ. V_{TOUT} = V_{VEE2} + 1.5 V to V_{TOUT} = V_{VCC2} - 1.5 V	PRQ-801
TOUT rise time 70 %	t_{Rise2}	–	–	35	ns	no C_{LOAD}, no R_{LOAD}, V_{VCC2} = typ., V_{VEE2} = typ., V_{TOUT} = V_{VEE2} + 1.5 V to V_{TOUT} = V_{VCC2} - 6 V	PRQ-958

(table continues...)

Table 9 (continued) Electrical characteristics switching

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fall time	t_{Fall}	–	–	45	ns	No C_{LOAD}, no R_{LOAD}, V_{VCC2} = typ., V_{VEE2} = typ., V_{TOUT} = V_{VCC2} - 1.5 V to V_{TOUT} = V_{VEE2} + 1.5 V	PRQ-802
TOUT RDSON High-side	$R_{DSON-OSHN}$		0.30		Ω	N-MOS, tolerances according to $R_{DSON-OSLN}$	PRQ-1032
TOUT RDSON High-side P&N	$R_{DSON-OSHtot}$	0.3	–	1	Ω	N-MOS and P-MOS, voltage drop V_{VCC2} - V_{TOUT} < 1 V	PRQ-849
TOUT RDSON Low-side	$R_{DSON-OSLN}$	0.07	–	0.35	Ω	N-MOS, voltage drop V_{TOUT} - V_{VEE2} < 1 V	PRQ-850

***Note**: The defined minimum/maximum value of I_{OUTx} is the minimum current which the device delivers under the given conditions. In general the device is capable to delives higher output currents than the defined minimum/maximum. The maximum output current needs to be limited by an external gate resistor to stay inside the defined absolute maximum rating parameters regarding maximum peak current (equivalent energy needs to be considered) and maximum junction temperature.*

7 Protection and monitoring functions

7.1 DESAT protection

7.1.1 Functional description DESAT protection

The device monitors the voltage across the power switch when TOUT = high(VCC2), after the DESAT blanking time is elapsed. If the corresponding reference level (V_{DESATx}) is reached, it issues a safe turn-off within $t_{DESAT2OFF}$, then changes into Error_Mode and signals a NFLT low in t_{NFLT_DESAT}.

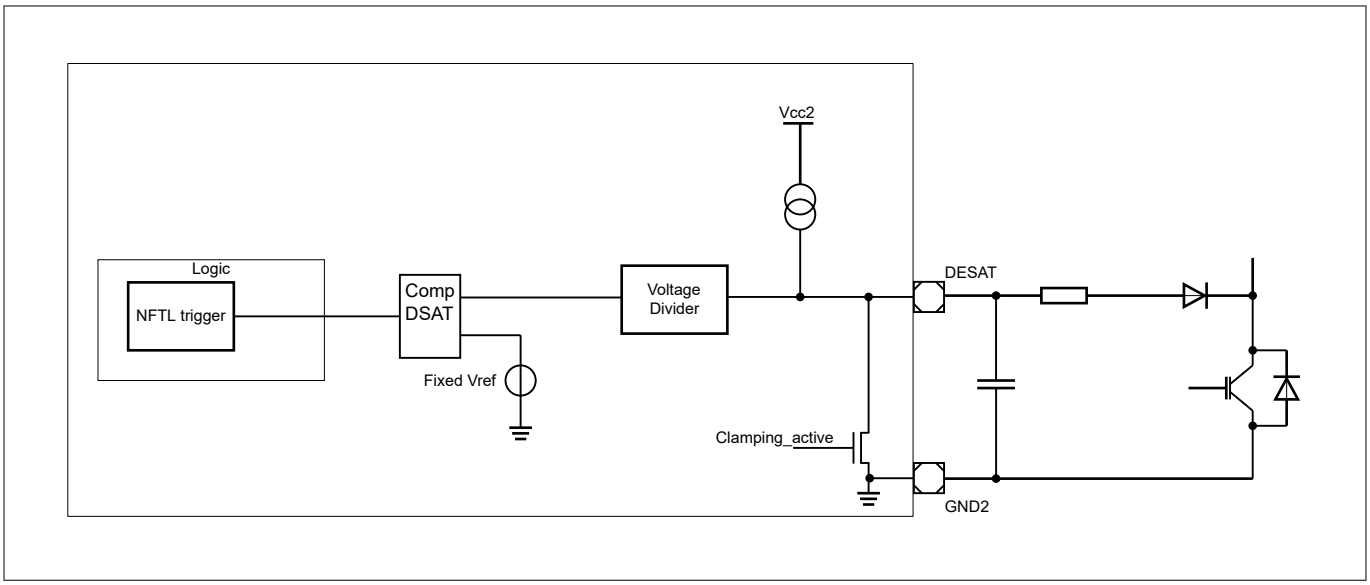


Figure 5 DESAT diagram of principal functionality

The DESAT pin has an internal clamping which clamps DESAT to V_{DESATL} in case TOUT = low (VEE2), TOUT = $V_{SOffPLT}$ or in case of OSM (tristate).

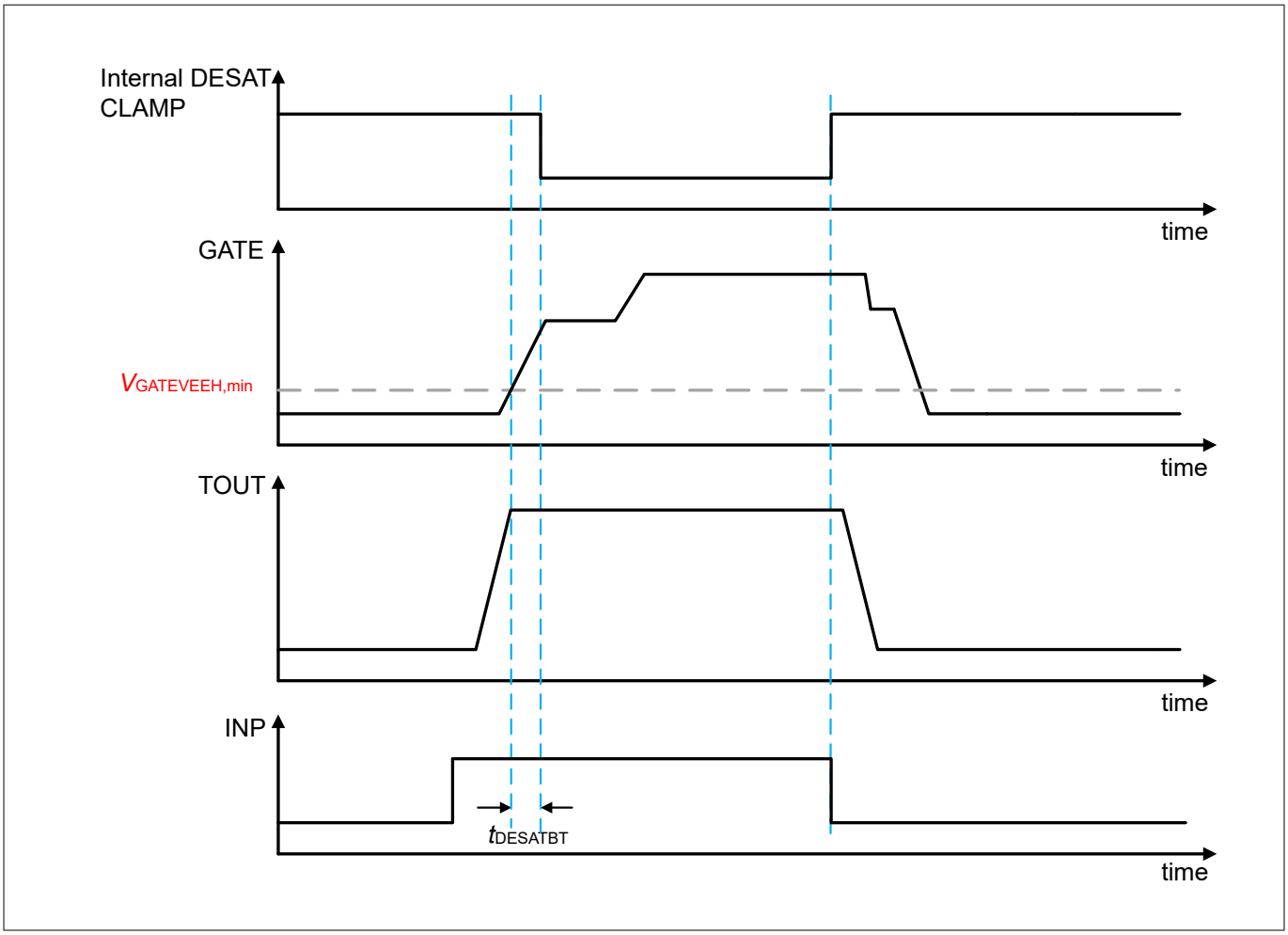


Figure 6 DESAT clamping and blanking timing diagram

7.1.2 Electrical characteristics DESAT protection

Table 10 Electrical characteristics DESAT protection

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT reference level	V_{DESAT0}	8.6	9	9.3	V	VCC2 = typ., VEE2 = typ.	PRQ-734
DESAT current source	$I_{DESATCS}$	-550	-500	-450	µA	V_{VCC2} = typ., V_{VEE2} = typ., V_{DESAT} ≤ 10 V	PRQ-800
DESAT low voltage	V_{DESATL}	0	200	300	mV	Referenced to GND2, DESAT clamping enabled, I_{sink} = 5 mA	PRQ-693

(table continues...)

Table 10 (continued) Electrical characteristics DESAT protection

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DESAT detection & reaction time	$t_{DESAT2OFF}$	100	300	400	ns	$V_{DESAT\_Overdrive}$= 2 V, Slew rate @ DESAT = 10 V/µs; TOUT = V_{VCC2} - 1.5 V, after DESAT blanking time elapsed, C_{LOAD_TOUT} = no load, no resistive load	PRQ-841
DESAT blanking time	$t_{DESATBT}$	120	320	400	ns	From $V_{GATEVEEH}$ to release of clamping (Desat pin voltage rising above 0.5 V, with internal current source, no external C_{DESAT}), no C_{Load}/R_{Load} on TOUT	PRQ-969
DESAT input voltage range	V_{DESAT}	0	–	V_{VCC2}	V	Referenced to GND2	PRQ-690

7.2 Over Current Protection (OCP)

7.2.1 Functional description OCP protection

The device monitors the voltage difference between OCPP and OCPN when TOUT = high (VCC2) after the OCP blanking time is elapsed. If the corresponding reference level (V_{OCPDx}) is reached, it issues a safe turn-off within $t_{OCP2OFF}$, then changes into Error_Mode and signals a NFLT low in t_{NFLT_OCP}.

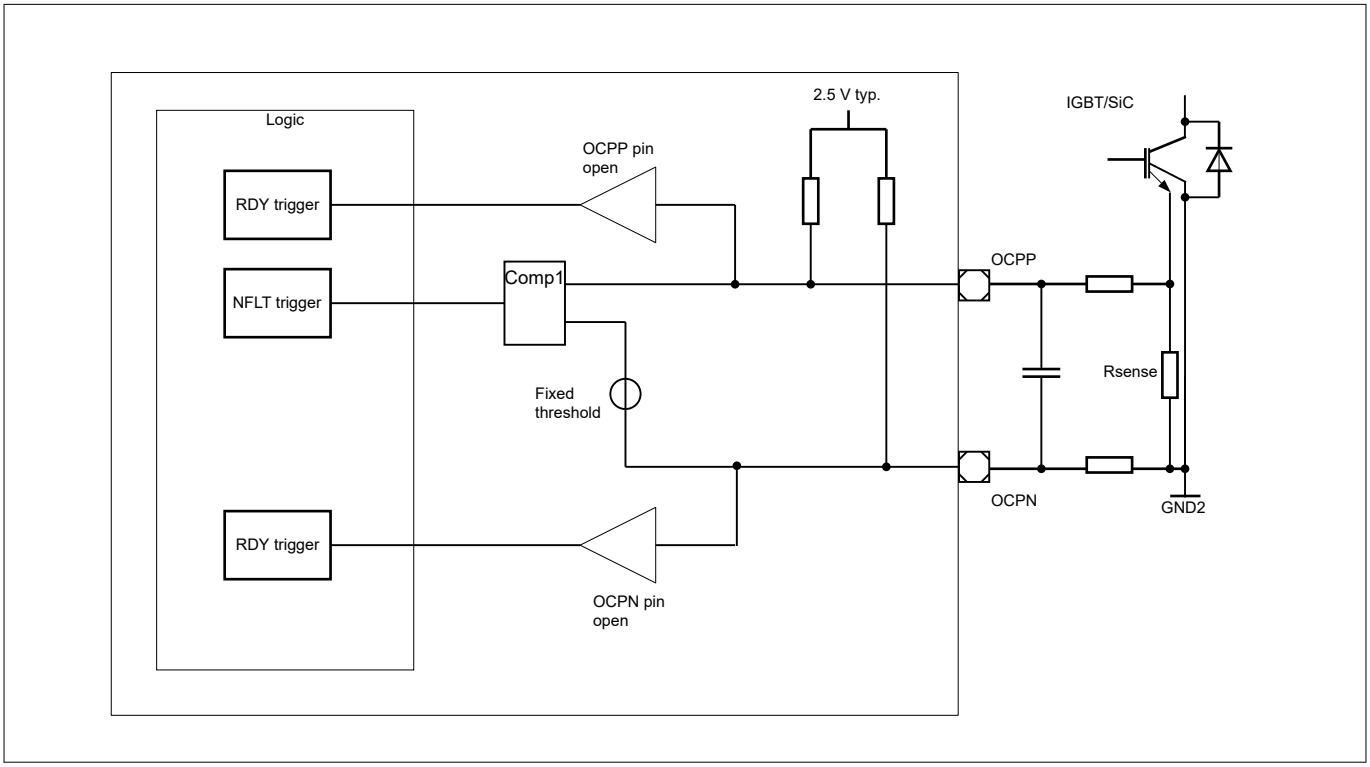


Figure 7 OCP diagram of principal functionality

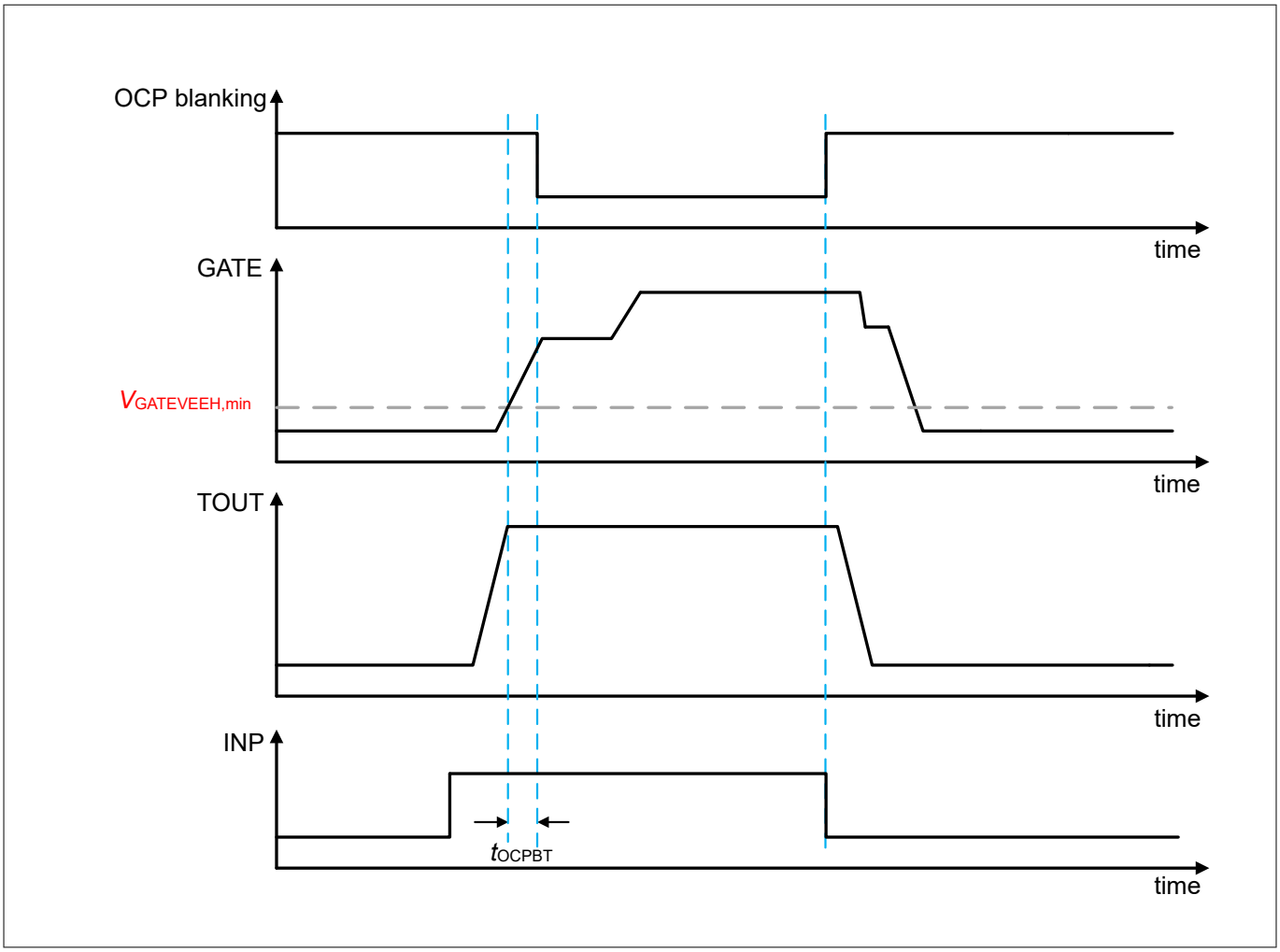


Figure 8 OCP blanking time

7.2.2 Electrical characteristics OCP protection

Table 11 Electrical characteristics OCP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent error detection threshold	V_{OCPD1}	270	300	330	mV	V_{OCPP} - V_{OCPN}	PRQ-695
OCPP & OCPN pull-up resistance	R_{PUOCP2}	26	38	50	kΩ		PRQ-697
OCPP & OCPN voltage	V_{OCP}	-1	–	1	V	referring to GND2	PRQ-793

(table continues...)

Table 11 (continued) Electrical characteristics OCP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP detection & reaction time	$t_{OCP2OFF}$	100	300	400	ns	$V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns, TOUT = V_{VCC2} - 1.5 V, after OCP blanking time elapsed, C_{LOAD_TOUT} = no load, no resistive load	PRQ-842
OCP blanking time	t_{OCPBT}	120	320	400	ns	From $V_{GATEVEEH}$ to release of blanking. $V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns, no C_{Load}/R_{Load} on TOUT	PRQ-1014
OCP pin open detection voltage	$V_{OCPOPEN}$	2.2	2.45	2.6	V		PRQ-1030

7.3 Safe turn-off

7.3.1 Functional description safe turn-off

The device enables a two-level turn-off in case of a fault.

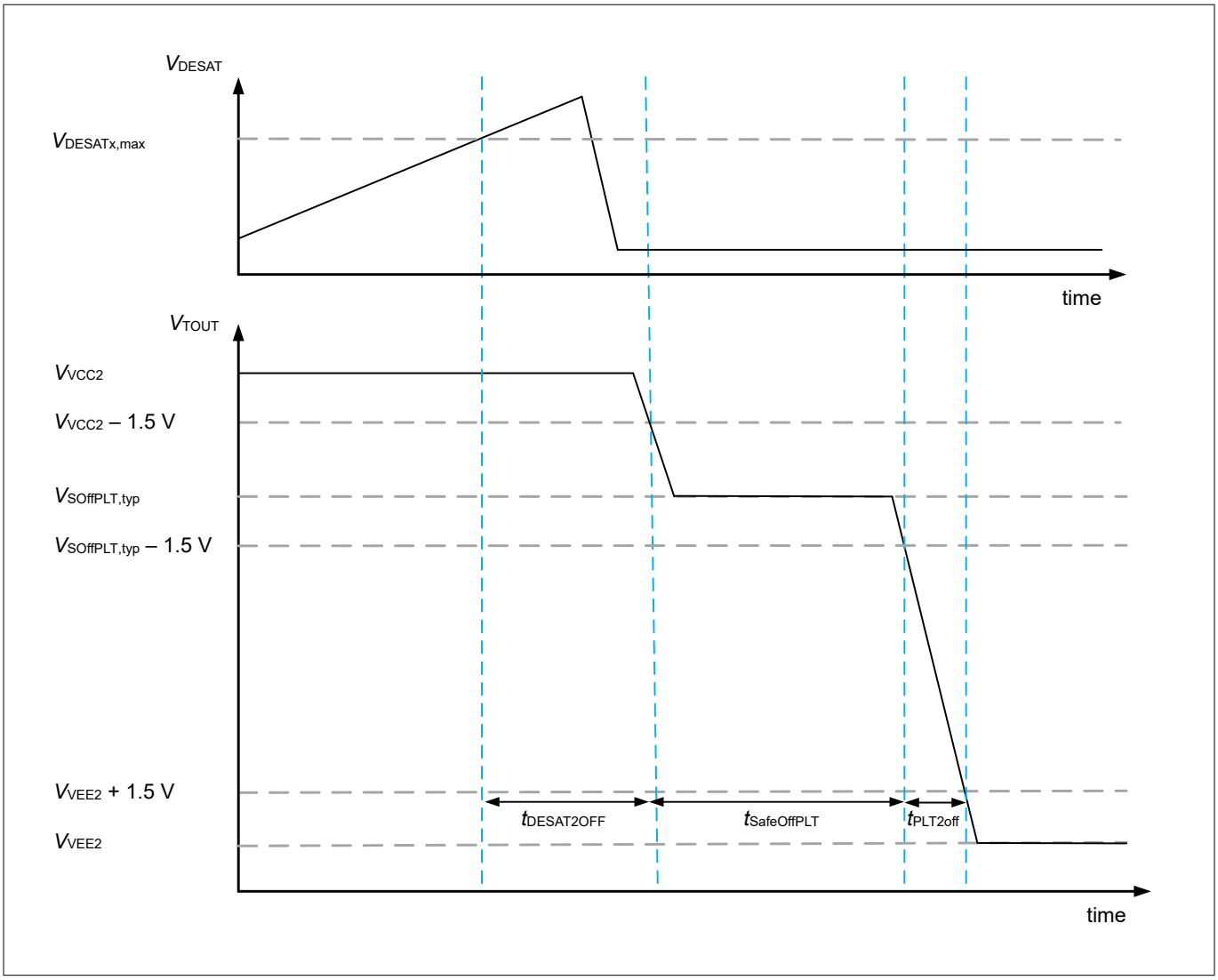


Figure 9 **Two level turn-off principle for safe turn-off**

Note:
- *Safe turn-off is only enabled at DESAT, OCP and gate monitoring error (if TOUT = high (VCC2) events.*
- *DESAT is only used as an example, can be replaced by OCP and gate monitoring.*

7.3.2 Electrical characteristics safe turn-off

Table 12 **Electrical characteristics safe turn-off**

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Safe turn-off plateau time	$t_{SafeOffPLT}$	1	–	1.5	µs		PRQ-918
Plateau to turn-off time	$t_{PLT2Off}$	10	–	50	ns	No R_{Load}, no C_{Load}	PRQ-973

(table continues...)

Table 12 (continued) Electrical characteristics safe turn-off

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Safe turn-off plateau voltage level	$V_{SOffPLT}$	8.46	9	9.54	V	$V_{VCC2} \geq V_{SOffPLT,max}$ + 2 V, C_{LOAD_TOUT} = 68 nF, R_{LOAD_TOUT} = 1.7 Ω	PRQ-919

7.4 Shoot Through Protection (STP)

7.4.1 Functional description STP

The device has a Shoot Through Protection (STP) function to prevent both high-side and low-side switches to be activated simultaneously.

***Note**: STP is always active. However, setting the INN pin to GND1 deactivates the function.*

If one of the drivers is in ON state, the driver's counterpart PWM input is inhibited, preventing it to turn on.

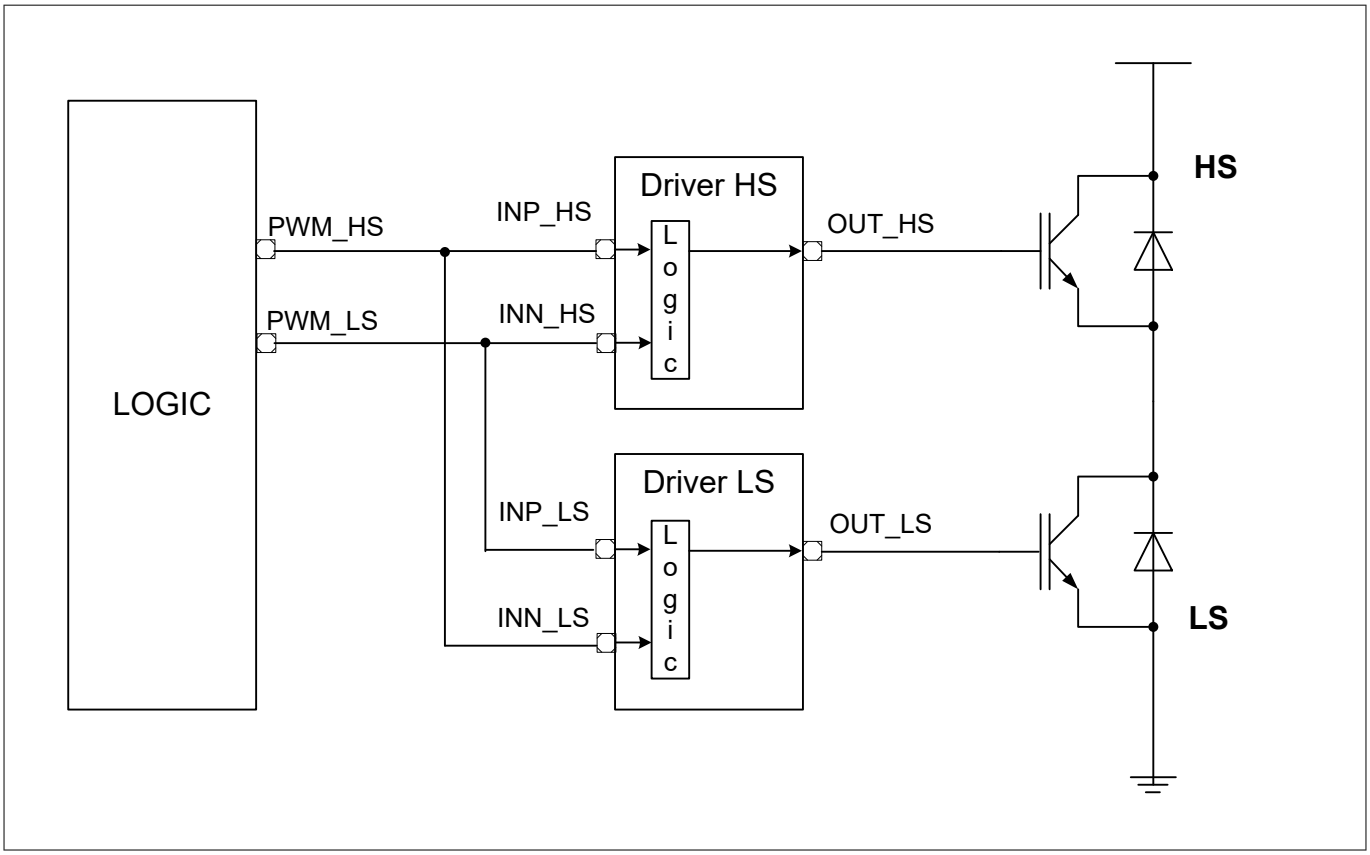


Figure 10 Shoot through protection application diagram

The device follows the shoot through protection timing diagram shown below:

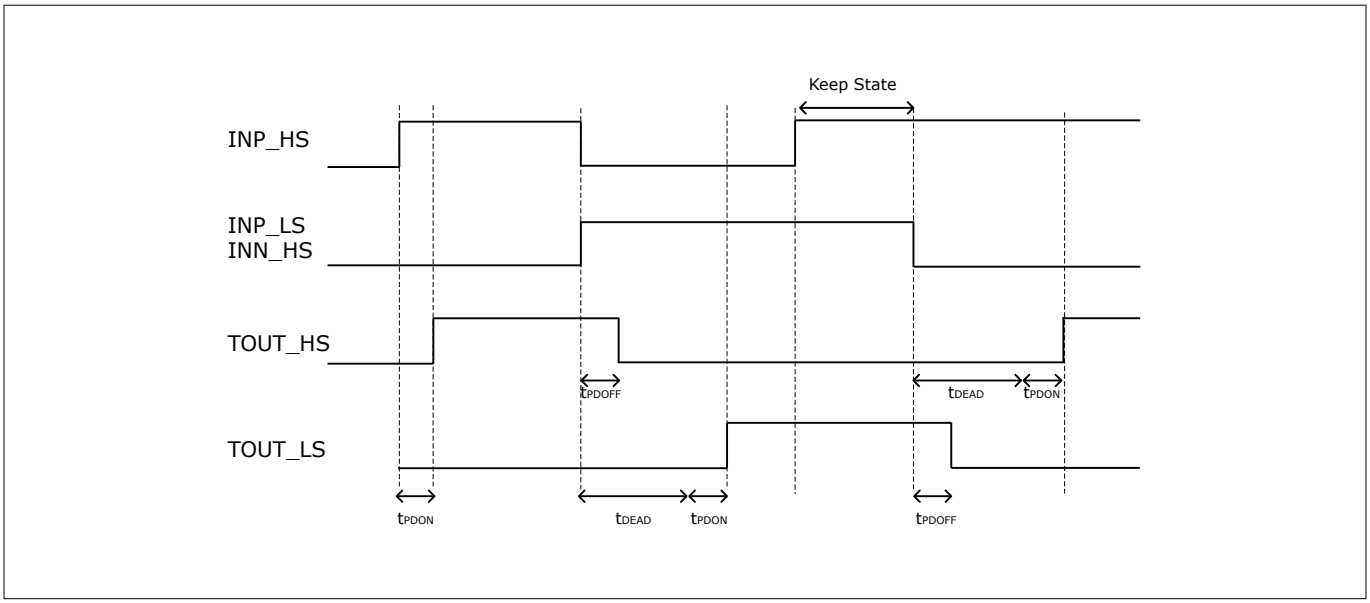


Figure 11 Shoot through protection timing diagram

7.4.2 Electrical characteristics STP

Table 13 Electrical characteristics STP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Dead time for shoot through protection	t_{DEAD3}	650	800	950	ns		PRQ-729

7.5 Power supply monitoring

7.5.1 Functional description power supply monitoring

The device is equipped with an undervoltage lockout for the primary supply (VCC1) and secondary supply (VCC2) in order to ensure correct switching of the power switch.

***Note**: In all under voltage conditions the ASC signal still works until the voltage drops below VASCOFF at VCC2.*

The device turns off the power switch and ignores signals at INP and INN (goes into Power_Down Mode) if the power supply VCC1 drops below V_{UVLO1L}. It returns to Ready_Mode if the voltage at VCC1 is above V_{UVLO1H} and the device received a rising edge at NRST.

The device turns off the power switch within $t_{UVLO22OFF}$ and ignores signals at INP and INN (go into Error_Mode) within t_{PS2RDY} if the power supply VCC2 drops below V_{UVLO2L_x}. It returns to Ready_Mode if the voltage at VCC2 is above V_{UVLO2H_x} and the device received a rising edge at NRST.

The device is equipped with an overvoltage lockout for the secondary supply VCC2 in order to prevent damage of the power switch.

***Note**: The ASC signal will overwrite the turn-off command, which may lead to damage of the power switch (power switch).*

The device turns off the power switch within $t_{OVLO22OFF}$ and ignores signals at INP and INN (go into Error_Mode) within t_{PS2RDY} if the power supply V_{VCC2} rises above V_{OVLO2H_x}. It returns to Ready_Mode if the voltage V_{VCC2} is below V_{OVLO2L_x} and the device received a rising edge at NRST.

***Note**:*
- *In Error_Mode, RDY changes to 0.*
- *Turn-off means normal switch-off and not a safe turn-off.*
- *Exception: ASC function → TOUT = high (VCC2).*

7.5.2 Electrical characteristics power supply monitoring

Table 14 Electrical characteristics power supply monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO1 threshold low	V_{UVLO1L}	2.6	2.75	–	V	@ VCC1, referenced to GND1	PRQ-741
UVLO1 threshold high	V_{UVLO1H}	–	2.85	2.95	V	@ VCC1, referenced to GND1	PRQ-740
UVLO1 hysteresis	$V_{UVLO1HYS}$	–	80	100	mV		PRQ-742
OVLO2 threshold high	V_{OVLO2H_3}	17.8	18.5	19.0	V	@ VCC2, referenced to GND2	PRQ-889
OVLO2 threshold low	V_{OVLO2L_3}	17.1	17.7	18.2	V	@ VCC2, referenced to GND2	PRQ-890
OVLO2 hysteresis	$V_{OVLO2HYS}$	400	800	–	mV	V_{OVLO2H_x} - V_{OVLO2L_x}	PRQ-896
UVLO2 threshold high	V_{UVLO2H_1}	12.2	12.6	13	V	@ VCC2, referenced to GND2	PRQ-750
UVLO2 threshold low	V_{UVLO2L_1}	11.4	11.8	12.2	V	@ VCC2, referenced to GND2	PRQ-752
UVLO2 hysteresis	$V_{UVLO2HYS}$	720	800	880	mV		PRQ-755
UVLO1 detection & reaction time	$t_{UVLO12OFF}$	–	500	800	ns	Slewrate = 2 V/µs, Overdrive = +/- 300 mV	PRQ-914

(table continues...)

Table 14 (continued) Electrical characteristics power supply monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UVLO2 detection & reaction time	$t_{UVLO22OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-915
OVLO2 detection & reaction time	$t_{OVLO22OFF}$	–	500	800	ns	Slewrate=10 V/µs; Overdrive=+/-200 mV	PRQ-916
Power supply monitoring detection and notification time	t_{PS2RDY}	–	–	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-976

7.6 Gate monitoring

7.6.1 Functional description gate monitoring

The device monitors in the time frame of t_{GMBT} (dynamic or static) the gate signal V_{GATE} at pin CLAMP/GATE to ensure the signal V_{TOUT} reaches the threshold value of V_{GATE} properly. If monitoring conditions are violated, the device issues a safe turn-off (if TOUT = high (VCC2) in less than $t_{GM\text{-}DaR}$ and changes to Error_Mode in less than t_{RDY_GM}.

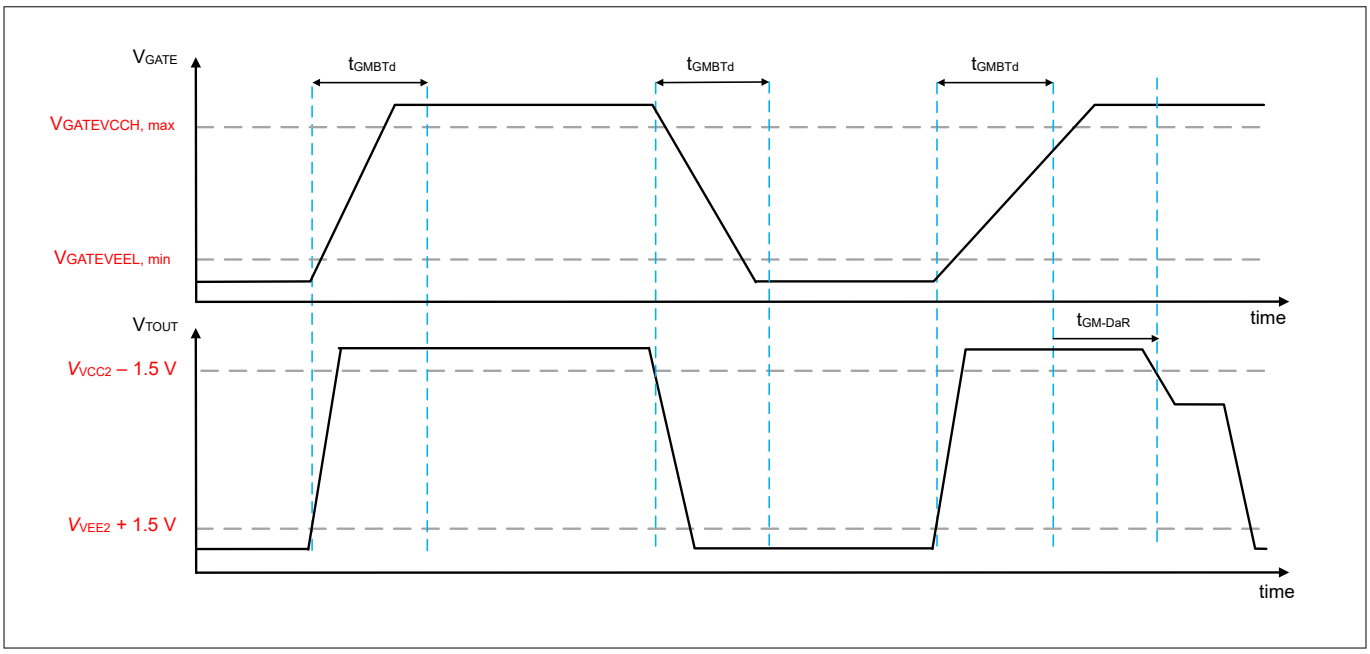


Figure 12 Dynamic gate monitoring timing diagram

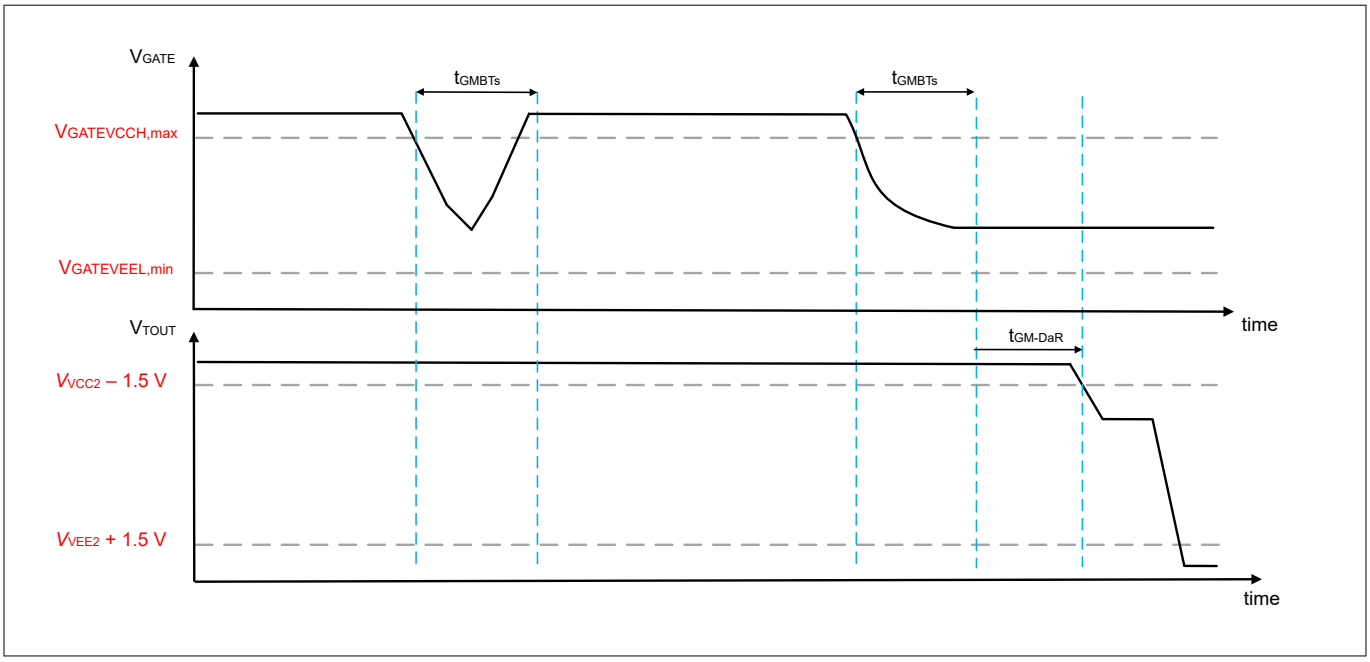


Figure 13 Static gate monitoring timing diagram

7.6.2 Electrical characteristics gate monitoring

Table 15 Electrical characteristics gate monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring detection and reaction time	t_{GM-DaR}	450	650	900	ns	VCC2 = typ., VEE2 = typ.	PRQ-853
Gate monitoring detection and notification time	t_{RDY_GM}	–	1.5	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-910
Dynamic gate monitoring blanking time	t_{GMBTd3}	6.99	7.6	8.21	µs	VEE2 = typ., VCC2 = typ.	PRQ-979
Static gate monitoring blanking time	t_{GMBTs3}	7.40	7.9	8.40	µs	VEE2 = typ., VCC2 = typ.	PRQ-983

(table continues...)

Table 15 (continued) Electrical characteristics gate monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring VCC2 voltage threshold high level	$V_{GATEVCCH}$	V_{VCC2} - 2.3	V_{VCC2} - 2.1	V_{VCC2} - 1.9	V	t_{GMBT} is active	PRQ-855
Gate monitoring VCC2 voltage threshold low level	$V_{GATEVCCL}$	V_{VCC2} - 3.2	V_{VCC2} - 3	V_{VCC2} - 2.8	V	t_{GMBT} is active	PRQ-962
Gate monitoring VEE2 voltage threshold high level	$V_{GATEVEEH}$	V_{VEE2} + 2.8	V_{VEE2} + 3	V_{VEE2} + 3.2	V	t_{GMBT} is active	PRQ-963
Gate monitoring VEE2 voltage threshold low level	$V_{GATEVEEL}$	V_{VEE2} + 1.9	V_{VEE2} + 2.1	V_{VEE2} + 2.3	V	t_{GMBT} is active	PRQ-856

7.7 Output stage monitoring

7.7.1 Functional description output stage monitoring

The output stage monitoring checks whether the internal output signal is according to the given PWM or ASC input signal in the time frame of $t_{OUTMBTx}$, otherwise the device issues a tri-state for the output stage in less than $t_{OUTM\text{-}DaR}$ and changes to Error_Mode in less than t_{RDY_OSM}.

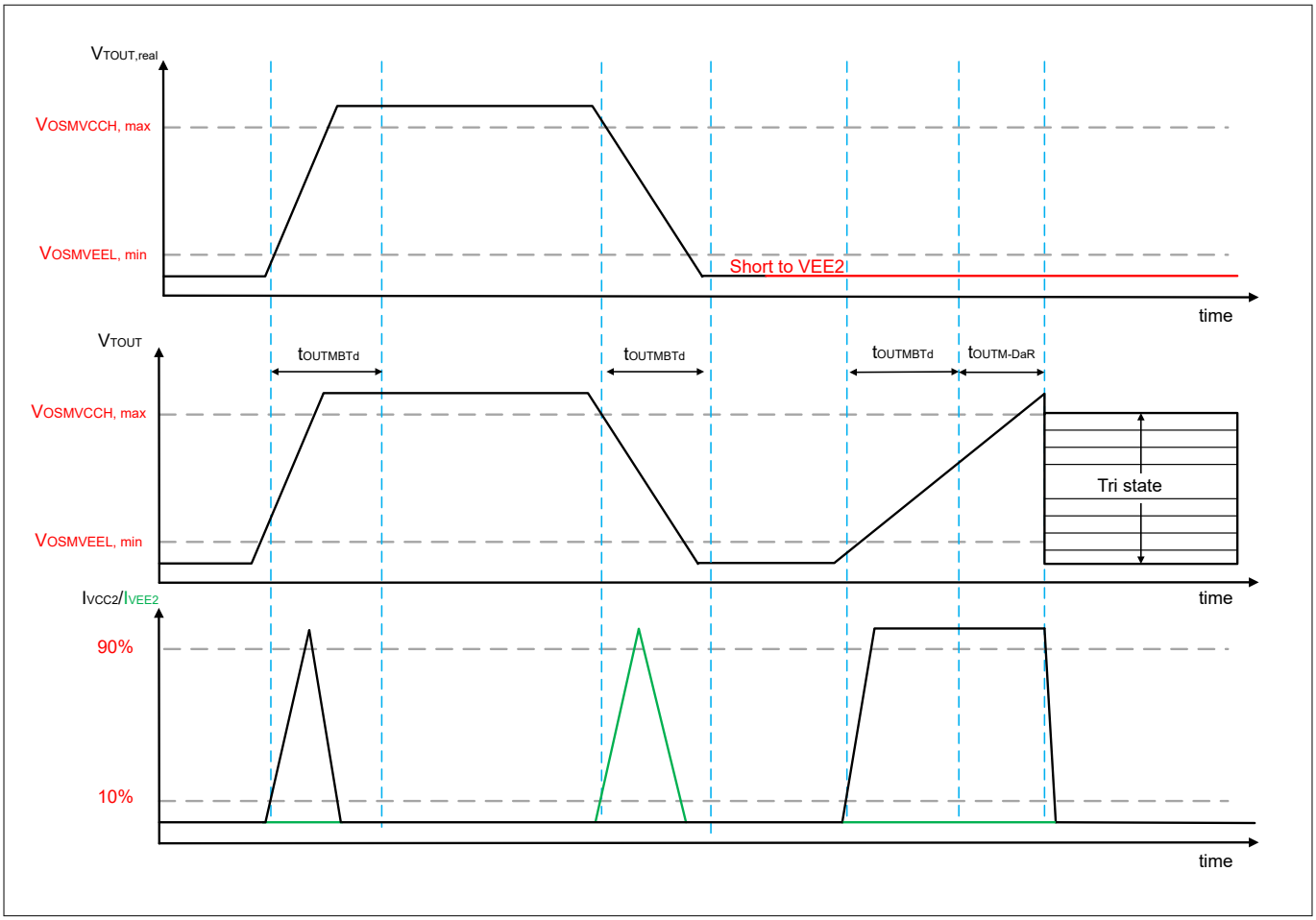


Figure 14 Dynamic output stage monitoring working principle

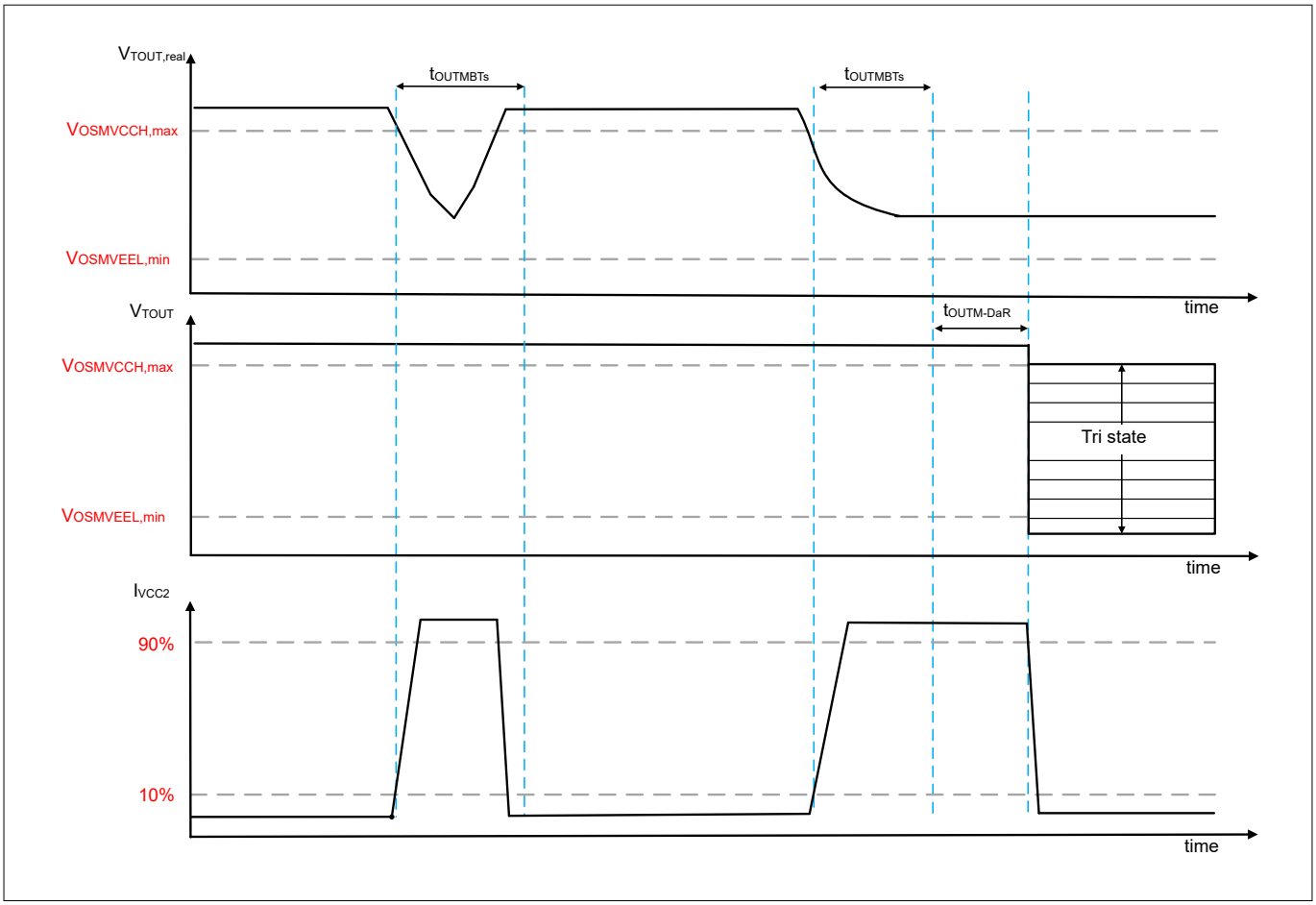


Figure 15 Static output stage monitoring working principle

***Note**: The passive clamping at TOUT is working.*

7.7.2 Electrical characteristics output stage monitoring

Table 16 Electrical characteristics output stage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output stage monitoring detection and reaction time	$t_{OUTM-DaR}$	200	350	500	ns	VCC2 = typ., VEE2 = typ.	PRQ-859

(table continues...)

Table 16 (continued) Electrical characteristics output stage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output stage monitoring detection and notification time	t_{RDY_OSM}	–	1.5	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-964
Dynamic output stage monitoring blanking time	$t_{OUTMBTd3}$	600	800	1000	ns	VEE2 = typ., VCC2 = typ.	PRQ-922
Static output stage monitoring blanking time	$t_{OUTMBTs3}$	1000	–	1200	ns	VEE2 = typ., VCC2 = typ.	PRQ-925
Output stage monitoring VCC2 voltage threshold high level	$V_{OSMVCCH}$	V_{VCC2} - 2.3	V_{VCC2} - 2.1	V_{VCC2} - 1.9	V	t_{OUTBT} is active	PRQ-863
Output stage monitoring VCC2 voltage threshold low level	$V_{OSMVCCL}$	V_{VCC2} - 3.2	V_{VCC2} - 3	V_{VCC2} - 2.8	V	t_{OUTBT} is active	PRQ-965
Output stage monitoring VEE2 voltage threshold high level	$V_{OSMVEEH}$	V_{VEE2} + 2.8	V_{VEE2} + 3	V_{VEE2} + 3.2	V	t_{OUTBT} is active	PRQ-966
Output stage monitoring VEE2 voltage threshold low level	$V_{OSMVEEL}$	V_{VEE2} + 1.9	V_{VEE2} + 2.1	V_{VEE2} + 2.3	V	t_{OUTBT} is active	PRQ-864

8 Clamping functions

8.1 Active Miller clamp

8.1.1 Functional description Active Miller clamp

The clamp output is activated if the gate voltage V_{GATE} goes below $V_{GATEVEEL}$ during turn-off.

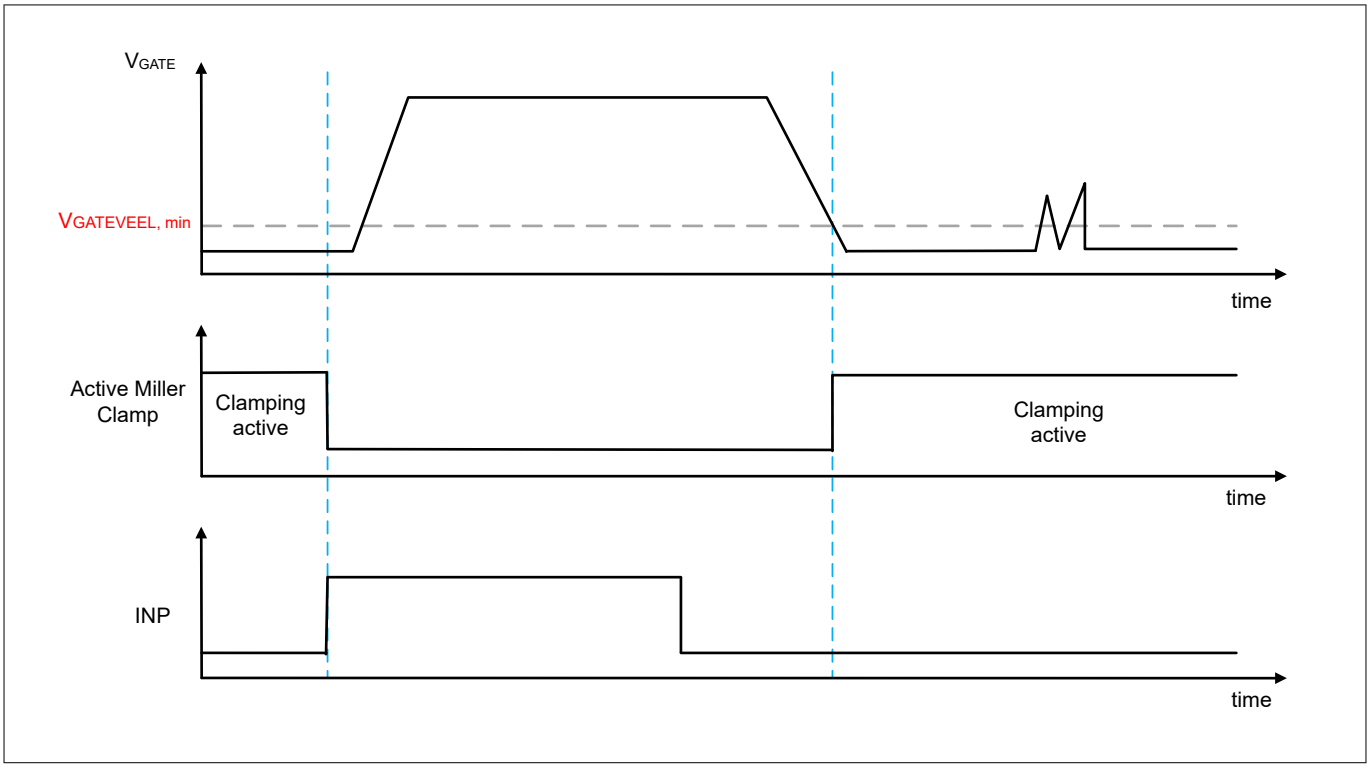


Figure 16 Active Miller clamp timing diagram

***Note**: In a half bridge configuration the switched off power switch tends to dynamically turn on during the turn on phase of the opposite power switch. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore, in many applications the use of a negative supply voltage can be avoided.*

8.1.2 Electrical characteristics Active Miller clamp

Table 17 Electrical characteristics Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level clamp peak current	I_{CLAMPL}	9.5	10		A	TOUT = low (V_{VEE2}), CLAMP/GATE = V_{CLAMP}, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-667

(table continues...)

Table 17 (continued) Electrical characteristics Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CLAMP/GATE voltage	$V_{CLAMP/GATE}$	V_{VEE2}	–	V_{VCC2}	V	Referenced to GND2, no load	PRQ-586
CLAMP RDSON	$R_{DSON-CLAMP}$	0.08	–	0.35	Ω	Voltage drop V_{VCC2} - V_{TOUT} < 1 V	PRQ-852

8.2 Passive clamping

8.2.1 Functional description passive clamping

If the secondary chip is not supplied, the pin GATE/CLAMP is passively clamped to VEE2.

8.2.2 Electrical characteristics passive clamping

Table 18 Electrical characteristics passive clamping

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GATE passive clamping voltage (ICLAMP = 10 mA)	V_{PCLPG1}	–	–	V_{VEE2} + 2 V	V	Secondary chip not supplied (VCC2 floating, VEE2 = 0 V), I_{Clamp} = 10 mA	PRQ-738
GATE passive clamping voltage (ICLAMP = 100 mA)	V_{PCLPG2}	–	–	V_{VEE2} + 2.2 V	V	Secondary chip not supplied (VCC2 floating, VEE2 = 0 V), I_{Clamp} = 100 mA	PRQ-882

9 Analog-to-Digital Converter (ADC)

9.1 Functional description ADC

The device has an ADC to measure the DC-link voltage.

The integrated ADC allows the measurement of the DC-link voltage. The internal current source $I_{ADC,ref}$ is deactivated. The voltage signal V_{AIP} is encoded to a PWM signal that is passed through the isolation to DATA pin on the primary side. The Total Unadjusted Error is the square sum of errors (INL, ER_{OFF} and ER_{GAIN}).

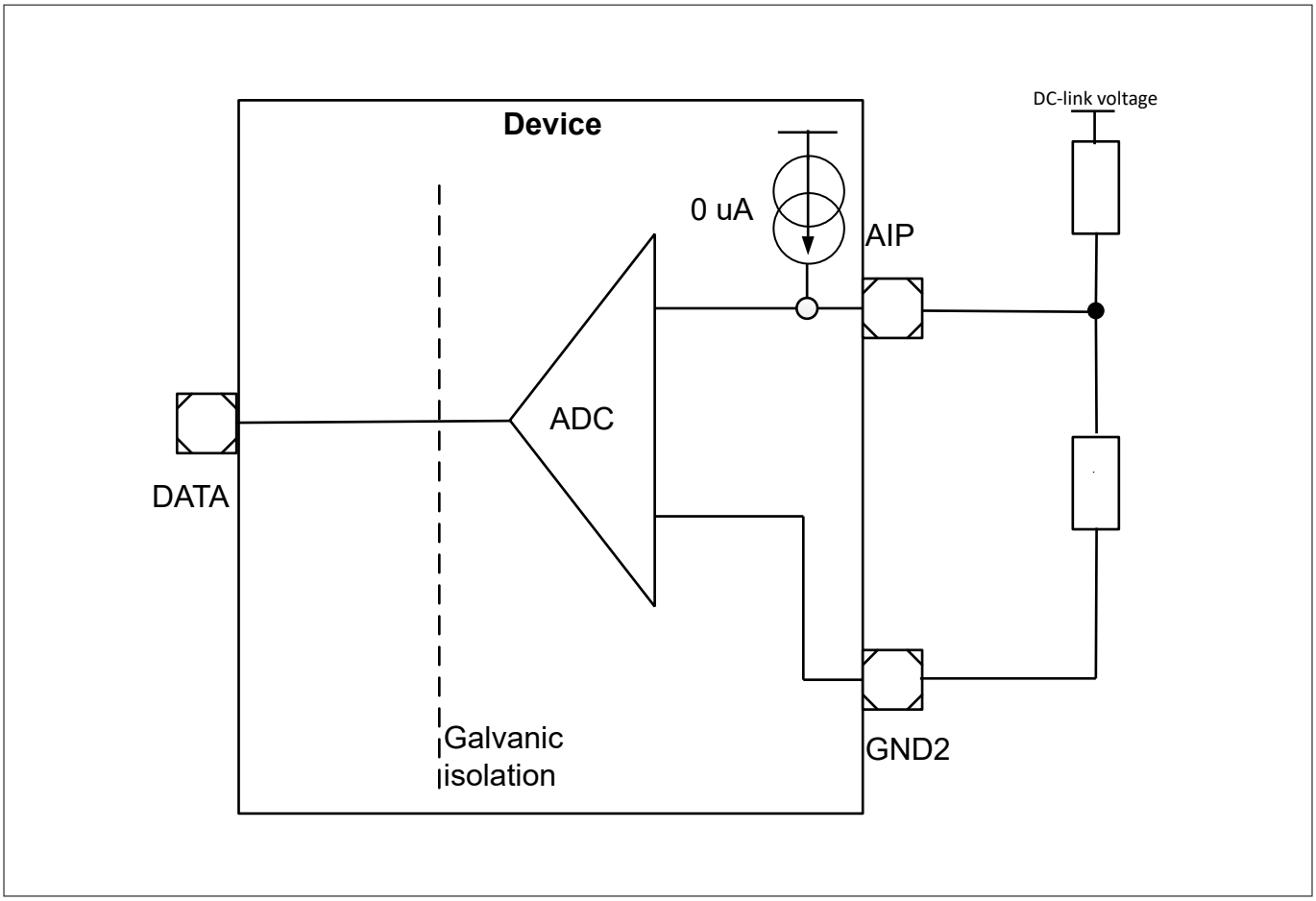


Figure 17 DC-link measurement diagram

The integrated ADC allows isolated temperature sensing. The internal current source $I_{ADC,ref}$ is disabled . The voltage signal V_{AIP} is encoded to a PWM signal that is passed through the isolation to DATA pin on the primary side. The Total Unadjusted Error is the square sum of errors (INL, ER_{OFF} and ER_{GAIN}).

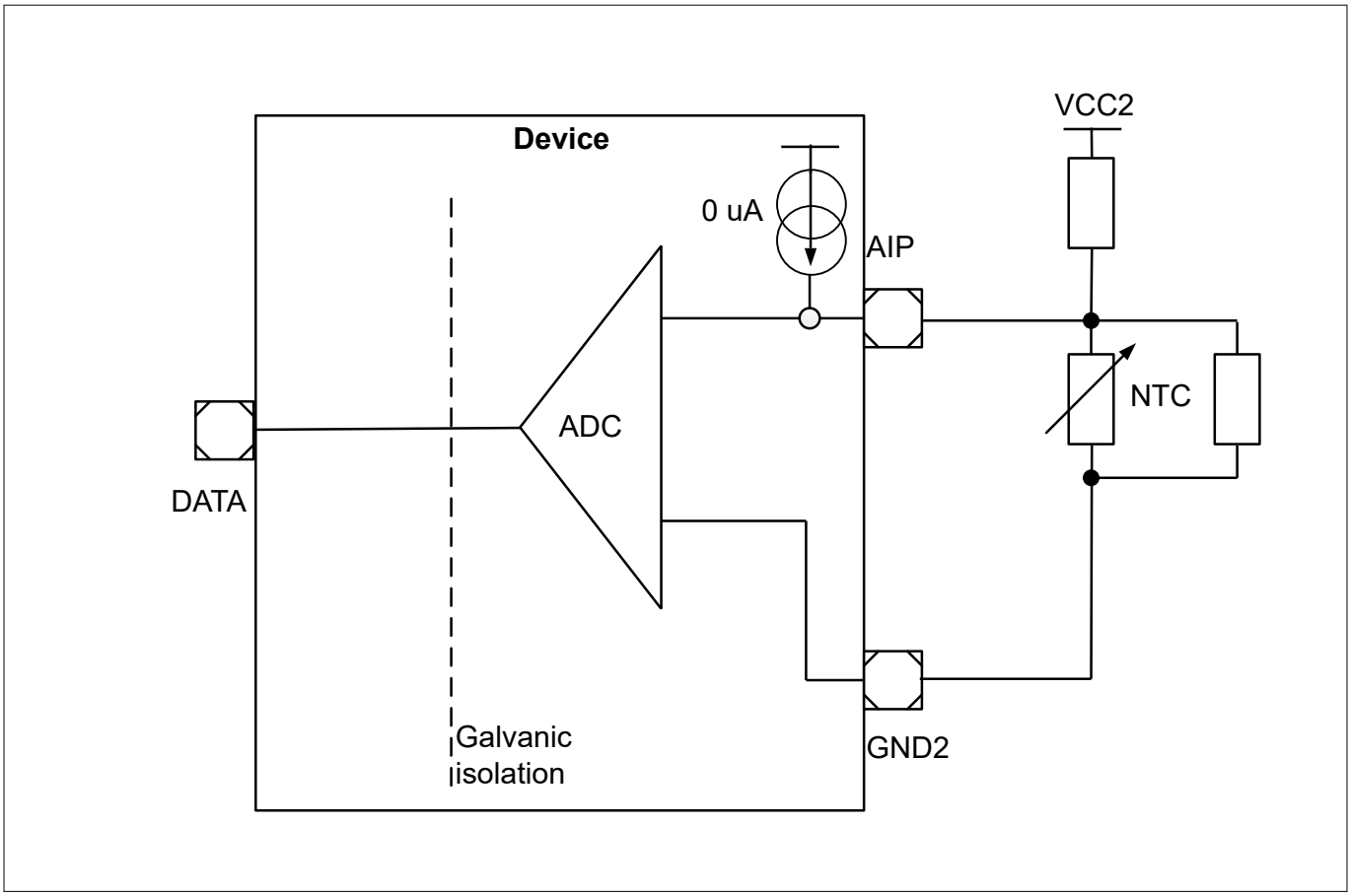


Figure 18 ADC application diagram with NTC.

***Note**:* $V_{IADC,effective} = (V_{IADC} * ER_{GAIN} / 100)$

9.2 Electrical characteristics ADC

Table 19 Electrical characteristics ADC

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC resolution		–	–	12	bit		PRQ-609
Ideal ADC input voltage full scale	V_{IADC}	–	4.82	–			PRQ-794
ADC Gain Error	ER_{GAIN}	- 1.5	–	+ 1.5	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...4.4 V	PRQ-897
ADC Offset Error	ER_{OFF}	-0.25	–	+0.25	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...4.4 V	PRQ-898

(table continues...)

Table 19 (continued) Electrical characteristics ADC

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC INL	INL	–	0.024	0.073	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...4.4 V	PRQ-899
ADC DNL	DNL	–	0.007	0.025	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...4.4 V	PRQ-900
ADC sample rate	f_{SAMPLE}	2.28	2.4	2.52	kHz	12 bit	PRQ-903
ADC leakage current	$I_{leakADC}$	- 3		3	µA	V_{AIP} = 4 V	PRQ-1034

10 Interface

10.1 Reset (NRST)

10.1.1 Functional description NRST

The NRST pin is the reset input of the device.

All errors cleared with a rising edge on NRST.

10.1.2 Electrical characteristics NRST

Table 20 Electrical characteristics NRST

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Minimum reset duration time	t_{NRST}	10	–	–	µs		PRQ-764

10.2 Ready (RDY)

10.2.1 Functional description RDY

The RDY pin reports whether the device is ready.

***Note**: Ready means: no OSM error, no gate monitoring error, no OVLO2, no UVLO2, no open pin at OCPx, no prim. or sec. internal supervision error, OTP read ok.*

The RDY pin has a passive clamping.

***Note**: Passive clamping keeps RDY = 0 in case of no supply.*

10.2.2 Electrical characteristics RDY

Table 21 Electrical characteristics RDY

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDY open drain output low level	$V_{RDY(low)}$	–	–	0.5	V	$V_{VCC1} \geq 3.0$ V, I_{load} = 5 mA	PRQ-840

(table continues...)

Table 21 (continued) Electrical characteristics RDY

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDY output low passive clamping	$V_{RDYCLAMP}$	–	0.5	1	V	$I_{RDYCLAMP}$ = 500 µA, V_{CC1} = floating, all I/O = floating	PRQ-834
Power up timing prim.	t_{PUprim}	–	100	1500	µs	Time from UVLO1 release to device operable, secondary chip running	PRQ-959
Power up timing sec.	t_{PUsec}	–	100	1500	µs	Time from UVLO2 release to device operable, primary chip running	PRQ-960
Time from rising Edge NRST to RDY = high	$t_{NRST2RDY}$	50	–	200	ns	No error detected	PRQ-961

10.3 Fault (NFLT)

10.3.1 Functional description NFLT

The device has an active low fault pin (NFLT) to report DESAT and OCP short circuit events.

If the device switches off the output stage due to a DESAT or OCP event, it goes to Error_Mode and signals the event on pin NFLT with NFLT = 0 within t_{NFLT_DESAT} or t_{NFLT_OCP}.

***Note**: Switch off means safe turn-off.*

The device keeps the fault signal available unless a reset event takes place.

10.3.2 Electrical characteristics NFLT

Table 22 Electrical characteristics NFLT

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP event detection to NFLT activation	t_{NFLT_OCP}	–	1.2	2.3	µs	$V_{OCP\_Overdrive}$= +/-200 mV, slew rate = 100 mV/ns, NFLT = 90 %, R_{PU_NFLT} = 1 kΩ	PRQ-614
DESAT event detection to NFLT activation	t_{NFLT_DESAT}	–	1.5	2.5	µs	$V_{DESAT\_Overdrive}$= +/-200 mV, slew rate = 10 V/µs, NFLT = 90 %, R_{PU_NFLT} = 1 kΩ	PRQ-844

(table continues...)

Table 22 (continued) Electrical characteristics NFLT

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
NFLT open drain output low level	V_{NFLT}	–	–	0.5	V	$V_{VCC1} \geq 3.0$ V; $\lvert I_{NFLT} \rvert = 5$ mA	PRQ-791

10.4 I/O levels

Table 23 I/O levels

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Primary digital input low level	$V_{digital,input(low)}$	0	–	0.8	V		PRQ-704
Primary digital input high level	$V_{digital,input(high)}$	2	–	V_{VCC1}	V		PRQ-705
INP high/low duration	t_{INPPD}	750	–	–	ns	V_{VCC1}=typ., V_{VCC2}=typ., V_{VEE2}=typ., 50% to 50%	PRQ-970
INN high/low duration	t_{INNPD}	750	–	–	ns	V_{VCC1}=typ., V_{VCC2}=typ., V_{VEE2}=typ., 50% to 50%	PRQ-971
Weak pull down resistance NRST, EN, INP	R_{PDIN1}	40	48	60.5	kΩ		PRQ-929
Weak pull up resistance INN	R_{PDINN}	40	52	60.5	kΩ		PRQ-930

10.5 DATA read-out

10.5.1 Functional description DATA

In case the device switches to Error_Mode and EN pin is low, diagnostic data are available, starting with the next frame. In Ready_Mode diagnostic data are available. In Normal_Mode and in Error_Mode, when EN pin is high, ADC result data are available.

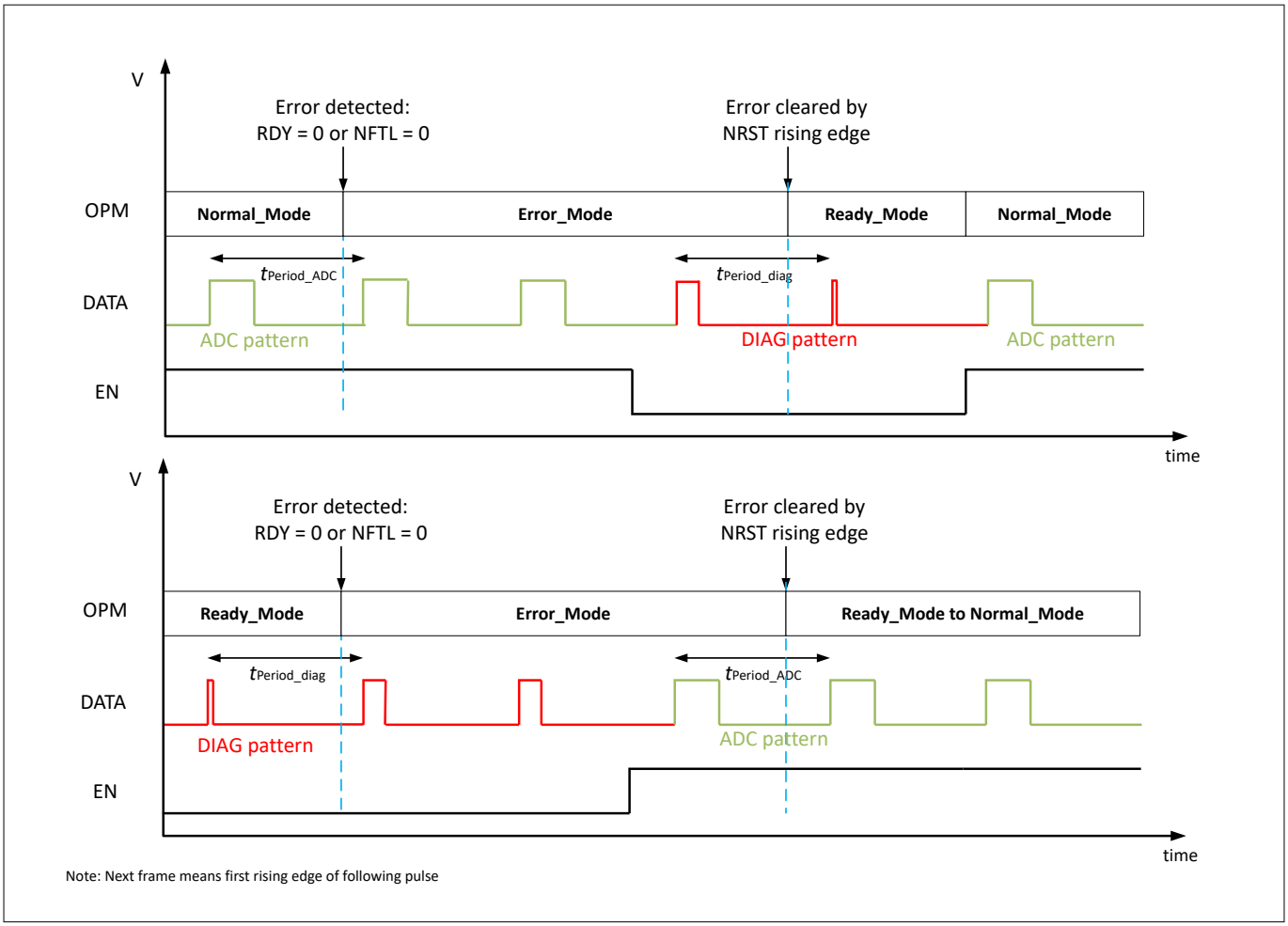


Figure 19 DATA pin ADC and diagnostic transition timing diagram

The 12 bit ADC data is pulse width modulated to a signal with a period of t_{Period_ADC}.
The duty cycle for 12 bit ADC data always remains in the range of D_{ADC} regardless of the ADC input.
The following diagnostic functions are reported in Ready_Mode and in Error_Mode, if EN = 0:

- UVLO2
- OVLO2
- Gate monitoring
- Output stage monitoring
- OCP
- DESAT
- Sec. internal supervision error (Parity, OTP, PMU_Supervision error)

The 8 bit diagnostic functions is pulse width modulated to a signal with a period of t_{Period_Diag}.
The duty cycle of the DATA pin always remains in the range of D_{Diag} regardless of the diagnostic status.

***Note**: 0% and 100% duties are not allowed at DATA pin.*

Table 24 Diagnostic read-out at DATA pin

BIT_x	Value	Description	Value	Description	Example: Single failure DESAT
BIT 0	0	PRIM NOT READY	1	PRIM READY	1
BIT 1	0		1		1
BIT 2	0		1		1
BIT 3	0		1		1
BIT 4	Reserved (always 0)				
BIT 5	0	No OSM Error	1	OSM Error	0
BIT 6	0	No GATEMON Error	1	GATEMON Error	0
BIT 7	0	No DESAT Error	1	DESAT Error	1
BIT 8	0	No OCP Error	1	OCP Error	0
BIT 9	0	No UVLO2 Error	1	UVLO2 Error	0
BIT 10	0	No OVLO2 Error	1	OVLO2 Error	0
BIT 11	0	SEC READY	1	SEC NOT READY	0
Result from example diagnostic read-out:					Duty cycle = 3.49 %

The duty cycle for diagnostic read-out can be calculated using the following formula:

$$DC = \frac{\sum(BIT_x \cdot 2^x)}{4096}$$

Figure 20 Formula to calculate the duty cycle for diagnostic read-out

10.5.2 Electrical characteristics DATA

Table 25 Electrical characteristics DATA

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC DATA duty cycle range	D_{ADC}	0.36	–	99.6	%	No life sign lost, no primary reset	PRQ-782
Diagnostic duty cycle range	D_{Diag}	0.36	–	99.6	%		PRQ-783

(table continues...)

Table 25 (continued) Electrical characteristics DATA

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC DATA period	t_{Period_ADC}	95	100	105	µs		PRQ-784
Diagnostic period	t_{Period_Diag}	95	100	105	µs		PRQ-785
DATA output low level	$V_{DATA,output(low)}$	–	0	0.5	V	$V_{VCC1} \geq 3.0$ V, $\lvert I_{load} \rvert = 5$ mA	PRQ-706
DATA output high level	$V_{DATA,output(high)}$	V_{CC1} - 0.5	V_{VCC1}	–	V	$V_{VCC1} \geq 3.0$ V, $\lvert I_{load} \rvert = 5$ mA	PRQ-707

11 Application information

The external component values are specified as typical values in a typical application. Deviation of the nominal values are specified as min or max values, if applicable. Unless otherwise specified the deviation for external components are:

- Resistor: ±10%
- Capacitor: -50% ... +30%

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

11.1 Electrical characteristics external components

Table 26 Electrical characteristics external components

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Decoupling capacitance (between VCC1 and GND1)	C_{dVCC1}	0.55	1.1	–	µF	Total capacitance refers to 1 µF capacitance + 0.1 µF close to the device. Max value depends on t_{RP1}.	PRQ-1002
Decoupling capacitance (between VCC2 and GND2)	C_{dVCC2}	–	11	–	µF	Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Values depend on external C_{LOAD}. Max value depends on t_{RP2}.	PRQ-1001
Decoupling capacitance (between VEE2 and GND2)	C_{dVEE2}	–	11	–	µF	Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Max value depends on t_{RP3}.	PRQ-1000
Pull-up resistance	R_{pu}	–	10	–	kΩ	Min value depends on I_{OUTx_MAX}.	PRQ-1015
Filter resistance	R_{Filter}	–	1	–	kΩ	Value must fit to application	PRQ-1016
Filter capacitance	C_{Filter}	–	47	–	pF	Value must fit to application	PRQ-1017
DESAT resistance	R_{Desat}	1	2.2	–	kΩ	Depends on maximum current and on V_{DESATx} deviation.	PRQ-1018
DESAT filter capacitance	C_{Desat}	50	100	–	pF	Depends on required response time.	PRQ-1019
OCP sense resistor	$R_{OCPSense}$	–	0.47	–	Ω	Value depends on power switch specification, voltage rating of OCP pin has to be considered.	PRQ-1021

(table continues...)

Table 26 (continued) Electrical characteristics external components

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCPP filter resistance	R_{OCPP}	–	10	–	Ω	Depends on required response time. Consider internal pull-up.	PRQ-1022
OCPP filter capacitance	C_{OCP}	–	10	–	pF	Depends on required response time	PRQ-1023
OCPN resistance	R_{OCPN}	–	10	–	Ω	Should match to OCPP filter resistor. Consider internal pull-up.	PRQ-1024
TOUT resistance	R_{Load}	1.7	–	–	Ω	Min resistor value required according to max output current in functional range. Max value limited by gate monitoring feature.	PRQ-1025
GATE/CLAMP series resistance	R_{GATE}	–	0	–	Ω	Optional component. Voltage across resistor impacts Active Miller clamping feature.	PRQ-1028

11.2 Typical application example

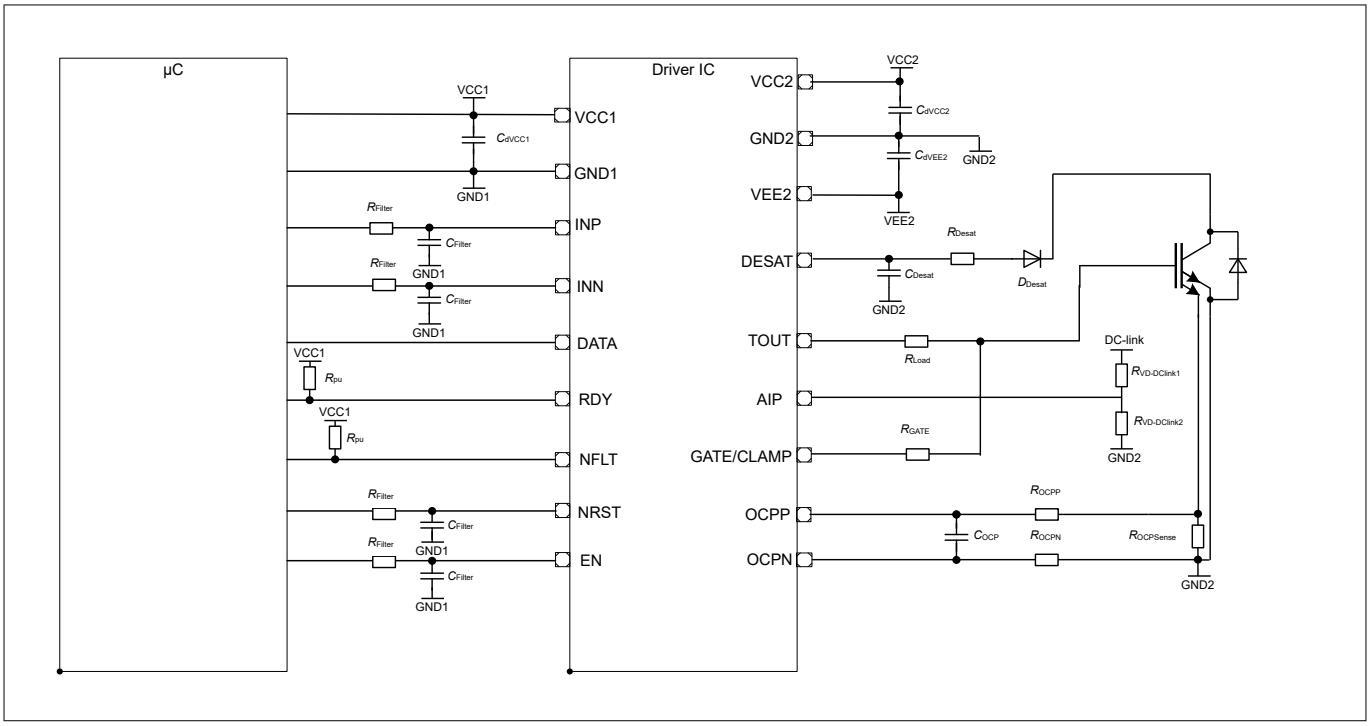


Figure 21 Typical application example with ADC

***Note**: This is a very simplified example. The function must be verified in the real application.*

12 Package information

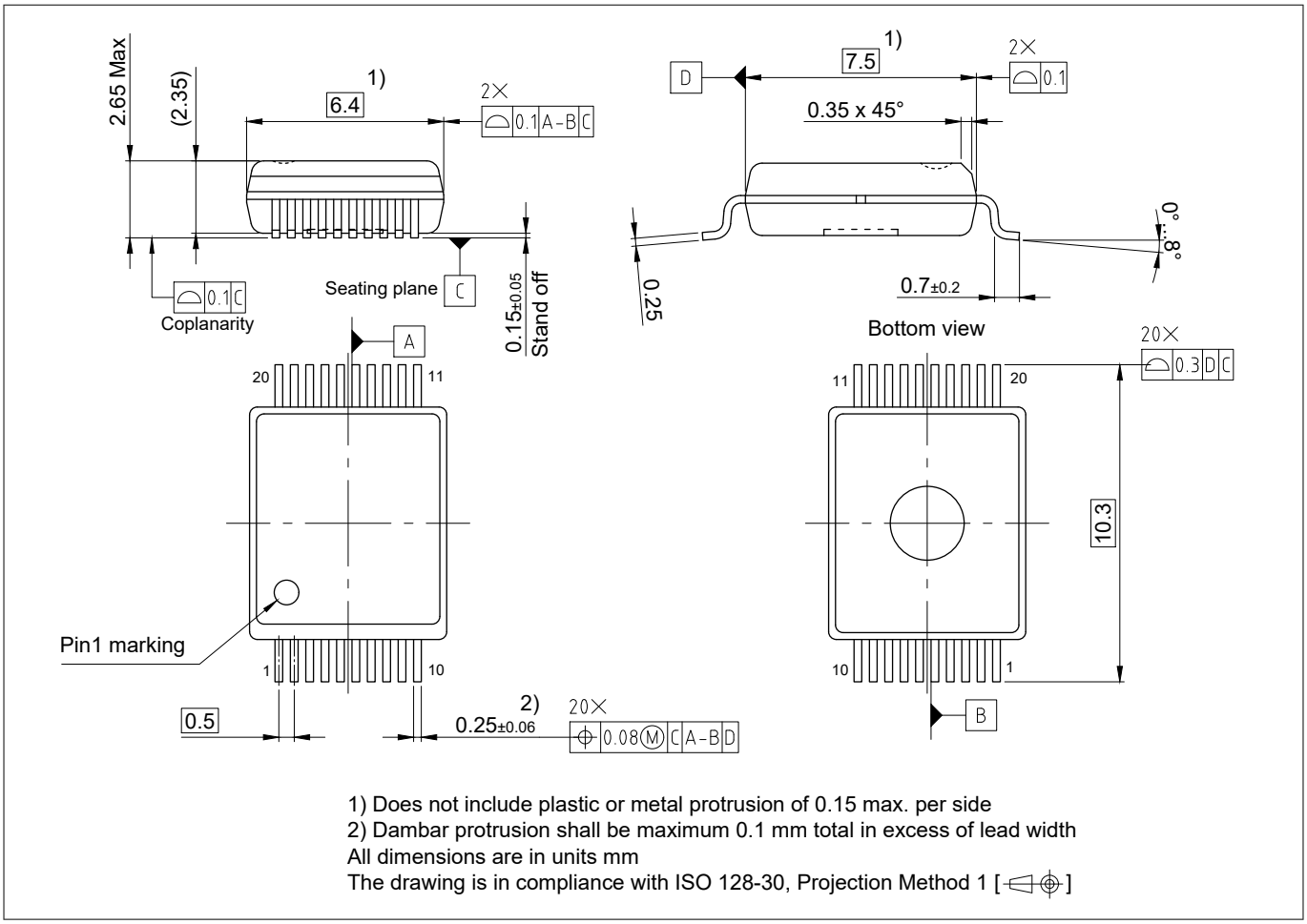


Figure 22 PG-DSO-20

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

Revision history

Revision	Date	Changes
1.2	2023-11-27	Front Cover updated Chapter 3.2 updated • Table 3 updated - VEE2, VCC2 - Min. / Max. adjusted Chapter 3.4 updated • Table 5 updated – Insulation upgraded to DIN EN IEC 60747-17 (VDE 0884-17):2021-10 Chapter 5.2 updated • Table 8 updated – I_{QPVCC1_ON} Max. adjusted
1.1	2022-02-17	Chapter 3.2 updated • Table 3 updated - VCC1, VEE2, VCC2 ramp-up slew-rates reduced - ramp-down condition removed Chapter 3.4 updated • Table 5 updated - extended by further electrical information - additional reinforced insulation options
1.01	2021-06-25	Typo in insulation certification standard corrected
1.0	2021-03-18	Initial datasheet created

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