Effective ESD protection for USB3.0/3.1 combined with perfect Signal Integrity

USB3.0/3.1 basics, ESD protection for SuperSpeed mode, Layout suggestions, Signal Integrity simulations

Application Note AN240

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Previous Revision: Rev. 1.1

Page	Subjects (major changes since last revision)
	Device update
	USB Specification update to USB3.1

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Terms and Abbreviations

BER	Bit Error Rate.
CTLE	Continuous Time Linear Equalizer.
DFE	Decision Feedback Equalizer.
DUT	Device Under Test.
Enhanced SuperSpeed	An adjective referring to any valid collection of USB defined features defined for the bus that runs over the SSRx and SSTx differential pairs in a USB 3.0 or USB 3.1 system. It is used in place of phrases like SuperSpeed/SuperSpeed Plus.
ESD	Electrostatic discharge.
FS, Full-speed	USB operation at 12 Mb/s.
Gen 1	An adjective used to refer to the Physical layer associated with a 5.0 Gbit/s signaling rate. The USB3.0 SuperSpeed PHY and a USB3.1 Gen 1 PHY refer to the same PHY.
Gen 2	An adjective used to refer to the Physical layer associated with a 10 Gbit/s signaling rate.
HS, High-speed	USB operation at 480 Mb/s.
LS, Low-speed	USB operation at 1.5 Mb/s.
PHY	An abbreviation for the physical layer of the OSI model and refers to the circuitry required to implement physical layer functions.
TLP	Transmission Line Pulse.
SuperSpeed	An adjective referring to the architectural layer portions of a device defined in USB 3.1 specification when operating with a Gen 1 PHY. In USB 3.0 defined as USB operation at 5 Gbit/s.
SuperSpeed Plus	An adjective referring to the architectural layer portions of a device defined in USB 3.1 specification when operating with a Gen 2 PHY.
TVS	Transient Voltage Suppression/Suppressor.
USB-IF	USB Implementers Forum, Inc. http://www.usb.org

1 Evolution of the USB interface

The well-known Universal Serial Bus (USB) was introduced first time in 1996 with version 1.0, providing data rates of 1.5 Mbit/s in Low-speed (LS) mode and 12 Mbit/sec in Full-speed (FS) mode. In 2000 USB 2.0 entered the market, adding the High-speed (HS) mode with up to 480 Mbit/s, and being still downwards compatible to Low-Speed and Full-Speed modes.

USB2.0 is one of the most widespread, general-purpose external data interfaces. It became the default standard in all computer systems from desktop computers through laptops and netbooks to tablet PC's. It is also widely used in consumer electronics like camcorders, digital cameras, MP3 players, game consoles, DVD/Blu-ray players and TV sets as well as in mobile phones and DSL/router units.

In 2008 3 billion units of new electronic equipment with USB interface were shipped. Estimation for 2013 is more than 4 billion new USB-enabled devices. The demand for an external interface with significant higher data rate grew constantly, driven by very high speed applications and rapidly increasing volume of external storage devices.

As an answer to this demand, the USB 3.0 specification was released in November 2008. Backward compatible to the USB 2.0, it introduced separate SuperSpeed data link. Physical layer of the SuperSpeed link consists of two separate differential data channels - one for data transmission (SSTx) and one for reception (SSRx). The maximum full duplex data rate in the SuperSpeed mode is 5 Gbit/s.

In July 2013 the next evolutionary step of the specification was released. USB 3.1 is primarily a performance enhancement to SuperSpeed USB 3.0 providing more than double the bandwidth for high-speed devices. In addition to 5 Gbit/s SuperSpeed mode it defines 10 Gbit/s operation or SuperSpeedPlus.

2 USB3.0/3.1 System overview

The USB 3.0/3.1 system architecture is comprised of two simultaneously active buses: A USB 2.0 bus and an (Enhanced) SuperSpeed bus (Figure 1). When referring to any valid collection of features defined for the bus that runs over the SSRx and SSTx differential pairs in a USB 3.1 system, term Enhanced SuperSpeed is used. It is equal to SuperSpeed/SuperSpeedPlus.

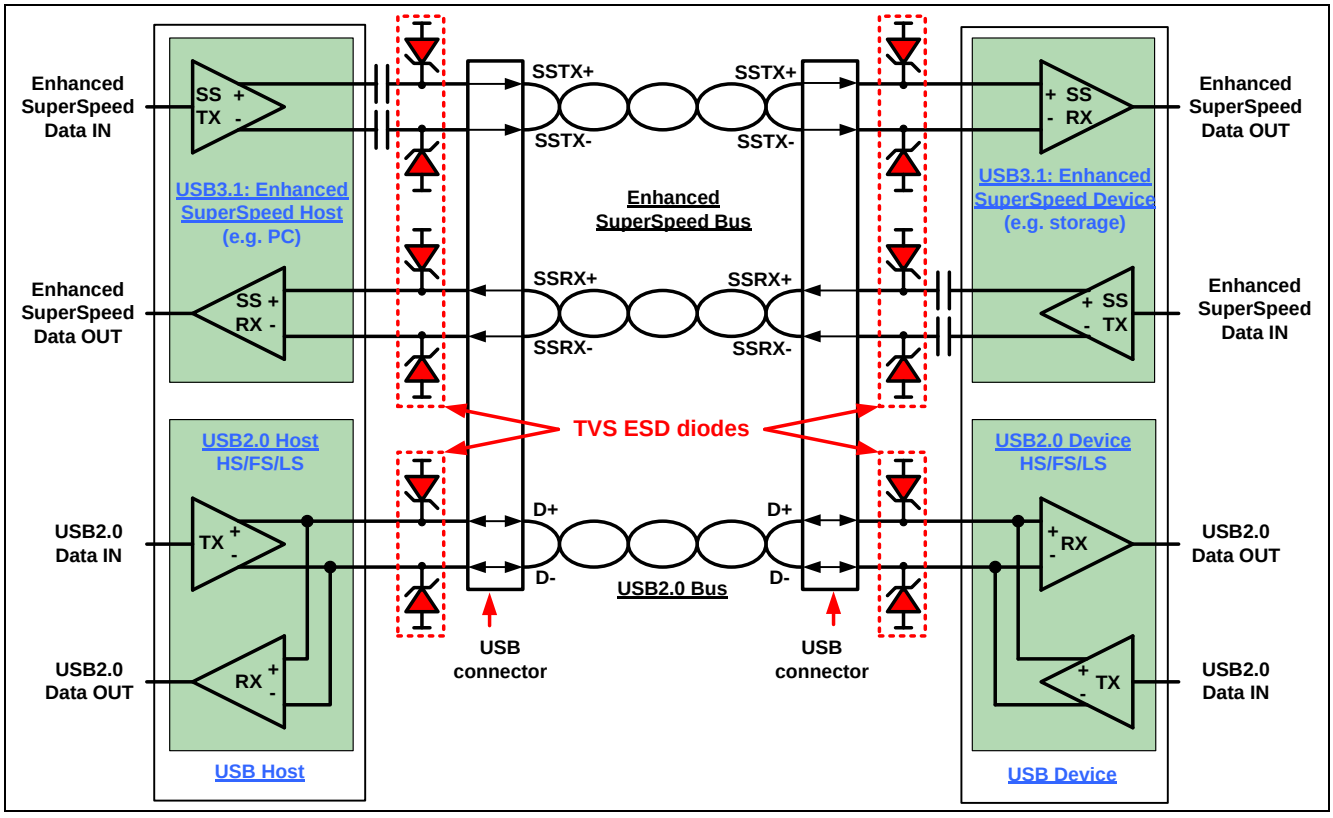


Figure 1 USB3.0/3.1 (Enchanced) SuperSpeed bus and USB2.0 bus including ESD protection at the host and at the device

Physical layer associated with each signaling rate has its own name. The original USB 3.0 SuperSpeed (5 Gbit/s) PHY is now called Gen 1 PHY. Gen 2 is used to refer to the Physical layer associated with a 10 Gbit/s signaling rate. Gen X is a generic term used to refer to any of the combinations Gen 1, Gen 2 or Gen 1/Gen 2 when the topic is specific to the physical layers but does not need to be specific to either Gen 1 or Gen 2. Figure 2 illustrates the reference model for the terminology in USB 3.1 specification.

The combination of USB 2.0 functionality and the Enhanced SuperSpeed mode requires a new cable construction serving three differential coupled signal lines (SSTx+/SSTx-, SSRx+/SSRx- and D+/D-). The Vcc and the GND line complete the cable set.

The challenge for low cost USB 3.0/USB 3.1 cable is to serve a high cut off frequency without interaction between the adjacent differential coupled line pairs (Figure 3). Another challenge is cable attenuation at high frequencies. To guarantee reliable communication between host and device USB specification puts strict requirements on cable performance. However, cable attenuation can still vary widely (0…-7.5 dB @ 2.5 GHz for USB 3.0, 0…-6 dB @ 5 GHz for USB 3.1) influencing signal to high degree.

The USB 3.0/USB 3.1 cable characteristic is a major contributor for the entire channel loss at high frequency.

To handle all lines for USB 3.0/USB 3.1 a new connector was introduced, which is backward compatible to the USB 2.0 connector. This results in a high probability of ESD strikes on the SuperSpeed lines (at both host and at device sides).

Another important problem for USB devices, like for all ultra-high speed data transmission systems, is to ensure good signal integrity at the receiver. USB specification uses eye diagram to assess signal integrity. The standard specifies minimal acceptable eye opening at $1 \cdot 10^{-12}$ Bit Error Rate (BER) level.

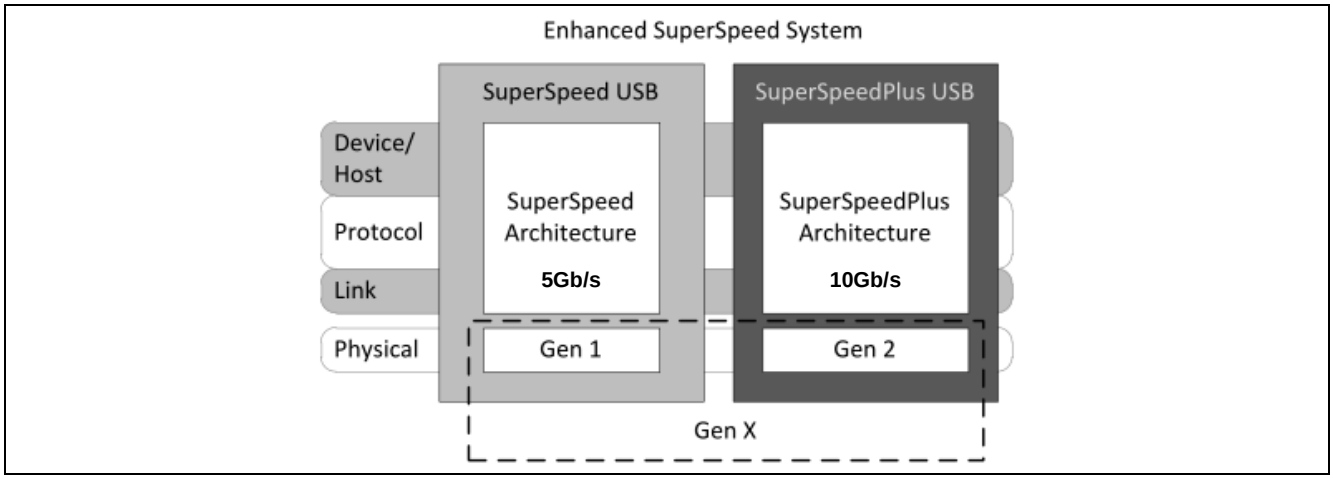


Figure 2 USB 3.1 Terminology Reference Model (Source: USB3.1 Rev.1.0 specification)

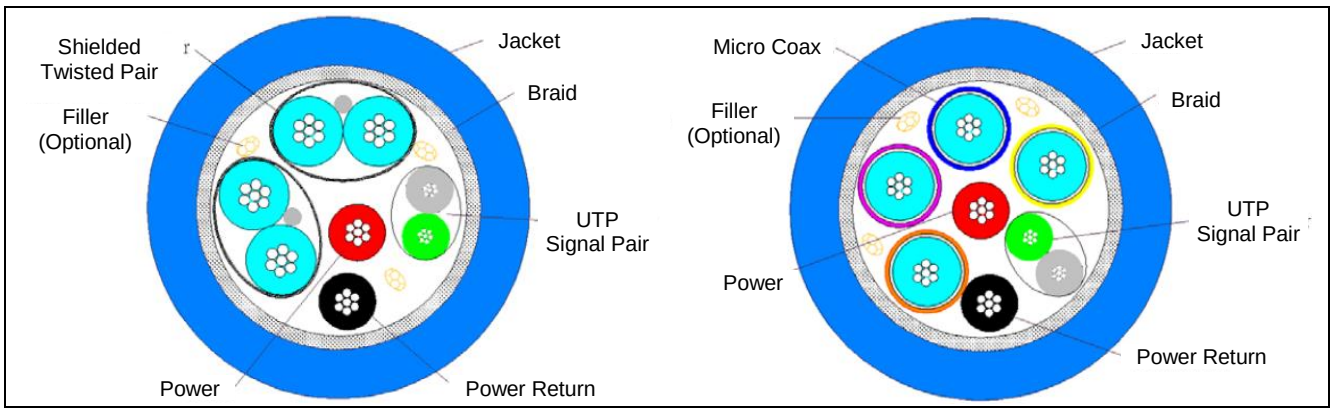


Figure 3 USB3.1 cable cross-section (Source: USB3.1 Rev.1.0 specification)

In a perfect system without limitation in bandwidth the eye diagram would be perfectly open. In reality the signal rise and fall times as well as amplitude are limited, closing the eye. Main limiting factors are:

- Impedance mismatch at TX and RX, along the transmission channel, at connectors;
- Transceiver IC parasitic parameters and shunt components;
- Channel attenuation, especially at higher frequencies.

Another phenomenon reducing the eye opening and leading to mode conversion is differential (intra-pair) skew. It is a delay between two single-ended signals in a differential pair. Usually the skew is caused by the difference in the effective length of two transmission lines, constituting a differential pair.

The most important steps to maintain good signal integrity are:

- Minimization of limiting factors listed above, especially capacitance of shunt components;
- A proper layout and symmetrical placement of components can minimize the skew;
- Equalization at both TX and RX sides.

Equalization compensates to some degree for all limiting factors in the transmission line, resulting in a more open eye pattern. Figure 4 shows simulated effect of equalization on signal integrity of the USB3.1 Gen 1 link. The left side of the Figure 4 shows an eye pattern simulation ($1 \cdot 10^6$ Unit Intervals) in front of the RX equalizer. On the right side an eye pattern after the RX equalizer is presented. The red inner contour shows the eye opening extrapolated to $1 \cdot 10^{-12}$ BER. The magenta contour is the USB 3.0/USB 3.1 Gen 1 specification valid for SuperSpeed compliance test. Comparing both eye diagrams the efficiency of the RX equalizer is obvious.

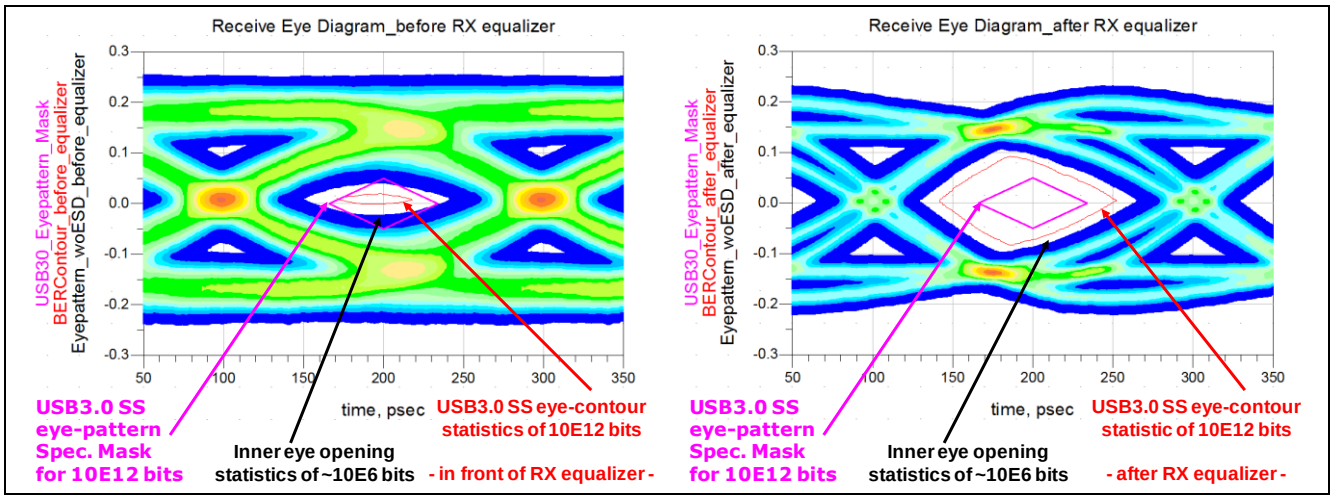


Figure 4 Eye diagram in front of the RX equalizer (left) and Eye diagram after the RX equalizer (right)

3 ESD protection for USB

3.1 Protection Strategy

On the one hand continuous miniaturization of all structures on the chip is the basis to reduce production cost and to extend the operating frequency, speed and data rate. On the other hand the drawback of miniaturized semiconductor structures is the weakness against overvoltage caused by an ESD strike.

High ESD sensitivity of chips combined with exposed placement of Enhanced SuperSpeed contacts in USB connectors makes ESD protection very important for USB 3.0/USB 3.1-enabled devices. However, implementing strong ESD protection on-chip causes parasitic effects (parasitic capacitances) and costs expensive chip area.

A very cost effective approach to ESD protection consists of two parts:

1. Internal ESD protection structure, integrated in the transceiver, designed to provide device level protection e.g. according to HBM (JEDEC JS-001) only, which is important for device handling during development, production and board assembly;

2. External ESD protection, implemented by the device/circuit designer on the PCB, designed to provide more stringent system level protection according IEC61000-4-2.

External protection can be efficiently realized by an external TVS diode tailored to the application.

To achieve proper system level ESD protection, the ESD protection device (TVS diode) has to fulfill requirements to its performance during normal operation, as well as during an ESD strike.

Most important parameters for performance during normal operation are diode capacitance and maximal reverse working voltage.

The ESD performance of a TVS diode can be judged by its clamping voltage during an ESD strike, usually according IEC61000-4-2. ESD performance is affected mainly by following TVS diode characteristics:

- R_{ON} ($R_{dynamic}$) – the lower the better
- $V_{breakdown/hold}$ – as low as possible, but higher than expected voltage level during normal operation

TVS diode clamping voltage V_{clamp} can then be calculated:

$$V_{clamp} \approx V_{breakdown/hold} + R_{dynamic} \cdot I_{ESD}$$

TVS diode dynamic resistance $R_{dynamic}$ can be extracted from TLP (Transmission Line Pulse) measurement (Figure 5). For more details on TLP measurements and $R_{dynamic}$ calculation see Infineon AN210.

Following this guidelines the residual ESD stress on the IC can be minimized. At the same time, for high signal integrity capacitance of the TVS diodes has to be kept low. With increasing operating frequency/data rate this requirement gains in importance.

There are three different busses needing protection inside the USB 3.0/USB 3.1 link:

- Enhanced SuperSpeed bus, operating at 5 Gbit/s or 10 Gbit/s
- Generic USB 2.0 bus
- Vcc bus

Requirements to ESD protection for each bus are discussed below.

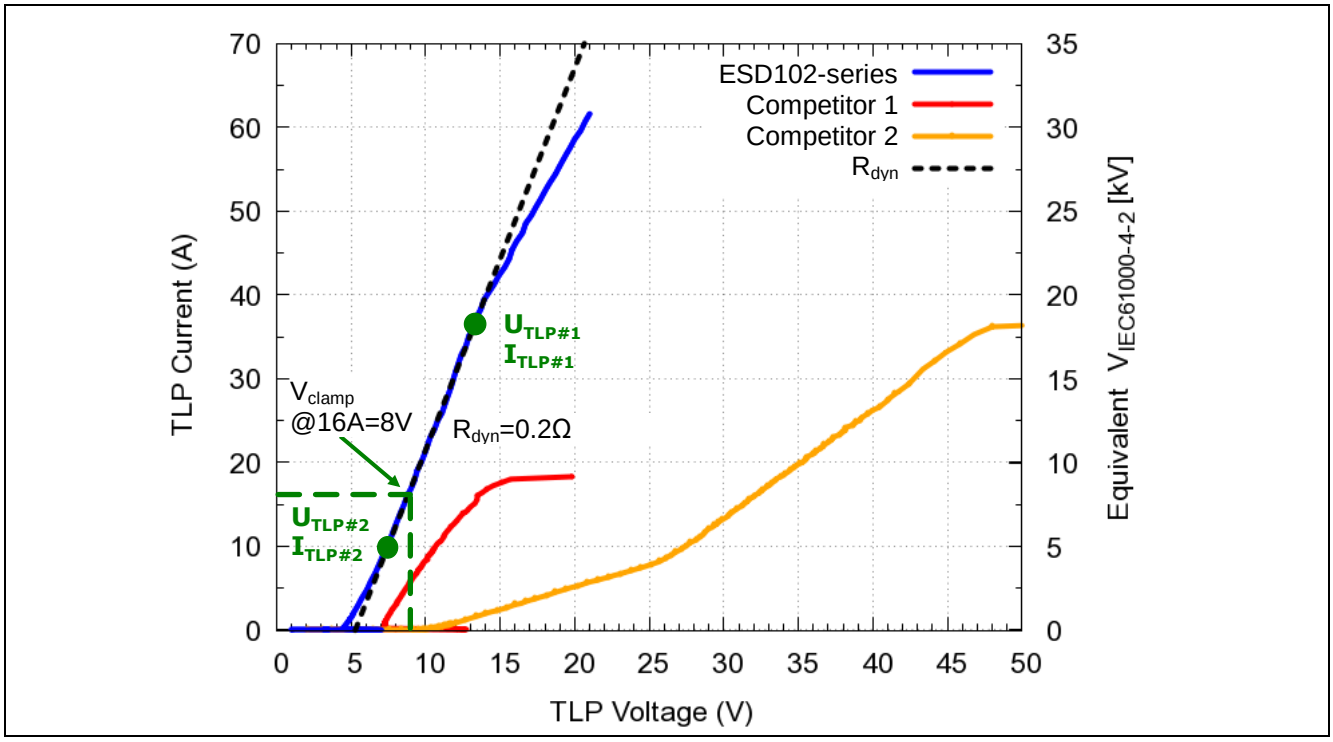


Figure 5 TLP measurement result for the Infineon ESD102-series tailored for USB3.0/USB3.1 Enhanced SuperSpeed ESD protection

3.2 Enhanced SuperSpeed bus (USB 3.0/USB 3.1)

SuperSpeed bus (USB 3.0, USB 3.1 Gen 1) has data rates up to 5 Gbit/s resulting in a Nyquist frequency up to 2.5 GHz. At such high operating frequencies capacitance of the diode becomes crucial. Simulations and measurements have shown that capacitance of 0.4 pF has minor influence on signal integrity.

SuperSpeedPlus bus (USB 3.1 Gen 2) operating at up to 10 Gbit/s and having Nyquist frequency up to 5 GHz has even higher sensitivity for parasitic capacitance. It would be desirable to get TVS diode capacitance even lower. However, USB 3.1 Specification still allows up to 1.1 pF and 1.0 pF parasitic capacitance to ground for Gen 2 transmitter and receiver respectively. Our simulations have shown that diode capacitance of 0.4 pF works very well in most circumstances, depending on actual transmitter/receiver.

For Enhanced SuperSpeed bus ESD protection Infineon provides an application tailored TVS diodes:

- **ESD102-U4-05L** - Unidirectional Ultra-low Capacitance ESD / Transient Protection Array in TSLP-5-2 package, with highly matched package parameters to reduce mode conversion and differential skew
- **ESD102-U1-02ELS** – single diode with same high performance as array, for more routing flexibility (replaces ESD3V3U1U-02LS)

For customers who prefer TSLP-9-1 package, another product is available:

- **ESD3V3U4ULC** - Ultra-low Capacitance ESD / Transient Protection Array in TSLP-9-1 package

All listed devices have $R_{dynamic}$ of only 0.2 Ohm (typical) and a maximal reverse working voltage of 3.3 V ($V_{breakdown}$: 4 V min). Clamping voltage for a 16 A ESD strike is as low as 8 V (typical), which is best in class.

Note: The 16 A TLP test pulse fits very well to an 8 kV contact ESD strike according IEC61000-4-2 that has a current of 16 A at 30 ns after the pulse start.

An alternative ESD protection device (lower capacitance) for the enhanced SuperSpeed line can be mentioned.

- **ESD108-B1-CSP0201** - Bidirectional Ultra-Low Capacitance ESD/Transient Protection Diode in 0201-size chip-scale package

3.3 USB 2.0 Bus

Due to USB 2.0 backward compatibility to earlier revisions of specification (FS/LS), voltages on D+/D- lines can reach 5 V in normal operation mode. Protection devices required to have slightly higher reverse working voltage and breakdown voltage.

Recommended devices for ESD protection of USB 2.0 lines are:

- **ESD108-B1-CSP0201** - Bidirectional Ultra-Low Capacitance ESD/Transient Protection Diode in 0201-size chip-scale package.
- **ESD114-U1-02 Series** - Unidirectional Ultra-Low Capacitance ESD/Transient Protection Diode in 0201 or 0402-size plastic package.

The ESD108-B1-CSP0201 has extremely low capacitance of 0.25 pF and maximal working voltage of ±5.5 V.

The ESD114-U1-02 Series have a maximal reverse working voltage of 5.3 V ($V_{breakdown}$: 6 V min) and a typical diode capacitance of 0.4 pF.

These devices have proven to work reliably in USB 2.0 interfaces for wide variety of applications.

3.4 Power supply (V_{CC}) bus

Power supply bus doesn't put any specific requirements regarding parasitic capacitance. However, is can be exposed to transients with more power/energy, i.e. from low quality wall charger, car charger, residual surge from AC outlet, etc. Thus, much higher ESD robustness is required from protection device.

Recommended devices for ESD protection of V_{CC} bus:

- **ESD200-B1-CSP0201** - Bidirectional ESD/Transient Protection Diode in 0201-size chip-scale package.
- **ESD206-B1-02 Series** - Bidirectional ESD/Transient Prot. Diode in 0201 or 0402-size plastic package.

Both ESD200-B1-CSP0201 and ESD206-B1-02 Series have working voltage of ±5.5 V, and very low $R_{dynamic}$.

4 Layout of ESD protected USB link

Design guidelines for the USB link:

- Fully impedance matched 90 Ohm differential design for all PCB lines and for interconnection cables is mandatory.
- Non-differential lines have to be minimized. They have significant negative impact on eye diagram opening.
- Line width and line gap of the 90 Ohm differential coupled PCB lines should not be too small to avoid ohmic loss and to be robust enough for manufacturing. On 200 µm thick FR4 substrate line width of 0.3 mm and line gap of 0.2 mm between the differential lines is perfect for production in most cases. (assumption ε_r=4 for FR4 dielectric).
- Identical delay (line length) between the positive and the negative line (including the USB cable) of the differential coupled link (minimizing differential skew). This is important to keep signal integrity high and to avoid common mode generation.

Rules for efficient ESD protection:

- TVS diode must be placed as close to potential ESD source (connector) as possible, to provide shortest path to the ground for ESD current;
- Especially sensitive transceiver ICs can be additionally protected with serial resistors between TVS diode and IC. Resistance values of as little as 1-3 Ohm can improve protection performance dramatically without much influence on useful signal.

Layout suggestions for the USB 3.0/USB 3.1 standard-A connector section in combination with an ESD protection circuit are given in Figure 6 and Figure 7.

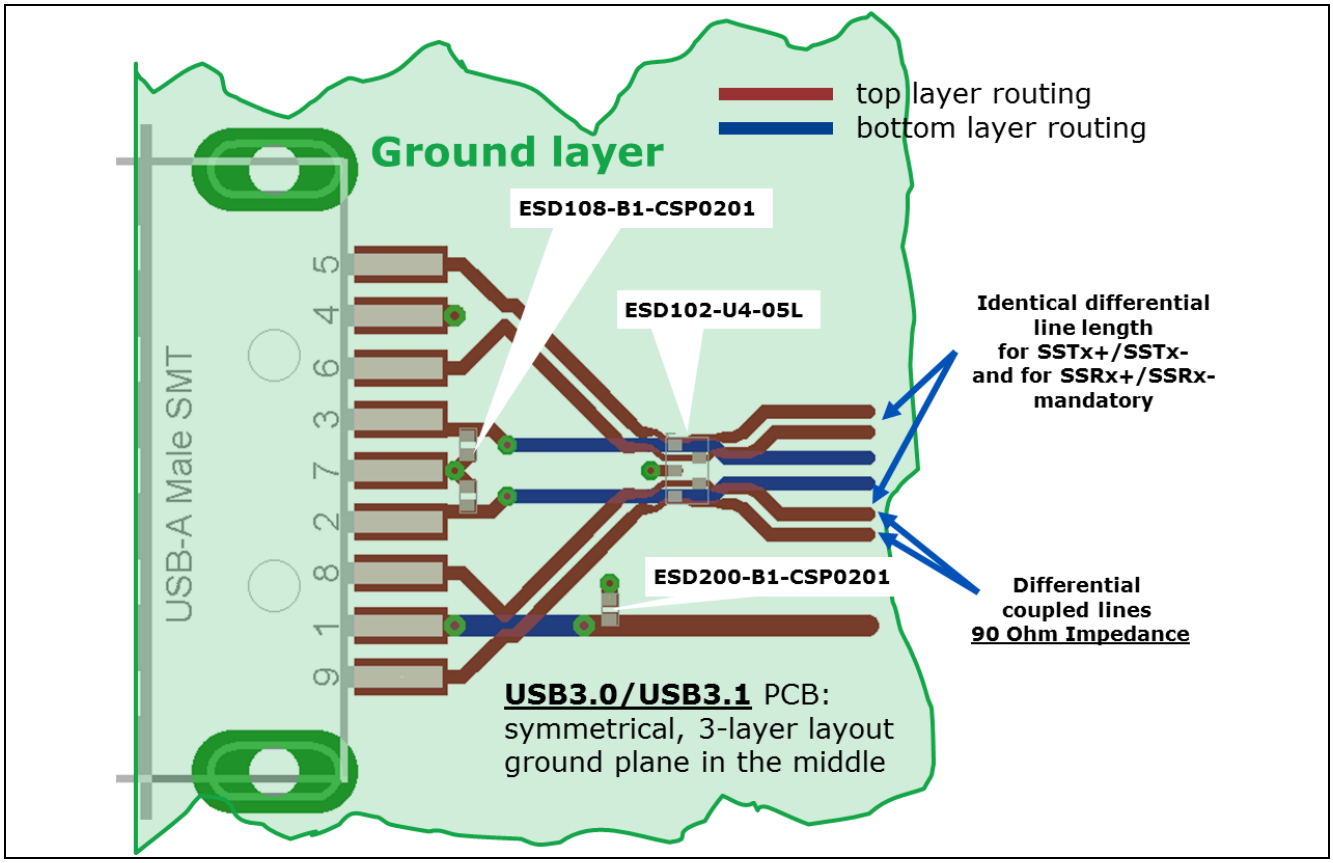


Figure 6 USB 3.0/USB 3.1 Layout for Standard-A plug + Infineon ESD protection devices

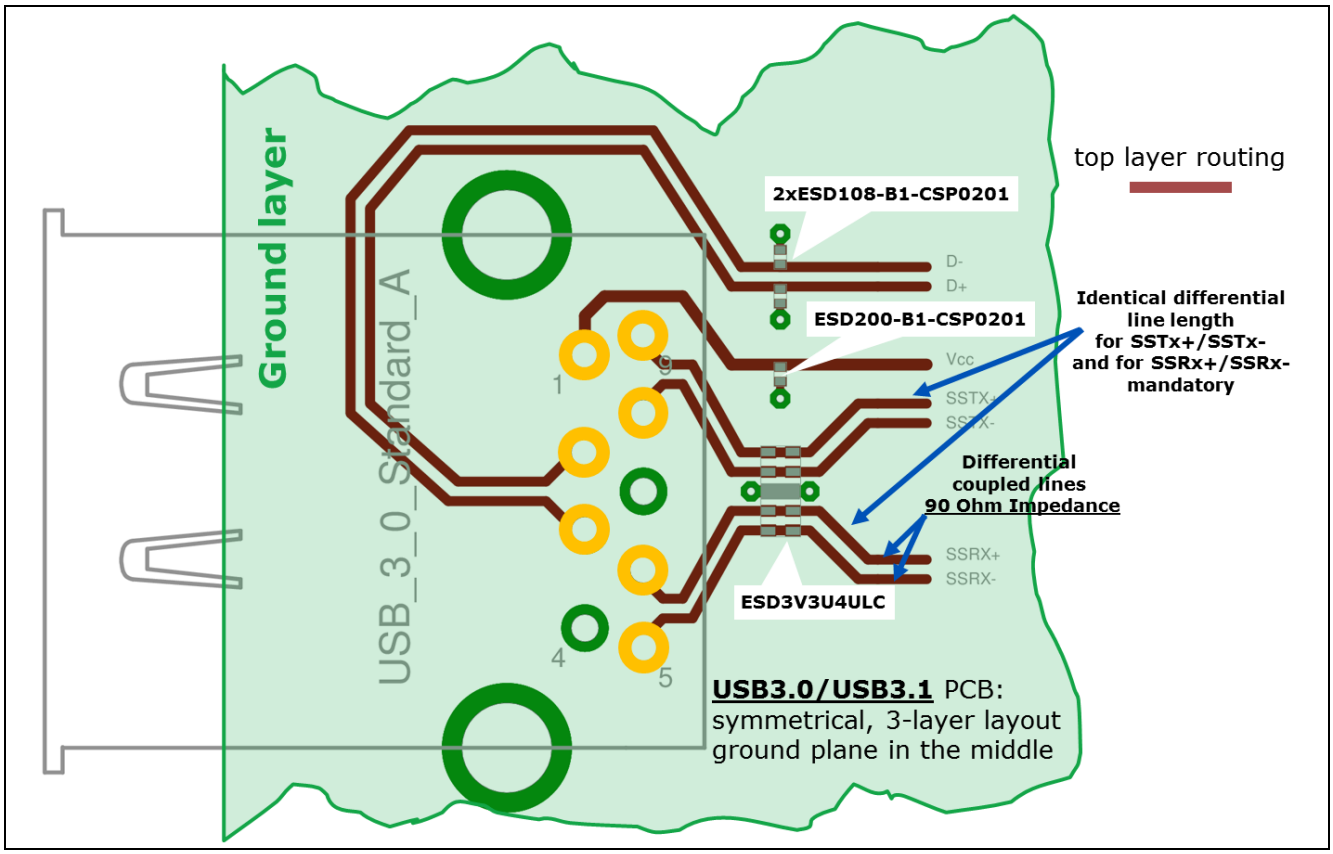


Figure 7 USB 3.0/USB 3.1 Layout for Standard-A socket + Infineon ESD protection devices

5 Signal Integrity of the ESD protected USB3.0/USB3.1 Enhanced SuperSpeed link

5.1 Signal integrity simulation in ADS

To ensure a high degree of interoperability between different USB-enabled devices, the USB specification sets normative requirements for electrical parameters of transmitter, receiver and transmission channel. The USB Implementers Forum, Inc. (USB-IF), provides the electrical compliance testing methodology for the USB standard. Compliance testing of USB-enabled devices consists of:

- Transmitter test;
- Receiver test.

The setup for the transmitter compliance test is shown in Figure 8. For this test, a Device Under Test (DUT) is put into compliance mode. A reference test channel with a cable is either connected physically or simulated in software in a measurement tool. The USB-IF provides test fixtures and a cable kit as well as a reference S-Parameter data in Touchstone format. All measurements are made at the test point (TP1), and the transmitter specifications are applied after processing the measured data with the compliance reference equalizer transfer function.

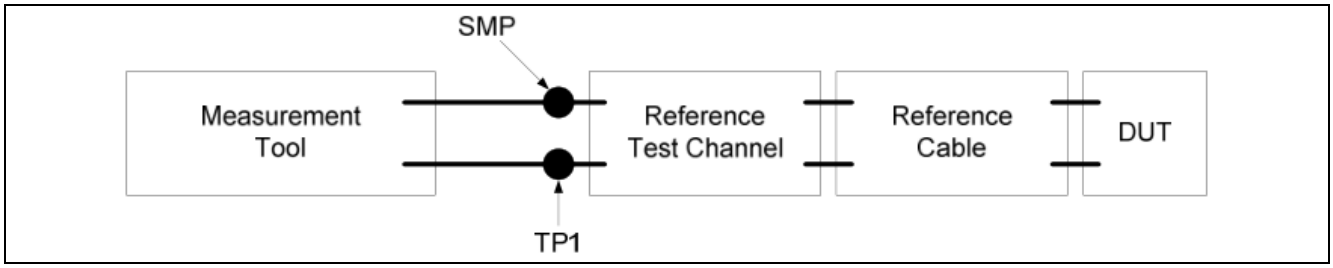


Figure 8 Transmitter compliance test setup

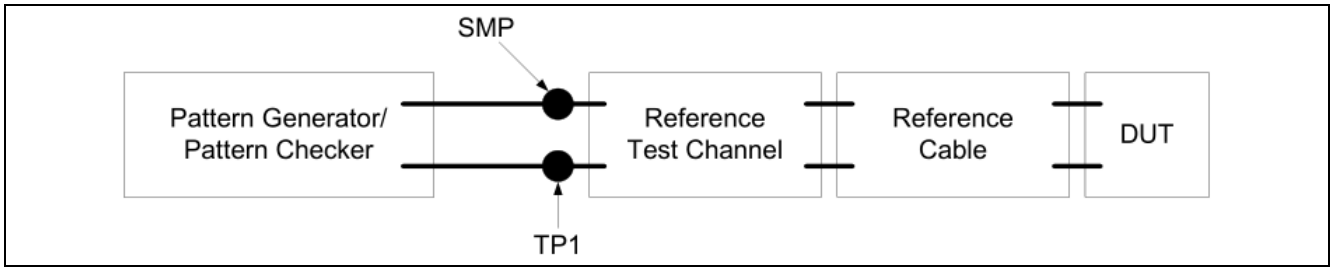


Figure 9 Receiver compliance test setup

The setup for the transmitter compliance test is shown in Figure 8. For this test, a DUT in loopback mode acts as a repeater. The test pattern is generated externally and fed through a reference channel to the DUT. DUT interprets logical value of the signal and sends it back. The returned signal is then compared to the original. Difference is counted as an error.

TX compliance test gives better estimation of ESD protection influence on the link quality, and was used as basis for simulations and measurements described below.

5.2 USB 3.1 Gen 2 SuperSpeed Plus (10 Gbit/s)

Simulation model for transmitter compliance test in USB 3.1 Gen 2 SuperSpeed Plus link is shown in Figure 10.

Simulated channel included:

- host and device models, provided by USB-IF
- silicon (transceiver) parasitics on transmitter side
- board parasitics
- high loss channel provided by USB-IF for compliance testing purposes
- ESD102-U4-05L TVS diode at transmitter side (for “protected” setup)
- Optional serial resistors between TVS diode and transmitter channel
- Specification compliant reference CTLE+DFE on receiver side

Voltage swing on transmitter side as well as de-emphasis parameters were set to fixed values, compliant to USB specification:

- V_{TX} = 1V (USB 3.1 Specification allows 0.8-1.2V)
- 3-tap FIR equalizer C_{-1}=-0.1, C_1=-0.125 (Suggested settings for lossy channel as per USB 3.1 Spec.)

Receiver CTLE and DFE implementer the reference equalizer function per USB 3.1 specification. Its parameters were chosen from the possible values given in the specification to achieve the best eye opening. This corresponds to compliance testing procedure, and simulates the training phase in the real-life communication between device and host.

Optimal receiver equalizer settings in the simulated case were:

- A_{DC} = -4dB
- A_{DFE} = 40mV

Simulations showed that ESD102-U4-05L has outstanding performance even in very fast USB 3.1 Gen 2 SuperSpeed Plus environment, influencing signal integrity only marginally. Figure 11 shows Eye diagrams of SuperSpeed Plus channel without and with ESD protection. For better comparison, eye opening extrapolated to $1 \cdot 10^{-12}$ BER is shown in Figure 12. Typically ESD102-U4-05L has capacitance of 0.4pF, which corresponds to

the outermost red curve. Other curves provided for reference. Figure 13 shows timing and voltage bathtubs without (blue) and with (red) ESD102-U4-05L.

More detailed simulation data available upon request.

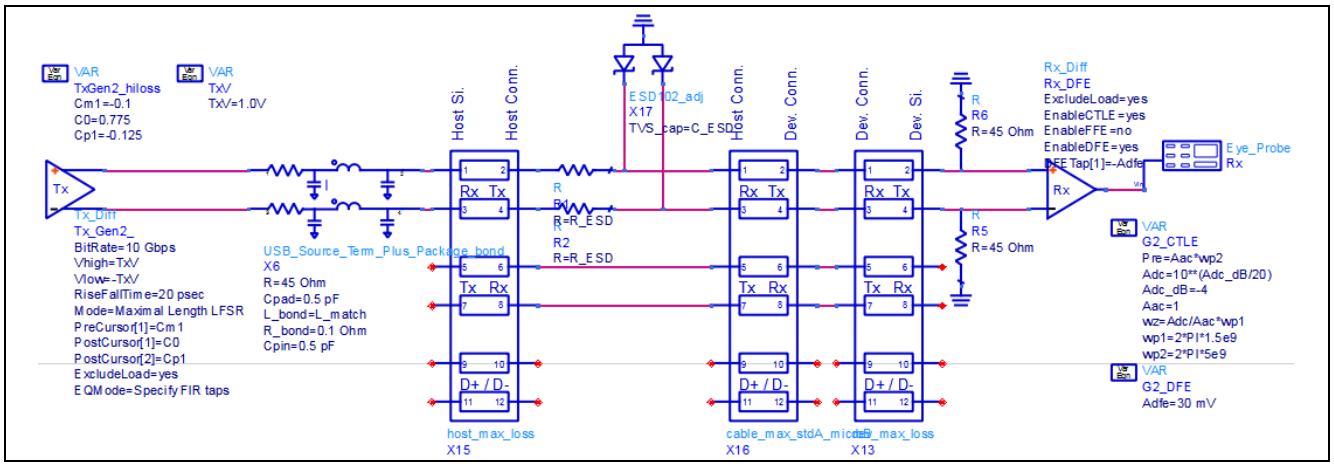


Figure 10 USB3.0/3.1 (Enchanced) SuperSpeed bus model for Transmitter compliance test

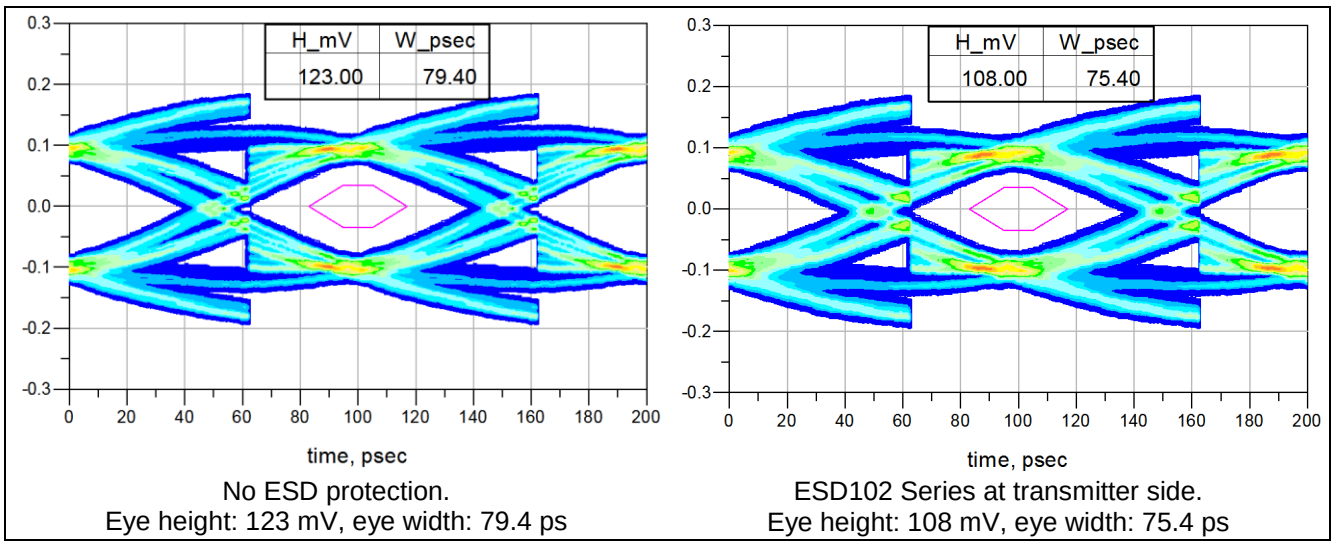


Figure 11 Eye diagram simulated at Rx side of USB3.1 Gen 2 SuperSpeedPlus link, without TVS diode and with ESD102-U4-05L at transmitter side

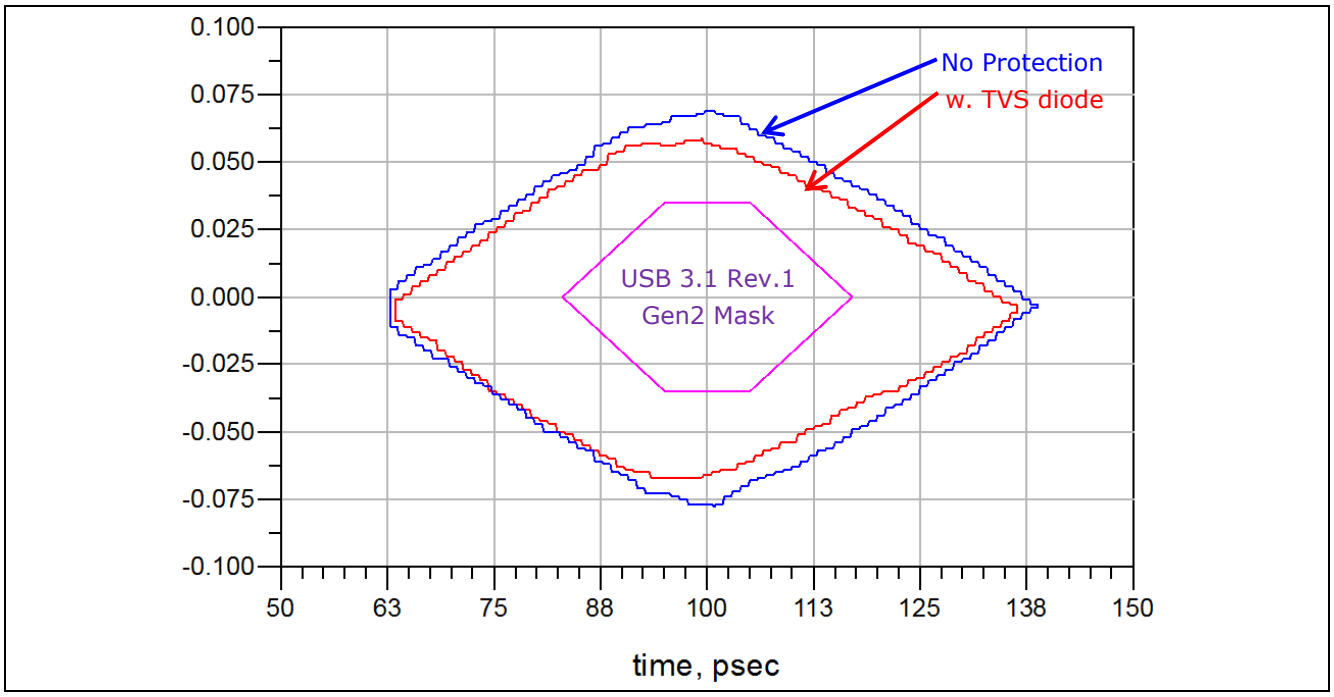


Figure 12 Eye diagram opening simulated at Rx side of USB3.1 Gen 2 SuperSpeedPlus link, without and with protection by ESD-102 Series (C_{ESD102}=0.4pF)

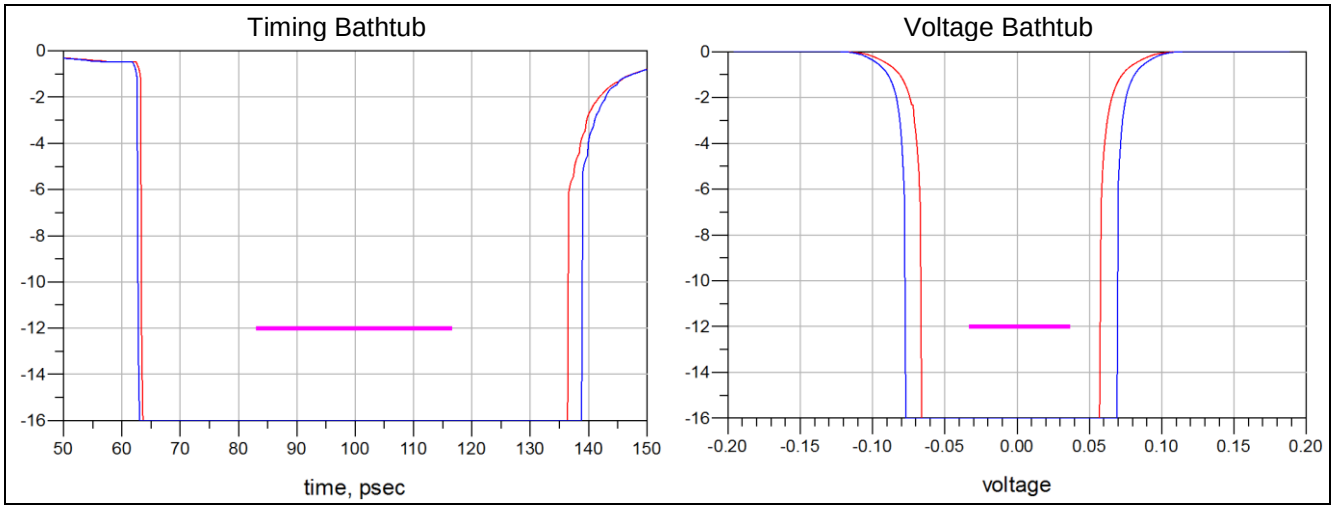


Figure 13 Timing and Voltage bathtubs simulated at Rx side of USB3.1 Gen 2 SuperSpeedPlus link, without TVS diode and with ESD102-U4-05L at transmitter side

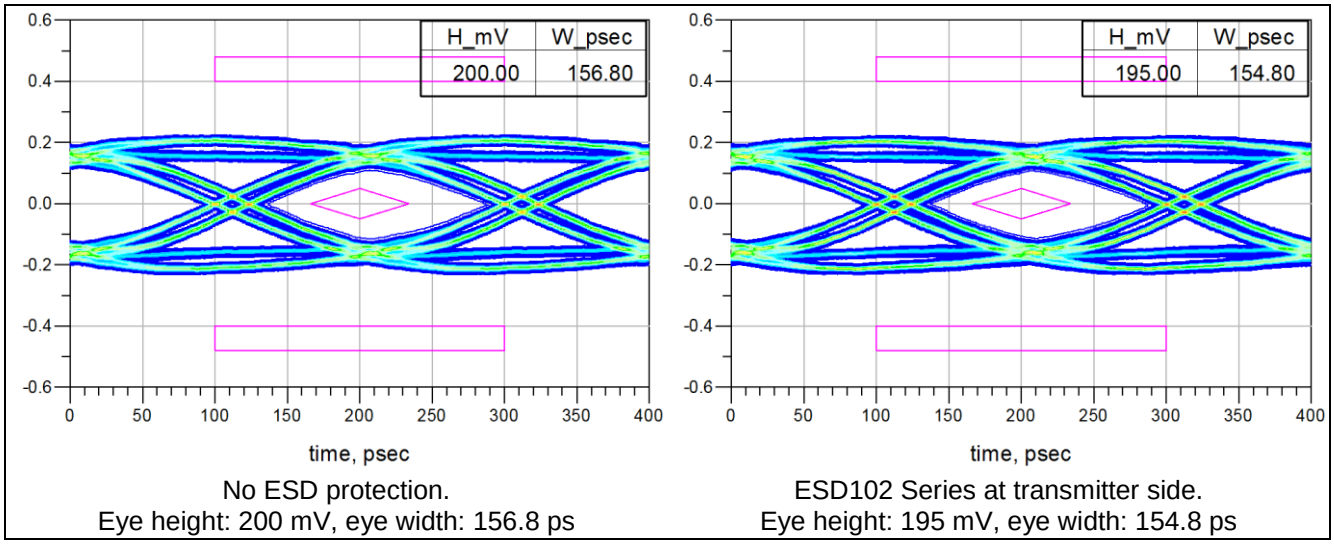
5.3 USB 3.0/USB 3.1 SuperSpeed (5 Gbit/s)

Simulation setup for SuperSpeed link is similar to one described in section 5.2, taking into account difference between Gen.1 and Gen.2 specifications:

- Lower data rate (5 Gbit/s)
- Longer cable (3 m)
- Gen.1 reference CTLE on receiver side
- 4 dB de-emphasis on transmitter side

Simulations showed that ESD102-U4-05L is perfectly suited for USB 3.1 Gen 1 SuperSpeed environment, influencing signal integrity only marginally. Figure 14 shows Eye diagrams of SuperSpeed channel without and with ESD protection. For better comparison, eye opening extrapolated to $1 \cdot 10^{-12}$ BER is shown in Figure 15. Figure 16 shows timing and voltage bathtubs without (blue) and with (red) ESD102-U4-05L.

The measurements conducted at independent pre-compliance test laboratory confirm simulation results (Figure 17).



No ESD protection.
Eye height: 200 mV, eye width: 156.8 ps

ESD102 Series at transmitter side.
Eye height: 195 mV, eye width: 154.8 ps

Figure 14 Eye diagram simulated at Rx side of USB3.1 Gen 1 SuperSpeed link, without TVS diode and with ESD102-U4-05L at transmitter side

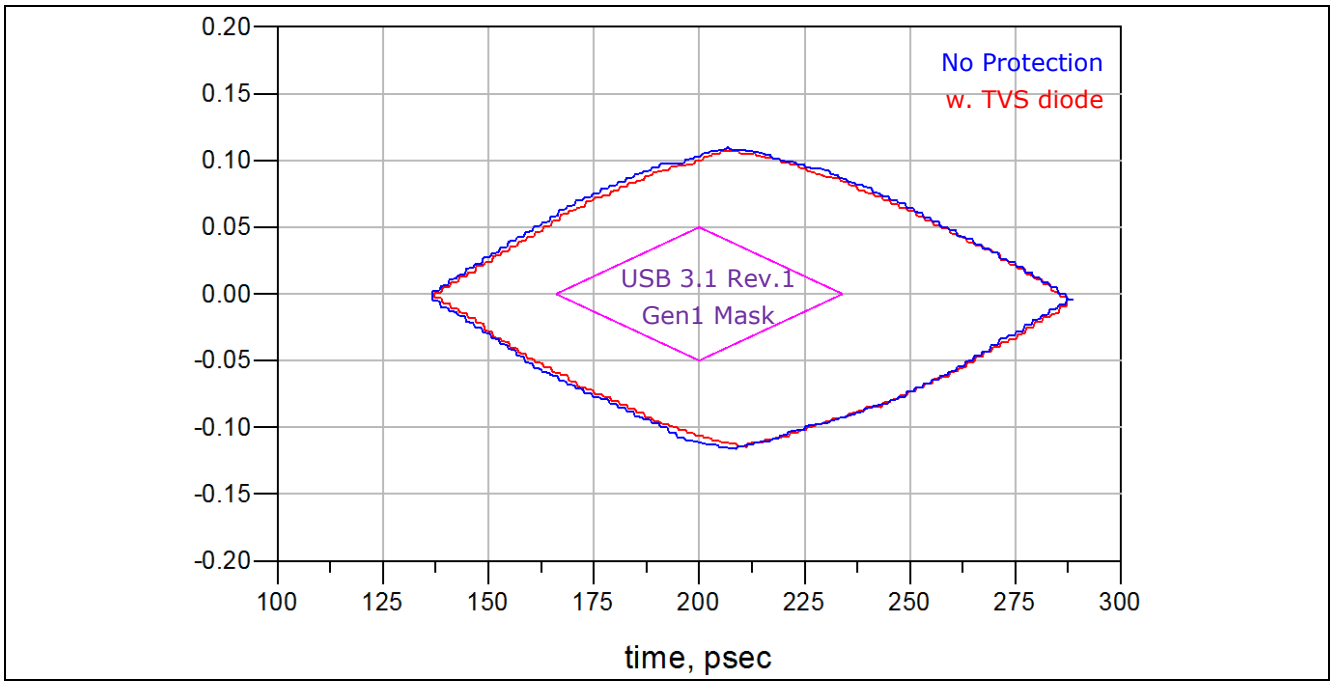


Figure 15 Eye diagram opening simulated at Rx side of USB3.1 Gen 1 SuperSpeed link, without and with protection by ESD-102 Series (C_{ESD102}=0.4pF)

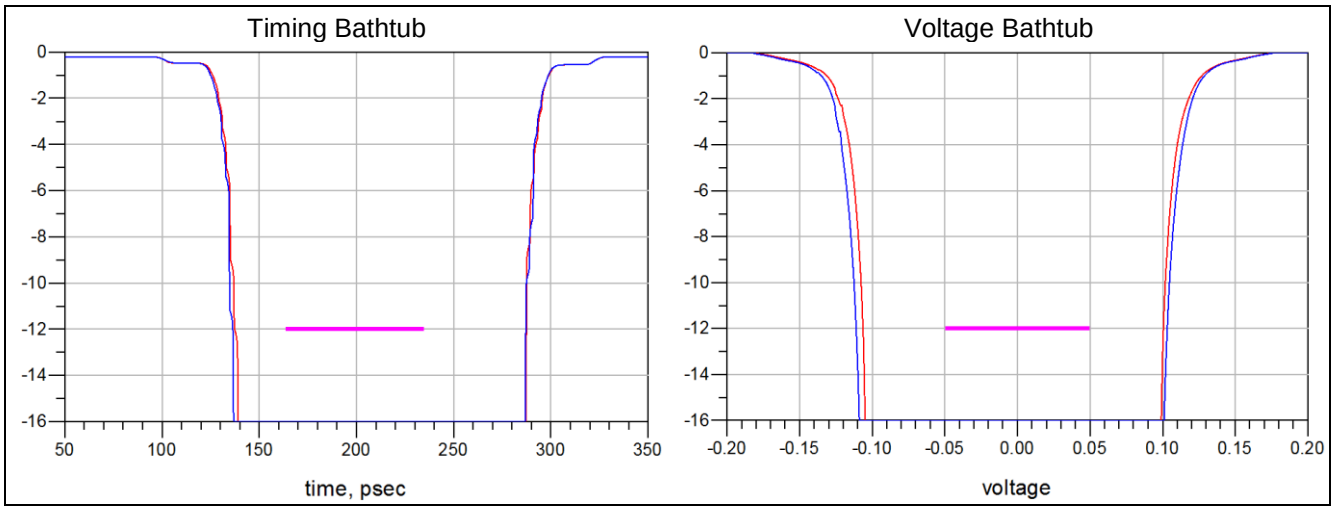
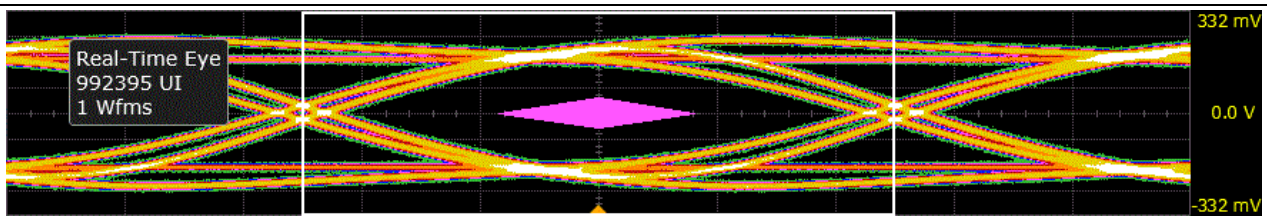
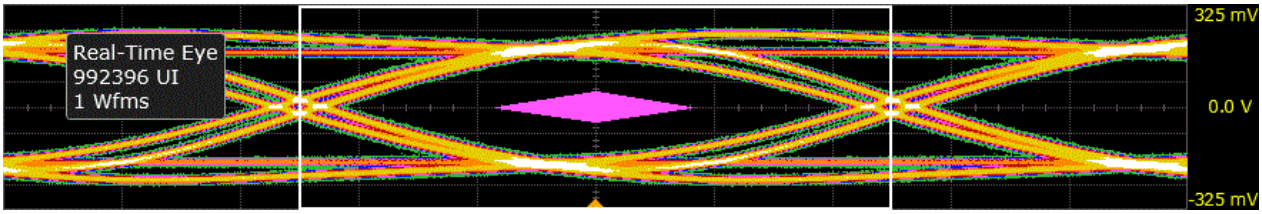


Figure 16 Timing and Voltage bathtubs simulated at Rx side of USB3.1 Gen 1 SuperSpeed link, without TVS diode and with ESD102-U4-05L at transmitter side



No ESD protection. Eye height: 294.00 mV, eye width: 165.35 ps)



ESD102-U4-05L included in USB 3.0 link. Eye height: 294.00 mV, eye width: 165.84 ps)

Figure 17 Eye diagram at Rx side of USB 3.0 link with (top) and w/o (bottom) ESD protection, measured at independent laboratory

6 Summary

It is mandatory to design the USB3.0/USB3.1 link for high system level ESD performance and high Signal Integrity.

This can be best achieved by using:

- Infineon **ESD102-U4-05L, ESD108-B1-CSP0201** for Enhanced SuperSpeed channel
- Infineon **ESD108-B1-CSP0201** for USB 2.0 channel
- Infineon **ESD200-B1-CSP0201** for V_{cc} power supply line

Easy inclusion of those devices in board layout saves costs and development overhead.

7 References

Infineon Technologies AG AN210 — Effective ESD Protection Design at System Level
IEC61000-4-2 — Testing and measurement techniques - Electrostatic discharge immunity test
JEDEC JS-001 — Human Body Model (HBM) - Component Level

8 Authors

Anton Gutsul, Application Engineer of Business Unit “RF and Protection Devices”
Alexander Glas, Principal Engineer of Business Unit “RF and Protection Devices”

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