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High Power Solutions with TO-Leadless

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1 Introduction

Handling high power in a drives application demands an optimized thermal management combined with high-performance MOSFETs.

Modern silicon packaged into the new TO-Leadless allows the designer to reach a higher motor power without the need of excessive parallelization.

Infineon offers with these demoboards a solution for applications like Light Electric Vehicles (µCars, forklifts, E-Scooters) a power platform for first evaluations.

Depending on the overall heat sinking system the Power Boards easily can handle 5kW and more, allowing investigations regarding switching and temperature behavior.

The TO-Leadless (P/PG-HSOF-8-1) is a molded package optimized for high power and high reliability applications. It´s small mechanical dimensions allows compact designs and the high current capability combined with the low thermal resistance ($R_{th(j-c)}$), resulting in lower chip temperatures, enable the designer to go for higher power density and higher reliability.

All mechanical details shown in the following chapters and additionally a general recommendation how to handle Infineon´s SMD devices could be found at www.infineon.com/packages.

Detailed mechanical information about the TO-Leadless (P/PG-HSOF-8-1) is available at TO-Leadless.

General information like datasheets, product brief etc. are available under www.infineon.com/toll.

2 Board description

2.1 Setup

The board offers all necessary power parts to handle several kilowatts. Depending on thermal management and electrical environment much more than 5kW of motor power are possible.

The board contains 3 halfbridges with 5 MOSFETs in parallel per switch. All power paths offer the possibility to connect wires via bolts or screws. Three connectors, each for PLUS and MINUS have to be wired together externally (dotted lines in Figure 2.3). A well suited electrolytic capacitor bank (Low ESR) has to be connected as close as possible to the connectors for PLUS and MINUS.

Depending on the current measurement system additional shunt resistors could be added between the halfbridge´s MINUS contacts and the common MINUS.

Gate resistors are included to optimize the switching speed. If necessary an additional external resistor could be added in the gate drive circuit. Additional source resistors (1Ohm) between the power board and the external driver circuit could avoid high currents between the sources of the halfbridges via the driver board.

R11 is not assembled but offers the possibility to add a NTC or a PTC.

2.2 Mechanical details

Board type	Bergquist Thermal Clad HT, single layer
Copper thickness	105µm/3oz.
Dimensions	102mm*139mm
Aluminum carrier thickness	2mm
Insulator thickness	76µm

Table 2.1: Details

2.3 PCB

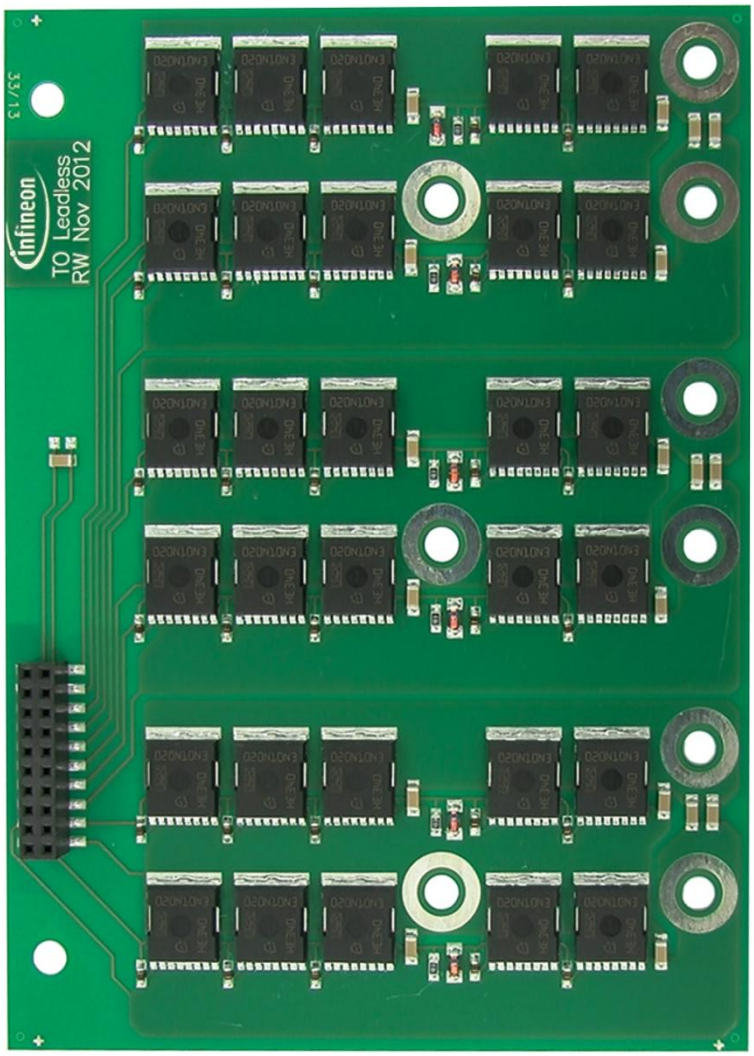


Figure 2.1: PCB, example with IPT020N10N

2.4 Position of assembled parts

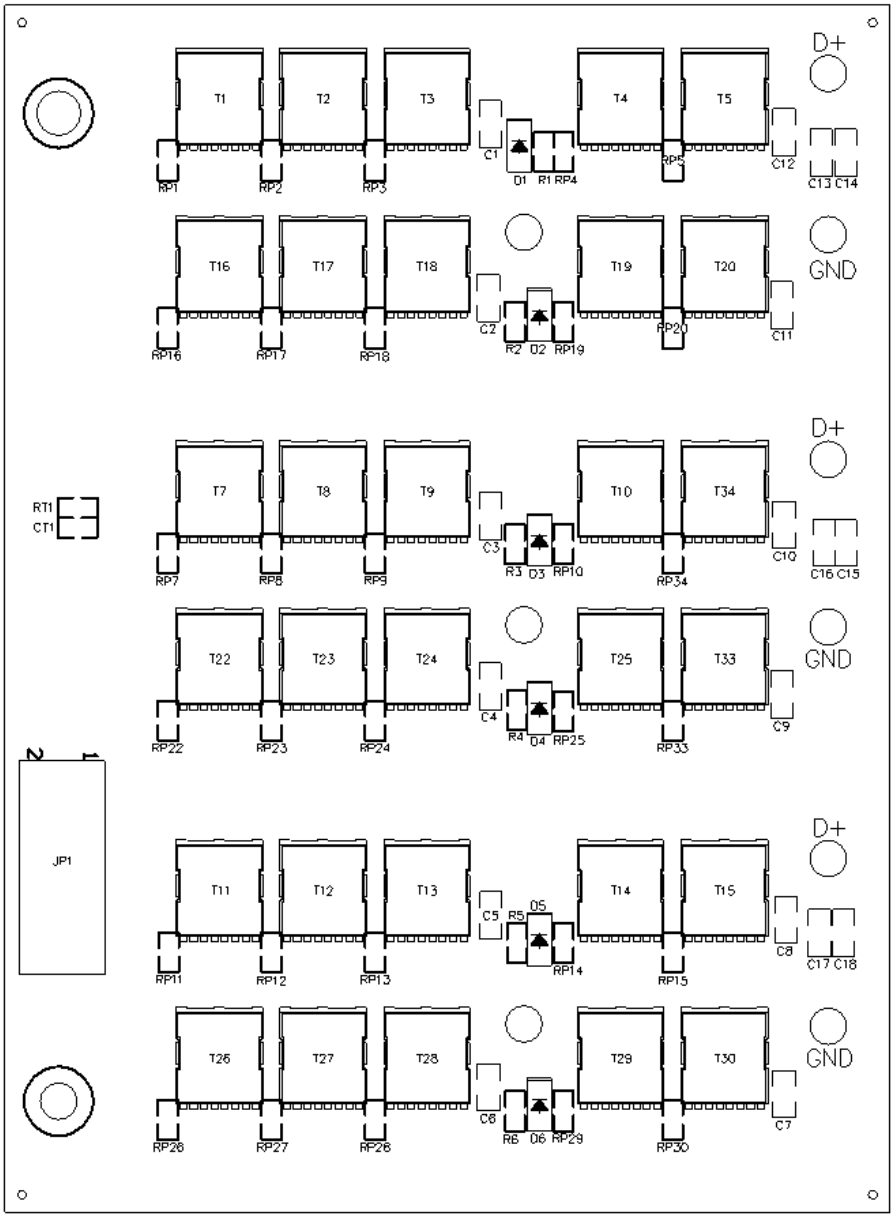


Figure 2.2: Placement

2.5 Copper

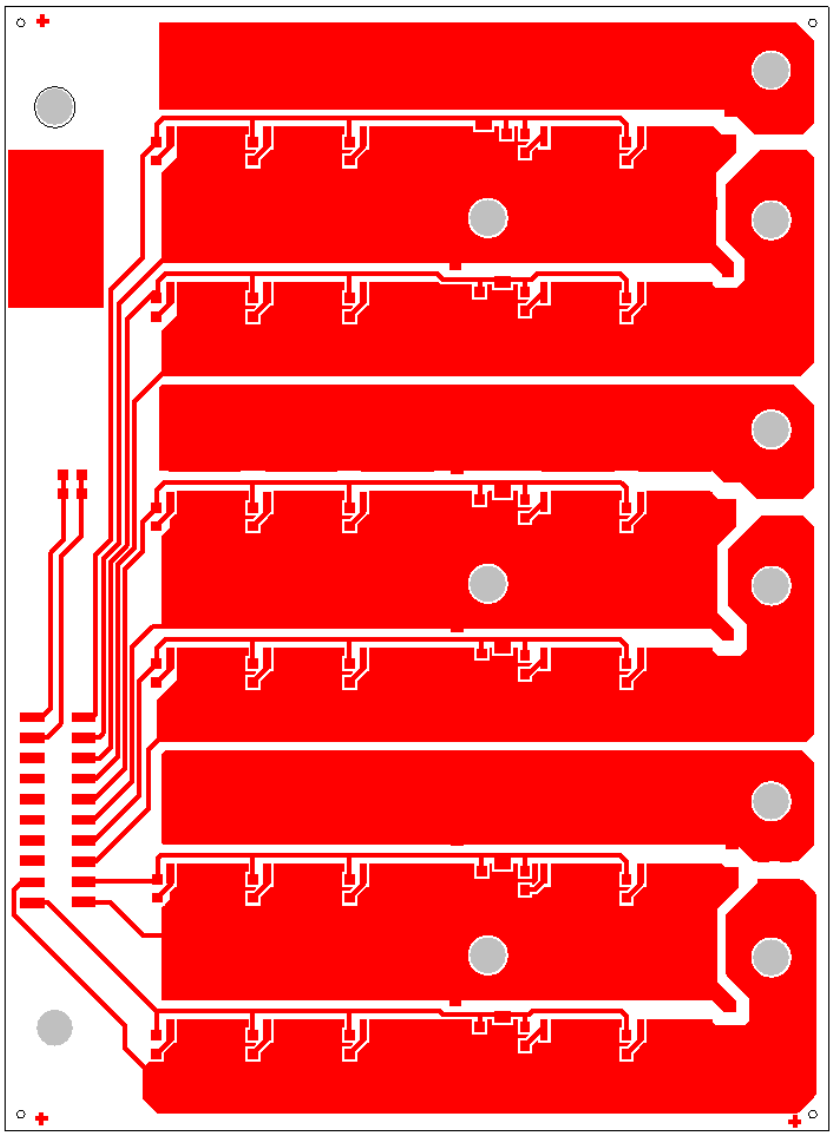


Figure 2.3: Copper tracks, 105µm/30z

2.6 Schematic

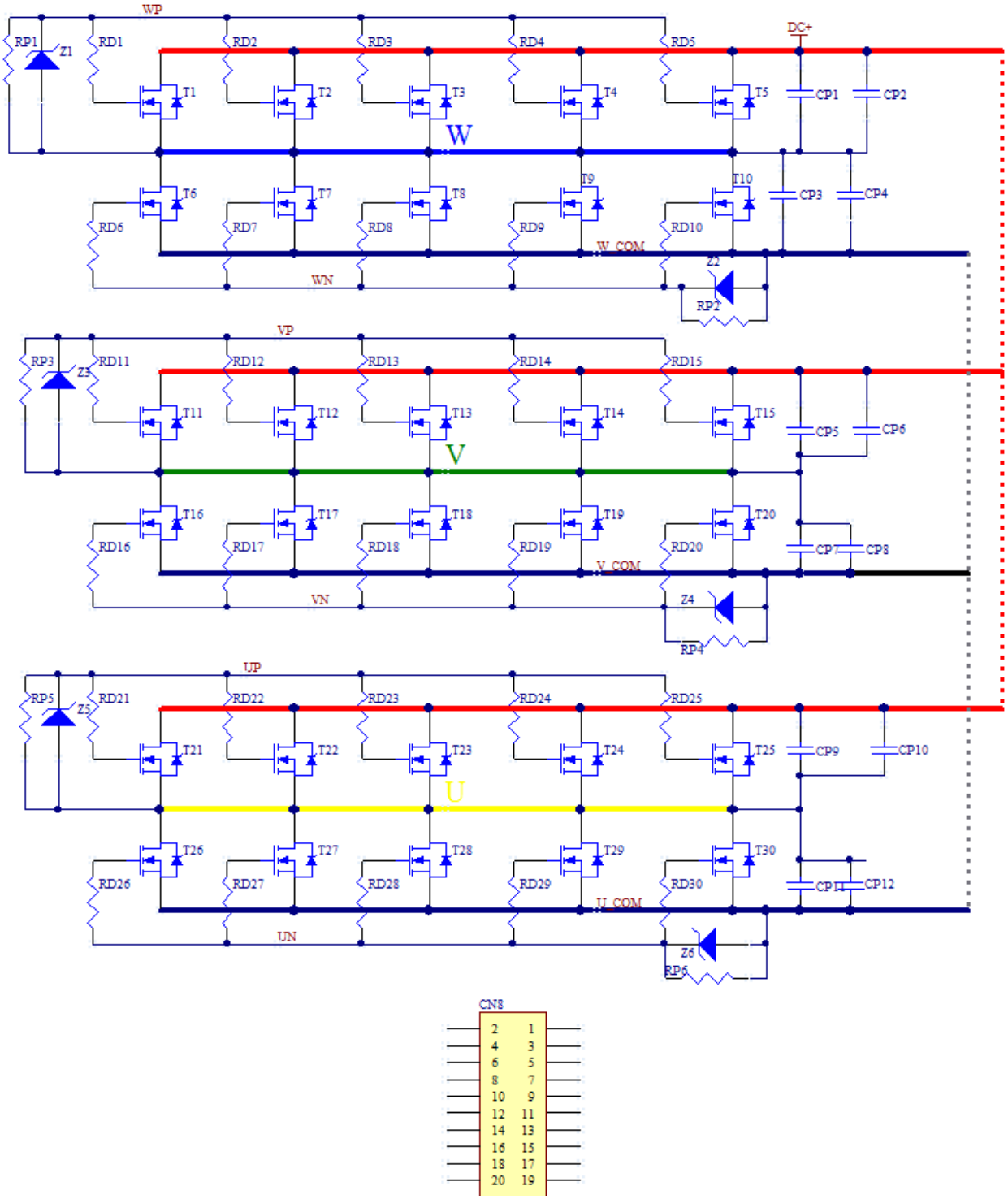


Figure 2.4: Schematic

2.7 Signals

Pin Number	Signal Name	Description
1	WP	Gate High Side “W”
2	---	NTC/PTC R11
3	W	“W”/Source High Side “W”
4	---	NTC/PTC R11
5	WN	Gate Low Side “W”
6	---	N. C.
7	W_COM	Minus “W”
8	---	N. C.
9	VP	Gate High Side “V”
10	---	N. C.
11	V	“V”/Source High Side “V”
12	---	N. C.
13	VN	Gate High Side “V”
14	---	N. C.
15	V_COM	Minus “V”
16	---	N. C.
17	UP	Gate High Side “U”
18	U_Com	Minus “U”
19	U	“U”/Source High Side “U”
20	UN	Gate Low Side “U”

Table 2.2: Signal names and description

3 Bill of Material

3.1 24V/36V version with 60V IPT007N06N

Comment	Description	Designator	Quantity
Header 10X2	Header, 10-Pin, Dual row	CN8	1
100nF/100V	Capacitor	CP1, CP2, CP3, CP4, CP5, CP6, CP7, CP8, CP9, CP10, CP11, CP12	12
1mR	Resistor	R120, R121, R122	3
15R	Resistor	RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24, RD25, RD26, RD27, RD28, RD29, RD30	30
10K	Resistor	RP1, RP2, RP3, RP4, RP5, RP6	6
TO-Leadless	IPT007N06N	T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T24, T25, T26, T27, T28, T29, T30	30
15V	Zener Diode	Z1, Z2, Z3, Z4, Z5, Z6	6

Table 3.1: BOM for 24V/36V input voltage

3.2 48V version with 100V IPT020N10N

Comment	Description	Designator	Quantity
Header 10X2	Header, 10-Pin, Dual row	CN8	1
100nF/100V	Capacitor	CP1, CP2, CP3, CP4, CP5, CP6, CP7, CP8, CP9, CP10, CP11, CP12	12
1mR	Resistor	R120, R121, R122	3
15R	Resistor	RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24, RD25, RD26, RD27, RD28, RD29, RD30	30
10K	Resistor	RP1, RP2, RP3, RP4, RP5, RP6	6
TO-Leadless	IPT020N10N	T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T24, T25, T26, T27, T28, T29, T30	30
15V	Zener Diode	Z1, Z2, Z3, Z4, Z5, Z6	6

Table 3.2: BOM for 48V input voltage

4 Datasheets

4.1 IPT007N06N

IPT007N06N

OptiMOS™ Power-Transistor

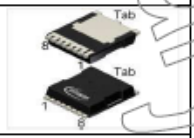
Features

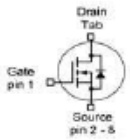
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC [1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	0.75	mΩ
I_D	300	A
Q_{oss}	227	nC
Q_G(0V..10V)	216	nC

RoHS Pb-Free Halogen-Free

Type	IPT007N06N
	
Package	PG-HSOF-8
Marking	007N06N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	300	A
		V_{GS}=10 V, T_C=100 °C	300	
		V_{GS}=10 V, T_C=25 °C, R_{thJA}=40 K/W [2]	52	
Pulsed drain current [3]	$I_{D,pulse}$	T_C=25 °C	1200	
Avalanche energy, single pulse [4]	E_{AS}	I_D=150 A, R_{GS}=25 Ω	1100	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See figure 3 for more detailed information

[4] See figure 13 for more detailed information

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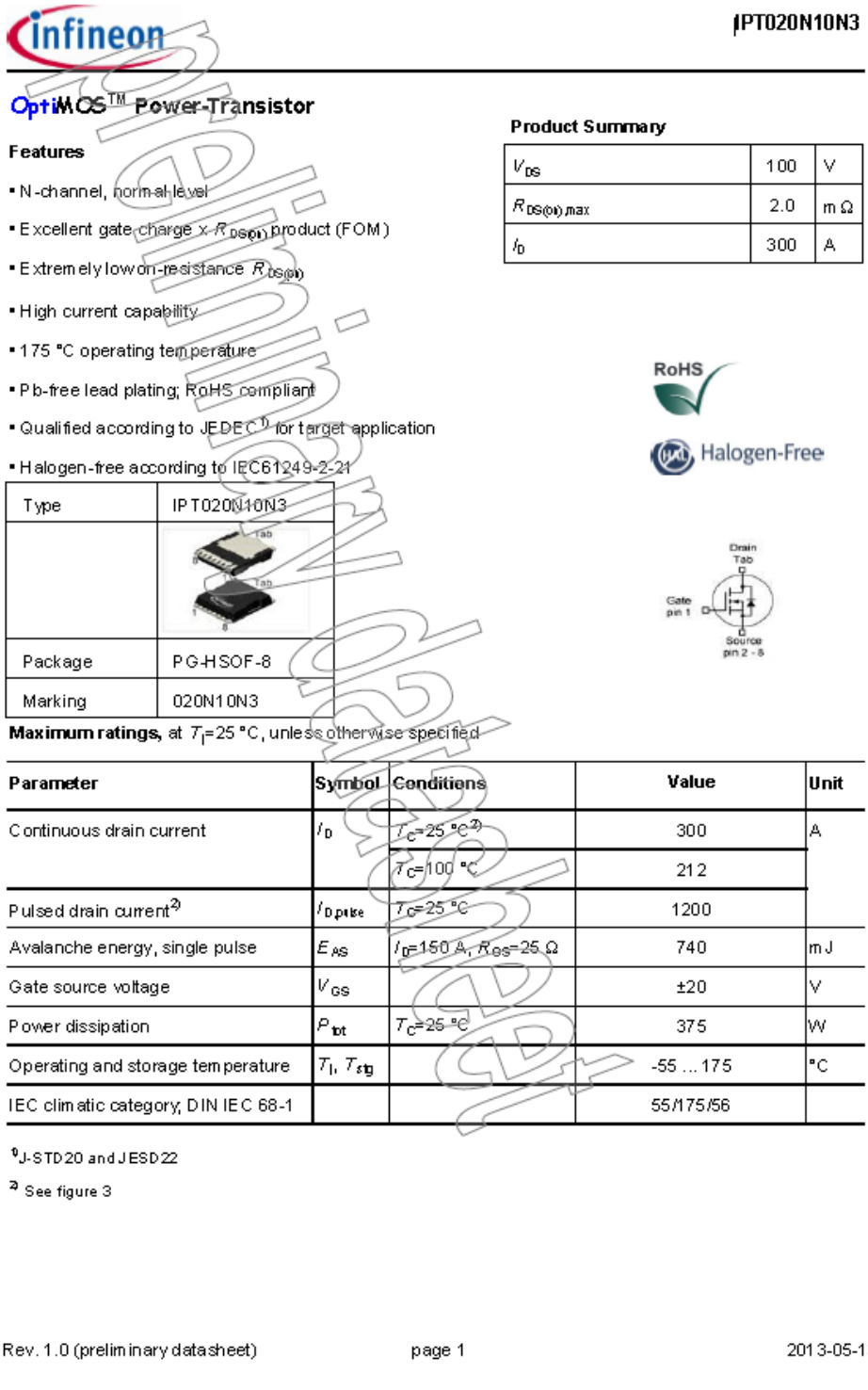
Figure 4.1: First page of datasheet - IPT007N06N

4.2 IPT020N10N



IPT020N10N3

OptiMOS™ Power-Transistor

Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Extremely low on-resistance $R_{DS(on)}$
- High current capability
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	2.0	mΩ
I_D	300	A

RoHS

Halogen-Free

Type	IPT020N10N3
Package	PG-HSOF-8
Marking	020N10N3

Drain Tab, Gate pin 1, Source pin 2 - 8

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	300	A
		T_C=100 °C	212	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	1200	
Avalanche energy, single pulse	E_{AS}	I_D=150 A, R_{GS}=25 Ω	740	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	375	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22

[2] See figure 3

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Figure 4.2: First page of datasheet – IPT020N10N