E I C E D R I V E R™

High voltage gate drive IC

1ED Family

Technical Description

1ED020I12-F2
1ED020I12-B2
1ED020I12-BT
2ED020I12-F2

Application Note

Revision 1.4, 2014-07-01

Infineon Technologies AG

Revision History: 2014-07 Rev.1.4	
Page or Item	
Previous Version: 1.3	

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Last Trademarks Update 2010-06-09

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1 Introduction

1.1 Scope and Product Family

The Infineon EiceDRIVER™ 1ED family is the high voltage gate drive IC with Coreless Transformer (CLT) Technology up to a maximum blocking voltage of 1200V. The EiceDRIVER™ single channel products 1ED020I12-F2 and 1ED020I12-B2 feature desaturation detection (DESAT), active Miller Clamp, undervoltage lockout (UVLO), active shut down, reset input (RST) and ready output (RDY) with functional or basic insulation. The 1ED020I12-BT also supports two-level-turn-off (TLTO) for safe overcurrent shut down. In the 2ED020I12-F2, two independent channels are implemented in a compact package providing the same features as the 1ED020I12-F2. The following Table 1 gives an overview for the EiceDRIVER™ 1ED family.

Product List	Technology	Max. Vol-tage [V]	Input Logic	Features	Basic Isolation*	Typ. UVLO [V]	Pack-age
1ED020I12-F2	Single channel-CLT	1200	pos & neg	RST, DESAT, RDY	–	11 / 12	DSO-16
1ED020I12-B2	Single channel-CLT	1200	pos & neg	RST, DESAT, RDY	X	11 / 12	DSO-16
1ED020I12-BT	Single channel-CLT	1200	pos & neg	RST, DESAT, RDY, TLTO	X	11 / 12	DSO-16
2ED020I12-F2	Dual channel-CLT	1200	pos & neg	RST, DESAT, RDY	–	11 / 12	DSO-36
*according to IEC60747-5-2							

Table 1   Members of 1ED family

This application note will be based on the 1ED020I12-BT since it includes most of the features and a common core functionality to the whole family of devices. Specific references to other 1ED variants will be noted.

1.2 Short Description

The 1ED020I12-BT is a galvanically insolated single channel IGBT driver in PG-DSO-16-15 package that provides an output current capability of typically 2A.

The device consists of two galvanically separated parts. The input chip can be directly connected to a standard 5V DSP or microcontroller with CMOS in/output and the output chip is connected to the power transistor side.

The device is designed to fully protect a power transistor in case of short circuit operation or parasitic influences, which come from the application.

An effective active Miller clamp function avoids the need of negative gate driving in some applications and allows the use of a simple bootstrap supply for the high side driver.

A rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes an IGBT desaturation protection with a FAULT status output.

A two-level turn-off feature with adjustable delay protects against excessive overvoltage at turn-off in case of overcurrent or short circuit condition. The same delay is applied at turn-on to prevent pulse width distortion.

A READY status output reports if the device is supplied and operates correctly.

2 Technical Description of 1ED020I12-BT

The following chapter describes functionality of the 1ED020I12BT in detail.

2.1 Power Supply

2.1.1 IC Supply Voltage

The supply voltage of the IC must reach initially at least a typical voltage of V_{UVLOH1}=4.1V and V_{UVLOH2}=12V for the input supply (VCC1) and output supply (VCC2) respectively, before the IC gets into an operational state. This is necessary in order to have a sufficient supply voltage for correct driving of the gate.
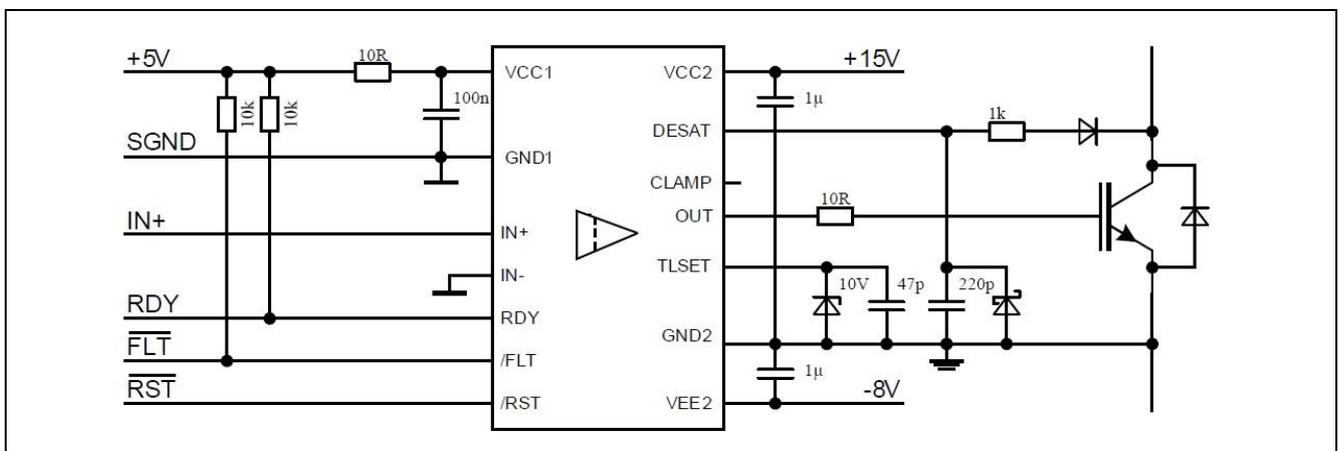
Figure 1   Typical application example bipolar supply

The 1ED020I12-BT offers the possibility of two types of supply topology: bipolar supply and unipolar supply as shown in Figure 1 and Figure 2. The pin GND2 is the reference ground of the output chip. VEE2 pins are the negative power supply pins of the output chip. If no negative supply voltage is available, both VEE2 pins have to be connected to GND2.
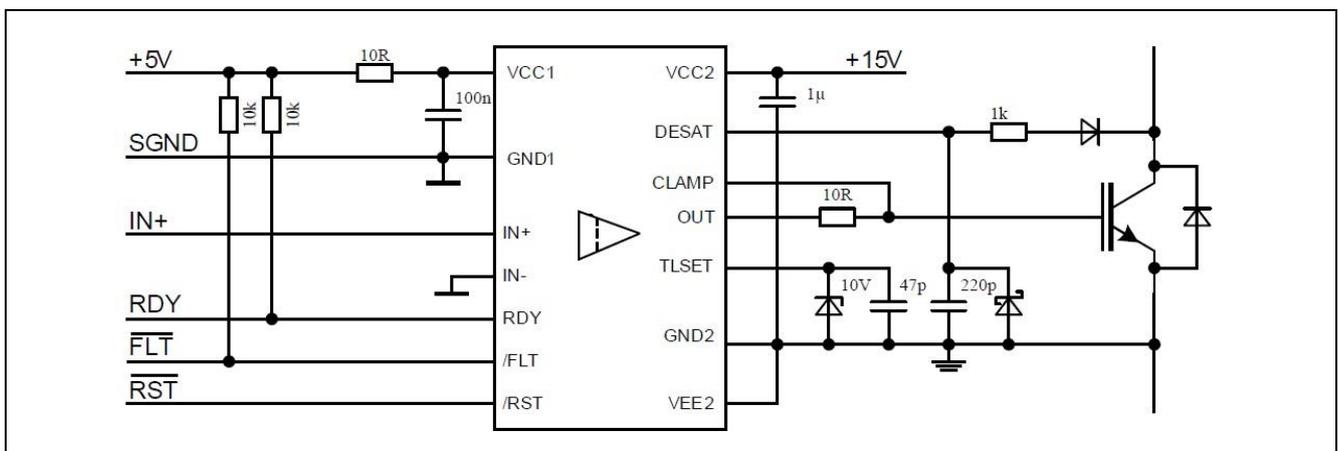
Figure 2   Typical application example unipolar supply

Although the maximum positive output side power supply V_{VCC2} is 20V and the minimum negative output side power supply V_{VEE2} is -12V (both reference to GND2), the actual maximum output side power supply voltage is V_{max2}=28V (V_{VCC2}-V_{VEE2}). Figure 3 shows the supply voltage range and the recommended range.
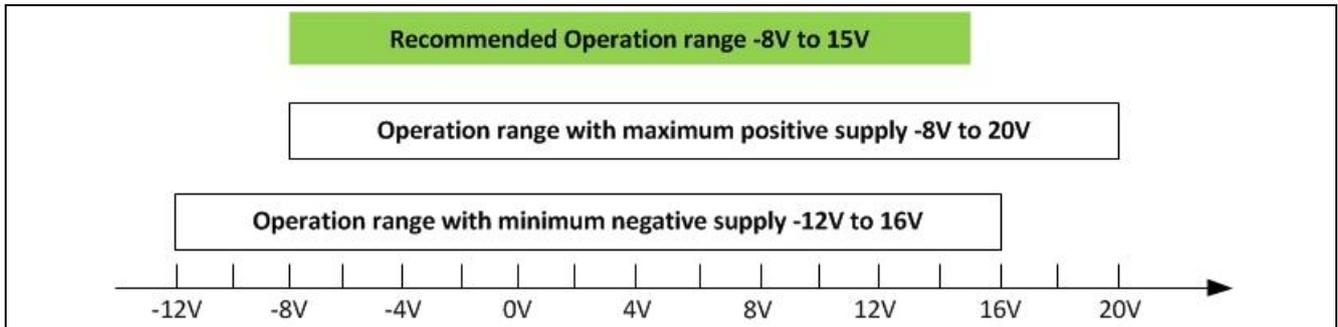
Figure 3   Supply voltage range

The recommended capacitor value for VCC1 is 100nF, and for VCC2/VEE2 is 1µF. They should be placed as close as possible to the power pins VEE2 and VCC2. Otherwise, parasitic circuit elements may lead to voltage spikes, which may trigger the undervoltage lockout threshold.

2.1.2   Undervoltage Lockout (UVLO)

The IC shuts down the individual gate drives, when the related supply voltage is below V_{UVLOL1}=3.8V and V_{UVLOL2}=11V for the lowside and highside supply respectively. This ensures correct switching of IGBTs. In case of an UVLO shut down, it is necessary to reach the start-up levels of V_{UVLOH1}=4.1V and V_{UVLOH2}=12V again to initialize the IC.

2.1.3   Bootstrap Circuit

A bootstrap circuit is a common and cost efficient technique to supply a floating high side driver section in a halfbrige configuration. Shown in Fig 4 below.

The supply voltage in IGBT based half bridge configurations is usually in a range of 15V to 18V. The supply voltage is also applied to the gate of the IGBT. This is sufficient in order to drive IGBT properly. The bootstrap capacitor should be large enough to support the I_{Q2} (Quiescent Current Output Chip in datasheet) of high side driver chip and also the gate charge of high side IGBT. Please consider different switching sheme to give enough margins for the bootstrap capacitor, so that the voltage can be stable in periods.
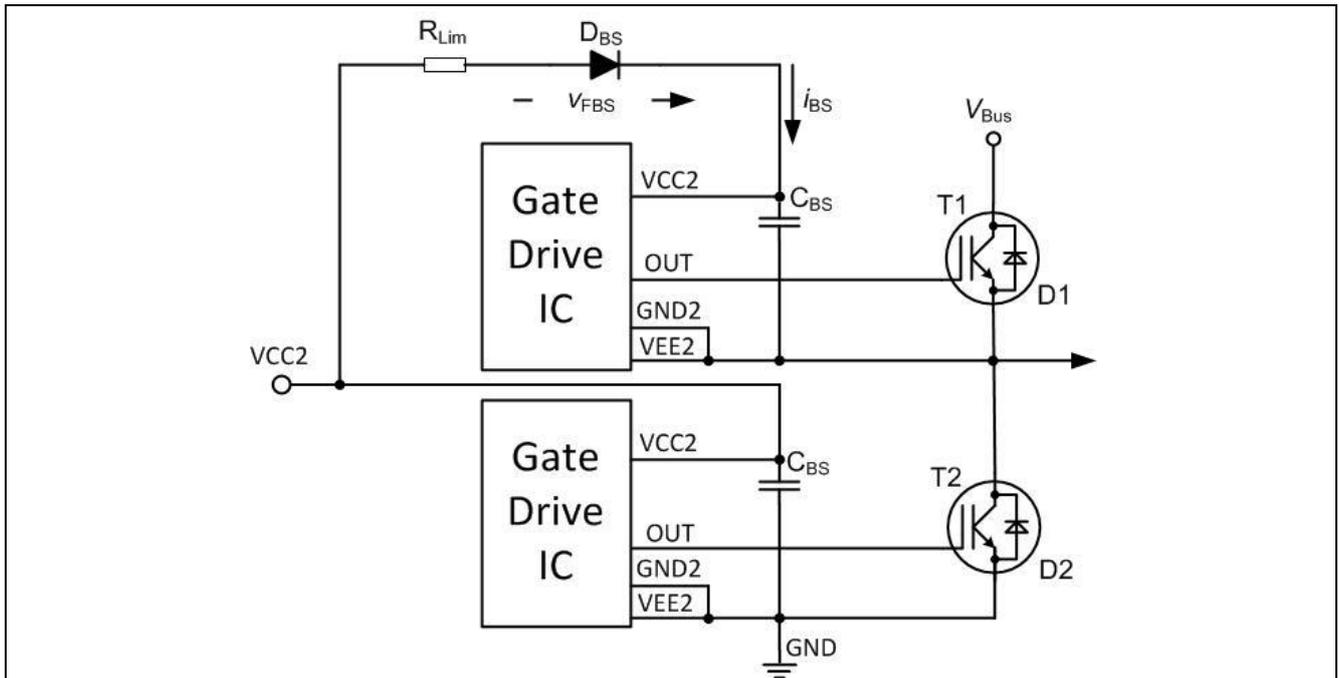
Figure 4   Bootstrap circuit for halfbridge

The turn on of transistor T2 will force the reference potential GND2 of high side drive IC to ground. It leads to a charging current i_{BS} into the capacitor C_{BS}. The current i_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor.

The reference potential GND2 of high side drive IC is high again when the current commutates from transistor T2 or diode D2 into transistor T1. At this time the bootstrap diode D_{BS} blocks a reverse current, so that the charge will remain in the capacitor C_{BS}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin VCC2 and 15V supply and should therefore have the same voltage rating as the driven power transistors. The voltage of the bootstrap capacitor can now supply the highside gate drive section.

The voltage of bootstrap capacitor is approximately

$$V_{BS} \approx V_{CC} - V_{FBS}$$ (1)

A current limiting resistor R_{Lim} reduces the peak of the pulse current during the turn-on of transistor T2. The pulse current will occur at each turn-on of transistor T2, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor can be used at higher switching frequencies. Please note here, that the current limiting resistor R_{Lim} (10Ω is recommended) must therefore endure both types of stresses: the rms current stress and the worst case pulse load stress (e.g. at the initial charging of C_{BS}). The bootstrap capacitor is mainly discharged by two effects: the highside quiescent current and the gate charge of the transistor to be turned on. The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{I_{Q2\_max} \cdot t_P + Q_{G\_max}}{\Delta V_{BS}}$$ (2)

with I_{Q2_max} being the maximum quiescent current of the output chip, t_P the switching period, Q_{G_max} the maximum total gate charge value and ΔV_{BS} the voltage drop at the bootstrap capacitor within a switching period.

Please note here, that Equation (2) is valid for continuous switching operation according to the switching frequency. The recommended bootstrap capacitance is in the range up to 10µF for IGBT current ratings up to 40A at a switching frequency of 20kHz. It is a general design rule for the location of bootstrap capacitors, that they must be placed as close as possible to the IC.

2.1.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply. That means, even with 200mA forced current, the pin OUT will be lower than 2V, which is used to prevent the IGBT from turning on unintentionally.

2.2 Input Logic

There are two possible input modes to control the IGBT. At non-inverting mode the signal at pin IN+ controls the driver output while IN- is set to low according to Figure 5. At inverting mode the signal at pin IN- controls the driver output while IN+ is set to high.
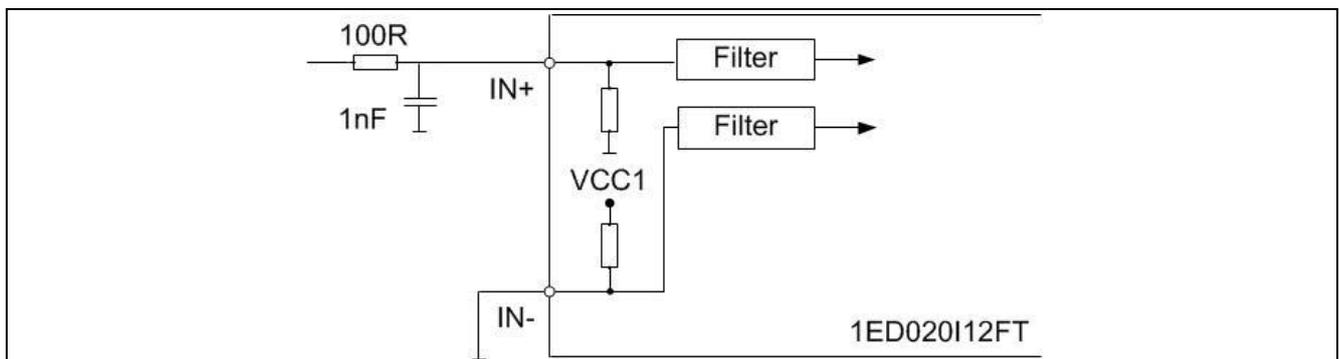

Figure 5   Example for non-inverting mode input including RC filter

The IN+ input logic has an integrated pull-down resistor and IN- input logic has an integrated pull-up resistor, this design is for safety reasons in case of input pin floating or driven from a high impedance source.

A HIGH level is identified, when the input is higher than 3.5V, and a LOW level is identified by input is lower than 1.5V. This setting of level provides a full compliance to 5V CMOS-level as referring to [1]. The maximum input bias current is 400µA for IN+ and IN-.

Figure 5 shows an example for non-inverting mode input. In this case, the input signal of driver IC is connected to IN+ pin through a RC-filter to reduce the influence from electromagnetic interference, which may cause distorsion of the input signal. Meanwhile the IN- pin needs to be grounded to ensure the non-inverting mode input. The RC-filter needs to be placed as close as possible to input logic pin.

A minimum input pulse width (~40ns) for both on and off states is defined to filter occasional glitches. This is called input pulse suppression timing. This means, that an input signal must stay on its level for this period of time in order that the state change is processed correctly. Otherwise the change in the status of the input signal will be ignored and the output keeps its state.

The internal pull-up/pull-down resistor (12.5kΩ ~ 50kΩ) can be calculated according to the datasheet and the according test condition

2.3 Driver Output

2.3.1 Basic Feature

The 1ED020I12-BT is designed for operation of IGBTs and MOSFETs up to a rating of 1200V, and the output capability of 1ED020I12-BT is +/- 2A for driving IGBT up to 100A directly. The output pin (OUT) is switched between VEE2 and VCC2. In normal operating mode V_{OUT} is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT) V_{OUT} is set to VEE2 independent of the input control signals.
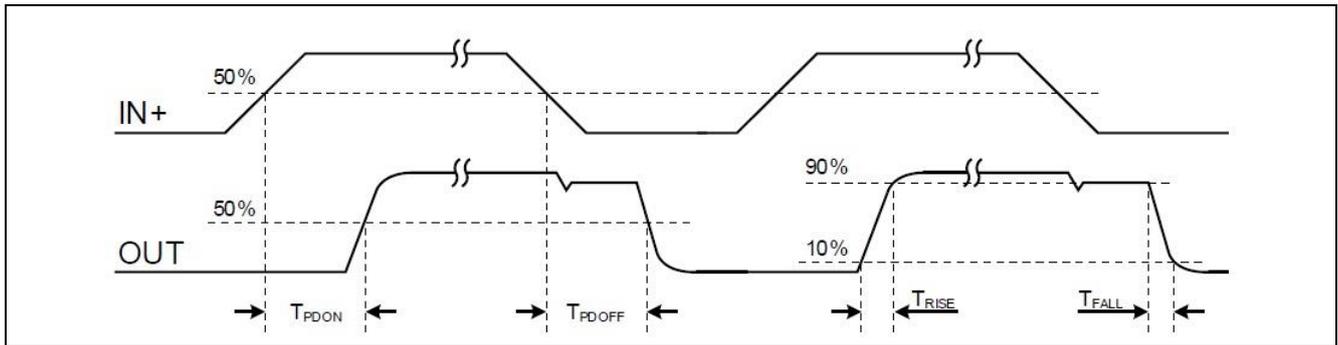
Figure 6   Propagation delay, Rise and Fall time

As shown in Figure 6, the intervals T_{PDON} and T_{PDOFF} are the propagation delay between the input pins IN+, IN- and the ouput pin OUT. The mismatch between T_{PDON} and T_{PDOFF} is called propagation delay distortion $T_{PDISTO} = T_{PDOFF} - T_{PDON}$. The propagation delay and rise/fall time all depend on the load which is connected with the driver IC (for IGBT, it is the gate input capacitance). The propagation delay distortion T_{PDISTO} will have the influence to the duty cycle of the driver output signal which finally also influence the application. Besides this, the T_{PDISTO} also influences the dead time which is used to avoid shoot through.

2.3.2   Short Circuit Clamping

The IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance during short circuit. An additional protection circuit connected to VCC2 and OUT limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10 µs may be fed back to the supply through one of these paths. If higher currents are expected or a tighter clamping is desired external diodes D_{Cl} may be added as shown in Figure 7.
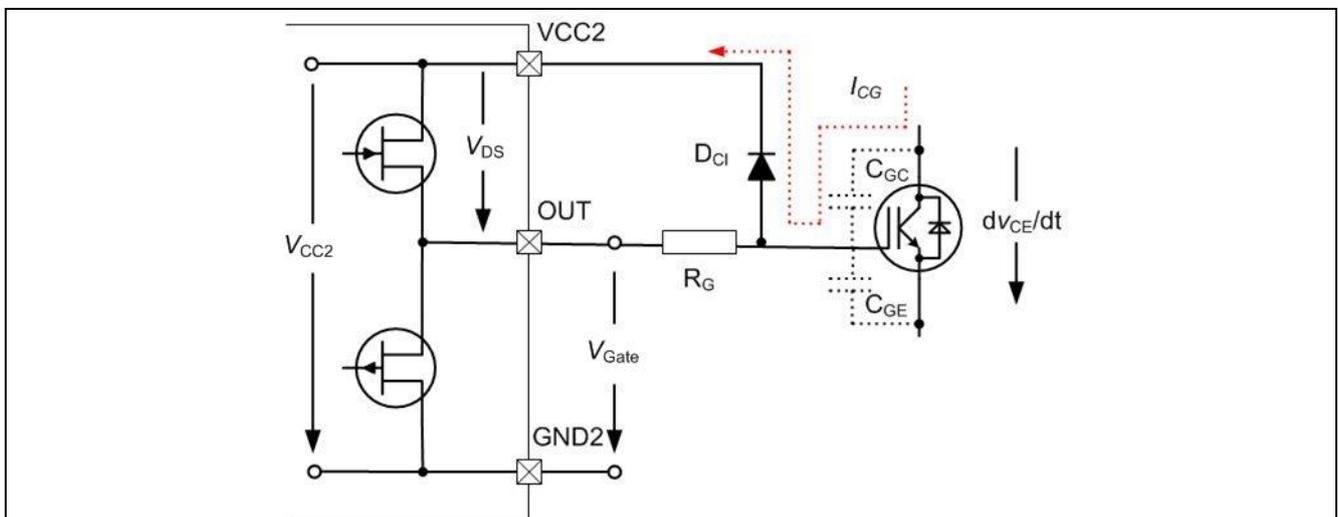
Figure 7   Short circuit clamping to VCC2, but without additional protection between OUT and CLAMP

In case of short circuit, dv_{CE}/dt due to short circuit tries to pull up gate terminial of the IGBT via its reverse capacitance C_{GC}, while the gate terminal is decoupled from gate driver IC by the gate resistor R_G. The increased gate terminal voltage opens the IGBT channel even more and increases the short circuit current further. Clamping is necessary and done by diode D_{CL}, which will effectively clamp the IGBT gate to VCC2 in case of short circuit and limit the short circuit current.

2.3.3 Rail-to-rail Output

The output driver section uses PMOS and NMOS to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop V_{DS} which is provided by PMOS and NMOS as shown in Figure 8, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.
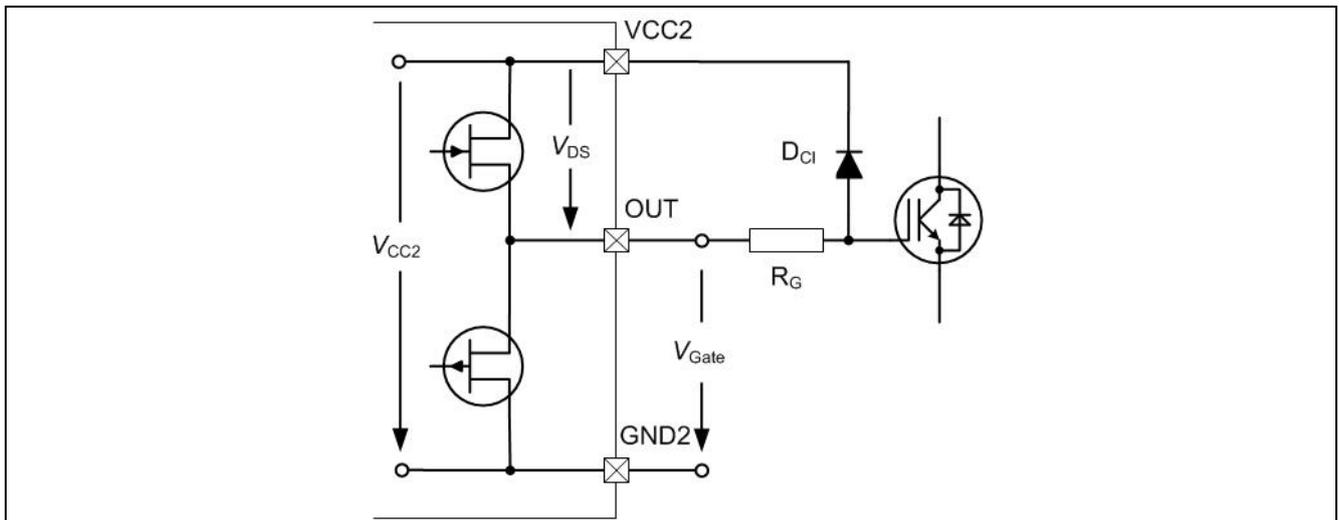

Figure 8   Rail-to-rail output

Increasing the gate voltage is a widely used method to overcome the potential voltage drop V_{DS} in the IC and to improve the conduction capability of the IGBT. Rail-to-rail output ensures, that output supply voltage V_{CC2} is given to the gate by almost 100% ($V_{Gate} = V_{CC2}$). No remaining voltage at the upper or lower gate drive transistor (e.g. no higher supply voltage is needed for achieving 15V at the gate). This feature is also important for the short circuit situation. When the IGBT gate is clamped to VCC2 by diode D_{CL}, the gate voltage will be limited to output supply voltage V_{CC2} plus the diode voltage. The lower V_{CC2} supply voltage the driver can use, the lower gate voltage can be limited and the safer the IGBT will be in short circuit situation.

2.3.4 Gate Resistor

The switching speed of the power device (e.g. IGBT) can be controlled by sizing the gate resistors which control the turn-on and turn-off gate currents. Small gate resistance value leads to fast switching which results in lower switching loss. The minimal gate resistance value is limited by the maximum gate driver output current I_{OUT_max} which is 2.4A for 1ED020I12-BT according to datasheet.

$$R_{\text{total\_min}} = \frac{VCC2 - VEE2}{I_{OUT\_max}} \tag{3}$$

here the $R_{\text{total\_min}} = R_{Gon} + R_{DriverH} + R_{Gint}$, R_{Gon} is the gate on-resistance, $R_{DriverH}$ is the driver output resistance during driving high (derived from driver datasheet) and R_{Gint} is the IGBT integrated gate resistor value (from IGBT datasheet).

The voltage change $-dv_{CE}/dt$ and the current change di_C/dt during the turn-on process may be influenced by varying the gate resistor R_{Gon}. Increasing the gate resistor reduces the voltage and current changes, which will lead to better EMI/EMC performance. It is always a trade-off between EMI/EMC, parasitic turn-on and switching loss. For detail discussion on the influence of gate resistance please refers to [2].

In many applications separated turn-on and turn-off resistors are used as shown in Figure 9. Choosing $R_{Goff} < R_{Gon}$ is due to the reason that for IGBT the turn-off delay time is normally larger than turn-on delay time, meanwhile it can also help to prevent a capacitive turn-on via the Miller capacitance. On the other hand, if the R_{Goff} value is too small, it could lead to big voltage overshoot across IGBT as explained in section 2.3.5 and

section 2.4. So it is always a trade-off inbetween. Depending on the individual parameters, R_{Goff} can be roughly half of the R_{Gon} value.
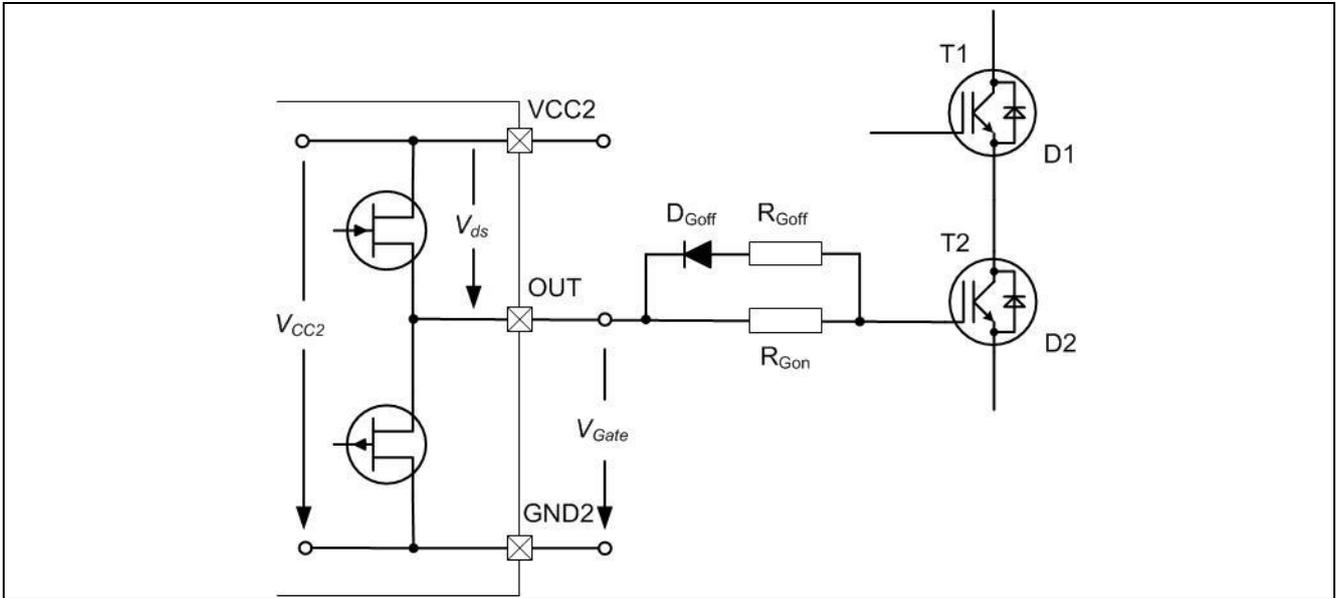
Figure 9   Gate resistors

2.3.5   Two-Level Turn-Off (1ED020I12BT only)

The Two-Level Turn-off is only available for 1 family member, which is 1ED020I12BT. This feature is user configurable and enabling a soft turn-off during short circuit. There will be a large voltage overshoot across the IGBT under short circuit condition, if the gate voltage is removed abruptly. This voltage overshoot could exceed the IGBT breakdown voltage, which could finally damage the IGBT.

The Two-Level Turn-Off introduces an additional turn off voltage level V_{ZDIODE} (as shown in Figure 10) at the driver output in between ON- and OFF-level. This additional level ensures lower V_{CE} overshoots at turn off by reducing gate emitter voltage of the IGBT in short circuits. The lowered V_{GE} level is limiting the current of the IGBT during the additional level interval T_{TLSET}, the required timing value is depending on stray inductance and di/dt at beginning of two level turn off interval.
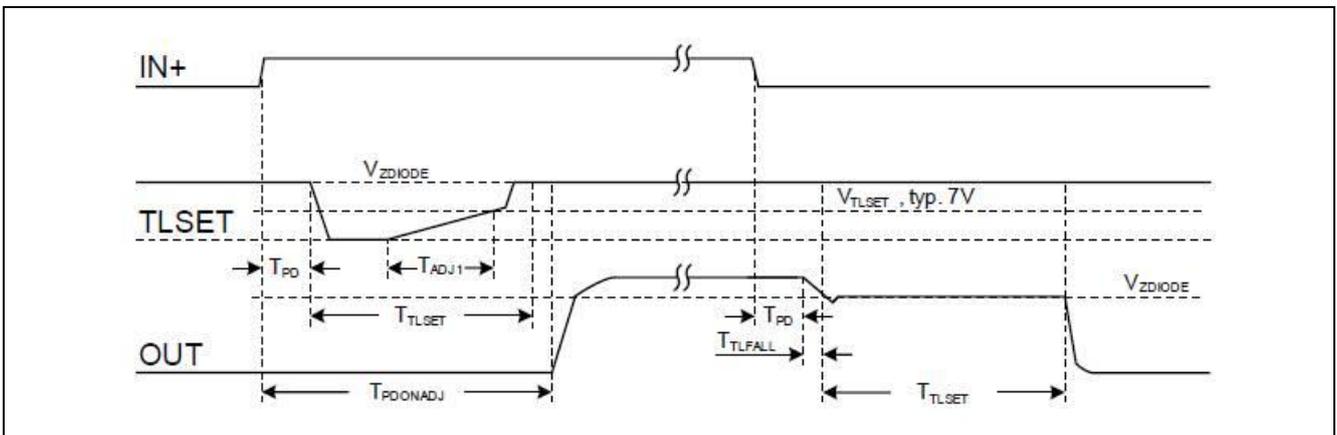
**Figure 10   Two-Level Turn-Off switching behaviour**

The additional turn off voltage level V_{ZDIODE} and hold up time T_{TLSET} could be adjusted at TLSET pin as shown in Figure 11. The V_{ZDIODE} is set by the external Zener diode D_{TLSET} connected between pin TLSET and GND2. The interval T_{TLSET} is set by the external capacitor C_{TLSET_ext} connected to the same pin TLSET and GND2.
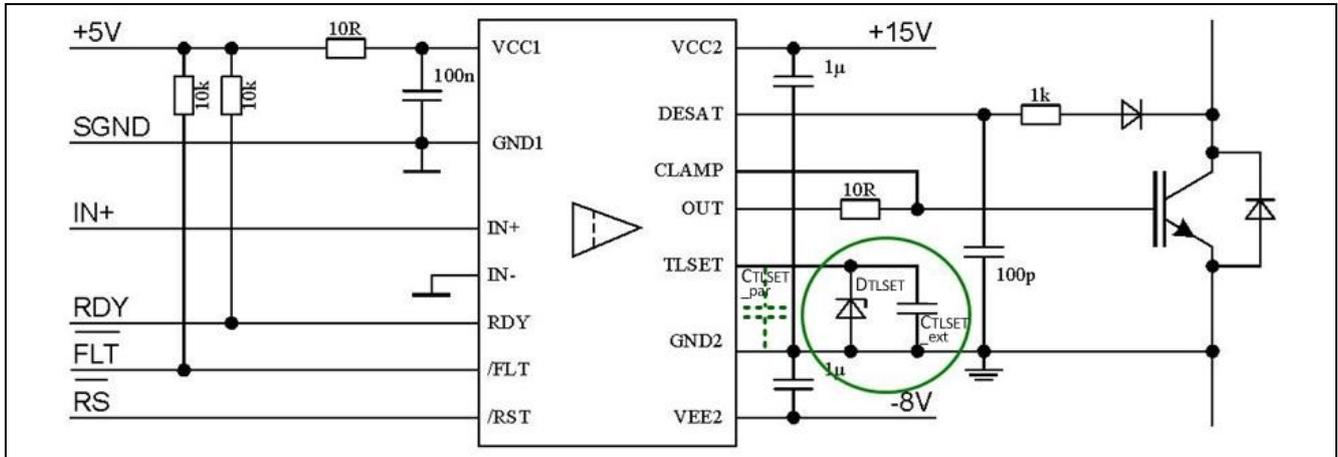
Figure 11   TLSET pin connection

Please be aware that the effective hold time T_{TLSET} at the additional turn off voltage level V_{ZDIODE} is defined by the total capacitance connected at pin TLSET including capacitance C_{TLSET_ext} of the external capacitor, parasitic wiring capacitance C_{TLSET_par} and junction capacitance $C_{Zenerdiode}$ of Zener diode as shown in the following equation.

$$C_{TLSET} = C_{TLSET\_ext} + C_{zener\ diode} + C_{TLSET\_par} \qquad (4)$$

With calculated C_{TLSET} value, the actual hold time T_{TLSET} at the additional turn off voltage level V_{ZDIODE} can be derived according to Figure 12.
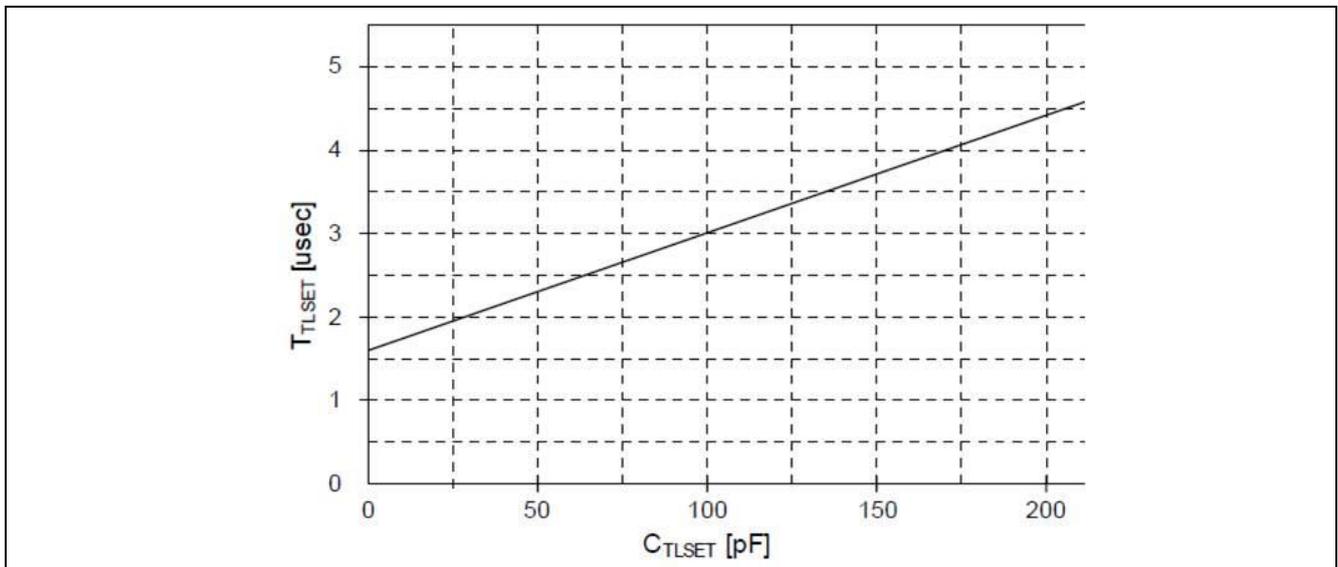
Figure 12   Typical T$_{TLSET}$ time over C$_{TLSET}$ capacitance

To leave enough margin for C$_{TLSET\_ext}$ and latter also C$_{DESAT}$ (DESAT capacitance which will define DESAT sensing time), it is recommended to choose Zener diode with small junction capacitance and small C$_{TLSET\_ext}$ (even without, according to application), e.g. the junction capacitance of the BZX384 series 10V Zener diode is already 90pF which could even be the dominating portion of the while C$_{TLSET}$ value. The placement of C$_{TLSET}$ and D$_{TLSET}$ should be close to TLSET pin to reduce the parasitic wiring capacitance.

Since the Zener diode D_{TLSET} defines the additional turn off voltage level, the selection of this Zener diode should depend on the IGBT device property. Normally the gate voltage level which fits to the nominal collector current is recommended as the Zener diode voltage. This can be derived from the IGBT output characteristic as shown in Figure 13.
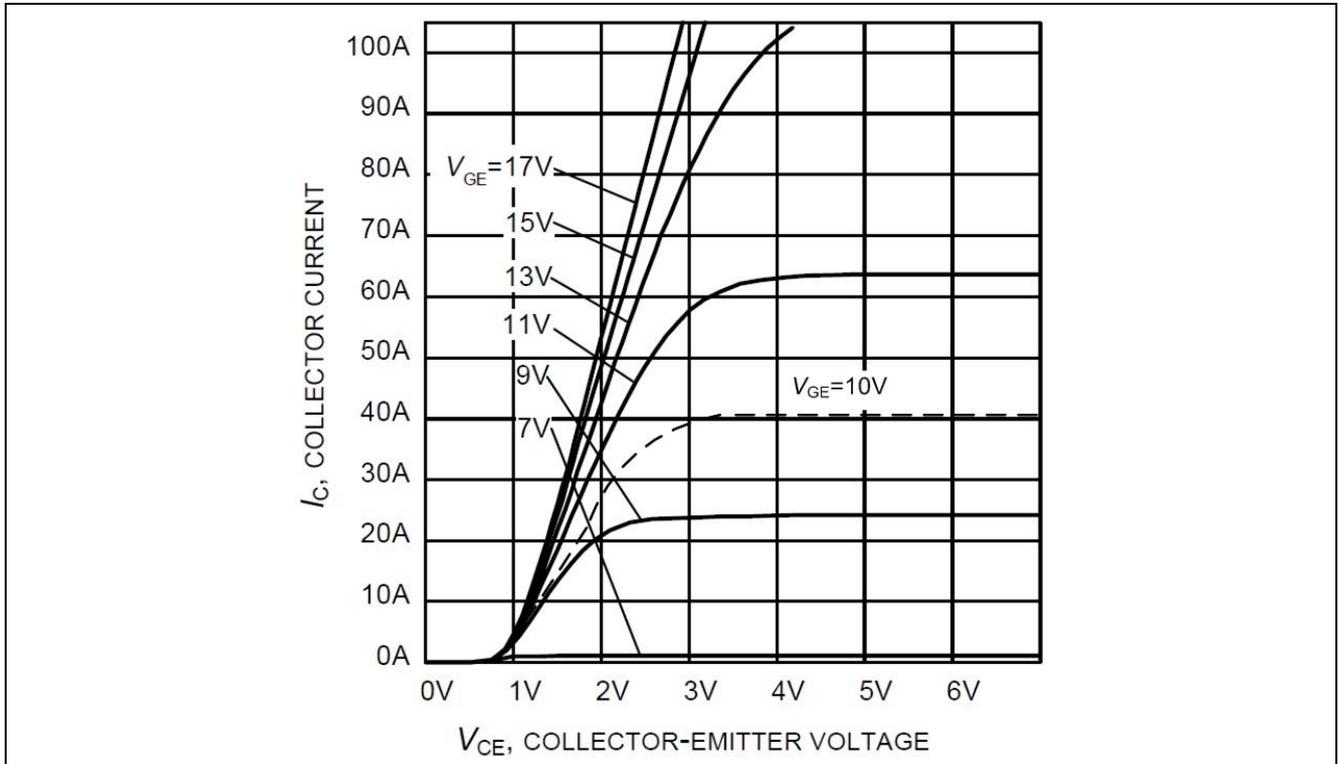

Figure 13   Output characteristic of Infineon IKW40T120 IGBT

In this example the Infineon IKW40T120 IGBT has a 40A nornimal collector current, and this will refer to 10V V_{GE} gate voltage which is derived with interpolation method according the IGBT output characteristic (dashed line in Figure 13). This voltage can be used to select the Zener diode voltage.

As shown in Figure 10, when a switch on signal is given the IC starts to discharge C_{TLSET} (voltage level of TLSET signal is decreasing). Discharging C_{TLSET} is stopped after 500nsec. Then C_{TLSET} is charged with an internal charge current I_{TLSET} (voltage level of TLSET signal is increasing). When the voltage of the capacitor C_{TLSET} exceeds 7V a second current source starts charging C_{TLSET} up to the voltage of Zener diode V_{ZDIODE}. At the end of this discharge-charge cycle the gate driver is switched on.

The time between IN+ initiated switch-on signal (minus an internal propagation delay of approximately 200ns) and switch-on of the gate drive is sampled and stored digitally as pre-sampled time. It represents the Two-Level Turn-Off set time T_{TLSET} during switch-off.

If switch off is initiated from IN+, IN- or /RST signal, the gate driver is switched off immediately after internal propagation delay of approximately 200ns and V_{OUT} begins to decrease. The output voltage V_{OUT} is sensed and compared with the Zener voltage V_{ZDIODE}. When V_{OUT} falls below the reference voltage V_{ZDIODE} of the Zener diode the switch off process is interrupted and Vout is adjusted to V_{ZDIODE} for the pre-sampled Two-Level Turn-Off time T_{TLSET} (to produce close pulse matching). OUT is switched to VEE2 after the hold up time has passed.

For switch off initiated by short circuit current detection DESAT (refer to section 2.4), the gate driver switch off is delayed by desaturation sense to OUT delay $T_{DESATOUT}$. After $T_{DESATOUT}$, input signal will be ignored and the Two-Level Turn-Off sequence is started immediately as shown in Figure 14. In this case, there will be no pulse matching anymore.
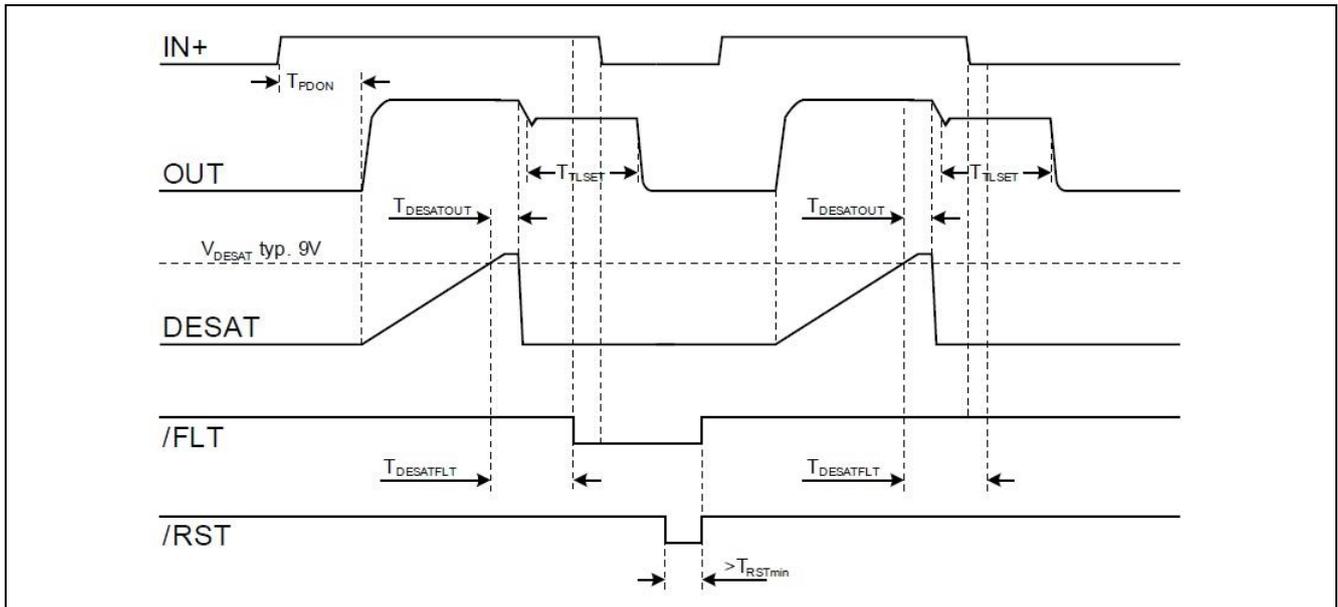
Figure 14   Two-Level Turn-Off under DESAT condition

Due to the Two-Level Turn-Off feature, the 1ED020I12-BT driver requires minimal on and off time for proper operation in the application. Minimal on time from IN+/IN- must be greater than the T_{TLSET}, shorter on time will be suppressed as shown in Figure 15.
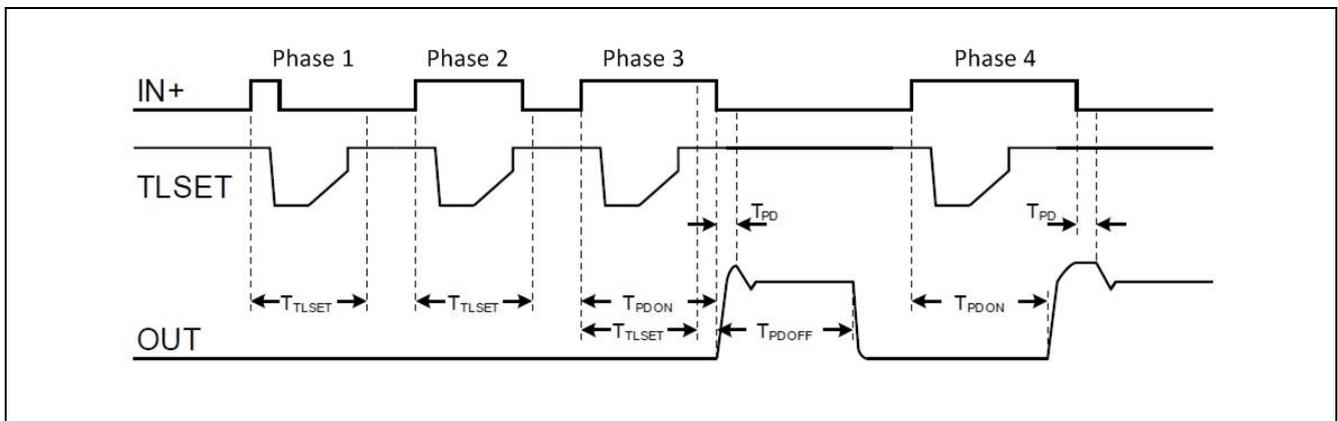
Figure 15   Short switch ON pulses

Due to the short on time (e.g. Phase 1 and Phase 2 in Figure 15), the driver does not turn on. A similar principle takes place for off time.
Minimal off time must also be greater than T_{TLSET}, shorter off times (e.g. Phase 2 in Figure 16) will be suppressed, which means OUT stays as it is.
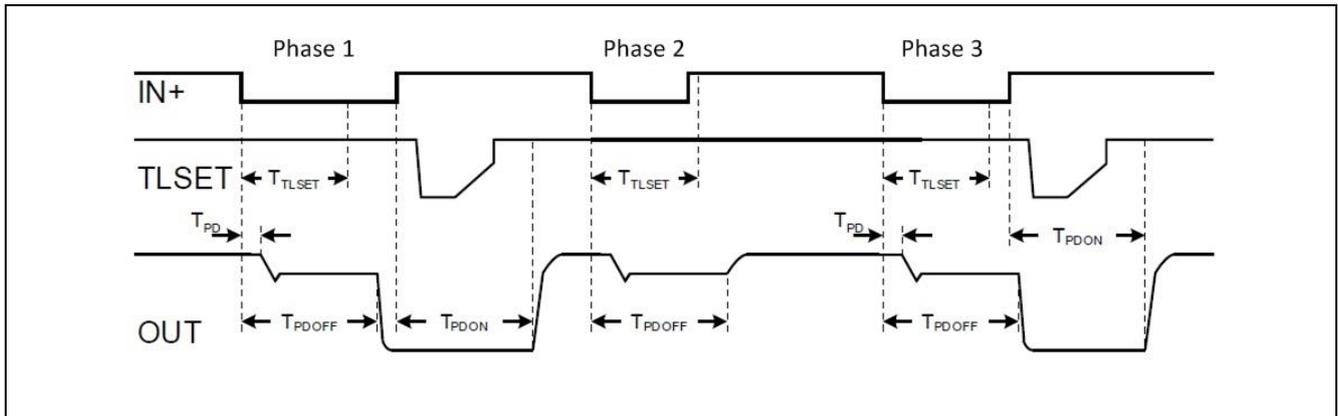
Figure 16   Short switch OFF pulses

A two level turn off plateau cannot be shortened by the driver. If the driver has entered the turn off squence it cannot quit due to the fact, that the driver has already entered the shut off mode. But if the driver input signal is turned on again, it will leave the lower level after T_{TLSET} time by switching OUT to high, as shown in Figure 17.
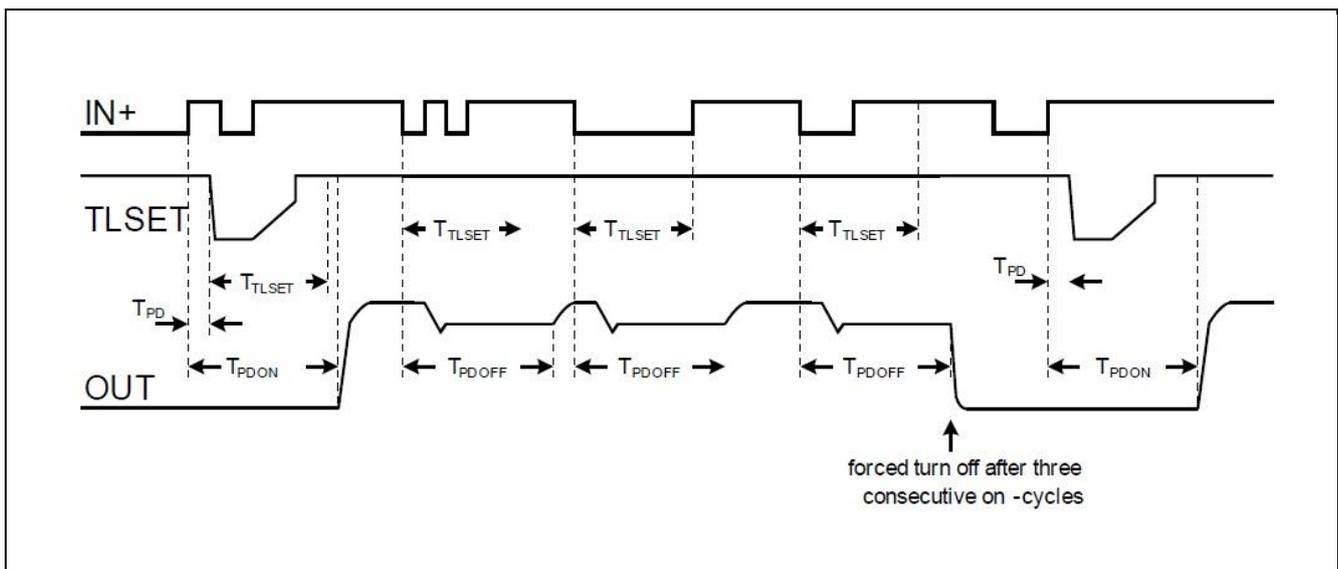
Figure 17   Short switch OFF pulses, ringing suppression

The Two-Level Turn-OFF function can not be disabled.

2.3.6   Booster Design

Some applications require the external booster circuit at the driver output. As shown in Figure 18, one complementary pair of transistors is used to amplify the driver ICs signal. This allows driving IGBTs that need more current than the driver IC can deliver. The NPN transistor is used for switching the IGBT on and the PNP transistor for switching the IGBT off.
The transistors are dimensioned to have enough peak current to drive 600V or 1200V IGBT. Peak current can be calculated like in following equation

$$I_{peak} = \frac{\Delta V_{out}}{R_{Gint} + R_G + R_{DriverH}} \tag{5}$$
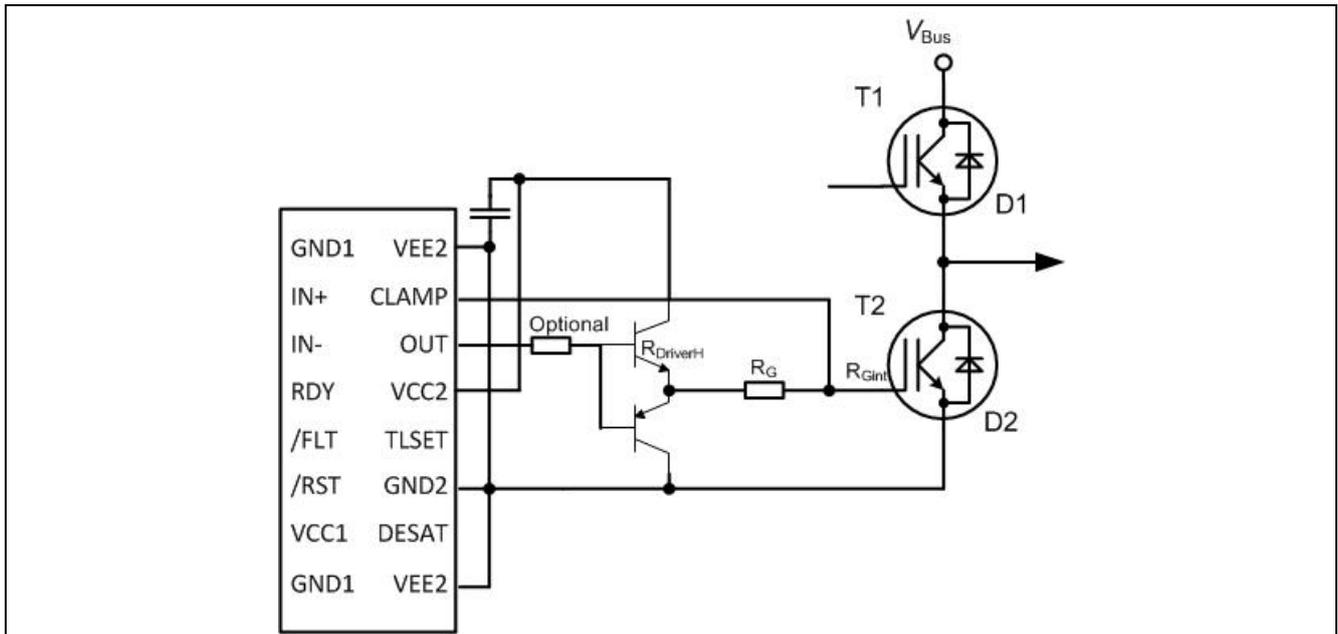
Figure 18   External booster design with clamp function and unipolar supply

Gate resistors are connected in between booster stage and IGBT gate connection. For some applications the value for these resistors is 0 Ohm. In this case just a jumper is required. If resistors are needed ensure that these resistors have a suitable rating for repetitive pulse power to avoid degradation.

2.4   DESAT

A desaturation protection ensures the protection of the IGBT at short circuit (current larger than 5 times rated value, not for over-current). The DESAT pin of the 1ED-family monitors the collector-emitter voltage (V_{CE}) of the IGBT to detect desaturation caused by short circuits. When the DESAT voltage goes up and reaches a defined value, the output of the driver chip is driven low. Further, the FAULT output is activated. A programmable blanking time $T_{DESATBLANK}$ is used to allow enough time for IGBT saturation during normal turn on operation. Blanking time is provided by a highly precise internal current source and an external capacitor.
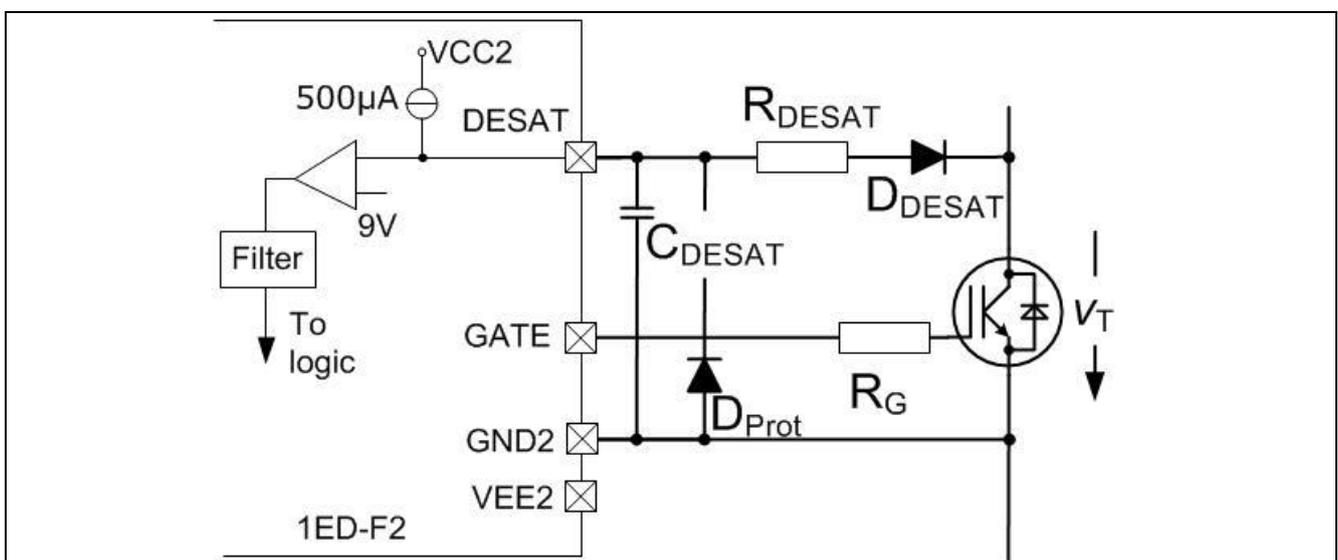

Figure 19   DESAT circuit

As shown in Figure 19, fault detetion circuit monitors the IGBT's emitter to collector voltage V_{CE}. A high current in IGBT may cause the transistor to desaturate and this condition results in an increase of V_{CE}. Due to the presense of diode D_{DESAT}, an internal current source I_{DESAT} (500µA with 10% tolerance) will start to charge up the external capacitor C_{DESAT}, When the DESAT voltage at C_{DESAT} goes up and reaches the DESAT reference level V_{REF_DESAT} (9V), the gate is turned off by the logic blocks of the output section.

A protective diode D_{Prot} at DESAT vs GND2 is recommended to limit negative voltage to DESAT input, which is not allowed to go below -0.3V according to the absolute maximum ratings. The diode D_{DESAT} should be chosen accordingly to IGBT collector-emitter absolute maximum ratings, low stray capacitance and low recovery current (in order to minimize noise coupling and switching delays).
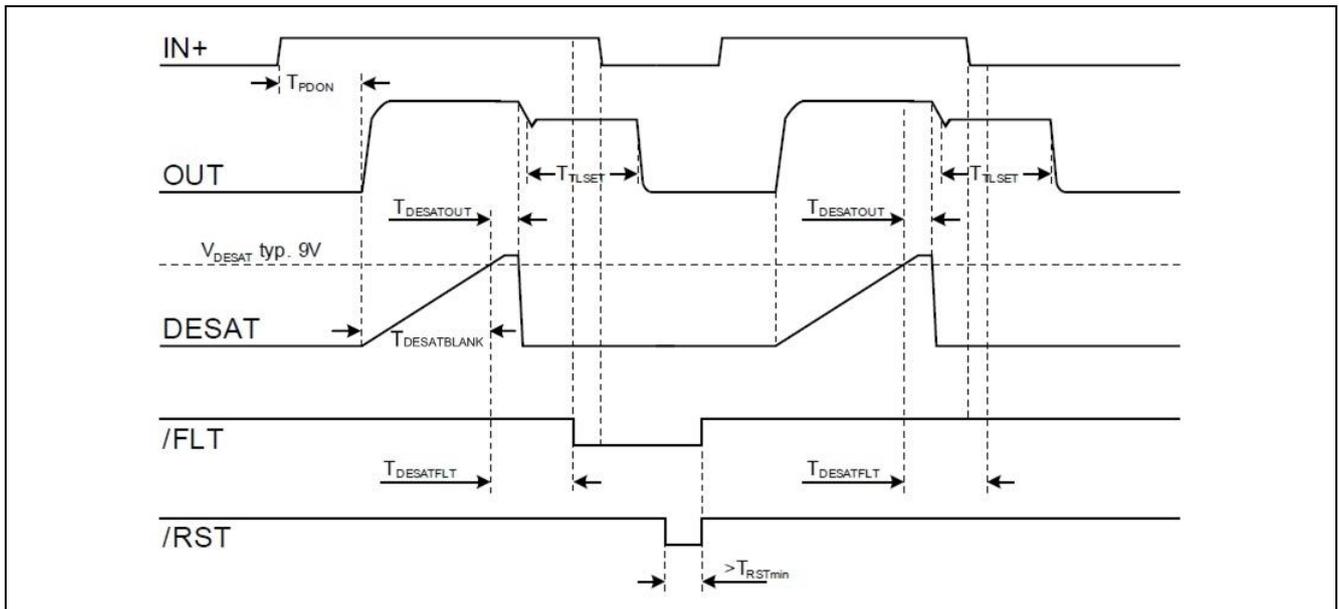

Figure 20   DESAT timing diagram

The external capacitor C_{DESAT} defines the DESAT blanking time $T_{DESATBLANK}$ (as shown in Figure 20) which can be expressed according to the following equation

$$C_{DESAT} = \frac{I_{DESAT} \cdot T_{DESATBLANK}}{V_{REF\_DESAT}}$$

(6)

Meanwhile, if the C_{DESAT} value is too big, it will slow down the charging procedure and lead to a slow sensing of desaturation current. This is dangerous when considering the short circuit withstand time T_{SC} of IGBT (typically 5µs for 600V IGBT and 10µs for 1200V IGBT). So, the choice of C_{DESAT} must fulfill the following condition

$$T_{DESATBLANK} + T_{DESATOUT} + T_{TLSET} + T_{TLFALL} < T_{SC} \quad \text{for 1ED020I12-BT}$$

(7a)

$$T_{DESATBLANK} + T_{DESATOUT} < T_{SC} \quad \text{for others}$$

(7b)

here the $T_{DESATOUT}$ is the desaturation sensing delay which is defined in the product datasheet, the T_{TLSET} is the Two-Level Turn-Off set time as explained in section 2.3.5, and the T_{TLFALL} (as shown in Figure 10) is mainly defined by gate resistance R_{Goff} and driver output resistance during driving low R_{DriveL} as explained in section 2.3.4. The values which are chosen for the calculation need be the maximum value so as to give enough marginality for safety reason. A good recommendation is to choose a DESAT capacitance of C_{DESAT} = 100pF for 1200V IGBT and C_{DESAT} = 56pF for 600V IGBT, which corresponds to a blanking interval of $T_{DESATBLANK}$ = 2µs (1200V IGBT) and = 1µs (600V IGBT) respectively.

In series with the desaturation diode D_{DESAT}, an external decoupling resistor R_{DESAT} is required in order to limit the current flowing in and out of the DESAT pin because of switching noise coupled through this desaturation diode D_{DESAT} during the DESAT sensing time. The calculation of R_{DESAT} can be based on following formula,

$$V_{R_{DESAT}} + V_{D_{DESAT}} + V_{CE(sat)\_max} < V_{REF\_DESAT} \tag{8a}$$

$$R_{DESAT} = \frac{V_{R_{DESAT}}}{I_{DESAT}} \tag{8b}$$

here, the $V_{R_{DESAT}}$ is the voltage drop on decoupling resistor R_{DESAT}, the $V_{D_{DESAT}}$ is the voltage drop on desaturaion diode, and the $V_{CE(sat)\_max}$ is the maximum collector-emitter saturation voltage. The recommendation value for this decoupling resistor R_{DESAT} is 1kΩ for half bridge topology. A higher value leads to a higher sensitivity of this function in respect of the collector current, but also to a higher sensitivity regarding a wrong triggering. This function should therefore only be used for dection of full desaturation instead of overcurrents.

The desaturation capacitor C_{DESAT} and decoupling resistor R_{DESAT} should be placed as close as possible to DESAT pin.

2.5 Active Miller Clamping

Turn-on or turn-off of IGBT can cause high dv_{CE}/dt. Displacement currents flow through the parasitic capacitances of power transistors and may lead to an unintended turn-on of IGBT. For example, in a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows to sink the Miller current across a low impedance path in this high dv/dt situation as shown in Figure 21. Therefore in many applications, the use of a negative supply voltage can be avoided and VEE2 can be directly connected to GND2.
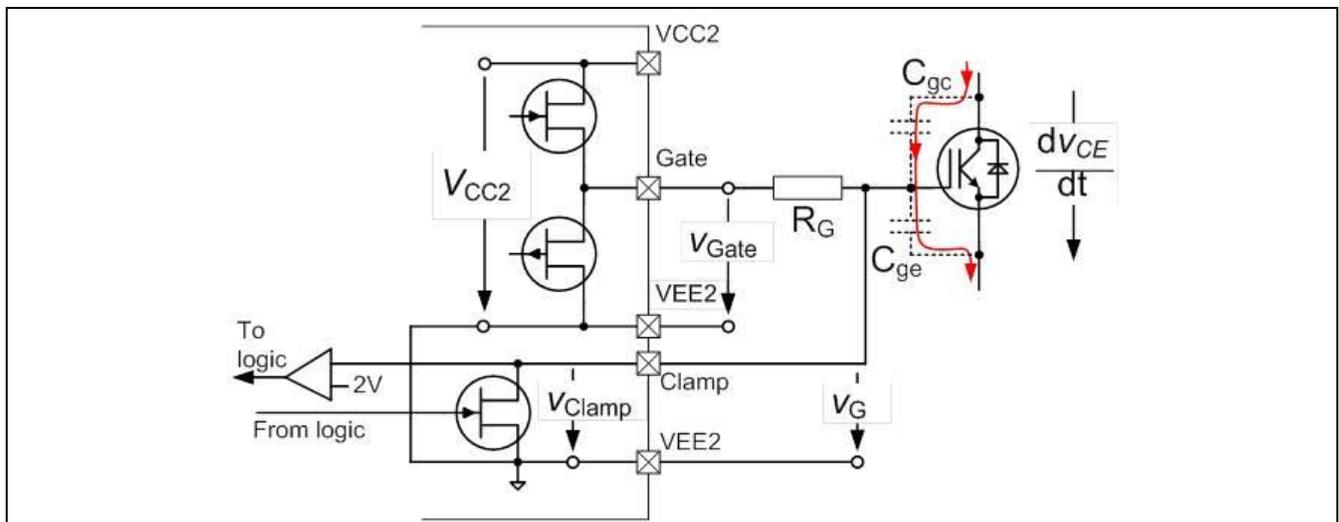

Figure 21   Active Miller Clamp

During turn-off, the gate voltage is monitored and the clamp output is activated (internal clamp FET is on) when the gate voltage goes below typical 2 V (related to VEE2).

The clamp is designed for a Miller current up to 2A. In case the external booster is used at the driver output stage, there could be over-current at this Miller clamp pin due to the large displacement current. So the calculation need to be done together with the turn-off gate resistance R_{Goff}, the resistance of the PNP transistor for booster (refer to Figure 18 in section 2.3.6), and the R_{DSon} (1.5Ω) of clamp MOSFET in driver IC, since the current is shared in-between these two paths. Carefully choosing the turn-off gate resistance and booster transistor according to the calculation can keep the clamp function safely.

2.6 Fault Output

The 1ED020I12-BT has a FAULT status output feature, which is an open-drain output to report a desaturation error of the IGBT (/FLT is low if desaturation occurs). The integrated pull-up resistor is designed for the case of input pin floating or driven from a high impedance source. It is highly recommended to still use an external pull-up (e.g. 4.7kΩ) as shown in Figure 22 for safety reason.
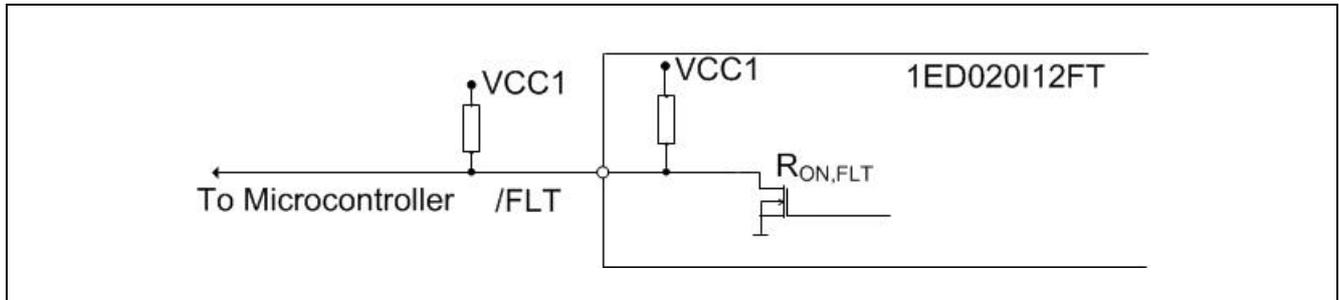
Figure 22   Fault output

Here the internal pull-up resistor (12.5kΩ ~ 50kΩ) can be calculated according to the /FLT Pull Up Current $I_{/PFLT}$ value from datasheet and the $R_{ON,FLT}$ (max. 60Ω) can be calculated according to the /FLT Low Voltage V_{FLTL} value from datasheet.

There is a delay time from the desaturation sensing finished to the /FLT low, which is maximum 2.25µs according to the datasheet for all family members.

The waveform of this Fault output function please refers to Figure 14 in section 2.3.5.

2.7 Ready Output

The 1ED020I12-BT has a READY output feature, which is an open-drain output to show the status of three internal protection features:
• UVLO of the input chip
• UVLO of the output chip after a short delay
•Successful establishment of the internal signal transmission after a short delay
RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless. It is not necessary to reset the READY signal since its state only depends on the status of the former mentioned protection signals. The waveform of this READY output function is shown in Figure 23.
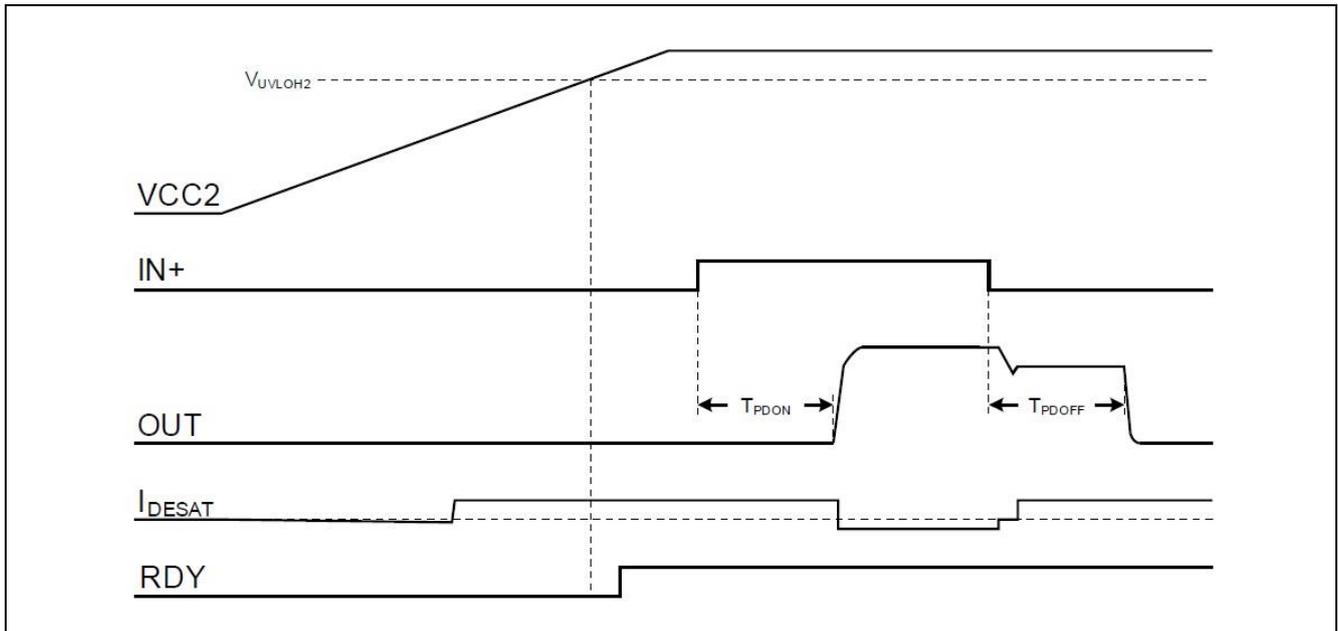
Figure 23   Ready output during VCC2 ramp up for 1ED020I12BT

The integrated pull-up resistor is designed for the case of input pin floating or driven from a high impedance source. It is highly recommended to still use an external pull-up setup as shown in Figure 24 for safety reason.
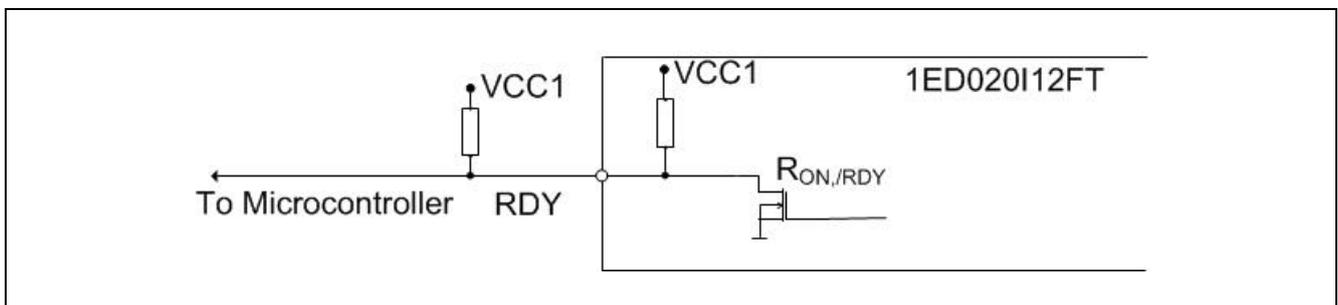
Figure 24   Ready output

Here the internal pull-up resistor (12.5kΩ ~ 50kΩ) can be calculated according to the RDY Pull Up Current I_{PRDY} value from datasheet and the according test condition. The $R_{ON,/RDY}$ (max. 60Ω) can be calculated according to the RDY Low Voltage V_{RDYL} value from datasheet and the according test condition.

2.8   Reset

The 1ED020I12-BT has a RESET feature, which is an input pin with internal pull-up resistor and has the following two functions:
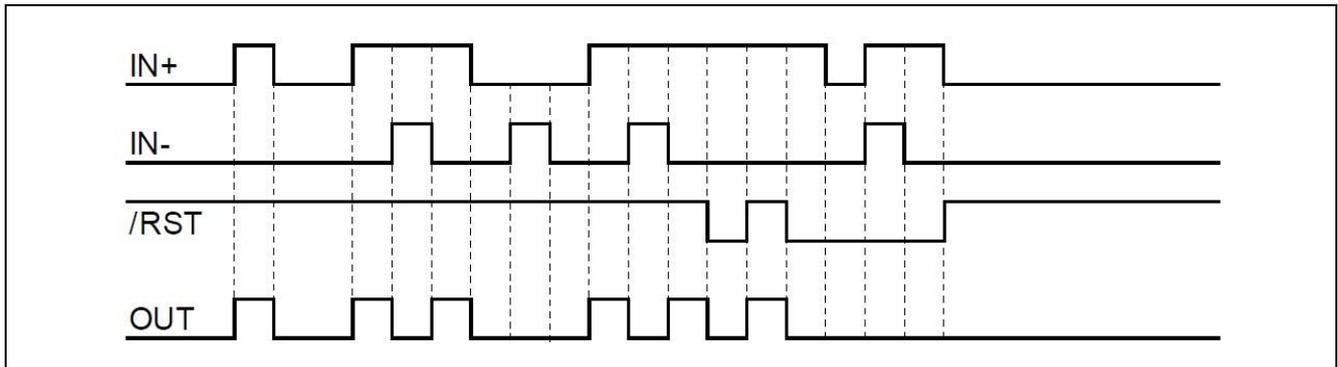
Figure 25   Principle switching behavior for RESET

Function 1: Enable/shutdown of the input chip. This means the IGBT is off if /RST is low (as shown in Figure 25). A minimum pulse width T_{MINRST} (30ns) is defined to make the IC robust against glitches at /RST.
Function 2: Reset of the DESAT-FAULT-state of the chip. If /RST is low for longer than a given time T_{RST} (minimum 800ns), the /FLT signal will be cleared at the rising edge of /RST. Otherwise, it will remain unchanged, refer to Figure 14 in section 2.3.5.
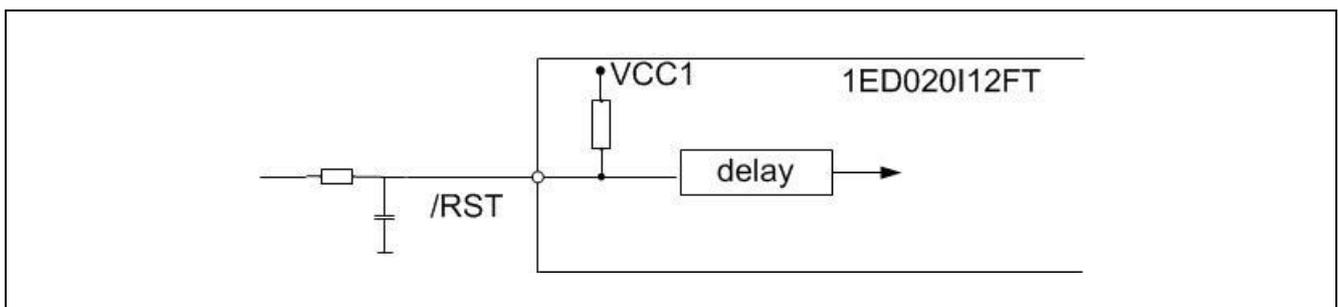
Figure 26   RESET circuit

Figure 26 shows the RESET circuit. The internal pull-up resistor (12.5kΩ ~ 50kΩ) can be calculated according to the /RST input current $I_{/RST}$ value from datasheet and the according test condition. It is recommended to use a RC-filter at the input to reduce the influence from electromagnetic interference, which may cause distorsion of the input signal and therefore to an unintended reset process. The values of the filter may be the same as for other control pins (100Ω, 100pF-1nF). The RC-filter needs to be placed as close as possible to the /RST pin.

2.9   Power Dissipation

The power dissipation for the input chip of the gate driver is mainly determined by quiescent current. The quiescent current is the current which is consumed by the input chip when it is in quiescent state. The power dissipation can be calculated as shown in following equations:

$$P_{\text{dis\_in}} = k_{\text{in}} \cdot P_{\text{Quiescent\_in}} = k_{\text{in}} \cdot V_{\text{VCC1}} \cdot I_{\text{Q1\_max}} \qquad (9)$$

In these equations I_{Q1_max} is the maximum quiescent current of the input chip from datasheet, V_{VCC1} represents the power supply voltage at input side, and k_{in} (the value can be assumed as 1.1) is the factor which takes into account the power dissipation also from the IN+/IN- and RESET pins.

The power dissipation for the output chip of the gate driver is mainly determined by quiescent current and output load current. The quiescent current is the current which is consumed by the output chip when it is in quiescent state, and the output load current is the current which is consumed by the load when the device is switching. So

the total power dissipation of the output chip can be calculated as the summation of quiescent power and output load power as shown in following equations (10a) ~ (10c):

$$P_{\text{dis\_out}} = k_{\text{out}} \cdot (P_{\text{Quiescent\_out}} + P_{\text{outputs}}) \tag{10a}$$

$$P_{\text{Quiescent\_out}} = \Delta V_{\text{out}} \cdot I_{\text{Q2\_max}} \tag{10b}$$

$$P_{\text{outputs}} = \Delta V_{\text{out}} \cdot f_{\text{S}} \cdot Q_{\text{G\_max}} \tag{10c}$$

In these equations $I_{\text{Q2\_max}}$ is the maximum quiescent current of the output chip from datasheet, f_s resembles the switching frequency, ΔV_{out} represents the voltage step at the driver output, which is $V_{\text{VCC2}} - V_{\text{VEE2}}$, $Q_{\text{G\_max}}$ is the maximum IGBT gate charge value, and k_{out} (the value can be assumed as 1.2) is the factor which takes into account the power dissipation also from the CLAMP, DESAT and TLSET pins.
With the calculated power dissipation value, the junction temperature T_J can be obtained by the equations (11a) ~ (11b):

$$T_{\text{J\_in}} = P_{\text{dis\_in}} \cdot R_{\text{THJA,IN}} + T_{\text{A}} \tag{11a}$$

$$T_{\text{J\_out}} = P_{\text{dis\_out}} \cdot R_{\text{THJA,OUT}} + T_{\text{A}} \tag{11b}$$

$R_{\text{THJA,IN}}$ and $R_{\text{THJA,OUT}}$ is the thermal resistance of input and output chip in the datasheet and T_A is the ambient temperature. The calculation junction temperature need to be smaller than the maximum allowed junction temperature which is defined by datasheet (150$^{\text{o}}$C for 1ED020I12-BT), otherwise the driver device will be thermally damaged.
In another way around, the maximum junction temperature will determine the maximum power dissipation of the driver, so as to the maximum switching frequency once the IGBT used in the application is defined ($Q_{\text{G\_max}}$ is certain) and the operation voltage step is known (ΔV_{out} is certain).
To better understand a total power dissipation calculation, consider the 1ED020I12-BT is driving Infineon IGBT module FS75R12KT4_B15 and operating under following conditions:

Input chip supply voltage: V_{VCC1} = 5.0V
Voltage step at output chip: ΔV_{out} = 15.0V − (-8.0V) = 23.0V
Switch frequency: f_{s} = 20kHz
Ambient temperature: T_{A} = 80$^{\text{o}}$C
Input chip coeffecient factor: k_{in} = 1.1
Output chip coeffecient factor: k_{out} = 1.2

According to the datasheets:
Max. input chip quiescent current: $I_{\text{Q1\_max}}$ = 9mA
Max. output chip quiescent current: $I_{\text{Q2\_max}}$ = 6mA
Max. IGBT gate charge: $Q_{\text{G\_max}}$ = 0.57μC
Input chip thermal resistance: $R_{\text{THJA,IN}}$ = 139K/W
Output chip thermal resistance: $R_{\text{THJA,OUT}}$ = 117K/W
Max. allowed junction temperature: T_{J} = 150 $^{\text{o}}$C

From (9), the power dissipation for the input chip is:
$P_{\text{dis\_in}} = k_{\text{in}} \cdot P_{\text{Quiecent\_in}}$
$\quad\quad = k_{\text{in}} \cdot V_{\text{VCC1}} \cdot I_{\text{Q1\_max}}$
$\quad\quad = 1.1 \cdot 5.0V \cdot 9mA$
$\quad\quad = 49.5mW$

From (10a-10c), the power dissipation for output chip is:

$P_{\text{dis\_out}} = k_{\text{out}} \cdot (P_{\text{Quiescent\_out}} + P_{\text{outputs}})$
$= k_{\text{out}} \cdot (\Delta V_{\text{out}} \cdot I_{\text{Q2\_max}} + \Delta V_{\text{out}} \cdot f_s \cdot Q_{\text{G\_max}})$
$= 1.2 \cdot (23.0V \cdot 6mA + 23.0V \cdot 20kHz \cdot 0.57\mu C)$
$= 480.24mW$

From (11a), the junction temperature for input chip is:
$T_{\text{J\_in}} = P_{\text{dis\_in}} \cdot R_{\text{THJA,IN}} + T_A$
$= 49.5mW \cdot 139K/W + 80^{\text{o}}C$
$= 86.68^{\text{o}}C$

From (11b), the junction temperature for output chip is:
$T_{\text{J\_out}} = P_{\text{dis\_out}} \cdot R_{\text{THJA,OUT}} + T_A$
$= 480.24mW \cdot 117K/W + 80^{\text{o}}C$
$= 136.19^{\text{o}}C$

The maximum allowable junction temperature for 1ED020I12-BT is 150$^{\text{o}}$C, so that this example application is within the allowed maximum.

3 References

[1] Logic signals voltage levels:
http://www.allaboutcircuits.com/vol_4/chpt_3/10.html

[2] Driving IGBTs with unipolar gate voltage:
http://www.infineon.com/dgdl/Infineon+-+AN2006-01+-
+Driving+IGBTs+with+unipolar+gate+voltage.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=
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