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Improving Efficiency of Synchronous Rectification by Analysis of the MOSFET Power Loss Mechanism

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1 Abstract

Driven by the 80 PLUS® [1] program the overall system efficiency in switched mode power supplies (SMPS) is targeting 90%. The main losses are the high diode forward losses of the secondary side rectification of an isolated converter. Reaching this efficiency level is therefore only possible with synchronous rectification (SR). For achieving ideal switching behavior, the power loss mechanism of a SR MOSFET has to be well understood. This paper analyzes the turn off process of the SR MOSFET and proposes a simple model for calculating the power losses to optimize the system efficiency.

2 Introduction

Taking a look into a switched mode power supply, a rectification stage can be found on the secondary side of the converter. The task of this stage is to rectify the rectangular power signal, which is being transferred from the primary side to the secondary side of the SMPS via a transformer. Typically this rectification is done with power diodes (see Fig. 1). But due to the forward voltage drop of the diodes (0.5V and higher) combined with the high output currents, these devices produce high conduction losses and therefore have a major contribution to the efficiency of the whole converter. To minimize these rectification losses, the diodes can be replaced with modern power MOSFETs, which tremendously reduces conduction losses

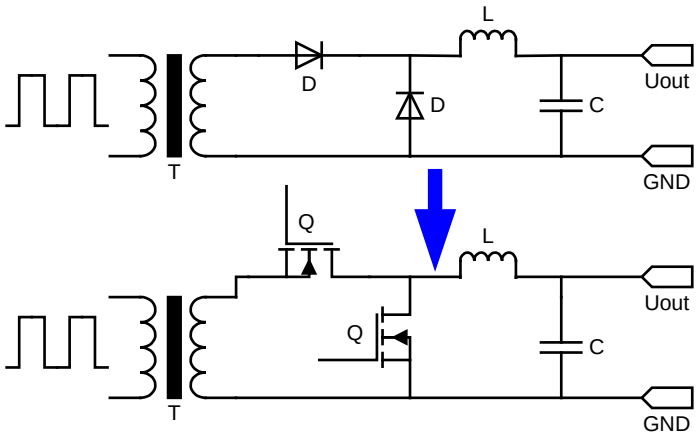

Fig. 1. Synchronous vs. diode rectification.

especially at high output currents. Considering low load efficiency, not the conduction losses but the switching losses are in the main focus. These are considerably higher compared to diodes.

Other important effects on system efficiency come from the gate drive and the snubber network for damping the turn-off voltage spike. As this system is very complex, the correlation of all parameters in respect to each other has to be well understood for optimizing the system efficiency. [2] [3]

3 Analyzing the turn off behavior of the SR MOSFET

To understand the turn-off process of a SR switch, a schematic diagram of the most important waveforms is shown in Fig. 2.

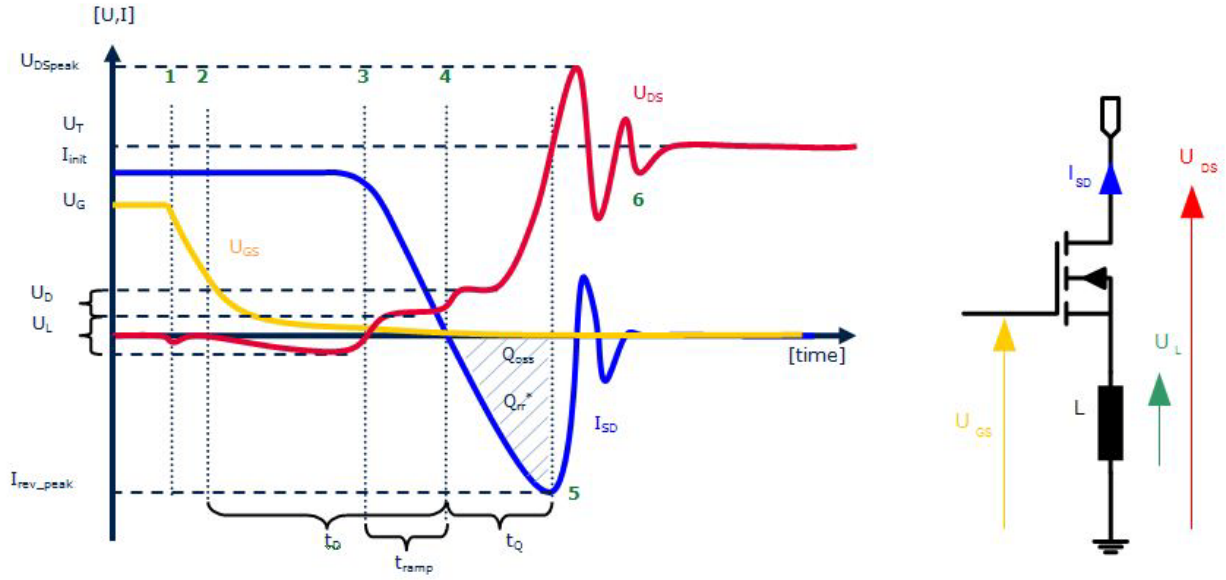

Fig. 2. Turn off behavior of the SR MOSFET with fragmentation in different switching points

The starting point for the analysis is the on state of the switch: gate voltage is at high level, drain-source voltage is almost zero and a current is flowing from source to drain. At point 1 the gate is turned off. This can also be seen in the U_{DS} waveform in form of a little negative voltage dip coming from the discharge of the gate capacitance C_G. This discharge produces a current peak with a high di/dt in the source connection of the MOSFET. Due to the inductive law

$$U_L = -L \cdot \frac{di}{dt} \qquad \textbf{(1)}$$

this inductance in the source leads to a voltage drop in the U_{DS} waveform. At point 2 the MOSFET channel closes, but nevertheless the current has to keep on flowing, driven by the output choke.

This forces the current to commutate to the body diode of the MOSFET, resulting in a negative voltage drop U_D over the switch. In Fig. 2 this time slot is marked with t_D. After switching the primary side at point 3, the current has to ramp down. If the switching of the primary side MOSFETs is fast, current commutation is limited by the secondary side loop inductances, resulting in a constant di/dt. In this phase t_{ramp} a voltage drop, caused by the source inductance of the MOSFET, can be seen in the drain-source waveform, now into the positive direction due to negative di/dt. When the current crosses the zero line (4), no current is flowing any more through the body diode. Therefore the forward voltage drop over the diode becomes zero, resulting in a further positive voltage drop at the U_{DS} waveform with the value of the forward voltage drop of the body diode U_D. After the zero crossing the current keeps on flowing with the same di/dt. But now the direction of the current is negative, removing the reverse recovery charge Q_{rr}^* of the body diode and charging the output capacitance C_{oss} of the MOSFET. In this case the Q_{rr}^* is considered as only the MOSFET body diode reverse recovery charge, whereas the Q_{rr} on datasheets is measured according to JEDEC standards and therefore contains besides the body diode Q_{rr}^* also some part of the output charge of the MOSFET Q_{oss} (more details in section 4). While the C_{oss} is being charged, the voltage over the MOSFET begins to rise towards the transformer voltage. In point 5 the maximum reverse current I_{rev_peak} is reached, this means the C_{oss} is now charged up to the transformer voltage. Ideally the system should now be stable, but there is still energy in the system defined by

$$E_{ind} = \frac{1}{2} \cdot L_{stray} \cdot I_{rev\_peak}^2 \qquad \textbf{(2)}$$

This inductive energy is now triggering a LC oscillation circuit and forcing the stored energy in the stray inductances L_{stray} to be transferred to the output capacitance of the MOSFET and therefore producing the turn off overvoltage spike. The LC circuit is defined by the inductance of the transformer, the layout, the package and the MOSFET C_{oss} as seen in Fig. 3.

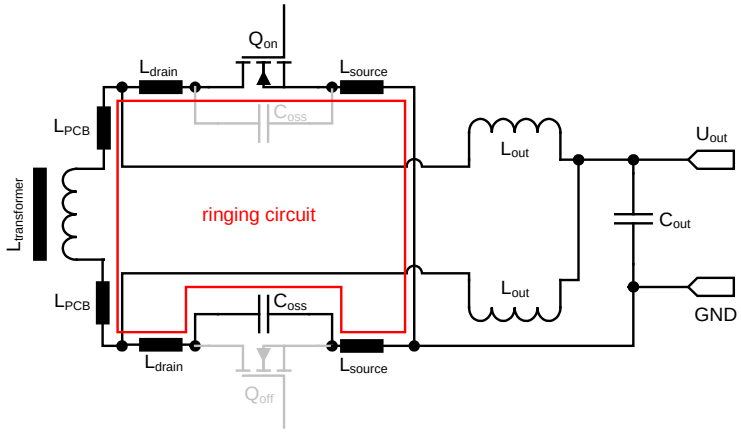

Fig. 3. LC turn-off oscillation circuit in a current doubler SR.

This circuit has an oscillation frequency of

$$f_0 = \frac{1}{2\pi\sqrt{L_{stray} \cdot C_{oss}}} \quad \textbf{(3)}$$

and is damped by the parasitic resistances in the loop (C_{oss} = output capacitance of the MOSFET and L_{stray} = L_{source} + L_{drain} + L_{PCB} + $L_{transformer}$). This discussed shape of the waveform is only valid if the current commutation on the secondary side is inductively limited. This means, the di/dt is not limited by the switching speed of the primary side MOSFETs, but by the stray inductances on the secondary side of the power supply.

4 Development of a power loss model

For the design of a high efficient power supply using SR, it is necessary to exactly know where the power losses in the SR MOSFET are generated. In the following all important sources of power losses are identified, based on ideal MOSFET switching behavior.

Conduction losses are defined by the $R_{DS(on)}$ of the MOSFET. The calculation can be done with the following formula:

$$P_{cond} = I_{RMS}^2 \cdot R_{DS(on)} \quad \textbf{(4)}$$

Here the I_{RMS} is the triangular current through the MOSFET, not the output current of the converter.
For assuring an interlock between the two SR MOSFETs to avoid a current shoot through, a certain dead time has to be guaranteed. Therefore the respective MOSFET has to be switched off before the primary side is turned on. This causes the current to commutate from the MOSFET channel to the MOSFET body diode, which can be seen in a negative voltage drop over drain source (Fig. 1). The time is called body diode on time t_D. The calculation of the diode power loss can be done by using following parameters: forward voltage drop of the body diode U_D, the source to drain body diode current I_{SD}, the body diode on time t_D and the converter switching frequency f_{sw}:

$$P_{diode} = U_D \cdot I_{SD} \cdot t_D \cdot f_{sw} \quad \textbf{(5)}$$

Gate drive losses of the SR MOSFET are defined by the gate charge Q_g, the gate driving voltage U_g and the switching frequency f_{sw}:

$$P_{gate} = Q_g \cdot U_g \cdot f_{sw} \tag{6}$$

These losses are generated due to the gate charge of the MOSFET, but they are dissipated in the gate resistor and the gate driver.

The output charge Q_{oss} and the reverse recovery charge Q_{rr}^* also produce losses while turning off the SR MOSFET. This formula can be derived from a simplified model of the turn-off behavior (Fig. 4).

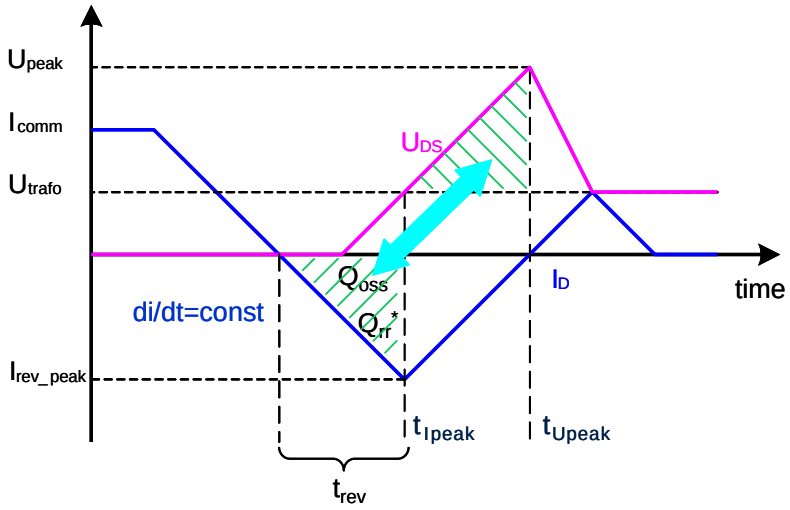

Fig. 4. Simplified model of the SR MOSFET turn-off.

By using the following approximations, a triangular shape of the current waveform and a constant output capacitance of the MOSFET, a calculation of the turn off energy can be done. The triangular shape of the current waveform can be assumed if the current commutation is inductively limited, which is the case for most applications. To calculate the equivalent constant capacitance C_{const} of the MOSFET at a certain transformer voltage U_T, the time variant nonlinear output capacitance $c_{oss(t)}$ has to be known:

$$Q_{oss} = \int_0^{U_T} c_{oss}(t) \cdot u(t) \cdot dt = U_T \cdot C_{const} \Rightarrow C_{const} = \frac{1}{U_T} \cdot \int_0^{U_T} c_{oss}(t) \cdot u(t) \cdot dt \tag{7}$$

For calculating the turn-off switching losses, first the reverse current peak I_{rev_peak} has to be fixed:

$$I_{rev\_peak} = \frac{di}{dt} \cdot t_{rev} \Rightarrow t_{rev} = \frac{I_{rev\_peak}}{di/dt} \quad \textbf{(8)}$$

The di/dt can be calculated by using the transformer voltage and the inductances in the current commutation loop:

$$\frac{di}{dt} = -\frac{U_T}{L_{stray}} \quad \textbf{(9)}$$

Now the switching charge $Q_{sw}=Q_{oss}+Q_{rr}^*$ can be evaluated:

$$Q_{sw} = \frac{I_{rev\_peak} \cdot t_{rev}}{2} = \frac{I_{rev\_peak}^2}{2 \cdot di/dt} \Rightarrow I_{rev\_peak}^2 = 2Q_{sw} \cdot \frac{di}{dt} \quad \textbf{(10)}$$

From this derivation the inductive switching energy is calculated:

$$E_{ind} = \frac{1}{2} L_{stray} I_{rev\_peak}^2 = L_{stray} \cdot \frac{di}{dt} \cdot Q_{sw} \Rightarrow E_{sw} = U_T \cdot Q_{sw} \quad \textbf{(11)}$$

Looking at the point t_{Ipeak} an inductive energy is stored in the stray inductances and a capacitive one in the C_{oss}. As a result an energy comparison can be done:

$$\begin{aligned} E_{lost} &= E_{ind} - E_{coss} = U_T \cdot \left(Q_{oss} + Q_{rr}^*\right) - 1/2 \cdot C_{oss} \cdot U_T^2 \\ \Rightarrow E_{lost} &= U_T \cdot \left(1/2 \cdot Q_{oss} + Q_{rr}^*\right) \end{aligned} \quad \textbf{(12)}$$

This energy is then transferred to the output capacitance of the MOSFET (Fig. 4), there it produces an overvoltage spike and then gets dissipated through the resistive part of the LC oscillation circuit (Fig. 1, point 6). Consequently, the switching-off power losses are fixed:

$$P_{sw} = U_T \cdot \left(1/2 \cdot Q_{oss} + Q_{rr}^*\right) \cdot f_{sw} \quad \textbf{(13)}$$

The accuracy of this calculation depends on the switching behavior of the MOSFET. It has to be assured that no second order effect like dynamic turn-on or avalanche is occurring. Furthermore best results are achieved for hard switched topologies. Any resonant soft switching topology may lead to a deviation. In this case the MOSFET can be optimized for lower $R_{DS(on)}$, as some part of the switching energy can possibly be recovered.

5 Reverse recovery charge of the body diode

The internal body diode of a MOSFET plays an important role if an optimization regarding efficiency has to be done. As it is typically flooded with current every switching cycle before the MOSFET gets turned off, a reverse recovery charge Q_{rr}* is being build up. Already mentioned in section 3, the real Q_{rr}* is not adequately represented by the Q_{rr} on datasheets. Datasheet values are measured with a di/dt of 100 A/µs, the diode is applied with the maximum drain current and the conduction time before turn off is in the range of up to 500 µs and more. This leads to a maximum possible Q_{rr}*. Furthermore the measurement method of the JEDEC standard includes besides the Q_{rr}* also some part of the output charge of the MOSFET, which gives in total a huge value not representing reality. Highlighting the real application, a di/dt of up to 1000 A/µs can be seen, which would increase Q_{rr}* compared to lower di/dt's. However, the main impact on the Q_{rr}* comes from the current and the flooding time of the diode. Therefore the application shows much lower Q_{rr}* values, due to currents of half the maximum drain current and below and a diode flooding time of 50 ns to 150 ns.

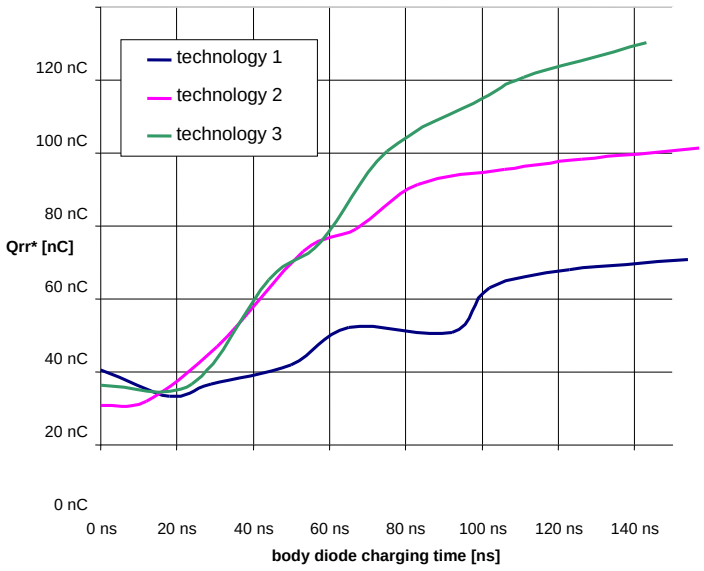

Fig. 5. Q_{rr}^* dependency of body diode charging time.

As shown in Fig. 5 there is a strong influence of the MOSFET gate timing on the effective present Q_{rr}^{*}. The longer the time the body diode is conducting current before turn off, the higher the reverse recovery charge will be. This will decrease efficiency and lead to a higher turn off voltage spike. As an example, technology 3 in Fig. 5 can be taken. Going from a perfect timing of just 20 ns up to 140 ns, an additional power loss of about 0.5W (transformer voltage = 40V, switching frequency = 125 kHz) can influence efficiency dramatically, especially at low load conditions.

Depending on MOSFET technology and flooding time of the body diode, the Q_{rr}, often is of secondary importance as the output capacitance is typically dominant. Furthermore no application relevant Q_{rr} value is provided on datasheets.

6 Optimizing SR MOSFET for efficiency

For optimizing the SR MOSFET regarding efficiency, a well balanced ratio between switching losses and conduction losses has to be found. Considering light load condition, the $R_{DS(on)}$ conduction losses play a minor role, as there is just a small current flowing through the MOSFET. In this case the switching losses, which are more or less constant over the whole load range, are dominant. In case of high output current the conduction losses are the biggest portion and therefore contribute the most to the total power losses, see Fig. 6.

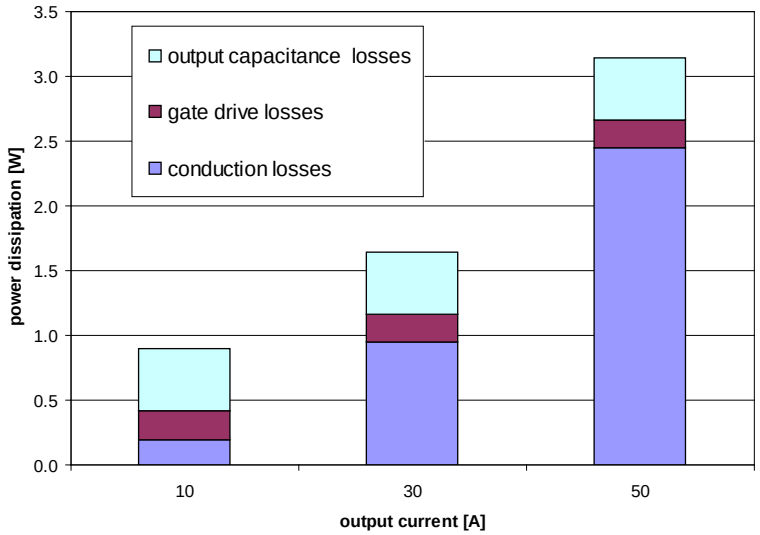

Fig. 6. Power loss distribution varying output current for the IPP028N08N3 G;
f_{sw} = 125 kHz, U_T = 40V.

For choosing the best fitting MOSFET, special attention has to be given to the $R_{DS(on)}$ class, which is illustrated in Fig. 7. Going beyond the optimum point (higher $R_{DS(on)}$) will increase total power losses linearly. But lowering the $R_{DS(on)}$ under the optimum will lead to dramatically increased losses. Furthermore in Fig. 7 can be seen, that the range of minimum power losses is quite wide.

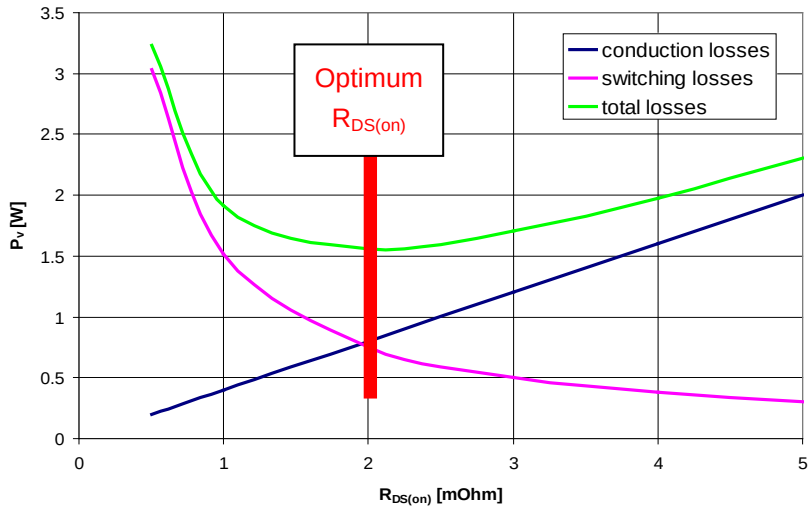

Fig. 7. Power losses vs. $R_{DS(on)}$ for the OptiMOS™3 80V technology; V_T = 40V, f_{sw} = 150 kHz, I_{MOSFET} = 20 A. V_{gate} = 10V

Between 1 mOhm and 3 mOhm total losses stay roughly the same. But a further decrease of $R_{DS(on)}$ of 0.5 mOhm will double the power losses and therefore extremely hurt the efficiency of the power converter.

The impact of different MOSFET $R_{DS(on)}$ classes in the real application can be seen in Fig. 8. A measurement in a server power supply unit was done the IPP028N08N3 G and the IPP057N08N3 G.

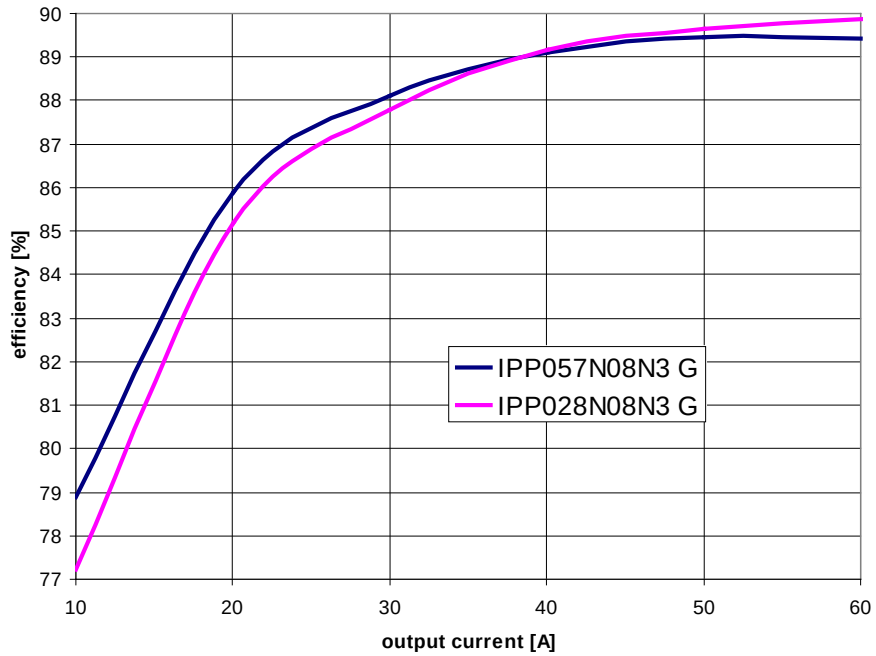

Fig. 8. Measured efficiency comparison of two SR MOSFET $R_{DS(on)}$ classes in server power supply unit.

Going for light load efficiency, the higher ohmic MOSFET gives much better efficiency. This device has a lower output capacitance and a lower gate charge, which in total gives lower switching losses. On the other hand efficiency is getting lower as the output current is increasing. In this case the lower ohmic switch gives a better performance. For optimizing efficiency over the whole current range, a balanced selection of the optimum SR MOSFET has to be done.

7 Conclusion

This Application Note presents a method to analyze power losses in the SR stage of switched mode power converters. An analytical, yet simple model for calculating the switching losses was developed. With these results developers of switched mode power supplies using synchronous rectification have the possibility to optimize topology and MOSFET selection. A rough calculation of the SR power losses can be done, which helps to speed up the design process and to boost efficiency.

8 References

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