

Infineon's 1200V SiC JFET – The New Way of Efficient and Reliable High Voltages Switching.

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Abstract

After 10 years of successful SiC diode production, we consider SiC technology mature enough to introduce our first SiC switch. SiC's unique physical properties give us the opportunity to design a new class of high-voltage switches beside Si super-junction devices and IGBTs. Low static and dynamic losses as well as the integration of a body diode are key features which will prove revolutionary for application topologies relying on hard switching with continuous body diode commutation as well as on resonant switching. The major technology features and their impact on selected applications will be discussed.

1. Device Concept and Control

The choice of device concept is crucial both in terms of reliability as well as expected performance in the application. A SiC MOSFET or JFET are devices with very similar device characteristics, both able to "transfer" the unipolar fast switching performance well known from Si super-junction MOSFETs up to 1200V blocking voltage. When it comes to technology maturity the MOSFET and JFET have though quite different merits. The main objective for us is to benefit from the proven robustness of our diode process line and avoid process concepts that are not yet thoroughly tested in the field. In this respect the MOSFET lacks maturity compared to a JFET. Mainly because the gate oxide process even if intrinsic reliability and threshold voltage stability is demonstrated introduces a failure risk due to the relatively high extrinsic defect density of the SiC material system. Effective screening strategies as a countermeasure to improve the quality have to be developed and proven. Excluding the MOSFET leaves the question of the best JFET concept. [1]

Vertical JFETs as reported in [2] have the advantage of normally-off operation, but this comes at the price of a non-standard driver scheme with negative voltage for turn-off and BJT-like high current turn-on. By design the useable threshold voltage window for operation is narrow and becomes even more critical due to a pronounced Drain Induced Barrier Lowering (DIBL) effect which makes it dependent on the blocking voltage. On the manufacturing side the process window with respect to threshold voltage stability is extremely narrow and requires ambitious control of critical lithography and patterning steps. On top of this the ∇ JFET structure makes it impossible to effectively integrate a body diode into the switch. It also shows an increased coupling of gate and drain which significantly contributes to the output capacitance [3].

Taking all this under consideration we choose a JFET structure with a horizontal channel (Fig.1). The basically 1-dimensional channel design enables tight threshold (pinch-off) voltage control by implantation and gives excellent R_{on} .

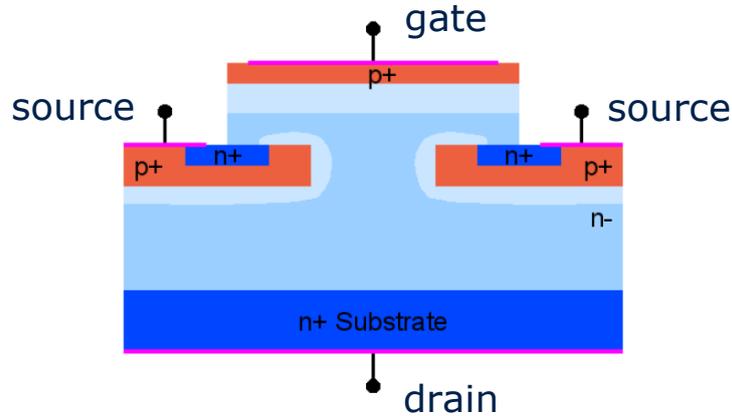


Fig. 1: Schematic JFET structure

By intention we choose as design point the normally-on operation mode. This gives us the flexibility to set a wide switching window between threshold voltage and punch through voltage (break through between gate and embedded p+ buried gate). We can hence use an easy drive scheme (e.g. 0 to -20V) for safe turn-on and turn-off with sufficient margins and no bipolar losses.

In case normally-off functionality is required the switch can be conveniently used in a "Direct driven JFET" configuration [4]. Here, in a Cascode topology a simple low voltage normally-off MOS device is connected in series to a SiC JFET. We suggest a p-channel device as this allows to reference the gate drive for both the JFET and the p-channel to the same potential (see Fig. 2). During normal operation the MOS device is conducting without significant contribution to the total R_{on} . In case of start-up and malfunction the normally-off MOS is turned off pushing the source of the JFET to a positive potential relative to its gate and hence turning the JFET into a safe off-state. This concept has been demonstrated in a commercial available photovoltaic inverter and has been proven to return the system into a safe operation during common faults such as loss of gate drive power [5].

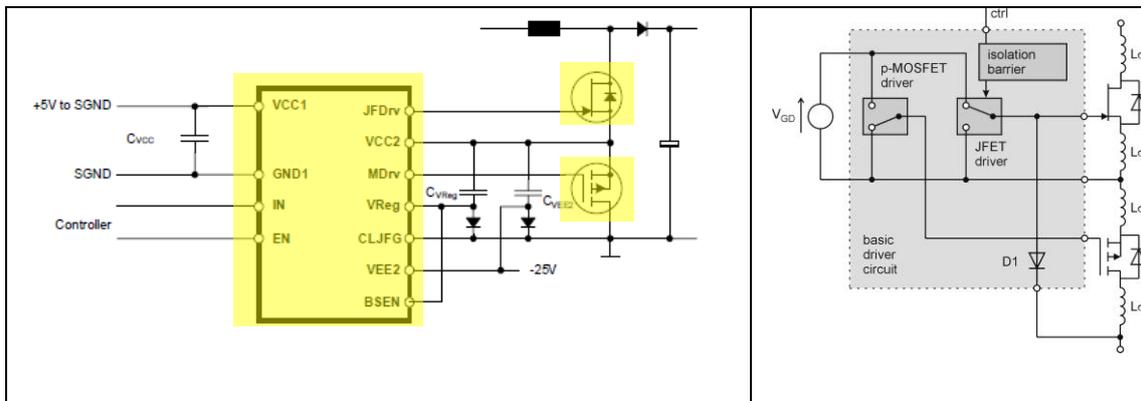


Fig. 2: Control of the normally-on SiC JFET with dedicated driver (left) and basic internal setup (right).

2. Device characteristics

The normally-on SiC JFET shows a MOSFET like forward characteristic with very good gate control and a very high pulse current capability. Fig. 3 shows the result.

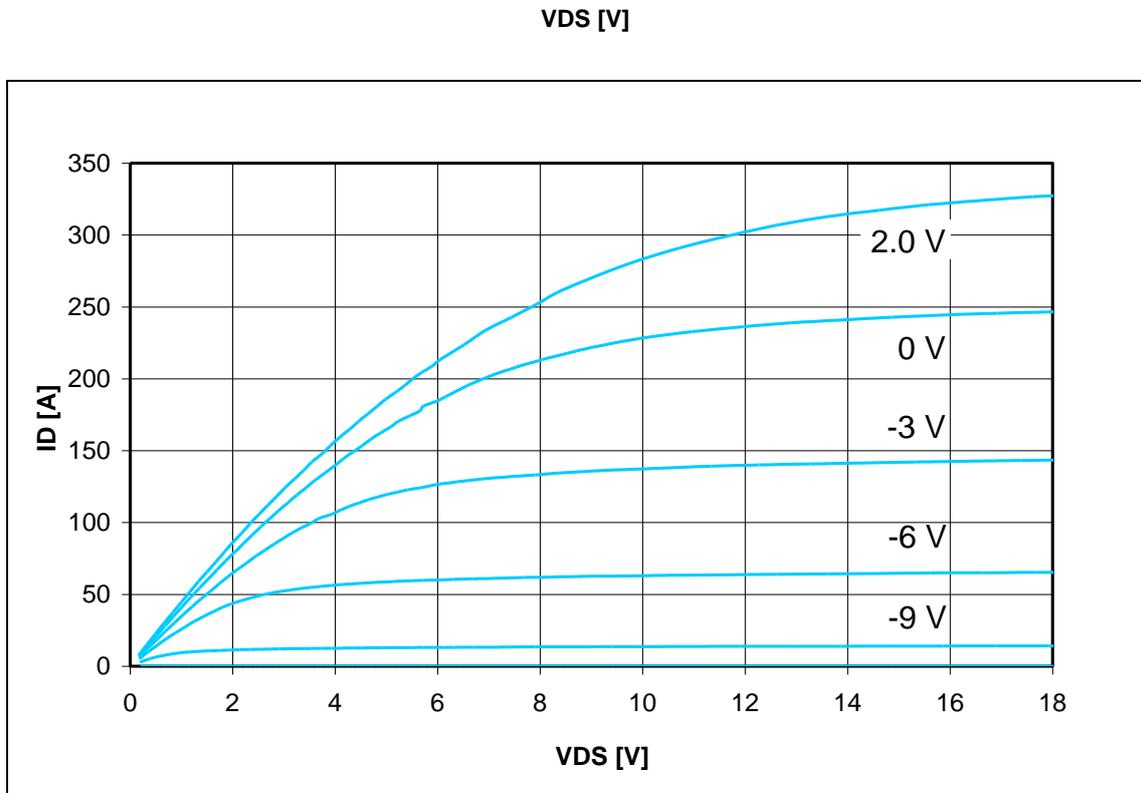


Fig. 3: Typical output characteristics of a 35mOhm rated 1200V JFET at 25°C, parametrized by the gate-source voltage.

The trend to enable more compact system design by higher switching frequency makes the reduction of dynamic losses a key element. Due to the intrinsic material properties of SiC the device shows extremely small capacitances. Furthermore, a specific advantage of our JFET device structure is the decoupling of gate and drain by the body diffusion which is connected to the source potential. As a consequence the capacitance measurements (Fig.4) show a smooth and almost ideal characteristics.

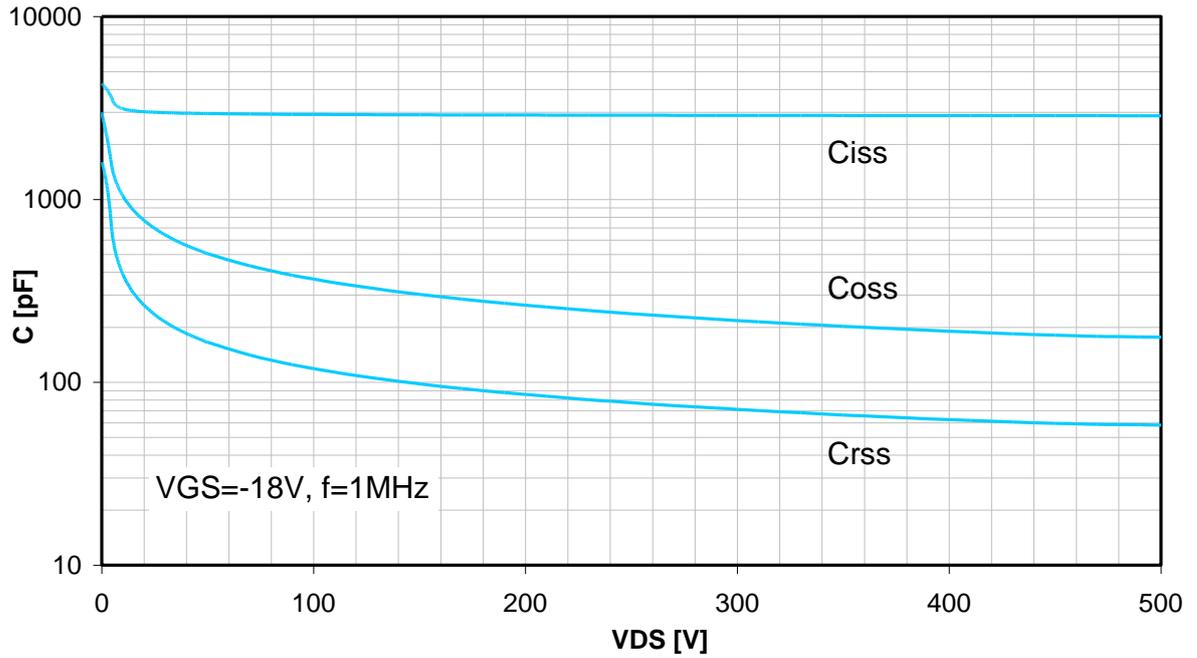


Fig. 4: Capacitances C_{ISS} , C_{OSS} and C_{RSS} vs. drain-source voltage V_{DS} ($V_{GS}=-19V$, $f=1MHz$) 35mOhm rated 1200V JFET.

This is also reflected in a favorable gate charge characteristics. Measurements show the Miller-plateau around -7V which is about half-way between turn-on and turn-off and promises a fast switching time [6].

The SiC JFET has been tested both in discrete packages [5] as well as in a half bridge module [7] in two different test platforms. Fig. 5 shows the turn-on and turn-off characteristic in our 1200V 30A Easy 1B Module.

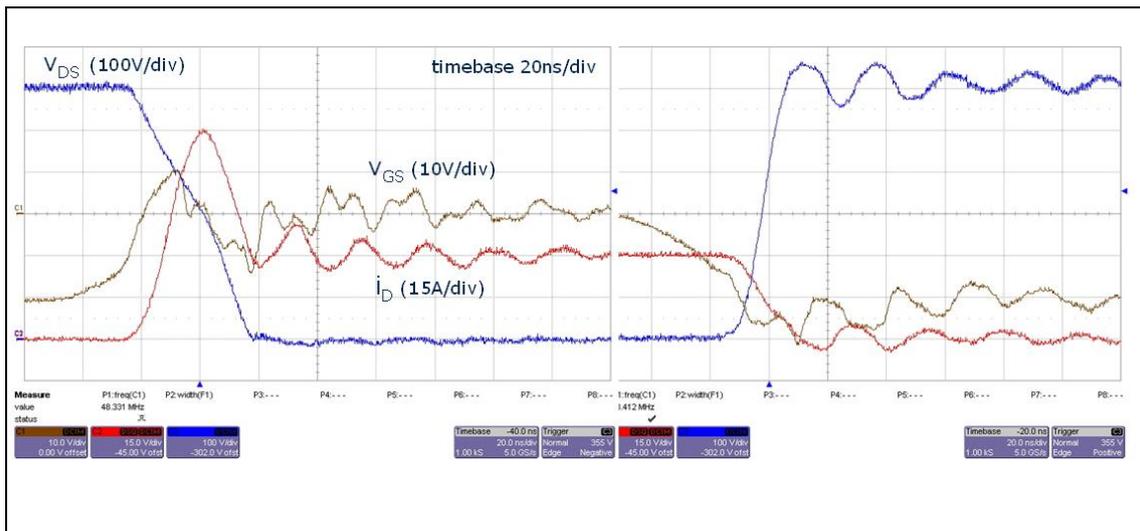


Fig. 5: Switching waveforms of the Direct Driven JFET module at $T_J=125^\circ C$, $V_{DC}=600V$, $I_D=30A$ and $R_{G,ext}=0$.

The switching waveforms show the current commutation between lowside JFETs and highside JFET body diodes. With respect to the recovery current in the turn on waveform, current only changes while the Drain-Source-voltage drops. Therefore, the main part of the reverse recovery current is of capacitive nature. The commutation against the JFET body diode can be regarded as quite similar compared to low loss Schottky diode commutation.

The switching losses are in comparison to our latest high speed IGBT generation, a factor of 2 better and nearly one order of magnitude better versus our drives-optimized TRENCHSTOP IGBT. Fig. 6 shows the comparison of the total switching losses from a comparison on discrete device level.

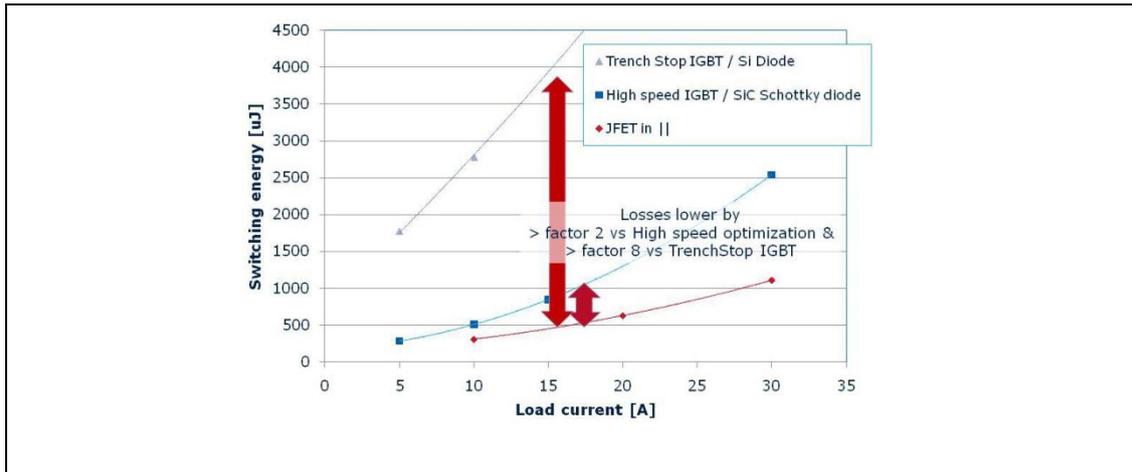


Fig. 6 : Comparison of switching losses (Turn-on plus turn-off) of a 1200V-50mΩ SiC JFET versus a combination of a high-speed optimized IGBT with a SiC Schottky barrier diode and a conventional 1200V IGBT combined with a fast Si pin-diode at $V_{DS}=800V$, $T_j =75^{\circ}C$, $R_g =3\Omega$.

3. Experimental results

For experimental validation of the device concept and its performance a 17kW-3phase inverter using the bipolar switched Neutral point clamped topology was chosen [5]. The two high frequency switches per phase – originally 1200V 40A trench stop IGBTs - were each replaced by 3 paralleled 100 mOhm-1200V SiC JFET in combination with respective 30V p-channel devices.

Fig. 7 shows efficiencies of the inverter system at optimum operation point over several output power levels. A significant difference between both solutions can be seen. The standard inverter based on Si switches achieves a maximum efficiency of 98.2%. For the inverter equipped with the new SiC JFETs 98.8% can be obtained. The presented efficiencies are system efficiencies and are the best results achievable in combination with passed EMI tests [5].

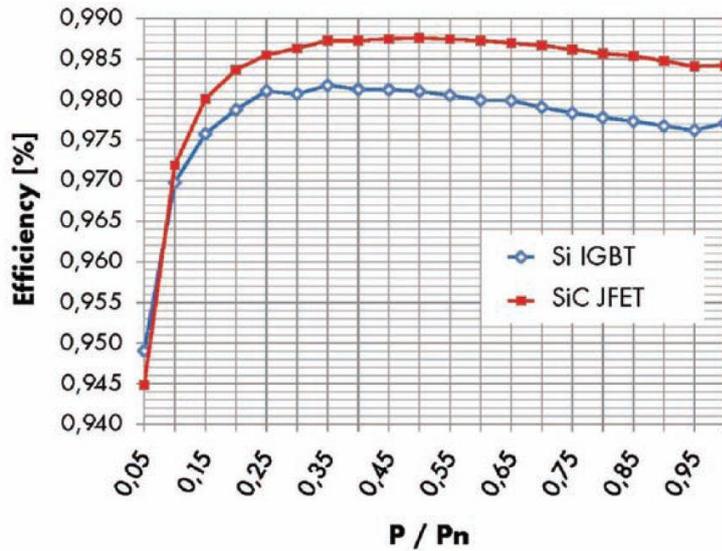


Fig. 7: Comparison of system efficiencies of a 17kW 3 phase PV inverter respectively equipped with 3 paralleled 100 mOhm 1200V SiC JFETs each versus the original setup using 40A 1200V trench stop IGBTs, taken from [5].

The efficiency as a function of input voltage and load, the so-called PHOTON tests, are depicted in Fig. 8. It can be seen that the SiC inverter reaches efficiencies equal to or more than 98% over a much wider voltage/power range in comparison to the Si based inverter.

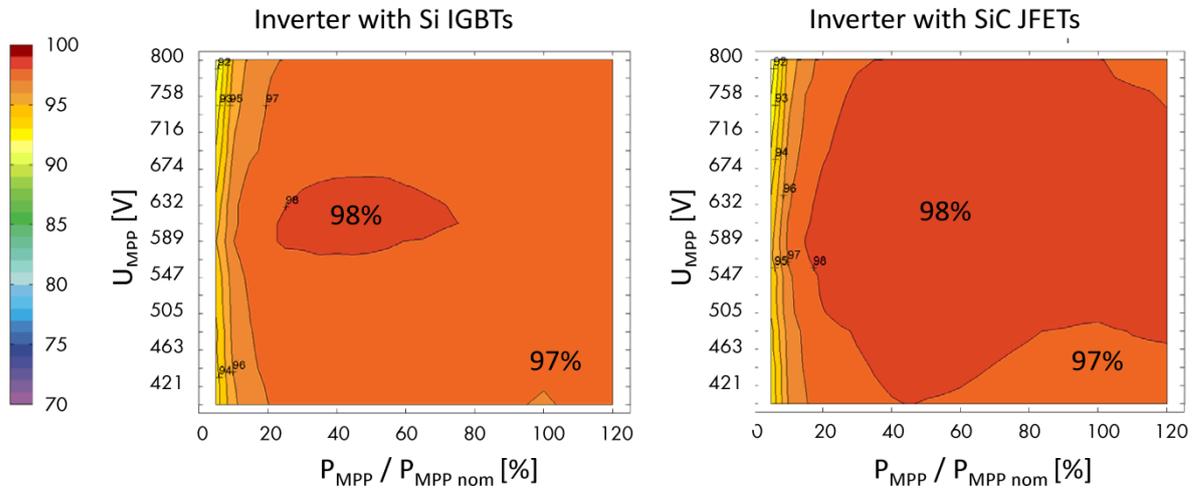


Fig. 8: Measured system efficiencies at several DC link voltages (400V up to 800V), taken from [5].

4. Conclusion

The normally-on 1200V SiC JFET shows superior forward and switching characteristics combined with a very good internal body diode. By choosing a JFET as device concept, which has no critical gate oxide, it pairs top performance with the reliability expected in demanding applications such as PV inverters.

As demonstrated the efficiency in the chosen PV inverter was increased significantly. This will pave the way towards much higher frequency operation, thus enabling more compact and cost-effective designs.

5. References

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