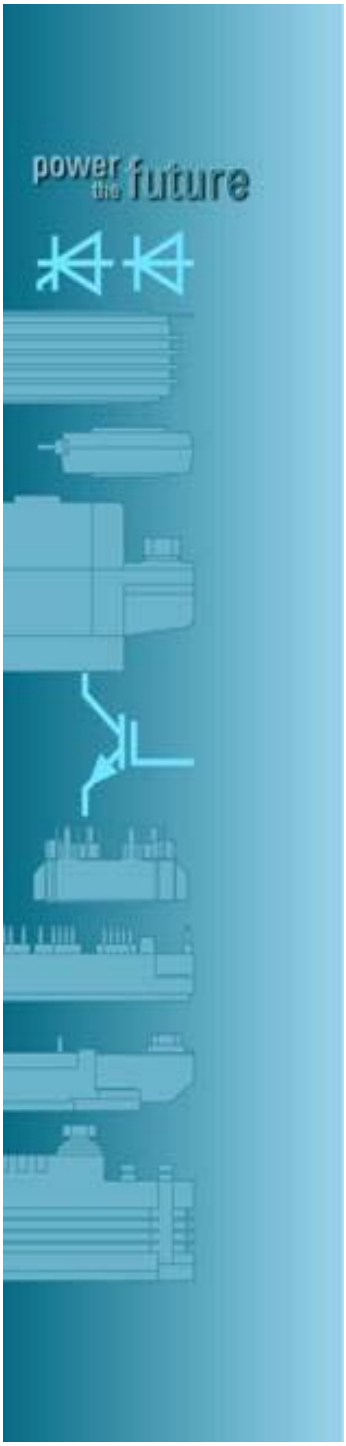
Switching behavior and optimal driving of IGBT^3 modules



1. Chip Technology

The IGBT chip of the third generation (IGBT^3) has a trench structure and combines the advantages of PT and NPT technologies thanks to an additional n-doped layer, known as the **F**ield **S**top (FS) layer, within the NPT structure.

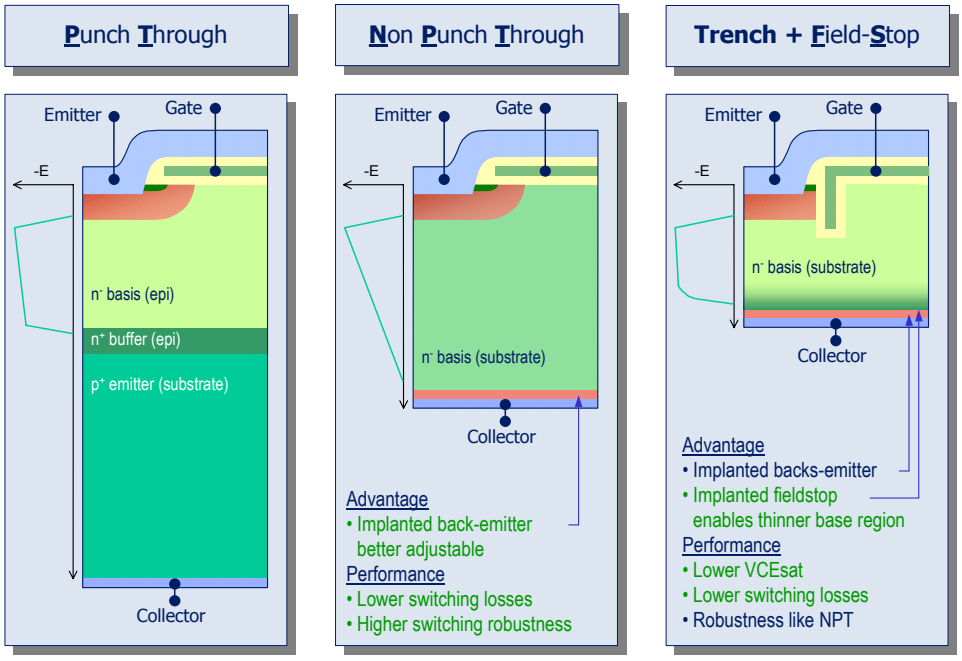


Bild 1.1. Chip Technologie

This technology allows both static and dynamic losses to be minimized. In combination with the higher current density of the IGBT^3, it allows the power range of this family of products to be extended.

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2. Switching behavior

2.1. Turn-on behavior

The rate-of-rise of voltage (-dv/dt) and of current (di/dt) during the turn-on process can be controlled by changing the gate resistance, a function already familiar from the NPT IGBTs of the second generation. Both switching transients are reduced as the gate resistance increases.

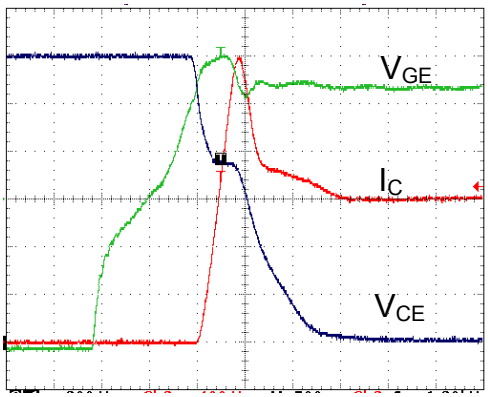


Fig. 2.1.1 Turn-on process with nominal gate resistance (minimum gate resistance specified in the data sheet)

V_{CE} = 1200V (dv/dt=0,9kV/µs)

I_C = 1200A (di/dt=6,4kA/µs)

V_{GE} = ±15V (I_{Cpeak} = 2,4kA)

Eon = 816mWs

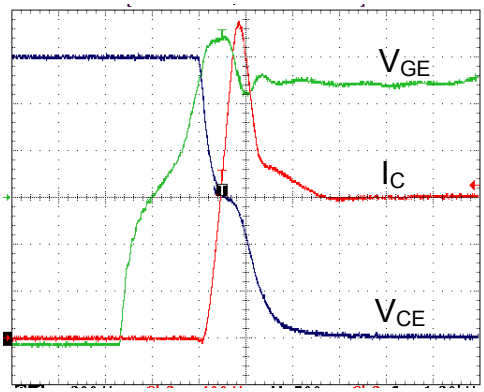


Fig. 2.1.2 Turn-on process with lower gate resistance (lower than the gate resistance specified in the data sheet not recommended)

V_{CE} = 1200V (dv/dt=1,4kV/µs)

I_C = 1200A (di/dt=8,7kA/µs)

V_{GE} = ±15V (I_{Cpeak} = 2,7kA)

Eon = 544mWs

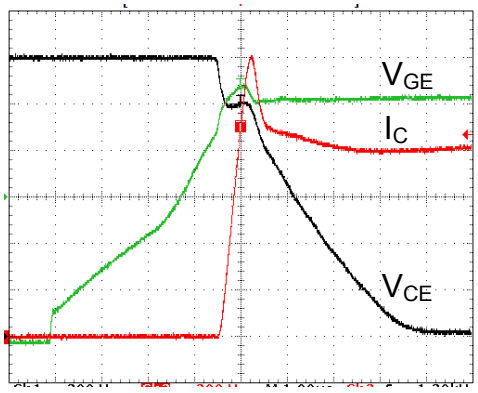


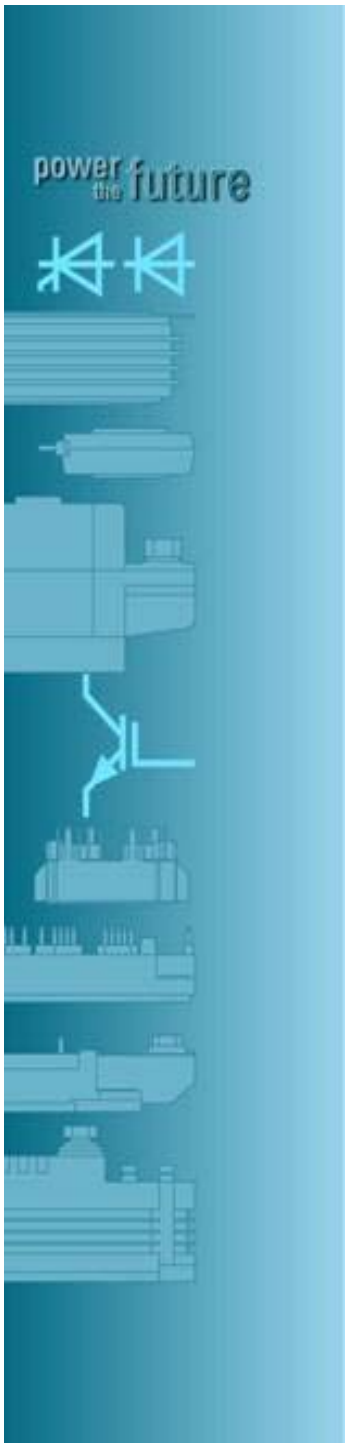
Fig. 2.1.3 Turn-on process with higher gate resistance (maximum gate resistance specified in the data sheet)

V_{CE} = 1200V (dv/dt=0,3kV/µs)

I_C = 1200A (di/dt=3kA/µs)

V_{GE} = ±15V (I_{Cpeak} = 1,81kA)

Eon = 2558mWs



2.2 Turn-off behavior

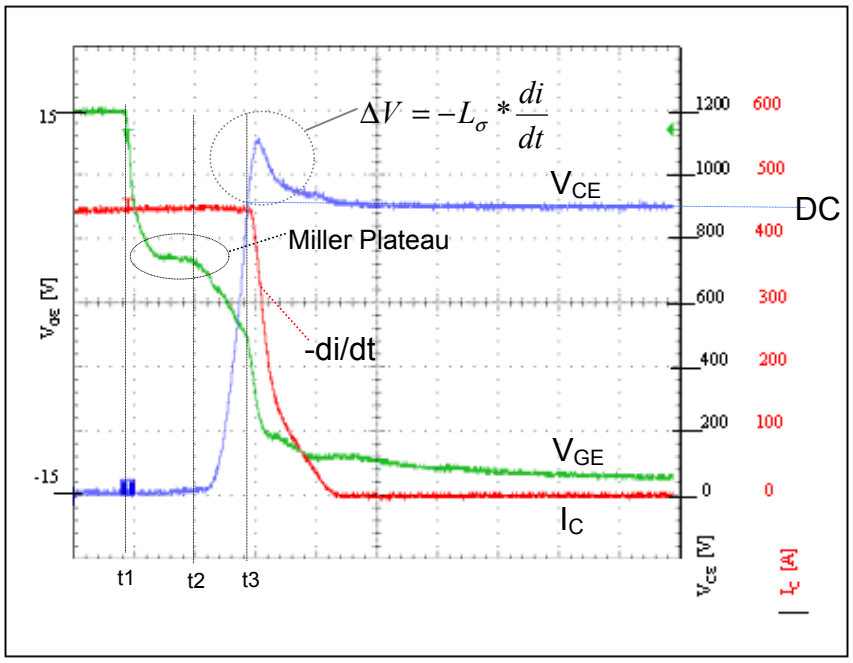
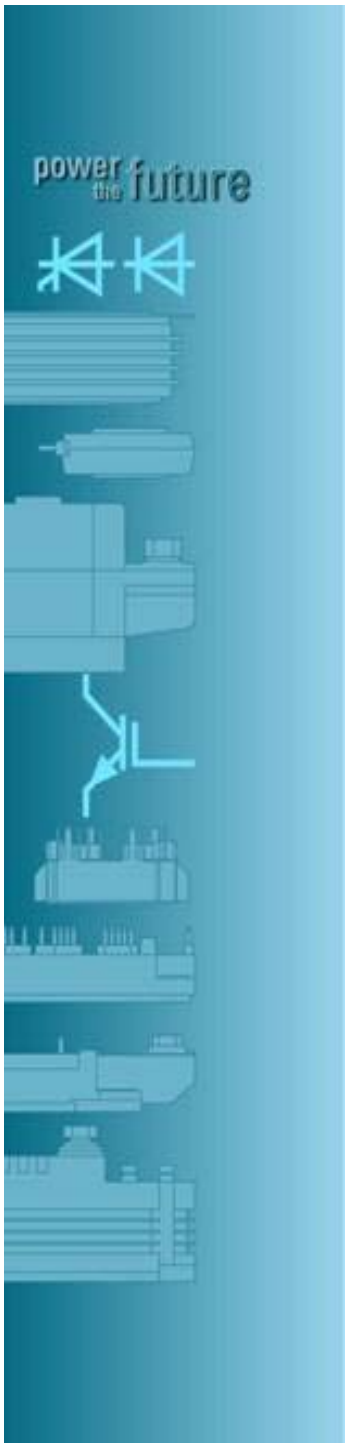


Fig. 2.2.3 Turn-off response of a 1700V IGBT³ with nominal gate resistance. Display of V_{GE}, I_C, and V_{CE}.

The turn-off process begins with a drop in gate voltage (t1). When this voltage drops to the Miller plateau (discharge of the reverse transfer capacitance C_{res}), the IGBT³ starts to build up a reverse voltage (t2). The (dv/dt) can be controlled by the gate resistance, i.e. it is reduced by an increase in the latter. However, the current slope (-di/dt) can no longer be controlled by the gate resistance when the gate voltage drops below the Miller plateau before the drop in the IGBT current (see Figs. 2.2.1 and 2.2.2). This is the case when a resistor is used with a rating close to its nominal value. Only in the region of large gate resistances can the current slope be controlled when the gate voltage remains at the Miller plateau up to current commutation. The current is commutated to the associated free-wheeling diode at inductive load (t3) whenever the reverse voltage at the IGBT reaches the level of the DC intermediate circuit.



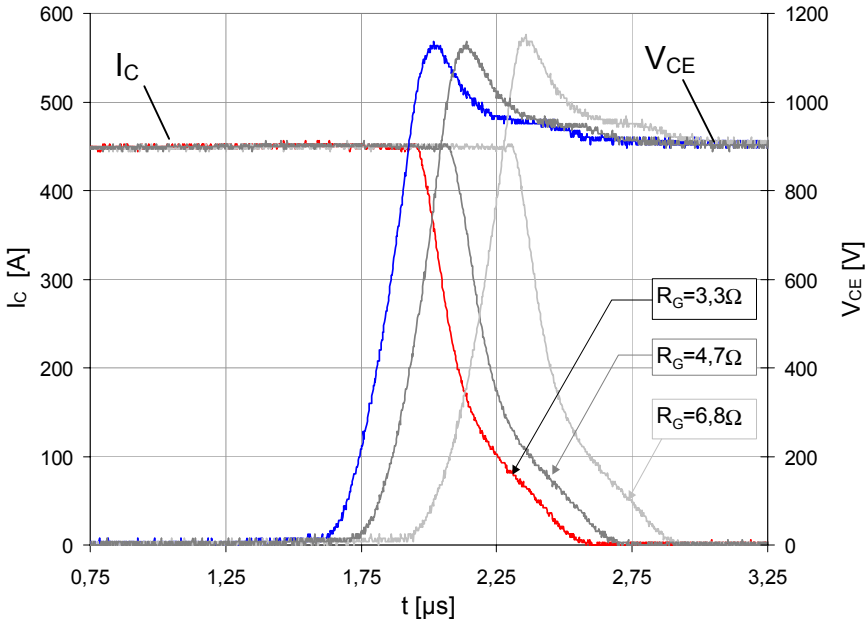


Fig. 2.2.1 Turn-off response of a 1700V IGBT³ with differently dimensioned gate resistors. Display of I_C and V_{CE}.

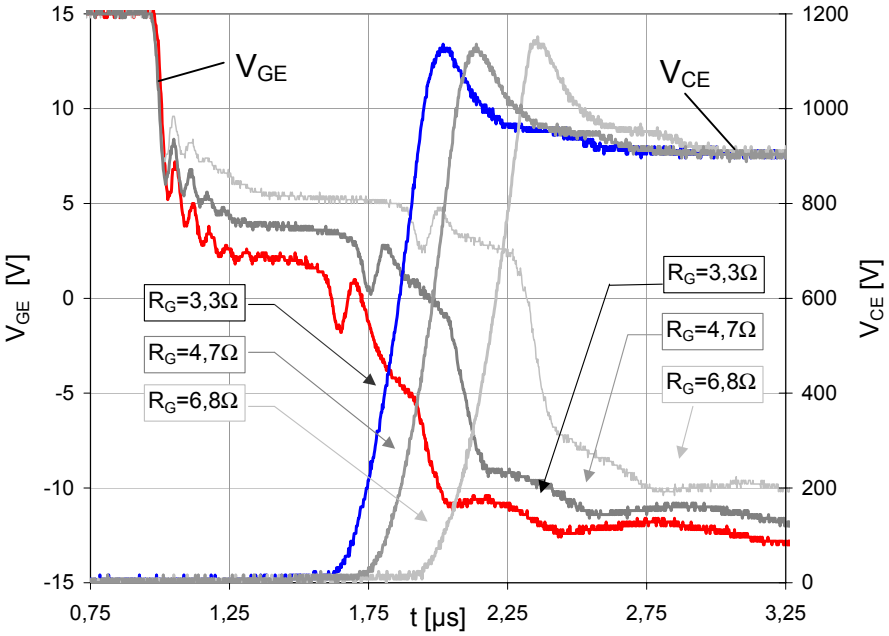
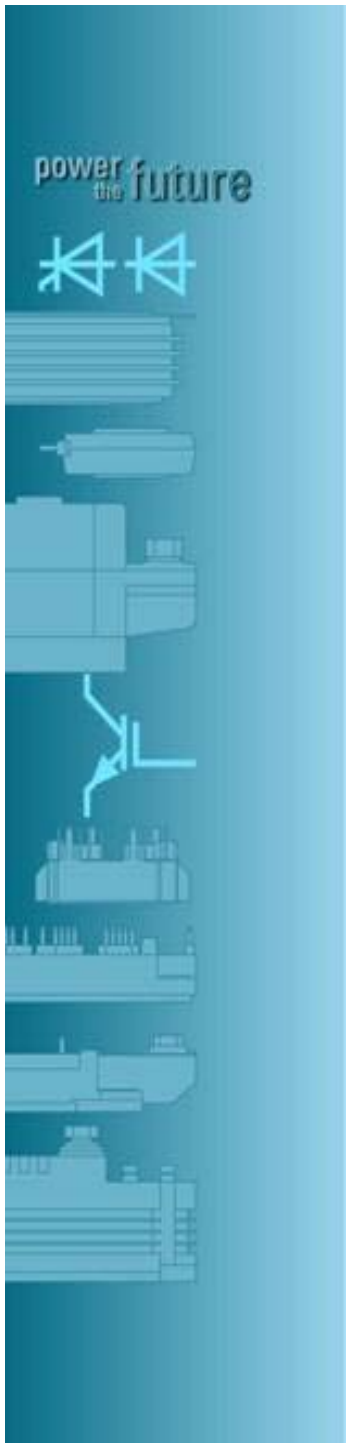


Fig. 2.2.2 Turn-off response of a1700V IGBT³ with differently dimensioned gate resistors. Display of V_{GE} and V_{CE}.

The position of the Miller plateau is determined through the ratio of external gate resistor of the module (data sheet value) to the internal gate resistor.



2.3. Limiting the turn-off overvoltage in IGBTs

Current slopes generate overvoltages (ΔV) at the IGBT due to the parasitic inductances (L_σ) of the DC intermediate circuit and the internal inductances of the IGBT module: $\Delta V = -L_\sigma * \frac{di}{dt}$

Overvoltages occurring at the IGBT module during the turn-off process must naturally always be limited to the maximum reverse voltage of the module.

To ensure that the IGBT^3 can be controlled during the turn-off process and thus to limit the overvoltage, the gate voltage must be at the Miller plateau at this time and must not yet have fallen below it. This may occur via capacitive feedback of the collector voltage to the gate, for example.

The (dv/dt) is coupled into the driver via C_{ZD}. At a sufficiently high (dv/dt), the gate voltage is raised to the Miller plateau or maintained there. The gate voltage must have reached this plateau before the reverse voltage of the IGBT attains the intermediate circuit voltage (the current starts to drop).

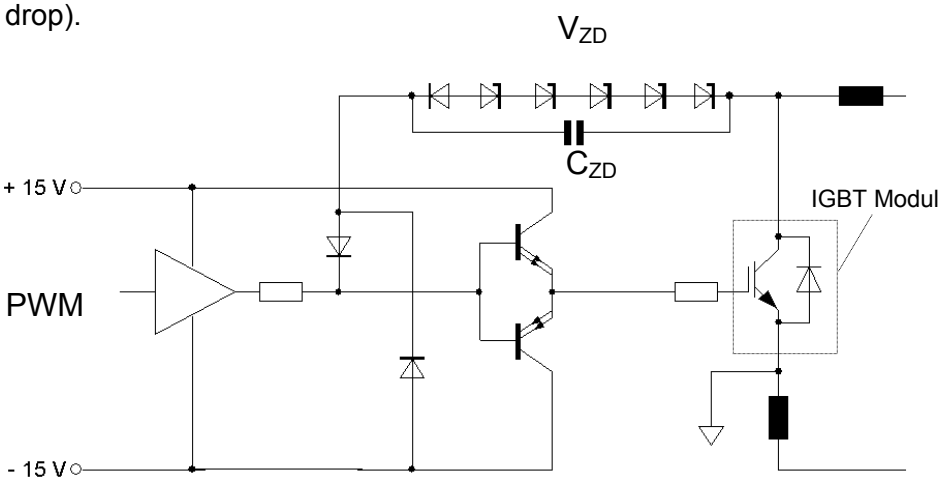


Fig. 2.3.1 Basic circuit diagram for capacitive feedback

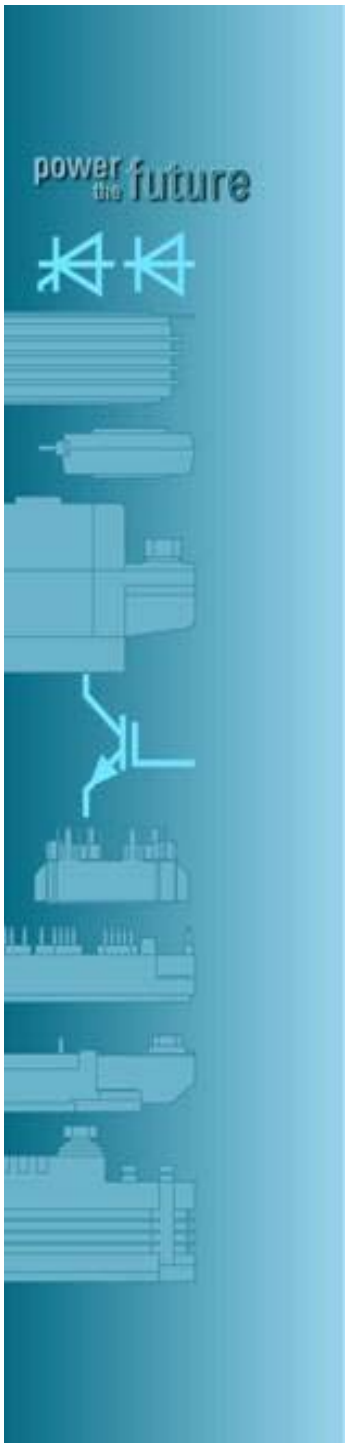
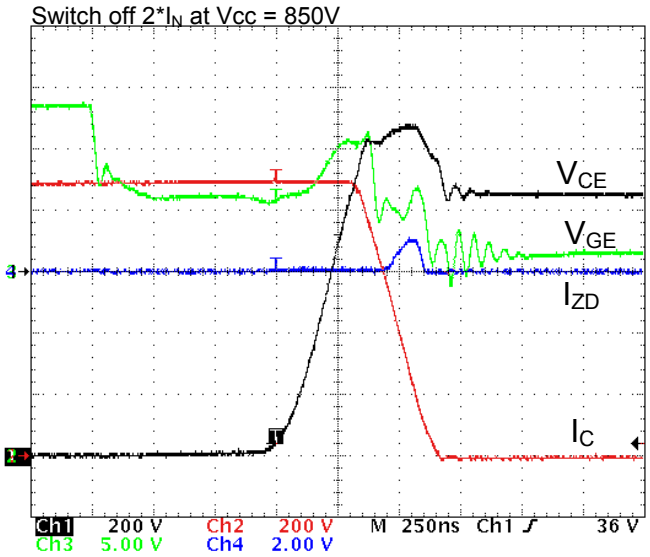


Fig. 2.3.2 shows the effectiveness of this circuit



V_{ZD} = 1000V

C_1 = 250pF

V_{Max} = 1080V

Fig. 2.3.2 Schematic mode of operation of the basic circuit for capacitive feedback

The turn-off losses are not increased significantly by this measure with corresponding dimensioning – thanks to the lower voltage peaks – and may even be reduced with optimization. The components must be dimensioned and optimized according to the requirements of specific applications.

The IGBT^3 can be used with a standard gate driver circuit or if required by the application, the circuit can be extended by the capacitive feedback which described above, and can thus be optimally deployed with its advantages of a low forward voltage and low switching losses.

The Dual IGBT 2ED300C17-S driver from eupec allows these optional functions to be implemented. It is a member of the ***EiceDRIVER***™ driver family (**e**upec **I**GBT **c**ontrolled **e**fficiency **DRIVER**). Further information on this driver may be obtained from the relevant data sheet.