Microcontrollers

Errata Sheet

29 June 2001 / Release 1.4

Device:	**C505L-4EM**
Stepping Code / Marking:	**CA**
Package:	**P-MQFP-80**

This Errata Sheet describes the deviations from the current user documentation. The classification and numbering system is module oriented in a continual ascending sequence over several derivatives, as well already solved deviations are included. So gaps inside this enumeration could occur.

The current documentation is: C505L User's Manual 11.99
C505L Data Sheet 06.99
Instruction Set Manual 05.98

Note: ***Devices marked with EES- or ES are engineering samples which may not be completely tested in all functional and electrical characteristics, therefore they should be used for evaluation only.***

The specific test conditions for EES and ES are documented in a separate Status Sheet.

Change summary to last Errata Sheet Rel. 1.3:

- New item numbered OTP.1.
- DC.2 has been updated on Data Sheet 06.99.

Functional Problems:

LCD.3: LCD display glitches occasionally at higher V_{DD} when clocked by RTC clock

At higher V_{DD}, the LCD may occasionally display some weird characters when clocked by the RTC clock at XTAL3.

Workaround:

To avoid the display glitches from becoming apparent, clock the LCD with the system clock. If it is required for the LCD to display when the microcontroller is in power down mode (LCD must be clocked by RTC clock in this mode), the clock input to LCD can be dynamically switched between system clock and RTC by software.
The following is a software workaround in C:

```
.....initialisations.....
PCON1=*;
RTINT*=0x**;      //set RTC interrupt value (necessary only if wakeup from power down by RTC is required)
RTCR*=0x00;       //set RTC reload value to 0
.....user codes.....
DAC0=0x**;        //set LCD contrast
LCON=0x01;        //LCD initialisation, use sys clk
LCRL=0x84;
LCRH=0xec;        //LCD is started
.....codes for LCD.....
.....just before power down is entered.....
LCON=0x03;        //LCD use RTC clock
LCRL=0x2e;        //no visible side effects even though LCRL & LCRH are changed later &
LCRH=0x80;        //while LCD is running
//(if wakeup from pd IS via RTC interrupt, this line of code must be just before power down is entered
RTCON=0x03;       //start RTC running, allow pd wakeup via RTC
//)
PCON|=0x02;       //power down enabled
PCON|=0x40;       //power down entered
Afterpd:          //Wakeup can be initiated by either RTC interrupt or external interrupt
                  //The following is executed after return from power down wakeup interrupt
LCON=0x01;        //LCD use sys clk again on wakeup from pd
LCRL=0x84;
LCRH=0xec;
.....user codes.....
```

RTC.1: When RTINT=00h, IRTC is set even when there is no input at XTAL3

Conditions are RTINT=00h, RTC interrupt enable bit ERTC=1 and RTC is started. Interrupt flag bit IRTC is set even when there is no input at XTAL3. If power down is entered and wakeup via RTC interrupt has been enabled, wakeup will occur immediately since the IRTC flag is set, which may be undesirable.

Workaround:

When ERTC=1, RTINT should not be set to 00h. Valid input at XTAL3 must be ensured before RTC is started.

RTC.3: RTC count inaccuracy

The RTC does not count 100% accurately within the specified range $4.25<V_{DD}<5.5$ although it counts fairly consistently at each V_{DD}. The percentage error may vary slightly from device to device, depending on board layout, operational voltage V_{DD}, capacitance and type of crystal used in the XTAL3/XTAL4 external clock circuitry.

(The following values are obtained using our evaluation board and actual errors may vary on another board. At V_{DD}=5V, error~0.26% in 5120s using C3=68pF, C4=48pF when the microcontroller is in power down mode. At V_{DD}=5V, error~1.29% in 4800s when the microcontroller is in normal operational mode.)

Workaround:

None.

However, to reduce count inaccuracy, ensure optimal board layout to minimise noise at XTAL3. Use crystal of good consistency and accuracy, and a suitable combination of capacitance in the XTAL3/XTAL4 clock circuitry (recommended values are C3=68pF,C4=33pF or C3=68pF,C4=47pF). Note that better accuracy can be achieved at lower V_{DD} (minimum specified=4.25V).

WDT.1: Watchdog Timer is not halted in idle mode

The Watchdog Timer (WDT) is not halted in the idle mode as defined. However, during the idle mode, an overflow condition of the WDT does not initiate an internal reset. In such a case the WDT starts a new count sequence.

Workaround:

1. Do not use the WDT function in combination with the idle mode.

2. In case of WDT is running before entry into idle mode, to avoid a WDT initiated reset upon exit of the idle mode, the following methods can be used.

(A) The WDT is refreshed immediately upon exit from idle mode.

(B) A timed interrupt can be used to exit the idle mode before the WDT reaches the counter state 7FFCh. This can be achieved by using Timer 0, 1 or 2. This timer can be programmed to generate an interrupt at a WDT counter state prior to overflow, for e.g., at 7F00h. Prior to entering idle mode, the WDT can be refreshed and the timer 0, 1or 2 can be started immediately to synchronize the WDT. In the interrupt service routine of the Timer 0, 1 or 2, the WDT must be refreshed. If required, idle mode could be entered again.

SWPD.1: Triggering of Software Power Down (SWPD) wake up immediately after SWPD entry via external interrupt on a frequent basis is not recommended

When the micro-controller is running at frequencies lower than 10MHz and the external wake up from SWPD occurs very soon (e.g. <200ms) after entering this mode and this happens on a regular basis, the internal clock may still be valid when the wake up trigger occurs. In this rare case, the micro-controller may get confused with its state and program execution becomes unpredictable.

Workaround:

In applications running at 10MHz or below, that enters and exits the SWPD mode on a frequent basis, it is recommended to enter Slow Down mode before Power Down mode entry. On SWPD wake up, the first instruction in the interrupt routine at 07bH should disable Slow Down mode. This method would only cause an insignificant delay in the range of μs and would ensure specified behavior of the micro-controller. Note that when Slow Down mode has been entered, there is no longer a minimum time requirement before SWPD external wake up is triggered.

OTP.1: OTP module may fail under special conditions, leading to undefined operation

The OTP module may malfunction, causing the chip to enter an undefined state with unsteady operation, if there is a remaining voltage at the V_{DD} pin before powering up. The critical remaining voltage is approximately 100-400mV. The undefined state can only be left by a complete power off (V_{DD}=0V) and not by any RESET-source (e.g. hardware reset, WDT-reset). The problem is due to variation in technology and manufacturing parameters.

Workaround:

The device should always be powered up from V_{DD}=0V, ensuring that there is no voltage at any pins which leads to a remaining voltage level at V_{DD} pin (coupling over the ESD-structure).

Deviation from Electrical- and Timing Specification:

DC.3: ADC TUE is +-3 LSB

The total unadjusted error of the A/D converter module is +-3 LSB, instead of +-2 LSB specified.

DC.4: V_{DD} is valid for a smaller range than specified on documents

V_{DD} is valid in the range from 4.5V to 5.5V at all specified temperatures, instead of 4.25V to 5.5V as specified on the documents. This smaller range is effective on devices with date code starting from *0116*.

History List (since last CPU Step ES-BB)

Functional Problems

Functional Problem	Short Description	Fixed
LCD.3	LCD display glitches occasionally at higher V_{DD} when clocked by RTC clock	
RTC.1	When RTINT=00h, IRTC is set even when there is no input at XTAL3	
RTC.2	RTC reset problem	Fixed in step ES-CA
RTC.3	RTC count inaccuracy	
WDT.1	Watchdog Timer is not halted in idle mode	
SWPD.1	Triggering of Software Power Down (SWPD) wake up immediately after SWPD entry via external interrupt on a frequent basis is not recommended.	
OTP.1	OTP module may fail under special conditions, leading to undefined operation	

AC/DC Deviations

AC/DC Deviation	Short Description	Fixed
DC.1	$I_{PD1,}$ I_{PD3} > 50µA	Fixed in step ES-BB
DC.2	V_{IH} minimum on EA pin does not meet the specification values	DS 06.99
DC.3	ADC TUE is +-3 LSB	
DC.4	V_{DD} is valid for a smaller range than specified on documents	

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