Design Note

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Design of 30W Off-Line SMPS using CoolSET ICE2B265

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1. Introduction

The CoolSET ICE2B265 is an integrated pulse width modulator with built in CoolMOS. It is an inexpensive controller combined with the CoolMOS power switch with which designers can obtain all the stringent requirements imposed on the present modern Switched Mode Power Supply (SMPS) like very low standby power, few external components count and minimized PCB size. This application note provides beside functional description of the ICE2B265, it presents also the design of simple low cost and high efficient 30W Flyback SMPS circuit.

2. Block Diagram

The control section of the CoolSET provides several special enhancements to satisfy the needs for low power standby and protection features. It consists of 5 main units, the Power Management, the Softstart, the Improved Current Mode, the Current Limiting, the Standby and the Protection Unit. The Standby Unit enables the frequency reduction to lower the power consumption in standby mode. The
frequency reduction is limited to 21kHz to avoid audible noise. In case of failure modes like open loop, overvoltage or overload due to short circuit the device switches into Auto Restart Mode, which is control by the Protection Unit. With the patented Propagation Delay Compensation circuit integrated in the Current Limiting Unit, the peak current limitation can be controlled precisely. It leads to more cost efficient dimension of the transformer and the secondary diode.

3. Power Management

Fig.2 shows the Power Management Unit of the IC. The external supply voltage $V_{CC}$ is monitored by the Undervoltage Lockout. The external capacitor $C_{VCC}$ is charged up by the current through the $R_{START-UP}$, when the SMPS is plugged to the main line. The IC remains inactive before $V_{CC}$ reaches the on-threshold $V_{CCON}=13.5V$. The current consumption of the IC at this moment is max. 55μA. When the on-threshold is exceeded, the IC is activated:

- The internal bandgap generates a reference voltage $V_{REF}=6.5V$ to supply the internal circuit.
- The internal Error-latch in the protection unit is reset by the Power Up Reset. The Error-latch flip-flop is then ready to shut down the gate drive if the Protection Unit is activated.
- The soft-start transistor switch $T_1$ is released by the Power-Down Reset. The current through $R_{SOFT-START}$ starts to charge the external soft-start capacitor $C_{SOFT-START}$. The soft-start is then activated.

To avoid uncontrolled ringing at switch-on a hysteresis at the Undervoltage Lockout is implemented which means that switch-off is only after active mode when $V_{CC}$ falls below 8.5V.

When $V_{CC}$ falls below the off-threshold $V_{COFF}=8.5V$ the internal reference is switched off and the Power Down Reset let the transistor switch $T_1$ to discharge the soft-start capacitor $C_{SOFT-START}$. Thus it is ensured that the soft-start is always activated at every switch-on.

4. Start-up delay

During startup, $C_{VCC}$ is charged by the current through $R_{START-UP}$. The IC is activated only when the $V_{CC}$ reaches the on-threshold of $V_{CCON}=13.5V$. Because of the very low IC current consumption before activation, high value startup resistor can be used to minimize power loss in start-up resistor. The value of $R_{START-UP}$ and $C_{VCC}$ will effect the startup delay time, which can be estimated by using equation as follow:

$$t_{delay} = \frac{C_{VCC} \times V_{CCON}}{V_{IN} \times R_{START-UP} - I_{VCC1}}$$

$t_{delay}$ is the duration of the startup time from the moment the SMPS is plugged to the main line until the IC is activated. $V_{IN}$ is the rectified line input voltage and $I_{VCC1}$ is the current consumption of the IC before activation. Fig.3 shows the $t_{start}$ delay of the actual SMPS with $R_{START-UP} = 2 \times 470k\Omega$, $C_{VCC}=47\mu F$ and $V_{IN}=380V$. (1) indicates that the start-up delay time depends not only on the main input voltage but also mainly on the value of $R_{START-UP}$ and $C_{VCC}$. The $t_{delay}$ can be shorten by reducing the $R_{START-UP}$ value. However, the loss at $R_{START-UP}$ will increase. It has to be compromised between shorter startup delay time and loss at startup resistor.
Startup circuit with transistor switch can be implemented to achieve startup without losses and constant shorter delay time.

\[ P = \frac{1}{2} \times L \times f \times i_p^2 \]  

(2)

Where \( P \) is the power stored in the primary inductor, \( L \) is the primary inductor, \( f \) is the switching frequency and \( i_p \) is the peak primary current.

As can be seen, the line-input voltage does not appear in (2). One of the advantages of the Current Mode is that the line variation does not influence the regulation of the output voltage. However, the Current Mode is extremely susceptible to noise on the sense voltage. A noise spike is generated each time the power Mosfet switch is turned on which might turn off the driver immediately especially when the power is small and the FB signal is low.

To improve the Current Mode during light load, a voltage ramp is implemented in the IC.

The amplified current sense voltage \( V_{CS} \) is superimposed on the voltage ramp, which is built by the switch \( T_2 \), the voltage source \( V_1 \) and 1st order low pass filter composed of \( R_1 \) and \( C_1 \) (see Fig.5).

Thus, the turn-on time of the power MOSFET as well as the peak primary current is well defined by the level of the FB signal. For flyback converter with discontinuous current operation the power stored in the primary inductor is represented by the equation
Fig. 6 shows the effect of the Voltage Ramp in normal load condition. The switch $T_2$ is opened at the falling slope of the oscillator. It enables the Voltage Ramp to rise. The Gate Driver turns on the power MOSFET when the Voltage Ramp reaches 0.3V. The primary current starts to flow and is sensed by $R_{CS}$. The current sense voltage $V_{CS}$ is amplified 3.65 times by the PWM OP, which is then superimposed on the Voltage Ramp. The current flow is terminated when the amplified sense voltage on the Voltage Ramp reaches the FB voltage level.

In case of light load (see Fig. 7) or no load, the current sense voltage $V_{CS}$ is so small that only the Voltage Ramp remains as a well defined signal for the comparison with the FB-signal.

The slope of the Voltage Ramp then controls the turn-on time of the Gate Driver. The Gate Driver is turned on only when the Voltage Ramp exceeds 0.3V due to the Comparator $C_5$. The turn-on time can then be continuously reduced to zero by decreasing $V_{FB}$ below that threshold.

6. Soft-Start

The Soft-Start voltage $V_{SOFTS}$ is generated by charging the external capacitor $C_{SOFTS}$ through the internal pullup resistor $R_{SOFTS}$ (see Fig. 8). The Soft-Start comparator compares the Soft-Start voltage $V_{SOFTS}$ at the negative input with the ramp voltage of the superimposed Voltage Ramp at the positive input. In Soft-Start phase $V_{SOFTS}$ is always smaller than the Feedback Voltage $V_{FB}$. In this case $V_{SOFTS}$ defines the pulse width of the Gate Driver through the Soft-Start Comparator by resetting the PWM-Latch. The Soft-Start phase is completed when $V_{SOFTS}$ reaches 5.3V (Fig. 9). The Soft-Start time is then defined by

$$T_{SOFT-START} = 1.69 \times R_{SOFTS} \times C_{SOFTS} \ (3)$$

The transistor switch $T_1$ at Soft-Start is controlled by the Power Down Reset. It is to ensure that the Soft-Start is always activated at the restart of the IC after power down or in Auto Restart mode.
The Soft-Start voltage $V_{SOFTS}$ is used not only for minimization of current and voltage stresses on the external power MOSFET switch during start-up, it is also used for activation of the Protection Unit (Fig.10).

When the Soft-Start phase is over ($V_{SOFTS} > 5.3V$), the Error Latch will be activated by Comparator $C_4$ if the feedback voltage $V_{FB}$ does not drop below 4.8V, which means that the output voltage $V_{OUT}$ at the secondary side of the SMPS does not reaches its nominal level. To ensure proper start-up of the SMPS, the duration of the Soft-Start phase has to be long enough to enable $V_{OUT}$ to rise to its nominal value. This will cause the control loop to pull down the level of the feedback signal $V_{FB}$ below 4.8V (see Fig.11).

7. Oscillator and Frequency Reduction

The oscillator, which generates the switching frequency $F=67kHz$, is integrated in the IC. The oscillator is adjusted so that the Gate driver pulse can reach a maximum duty cycle of $D_{MAX} = 0.72$.

The frequency of the oscillator can be influenced by the feedback voltage $V_{FB}$ as shown in Fig.12. This feature allows a SMPS to operate at lower frequency at light loads thus lowering the switching losses while maintaining good cross regulation performance and low output ripple. The power consumption of the whole SMPS can be reduced very effectively at light load. The minimal reachable frequency is limited to 20kHz to avoid audible noise in any case.
8. Current Limiting

The cycle by cycle current limiting is performed by the Current Limit Comparator (see Fig. 13). The primary current \( I_p \) is converted into a sense voltage \( V_{CS} \) by an external sense resistor \( R_{CS} \). The sense voltage \( V_{CS} \) goes through the 200ns Leading Edge Blanking before reaching the Current Limit Comparator. When \( V_{CS} \) exceeds the internal threshold voltage \( V_{CSTH} \), the Current Limit Comparator immediately turns off the Gate Driver via the PWM Latch. A Propagation Delay Compensation is added to the Current Limiting circuit to avoid excessive overshoot of the primary current, especially at the high line voltage (refer to chapter 10 Propagation Delay Compensation).

9. Leading Edge Blanking

Each time when the CoolMOS is switched on a leading spike is generated due to the primary-side capacitance and secondary-side rectifier reverse recovery time (Fig. 14). This spike causes a premature turn-off of the Gate Driver if it exceeds the threshold voltage \( V_{CSTH} \). To avoid it, the spike is blanked out with a time constant of \( t_{LEB} = 220\text{ns} \). During the blanking time the Gate Driver can not be switched off by the Current Limit Comparator.

10. Propagation Delay Compensation

In case of overcurrent detection, that is when the sense voltage \( V_{CS} \) reaches the threshold voltage of the Current Limit Comparator \( V_{CSTH} \), the shut down of the internal CoolMOS is delayed due to the propagation delay of the circuit between the current sense input \( I_{SENSE} \) and the Gate Driver output. This delay causes an overshoot of the peak primary current \( I_{PEAK} \). The overshoot is serious particularly at high input line voltage. Fig. 15 shows an example of different current overshoots at two different line voltages. The example assumes that the primary inductance is 500\( \mu \text{H} \), the current sense resistor \( R_{SENSE}=1\Omega \), the propagation delay time \( t_{PROP\text{ DELAY}}=200\text{ns} \) and the input line voltages after rectification are \( V_{IN1}=100\text{V} \) and \( V_{IN2}=370\text{V} \).

The result of the example obviously shows that if the current sense threshold \( V_{CSTH} \) is set at a constant level \( V_{CSTH} = 1\text{V} \), the current overshoot \( I_{OVERSHOOT2} \) at high line input voltage of \( V_{IN2}=375\text{V} \) and at \( t_{DELAY} = 200\text{ns} \) is 15% higher than the actual current limit \( I_{LIMIT} \).
The Propagation Delay Compensation which is done by means of a dynamic voltage threshold $V_{CSTH}$ as shown in Fig.16 is integrated in the IC to minimize the overshoot.

At high line input voltage, when the slope of the current sense voltage $V_{CS}$ is steeper, the Gate Driver is switched off earlier due to the lower $V_{CSTH}$. The effect of the overshoot is then compensated.

The Propagation Delay Compensation in the IC is designed so that the tolerance of the internal current limiting is at +/- 5%. The propagation delay time is compensated over temperature within a range of at least

$$0 \leq R_{CS} \times \frac{dI_p}{dt} \leq 1 \frac{dV_{CS}}{dt}$$

In this way, the IC is able to accurately limit the overcurrent (see Fig.17).

11. Protection Unit

An overload, open loop, overvoltage detection and a thermal shutdown are integrated within the Protection Unit (see Fig.1, Block Diagram). If the Protection Unit is activated, the Error Latch is set that disables the external power MOSFET after a blanking time of 5μs. The blanking is used to avoid mistriggering of the Error Latch by voltage spikes during normal operation mode.

12. Overload + Open Loop with normal load and Auto Restart Mode

Fig.18 shows the Auto Restart Mode in case of overload or open loop with normal load. The detection of open loop or overload is provided by the Comparator C3, C4 and the AND-gate G2 (see Fig.19).

During operation at normal load the supply voltage of the IC $V_{CC}$ is in the range of...
8.5V and 13.5V, the Soft-Start voltage \( V_{SOFTS} \) is above 5.3V and the feedback voltage \( V_{FB} \) stays lower than 4.8V. At this time the Comparator \( C_4 \) has released one of the input of the AND-gate \( G_2 \). The comparator \( C_3 \) is now able to set the Error-Latch in case of open loop or overload, which leads the feedback voltage \( V_{FB} \) to rise above 4.8V. 5us after the \( V_{FB} \) reaches the threshold voltage of 4.8V, the Gate Driver is terminated. The SMPS stops to operate which causes the supply voltage of the IC \( V_{CC} \) to drop. The IC is turned off when \( V_{CC} = V_{CCoff} = 8.5V \). At this time the external soft-start capacitor \( C_{SOFTS} \) is discharged by the internal switch \( T_1 \) due to the Power Down Reset and the consumption current of the IC is reduced to maximum 55µA. The SMPS then goes into Auto Restart Mode. The \( V_{CC} \) increases again by charging the capacitor \( C_{VCC} \) through the Start-up Resistor \( R_{START-UP} \) during the IC is inactive. When it reaches the turn-on threshold \( V_{CCon} = 13.5V \), the IC is turned on again. The Error Latch is then reset by the Power Up Reset and the internal pull-up resistor \( R_{SOFTS} \) starts to charge the external Soft-Start capacitor \( C_{SOFTS} \) to start the Soft-Start Phase. During Soft-Start Phase the detection of overload and open loop by \( C_3 \) and \( G_2 \) is disabled by the Comparator \( C_4 \). The Soft-Start Phase ends with the Soft-Start voltage \( V_{SOFTS} \geq 5.3V \). If the overload or open loop failure is not removed after the Soft-Start Phase, the Error Latch is activated and the SMPS goes into Auto Restart Mode again.

13. Overvoltage due to open loop with no load

Fig.20 shows the Auto Restart Mode for open loop and no load condition. In case of this failure mode the SMPS output voltage as well as the \( V_{CC} \) increases. Additional comparators \( C_1, C_2 \) and the AND-gate \( G_1 \) are implemented to detect this failure mode (see Fig.21).
The overvoltage detection is provided by Comparator C1 only when the Soft-Start voltage $V_{SOFTS}$ is below the threshold of the Comparator C2 at 4.0V and the voltage at pin FB is above 4.8V. During this overvoltage detection phase Comparator C1 can set the Error Latch and terminates the Burst Phase earlier during Auto Restart Mode when $V_{CC}$ exceeds 16.5V. Once the Soft-Start phase is over, which means that the $V_{SOFTS}$ is above 4.0V, the overvoltage detection by C1 is disabled. This will enable the $V_{CC}$ to vary in the range of 8.5V to 21V caused by output load changes at normal operating mode.

14. 30W Demo Power Supply Board

Fig.22 shows a very simple and low cost 30W switching power supply circuitry utilizing the ICE2B265P. It is designed for used as the power supply of a Digital Photo Printer.

The specification of the circuits:

**Input voltage range**
85 – 265 VAC 50/60Hz

**Output**
18V/1.67A

**Maximum output power**
$P_{OMAX} = 30W$

**Input power at standby mode**
$P_{IN} \leq 0.5W$ at $P_{O} = 0W$ and $V_{IN} = 240Vac$

**Efficiency**
$\eta \geq 80\%$

Fig.22. 30W SMPS Demoboard using CoolSET ICE2B265

011005 - M.K.Jeoh
15. Design of the Power Supply

15.1. Determine input capacitor $C_3$ and minimum DC input voltage $V_{1\text{MIN}}$

To choose the value of the input capacitor $C_5$, the following rule of thumb is applied:

$C_5 = 2 \text{ to } 3 \mu F \text{ per W for } 100/115V_{AC}$ or universal input.

$C_5 = 1\mu F \text{ per Watt for } 230V_{AC}$.

$C_5 = 68\mu F$ is selected for this design. The minimum DC input voltage $V_{1\text{MIN}}$ (see Fig. 24) at the lowest line voltage of 85V is a very important parameter for the calculation of the transformer. It can be obtained with good approximation by the following equations:

$$V_{1\text{MIN}} = \sqrt{V_{ACMIN,PK}^2 - \frac{2 \times W_{\text{IN}}}{C_5}}$$  \hspace{1cm} (5)

$V_{ACMIN,PK}$ is the minimum peak input voltage, whereas $W_{\text{IN}}$ is the energy which is discharged out of $C_5$.

$$V_{ACMIN,PK} = V_{ACMIN} \times \sqrt{2}$$  \hspace{1cm} (6)

The discharged energy $W_{\text{IN}}$ is equivalent to the required peak output power $P_{\text{OPK}}$ for the duration of the discharge time $T_L/2 - t_C$.

$$W_{\text{IN}} = \frac{P_{\text{OPK}}}{\eta} \times (\frac{T_L}{2} - t_C)$$  \hspace{1cm} (7)

Assuming that the conduction time of the bridge rectifier diodes is about 3 ms and substitute the specified values in (5), (6) and (7), we obtain:

$$V_{ACMIN,PK} = 85V \times \sqrt{2} = 120V$$  \hspace{1cm} (8)

$$W_{\text{IN}} = \frac{30W}{0.8} \times (\frac{20ms}{2} - 3ms)$$  \hspace{1cm} (9)

$$W_{\text{IN}} = 0.26Ws$$

$$V_{\text{MIN}} = \sqrt{(120V)^2 - \frac{2 \times 0.26Ws}{68\mu F}}$$  \hspace{1cm} (10)

Taking the voltage drop at the bridge rectifier into consideration, the $V_{1\text{MIN}}$ should then be:

$$V_{1\text{MIN}} = 80V.$$  \hspace{1cm}

15.2 Transformer Calculation

15.2.1. Maximum Duty Cycle

The transformer is designed so that the SMPS is operated in discontinuous current mode for the whole operating range.

The maximum duty cycle $d_{\text{MAX}}$ at minimum input voltage $V_{1\text{MIN}}$ is chosen as

$$d_{\text{MAX}} = 0.5$$  \hspace{1cm} (11)

15.2.2 Reflected Output Voltage

The reflected output voltage $V_R$ is the reflected value of the secondary voltage across the primary winding. It can be obtained by the equation

$$V_R = \frac{d_{\text{MAX}}}{1 - d_{\text{MAX}}} \times (V_{\text{MIN}} - V_{DS})$$  \hspace{1cm} (12)

The Drain-Source voltage $V_{DS}$ of the internal CoolMOS is negligible due to the smaller $R_{DSON}$. $V_R$ is then:

$$V_R = \frac{0.5}{1 - 0.5} \times 80V = 80V$$  \hspace{1cm} (13)
15.2.3 Maximum Primary Peak and RMS Current

The maximum primary peak current $I_{PKMAX}$ is proportional to the maximum output power. It can be derived as follow:

$$I_{PKMAX} = \frac{2 \times P_{OMAX}}{\eta \times V_{MIN} \times d_{MAX}}$$  \hfill (14)

Substitute the known values of $P_{OMAX}$, $V_{MIN}$, $d_{MAX}$ and the efficiency $\eta$ into (14), $I_{PK}$ becomes:

$$I_{PKMAX} = \frac{2 \times 30W}{0.8 \times 80V \times 0.5} = 1.875A$$  \hfill (15)

The maximum primary RMS current can be calculated from $I_{PKMAX}$ and $d_{MAX}$:

$$I_{RMS,MAX} = I_{PKMAX} \sqrt{\frac{d_{MAX}}{3}}$$  \hfill (16)

$$I_{RMS,MAX} = 1.875A \sqrt{\frac{0.5}{3}} = 0.77A$$  \hfill (17)

15.2.4 Primary Inductance $L_1$

Primary inductance can be determined by the energy equation of the flyback transformer defined below:

$$L_1 = \frac{2 \times P_{OMAX}}{\eta \times I_{PK,MAX}^2 \times f}$$  \hfill (18)

$f$ is the switching frequency of the SMPS which is around 67kHz.

$$L_1 = \frac{2 \times 30W}{0.8 \times 1.875^2 \times 67kHz} = 320\mu H$$  \hfill (19)

15.2.5 Number of Primary turns

For this design, core size of EF25 is recommended due to its low cost and easy availability. For 67kHz operation, Epcos N67 material is a good choice.

In the discontinuous current mode operation, at switching frequency of 67kHz, the maximum flux density in the core $B_{MAX}$ is usually limited by the core loss. To keep the loss in the core at acceptable level (see Epcos datasheet, N67 Core loss vs frequency), $B_{MAX} = 0.2T$ is chosen for the calculation of the number of primary turns $N_1$.

$$N_1 = \frac{L_1 \times I_{PK,MAX}}{B_{MAX} \times A_{MIN}}$$  \hfill (20)

$A_{MIN}$ is the minimum cross sectional area of the core. For EF25, $A_{MIN} = 51.5mm^2$.

$$N_1 = \frac{320 \times 2}{0.2 \times 51.5} = 60$$  \hfill (21)

The required core gap $L_{GAP}$ to achieve the primary inductance $L_1$ with the number of primary turns $N_1$ can be calculated by using the equation given in Epcos data book for “Ferrites and Accessories”

$$L_{GAP} = \left(\frac{L_1}{N_1^2 \times K_1}\right)^{K_2}$$  \hfill (22)

$K_1$ and $K_2$ are the core-specific constants. For EF25, $K_1=90$, $K_2=-0.731$ are specified in the datasheet. In the calculation $L_1/N_1^2$ has to be in the dimension of nH. The needed core air gap is then

$$L_{GAP} = \left(\frac{320 \times 10^3}{60^2 \times 90}\right)^{-0.731} mm$$  \hfill (23)

$$L_{GAP} = 1.02mm$$

15.2.6 Number of Secondary Turn

The number of turn for the secondary output can be derived from the reflected output voltage $V_R$ in (13) and the number of primary turns $N_1$. During the flyback time all windings will have the same volt per turn $V_T$:

$$V_T = \frac{V_R}{N_1} = \frac{80V}{60 \text{ turns}} = 1.33 \frac{V}{\text{turn}}$$  \hfill (24)

The number of turns $N_{O1}$ for 18V-output $V_{O1}$ is then:

$$N_{O1} = \frac{V_{O1} + V_D}{V_T}$$  \hfill (25)
$V_D$ is the output diode forward voltage drop, which is typically about 1V.

$$N_{D1} = \frac{18 + 1}{1.33} = 14 \quad (26)$$

The bias voltage for the $V_{CC}$ should be around 15V. The number of turn for the bias winding is then:

$$N_{BIAS} = \frac{V_{BIAS} + V_D}{V_T} = \frac{16}{1.33} = 12 \quad (27)$$

### 15.2.7 Output Rectifier Diodes

To select the proper output rectifier diode, the maximum peak inverse voltage across the diode $V_{D1,PK}$ has to be defined. $V_{D1,PK}$ can be obtained by the equation defined below:

$$V_{D1,PK} = V_{D1} + \left( \frac{N_{D1}}{N_1} \times V_{IMAX} \right) \quad (28)$$

whereas $V_{IMAX}$ is the maximum DC input voltage. The calculation result is:

$$V_{D1,PK} = 18V + \left( \frac{14}{60} \times 375V \right) = 105.5V$$

The reverse voltage rating of the selected diode $V_{DR}$ should be greater than 1.25x $V_{Dpk}$ and the rated DC current has to be at least 3 times the maximum output current. MUR520 is chosen for used in this design.

### 15.2.8 Maximum Secondary Peak and RMS Current

The maximum secondary peak and RMS currents are proportional to the maximum DC output current as follows:

$$I_{OPK,MAX} = \frac{2I_{OMAX}}{1-d_{MAX}} \quad (29)$$

$$I_{ORMS,MAX} = I_{OPK,MAX} \times \sqrt{\frac{1-d_{MAX}}{3}} \quad (30)$$

$I_{OMAX}$ is the maximum DC output current, $I_{OPK,MAX}$ is the maximum peak output current and $I_{ORMS,MAX}$ is the maximum RMS output current. The results of the calculation is listed in Table 1.

<table>
<thead>
<tr>
<th>Secondary Output</th>
<th>Max. Peak Current</th>
<th>Max. RMS Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>18V/1.67A</td>
<td>$I_{OPK,MAX}$ = 6.68A</td>
<td>$I_{ORMS,MAX}$ = 2.73A</td>
</tr>
</tbody>
</table>

Table 1. Max. Peak and RMS Output Current

### 15.2.9. Output Capacitors

Output capacitor selection is dominated by the $R_{ESR}$ (equivalent series resistance) and the ripple current rating of the capacitor. The ripple current, which flows through the output capacitor, can be calculated as follows:

$$I_{OL,RIPE} = \sqrt{I_{ORMS,MAX}^2 - I_{OMAX}^2} \quad (31)$$

The ripple current in the output capacitor of the 18V/1.67A will then be:

$$I_{OL,RIPE} = \sqrt{2.73^2 - 1.67^2} = 2.16A$$

The Epcos datasheet of her B41858-series aluminum electrolytic capacitor shows that the rms current rating of a 1000µF/25V capacitor at 100kHz switching frequency and 105°C ambient is 1.69A. 2 pieces of this capacitors (Fig.22) have to be used to accommodate the required ripple current of $V_{OL}$. The $R_{ESR}$ of these capacitors are specified as 0.034Ω. The output ripple voltage caused by the parallel of these two $R_{ESR}$, which is $R_{ESR,TOT}$ = 0.017Ω, is then:

$$V_{OL,RP} = I_{OPK,MAX} \times R_{ESR,TOT} \quad (36)$$

This switching ripple voltage is further reduced by the additional L-C filter (L3 and C14 in Fig.22). The 220µF/25V with $R_{ESR} = 0.12\Omega$ is chosen for C14. To eliminate the pole in the control loop caused by the L1-C14 filter, L1 has to be around 1.5µH. With this L1-C14 values combination, $V_{OL,RP}$ is reduced to:

$$V_{OL,RP} = 6.68A \times 0.017\Omega = 0.11V$$
The switching ripple voltage $V'_{O1,RP}$ appears at the output terminal has been attenuated to around 18mV.

### 15.3 Current Sense Resistor

The current sense resistor ($R_{14}$ in Fig.22) is defined by the maximum primary peak current and the minimum threshold voltage of the Current Limiting $V_{CSTHMIN}$.

$$R_{14} = \frac{V_{CSTHMIN}}{I_{PK,MAX}} = \frac{0.95V}{2A} = 0.45\Omega$$  \hspace{1cm} (35)

Since the maximum loss occurred in $R_{14}$ can be:

$$P_{R14MAX} = I_{RMS,MAX}^2 R_{14} = 0.765^2 \times 0.45W = 0.26W$$  \hspace{1cm} (36)

a 1W low inductance resistor is recommended.

### 15.4 Soft-start capacitor $C_7$

As mentioned in chapter 6 “Soft-Start” on page 4 and 5, the duration of the soft-start phase $T_{SOFT-START}$ has to be long enough to ensure proper start-up of the SMPS. That means $V_{O1}$ has to be at 18V before $V_{SOFTS}$ reaches 5.3V (see Fig.11 on page 5, $T_{SOFT-START} > T_{START-UP}$).

To estimate the $T_{START-UP}$, the available power during the soft-start phase, which charges the output capacitors, has to be defined. The total value of all capacitors at the output is:

$$C_{O1} = C_{12} + C_{13} + C_{14} = 2220\mu F$$  \hspace{1cm} (37)

In case of hard-start (if soft-start does not exists), the power which will charge $C'_{O1}$ is:

$$P'_{O1} = \eta \times \frac{1}{2} \times L_1 \times f \times \left( \frac{V_{CSTHMIN}}{R_{14}} \right)^2$$  \hspace{1cm} (38)

$$P'_{O1} = 0.8 \times \frac{1}{2} \times 320 \times 67 \times 10^{-3} \times \left( \frac{0.95}{0.45} \right)^2 W = 38.2W$$

Assuming that the charge-up power to the $C'_{O1}$ rises linearly during the soft-start phase, the charge power is then only half of 38.2W. $T_{START-UP}$, which is needed to raise the voltage $V_{O1}$ to 18V, can then be estimated:

$$T_{START-UP} = \frac{1}{2} \times \frac{V_{O1}^2 \times C'_{O1}}{0.5 \times P_{O1}}$$  \hspace{1cm} (39)

$$T_{START-UP} = \frac{16^2 \times 2220}{38.2} \mu s = 18.8ms$$

In the application circuit of Fig.22, the external soft-start capacitor $C_7 = 1\mu F$ is recommended. The internal soft-start resistor $R_{SOFTS} = 50k\Omega$ is specified on the datasheet of the IC. The soft-start time $T_{SOFT-START}$ can then be calculated using (3):

$$T_{SOFT-START} = 1.69 \times 50 \times 1 ms = 84.5ms$$  \hspace{1cm} (40)

In this case, $T_{SOFT-START} > T_{START-UP}$ and the start-up of the SMPS is secured.

### 15.5 Capacitor at $V_{CC}$ $C_6$

The $V_{CC}$ capacitor $C_6$ ($C_{VCC}$ in Fig.22) needs to ensure the power supply of the IC until the power can be provided by the auxiliary bias winding. Regardless the current transfer from the start-up resistor $R_1$ and the auxiliary winding during start-up time $T_{START-UP}$, the capacitance value $C_6$ can be estimated as below:

$$C_6 = \frac{I_{VCC3} \times T_{START-UP}}{V_{CCHY}}$$  \hspace{1cm} (41)

$I_{VCC3}$ is the IC supply current with active gate-drive. Its maximum value is 8mA as specified on the datasheet. $V_{CCHY} = 5V$ is the turn-on/off hysteresis of the IC supply voltage $V_{CC}$. Based on the estimated value of $T_{START-UP}$ in (39), $C_6$ should then be:

$$C_6 = \frac{8mA \times 18.8ms}{5V} = 30\mu F$$  \hspace{1cm} (42)
C6 = 47µF is selected to sustain the Vcc.

15.6 Start-up Resistor R2 and R3

The start-up resistor RSTART-UP consists of R2 and R3, which is connected in series as shown in Fig.22. By using (1) on page 2, the longest start-up delay time, which happens at the lowest line- input voltage VACMIN = 85V can be estimated:

\[
t_{\text{START-DELAY}} = \frac{C_6 V_{\text{CCON}}}{V_{\text{ACMIN}} V_{\text{FB}}^{1/2}} - t_{\text{IC1}} \tag{43}
\]

\[
t_{\text{START-DELAY}} = \frac{47\mu\text{F} \times 13.5\text{V}}{85\text{V}^{1/2}} = 8.7\text{s}
\]

In worst case, the IC is turned on only in 8.7s after the SMPS is plugged to the main line. The maximum loss occurs in RSTART-UP is roughly:

\[
P_{\text{ST-LOSS}} = \frac{V_{\text{ACMAX}} V_{\text{FB}}^{1/2}}{2 \times 470k\Omega} = 0.15W \tag{44}
\]

15.6 Control Loop Design

15.6.1 Power Stage Transfer Function

Fig. 24 shows the essential elements of the control loop.

Following equations are used to define the DC or low frequency gain of the feedback loop of the power stage (from the control voltage \( v_{\text{FB}} \) at the feedback-input pin2 to the output voltage node \( v_{\text{O}} \)):

\[
P_O = \frac{1}{2} L_1 f \times I_1 \times \eta \tag{45}
\]

\[
P_O = \frac{v_{\text{O}}}{R_O} \tag{46}
\]

\[
I_1 = \frac{V_{\text{CSTH}}}{V_{\text{FB}} R_{14} \times A_v} \tag{47}
\]

Substitute \( P_O \) and \( I_1 \) in (45) with (46) and (47) and rearrange the equation in term of \( v_{\text{O}}/v_{\text{FB}} \), we obtain

\[
G_{\text{PS}} = \frac{v_{\text{O}}}{V_{\text{FB}}} = \frac{V_{\text{CSTH}}}{R_{14} \times A_v} \frac{\eta L_1 R_{\text{O}} f}{2} \tag{48}
\]

\( A_v \) is the PWM-OP gain, which is equal to 3.65 as specified in the datasheet of ICE2B265. Equation (48) shows that the DC or low frequency gain \( G_{\text{PS}} \) of the power stage is proportional to the square root of the output load \( R_O \) and independent of the input voltage variation due to the current mode control. For \( R_{\text{OMIN}} = 10.8\Omega \) (at \( P_{\text{OMAX}} = 30W \)), the minimum gain is

\[
G_{\text{PS,MIN}} = 0.95 \times \frac{0.45 \times 3.65 \times \sqrt{0.8 \times 320 \times 10.8 \times 67 \times 10^{-3}}}{2} \tag{49}
\]

\( G_{\text{PS,MIN}} = 14.9 \text{ dB}. \)

In case of \( P_{\text{OMIN}} = 0.5W \), the output load will be \( R_{\text{OMAX}} = 648\Omega \), the maximum power stage gain will then be

\[
G_{\text{PS,MAX}} = 0.95 \times \frac{0.45 \times 3.65 \times \sqrt{0.8 \times 320 \times 648 \times 67 \times 10^{-3}}}{2} \tag{50}
\]

\( G_{\text{PS,MAX}} = 43 \text{ dB}. \)

\( G_{\text{PS,MAX}} = 32.7 \text{ dB}. \)

The small signal transfer function of the power stage with its pole and ESR-zero is shown below:

\[
G_{\text{PS}}(s) = \frac{1 + s R_{\text{ESR}} C_{\text{O}}}{1 + s R_{\text{O}} C_{\text{O}} / 2} \tag{51}
\]
Co consists of \( C_{12} \) and \( C_{13} \) (see Fig.22) with the total value of 2000 \( \mu \)F and \( R_{ESR} \) is the ESR values (see page 12) of both capacitor in parallel, Thus \( R_{ESR} = 0.017 \Omega \). The poles and zero at minimum and at maximum power are listed in Table 2 below:

<table>
<thead>
<tr>
<th>Output Power</th>
<th>Poles ( F_p = 1/\pi \pi \pi \pi R_Co )</th>
<th>Zeros ( F_z = 1/2\pi \pi \pi \pi R_{ESR}C_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{O_{MAX}} = 30W )</td>
<td>( F_{PH} = 14.7Hz )</td>
<td>( F_z = 4.68kHz )</td>
</tr>
<tr>
<td>( R_o = 10.8\Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( P_{O_{MIN}} = 0.5W )</td>
<td>( F_{PL} = 0.24Hz )</td>
<td>( F_z = 4.68kHz )</td>
</tr>
<tr>
<td>( R_o = 648\Omega )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Poles and zero

The transfer function of the output filter \( L_1-C_{14} \) can be expressed as follows:

\[
G_{LC} = \frac{1}{1 + sC_{14}R_{14ESR}} \left( \frac{1}{1 + sL_1 - \frac{1}{\omega^2C_{14}R_{14ESR}}} \right) \tag{52}
\]

\( C_{14} \) and \( L_1 \) have to be selected so that the pole of the filter \( F_{PLC} \) is located far away from the crossover frequency \( F_{CO} \) to avoid its influence in the control loop. The control loop bandwidth can only be kept high with high \( F_{PLC} \), which is desirable. The L-C filter has a –2 gain slope with rapid changes of phase shift, which could induce instability in the control loop. To prevent it, the pole has to be compensated by the zero as mentioned on page 12. Based on this consideration, Epcos Alcapacitor B41858-series of \( C_{14} = 220\mu F/35V \) with \( R_{14ESR} = 0.084\Omega \) is selected. The zero frequency is then at:

\[
F_{Z_{14}} = \frac{1}{2\pi R_{14ESR}C_{14}} = 8.6kHz \tag{53}
\]

Set the pole equal to zero and solve for the inductance \( L_1 \):

\[
L_1 = 1.55\mu H
\]

With this combination of \( L_1 \) and \( C_{14} \), the influence of the filter on the control loop can thus be neglected; the small signal transfer function of the power stage is then dominated only by (51).

The open loop gain and phase responses of the transfer function for the minimum and maximum output power are shown in Fig.26 and in Fig.27.

To close the loop, the feedback loop circuitry as shown in Fig.25 is added. It consists of a compensation network (TL431, \( R_6 - R_{11} \), \( C_9 \) and \( C_{10} \)) and the optocoupler IC2.

The transfer function of the feedback loop is

\[
G_{FB}(s) = \frac{V_{FB}(s)}{V_O(s)} = \frac{G_C R_{FB}}{R_6} \frac{1 - s(C_9 + C_{10})R_8}{sC_9R_6(1 - sC_9R_8)} \tag{55}
\]

\( G_C \) is the current transfer ratio of the optocoupler. For SFH617-3, \( G_C = 100\% \). The internal pull-up resistor at FB (pin2) is specified as \( R_{FB} = 3.7k\Omega \).

\[
\left| G_{PSH}(s) \right| = G_{PSMIN} \times \frac{1 + \frac{F_C}{F_{PH}}}{1 + \frac{F_C}{F_{PH}}^2} \tag{56}
\]
\[ |G_{PSH}(s)| = \frac{5.2 \times \left( 1 + \frac{3kHz}{4.6kHz} \right)^2}{\left( 1 + \frac{3kHz}{14.7Hz} \right)^2} = 0.03 \]

\[ G_{PSH}(f_C) = -30.4\text{dB} \]

The feedback loop gain with TL431 has to be 30.4dB at \( f_C \) and must have zero slope response. For further calculation, \( R_9 \) has to be defined first. \( R_{11} \) determines the bias current of the resistor divider \( R_9 - R_{11} \). If \( R_{11} = 3.9k\Omega \) is selected, \( R_9 \) can be calculated by

\[ R_9 = R_{11} \left( \frac{V_0}{V_{REF}} - 1 \right) \] (57)

\[ R_9 = 3.9k\Omega \times \left( \frac{18}{2.5} - 1 \right) = 24k\Omega. \]

\( V_{REF} \) is the reference voltage of TL431. To calculate the feedback loop gain at \( f_C \), (55) can be simplified as below:

\[ |G_{FB}(f_C)| = \frac{G_C R_{FB} R_8}{R_6 R_9} \] (58)

Since \( |G_{FB}(f_C)| = 30.4\text{dB} \),

\[ R_8 = R_9 \times 10^{-20} \times \frac{R_9}{G_C R_{FB}} = 200k\Omega \] (59)

\( C_9 \) is obtained by placing the pole at \( F_{PFB} = 2 \times f_C \).

\[ C_9 = \frac{1}{2 \pi R_9 F_{PFB}} = 133pF \] (60)

In order to have sufficient phase margin, especially at light load, the zero is placed at \( F_{ZFB} = 20Hz \). The value of \( C_{10} \) is then

\[ C_{10} = \frac{1}{2 \pi R_9 F_{ZFB}} - C_9 = 39nH \] (61)

Based on above calculation, the values of the feedback network components are selected as follows:

\[ C_9 = 120pF \]

\[ C_{10} = 47nF \]

\[ F_{ZFB} = 15.4Hz, \ F_{PFB} = 6kHz \]

Fig.26 and Fig.28 also illustrate the responses of the feedback loop circuitry and the total open loop, whereas Fig.27 and Fig.29 show its respective phase responses.

**16. Summary**

This application note introduced briefly the features and functions of the CoolSET™, the new integrated product that includes PWM control IC and the CoolMOS™, the new generation Power MOSFET. A low cost 30W SMPS demo-board circuit is developed and its operation is analyzed in detail. The detail explanation of the board and the experiment results are described in the application note “30W Off-line SMPS Demoboard using CoolSET™ ICE2B265”.

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References


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