IPextreme

Product Brief

C166S V1

Licensable 16Bit Microcontroller Core

Infineon technologies

The ***Infineon C166S*** synthesizable processor core is derived from the successful C166 microcontroller family and is fully instruction set compatible to run all your legacy code. It has been designed to meet the high performance requirements of real-time embedded control applications. The architecture of the C166S combines the benefits of both RISC and CISC (Reduced and Complex Instruction Set Computing). This well-balanced approach delivers the memory saving code density and fast context switching of CISC with the easy RISC instruction decode that enables fast clocking. The sum of the features results in a high performance microcontroller, which is the right choice not only for today's applications, but also for future engineering challenges.

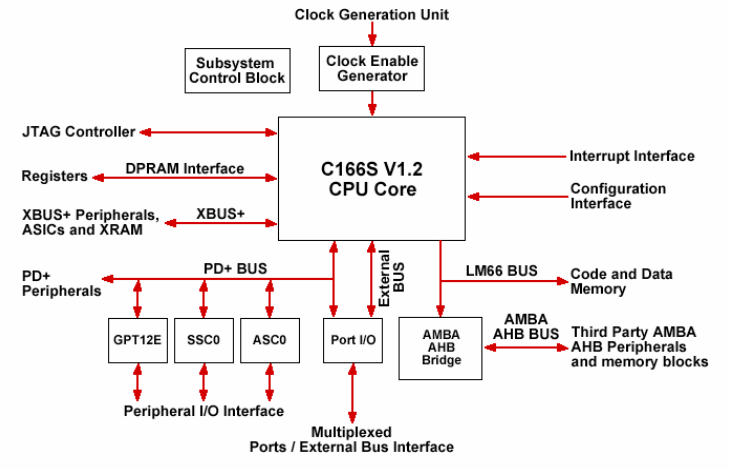
The architecture of this processor family has been optimized for high instruction throughput and minimum response time to external interrupt stimuli. Intelligent peripheral subsystems have been integrated to reduce the need for CPU (Central Processing Unit) intervention, which also saves power and frees bandwidth by minimizing communication via the external bus interface. The flexibility of this architecture allows the C166S to serve the diverse and varying needs of different application areas such as automotive, industrial control, or data communications.

New enhancements include an improved bus structure and an optional MAC unit, to create a unique combination of real time control and DSP capability in one core. Advanced on-chip debug and emulation are also supported for easy integration into SoC designs.

The C166S V1 is a complete configurable subsystem, including a rich set of standard peripherals such as general purpose timers, synchronous and asynchronous serial ports, and an AMBA AHB interface. This enables easy integration into a wider platform, saving engineering effort and time to market. The C166S V1 is delivered in IPextreme's innovative XPack format (see inset other side) to maximize ease of use and value for customers.

History of the C166 – A Proven Design

Since 1990, more than 30 microcontroller chips using the C166 architecture have been designed into thousands of applications. The architecture and its tools have undergone many years of testing and use, making it one of the most robust micro-controllers on the market. Overall, the architecture has a 17% market share in the worldwide 16-bit MCU market. In the automotive market, about 200 million units have been sold, mostly in power trains where reliability and quality are key. In the wireless market, about 300 million cell phones incorporating the C166S architecture have been sold and it has also been deployed recently in leading MP3 players.



IPextreme C166s V1 Subsystem Block Diagram

C166S V1 Features

- C166s v.1.2 CPU
- AMBA AHB Bus for easy connection of industry standard peripherals
- Synchronous and Asynchronous serial communication interfaces
- General Purpose Timer

C166S V1 Core Units & Interfaces

Four-Stage Pipelined CPU

- 100MHz clock speed in 0.18µm CMOS (cycle time =20ns)
- C166 Instruction-set compatible
- Additional DSP instructions (with optional Multiplier-Accumulator Controller) Unit)
- Most instructions execute in 2 cycles
- Multiple register banks
- Single cycle context switching
- 16 * 16 multiply in 1 cycle with MAC unit or 5 cycles without MAC
- 32/16 division in 10 cycles
- On-Chip Debugging System (OCDS)

Multiple High-Bandwidth Internal Data Bus System

- Improved X Bus (XBUS+) & PD Bus (PD+)
- Local Memory Bus (LM66)
- Dual port RAM interface (DPRAM)

External Bus Controller (EBC)

- 8bit/16bit multi or de-multiplexed modes
- Multiplexed Port / External Bus Interface

Interrupt Controller

- Up to 112 interrupt nodes with separate vectors
- 16-level / 8 group-level priority system

Peripheral Event Controller (PEC)

- Interrupt-driven single cycle data transfer
- Counter options, channel linking

Core Control Block (CCB)

- Power & clock management for CPU & peripherals
- Power-on reset control
- Programmable watchdog

Debug Interface for Advanced Emulation

- Hardware, software & external breakpoints
- Access to internal registers & memory through JTAG port

Testability

- Full scan production test with >99% coverage

— C166S V1 XPack —

XPack is an innovative IP packaging technology from IPextreme that enables customers to quickly and easily integrate IP into their designs. This lightweight IP packaging technology is based on the familiar metaphor of a datasheet which contains all the descriptions and diagrams one would expect from a datasheet, but in reality, it is the cockpit by which users interact with the IP. Customers change configuration parameters or modify timing information by updating fields on the interactive datasheet, which automatically generates code reflecting those changes.

XPack is the result of over a decade of experience delivering IP in the manner most readily usable by customers and IPextreme packages all its products using this technology.

XPack Features

- Automatic configuration of source code based on user selectable options for both hardware and software parameters
- Automatic generation of the module instantiation RTL interface code that describes the connection between the configured core and the SoC design
- Generation of synthesis scripts and constraints for major EDA synthesis tools.

C166S V1 XPack Contents

- RTL source code (Verilog and VHDL)
- Integration test bench to verify top level connectivity
- Self-checking integration tests
- Extensive user documentation

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About IPextreme Inc.

IPextreme helps designers reliably complete ever more complex integrated circuits by providing on-chip subsystems combining hardware and software in a complete, easy-to-use, EDA-tool-neutral package. We consolidate proven designs through a collaborative formal development process focused on rapidly delivering a high quality result. For almost a decade our team has been helping large semiconductor companies to package, commercialize and support their intellectual property (IP), which forms the basis of our product portfolio. IPextreme has offices in Campbell, California and Munich, Germany. www.ip-extreme.com.

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