C11N

130 nm CMOS Platform Technology

www.infineon.com

Never stop thinking

C11N Technology at a glance ...

Infineon Stands for Customer Orientation
Target Markets & Applications / Core Competencies

Automotive, Industrial & Multimarket

Car Electronics: power train, safety management, body & convenience, infotainment,
Power control: distributed power generation, automation / motor control, transportation, power supplies, medical, building control,
Chipcard & Security: communications, payment, identification, entertainment

Communication Solutions

Wireless communications: mobile phones, cellular base stations, cordless telephones, RF technology for short, medium and long-range distances, TV receivers, navigation,
Wireline communications: Voice and broadband data communications, integrated voice and data communications, wireless infrastructure, home networks

Analog/Mixed Signal

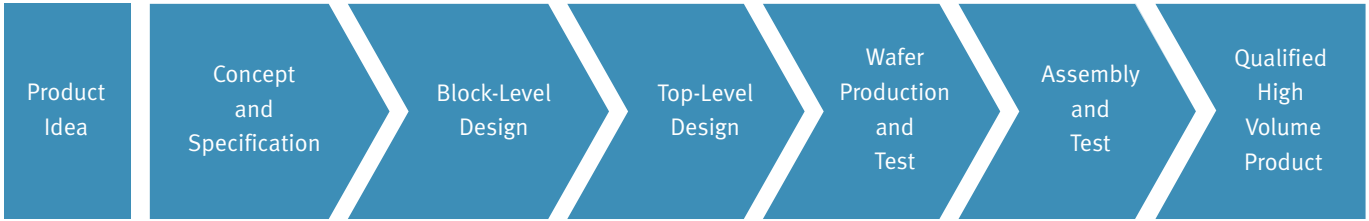
RF

Power

Embedded Control

Customers

Complete Offering over the Value Chain



Support & Services from Infineon Technologies

- Process design kit (PDK)
- Concept reviews
- Design and layout reviews
- Concept and specification
- Design and layout services
- IP blocks
- Test development
- Manufacturing services
- Logistics
- Quality
- Assembly and test

Design System, Tools, Methods, Environment

Fully integrated design system

- "Exportable" + flexible design infrastructure
- Leading RF design and highly optimized low power methodology
- Fast cycle time from RTL to chip
- Re-usable IP macros leveraging IFX' ASSP roadmaps
- Netlist and RTL sign-off procedures with tight parameter bands and small margins for most efficient designs
- DFM - Design for Manufacturability

Intimate technology know-how for full exploitation of internal and 3rd party manufacturing for first-time right designs

- Methodology to assess cost, performance, leakage/power of target manufacturing platform and site
  - Simulation environment for frontend (device) and backend technology
  - Testchip architectures for accurate model-hardware correlation
- Area optimized standard cell libraries and high performance I/O
- Highly configurable memories, optimized for lowest standby power, small area and high yield
- Digital and analog circuit and system know-how for custom solutions

- 130 nm (0.13 µm) CMOS Technology for Logic, SRAM and Analog/Mixed Signal Applications
  – L_{Drawn} = 120 nm → L_{Poly} = 92 nm
- High density, high performance, low power technology
- Supply voltage of 1.2 V – 1.5 V for standard digital operation
- Analog device voltage of 2.5 V
- I/O voltages of 2.5 V/3.3 V
- eSRAM (6T: 2.28 µm^2)
- Temperature range: -40˚C to +125˚C for 10 years operational lifetime
- Average gate density: 204 K/mm^2
- Available in multiple manufacturing locations (second source)
- Derivative technologies for integration of embedded NVM and RF are available

Standard Features

- Non-epi substrate
- Shallow-Trench Isolation (STI)
- Dual gate-oxide (2.2 nm & 5.2 nm)
- Salicide technology ($CoSi_2$)
- 4 layer thin wire metal (Cu)
- Last metal aluminum (routing possible)
- MOS Devices (N & P)
  - Regular V_T (Base)
  - High V_T (Low Power)
  - Low V_T (High Performance)
  - Thick oxide for 2.5 V analog and 2.5/3.3 V I/Os
- PNP bipolar transistor
- Diodes
- Mixed V_T designs are supported

Options

- Embedded memory
  - SRAM (SP & DP)
  - ROM (via & diffusion programmable)
- 1 - 2 layer fat wire metal (Cu)
- Fuses: laser (metal) or poly eFuse
- High Performance option by shorter gate dimensions
- High Q Metal-Insulator-Metal (MIM) capacitor
- Salicide-blocked devices
- Passive devices
  - Low & high ohmic resistors
  - Metal & gate oxide capacitors
  - Low-cost inductors

Device Specifications

		HVT	RVT	LVT	Analog	Analog & I/O
V_{DD}	[V]	1.5/1.2			2.5	3.3
T_{OX}	[nm]	2.2			5.2	
L_{Gate}	[nm]	92			297 NFET 251 PFET	
V_T N V_T P	[mV]	490/500 420/430	355/370 300/310	280/295 240/250	385 360	370 345
$I_{d\text{-}sat}$ N $I_{d\text{-}sat}$ P	[µA/µm]	600/375 255/145	730/500 335/210	795/560 370/240	513 238	751 384
$I_{d\text{-}leak}$ $L_{nom\ @\ 300\ K}$	[nA/µm]	0.015/0.01	0.3/0.2	2/1.2	0.02	0.025
t_{RO}	[ps]	20.5/27	14.5/18.5	na/15.5		

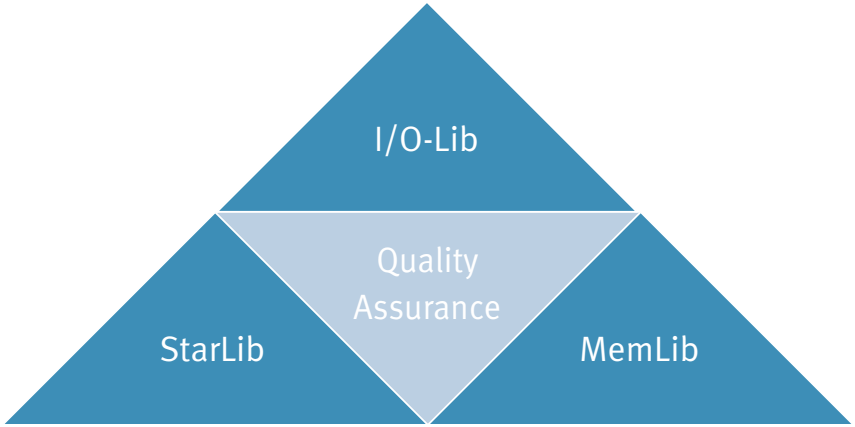
		MIMcap
C_{area} Q @ 2.4 GHz	[fF/µm²]	1.04 > 100

Key Design Rules

	Min. Width [nm]	Min. Space [nm]
N-Well	680	700
Diffusion	160	180
Polysilicon	120	200
Salicide Blocking	400	400
Contact	160 (fixed)	240
Metal 1	160	160
Via 1 – 3	200 (fixed)	200
Via 4 – 5	400 (fixed)	400
Metal 2 – 4	200	200
Metal 5 – 6	400	400

Library Components at a Glance

Library Components ... the perfect Building Blocks for Market Success



Standard Cell Library

World Class I/O-Interfaces for Market Success

Features and Benefits

- Targeted for high performance (low V_t), low power (high V_t) and standard (regular V_t) process
- Fully adapted to InWay design flow, widely automated by in-house Characterization and Modeling Tools
- Performance optimized, fully exploiting process
- Optimized for synthesis (rich and complex cell set, special ultra low power register set, scan version for every FF)
- Accurate front end deep-sub-micron modeling for 100% first silicon success
- Optimized for place & route (metal1 only, except few 9t cells)

Key Parameters		
Number of cells	620	
Number of tracks	10	
Number of drive strengths	4 ... 11	
NAND gate density [k/mm²]	156	
Average gate density [k/mm²]	204 (tr. count m.)	
Supply Voltage [V]	1.5	1.2
High Speed	**Low V_t**	
typ. NAND2P delay, FO = 2 [ps]	29	35
typ. power NAND2P, C_L = 0 [nW/MHz]	13	8
Leakage current (@ 85°C/I_{min}) [nA/µm]		< 100
Low Speed	**High V_t**	
typ. NAND2P delay, FO = 2 [ps]	41	56
typ. power NAND2P, C_L = 0 [nW/MHz]	12	8
Leakage current (@ 85°C/I_{min}) [nA/µm]		< 2
Standard	**Regular V_t**	
typ. NAND2P delay, FO = 2 [ps]	33	42
typ. power NAND2P, C_L = 0 [nW/MHz]	12	8
Leakage current (@ 85°C/I_{min}) [nA/µm]		< 40

RAMs and ROMs

Features and Benefits

- Available for Single Port RAMs, Dual Port RAMs, diffusion and contact programmable ROMs, V_{DD} = 1.5 V (1.2 V)
- Fully adapted to InWay design flow, comfortable WEB interface
- Support different V_ts, highly configurable, flexible aspect ratios
- Edge-sensitive synchronous interfaces
- Extremely dense (use 4 metal layers, routing over memory at metal 5 and above is possible)
- Power efficient, leakage-only static power
- Special features (e.g. bit write enable, antenna diodes, BIST)
- Scalable redundancy (High Density Fault Repair SPRAM)

Key Parameters			
MemLib	Sync. High Speed Single Port SRAM	Sync. High Density Low Power Dual Port SRAM	Sync. High Speed Diffusion ROM
Core cell size	2.28 µm²	4.36 µm²	0.25 (cont. 0.33) µm²
Max. size	512 kbit	256 kbit	2 Mbit
Max. bits/word	128 bit	128 bit	128 bit
Ex.: PVT = typ./1.5 V/27°C	4 k x 16, reg. V_t:	4 k x 16, reg. V_t:	4 k x 16, reg. V_t:
Area	0.21 mm² [1)] (normal)	0.43 mm² [1)] (wide)	0.064 mm² [1)] (normal)
Cycle time / read acc. time	1.0 ns/0.94 ns	2.54 ns/1.55 ns	1.33 ns/1.36 ns
Dyn. Power (av. read/wr.)	0.063 mW/MHz	0.096 mW/MHz	0.110 mW/MHz

1) Area without power rings

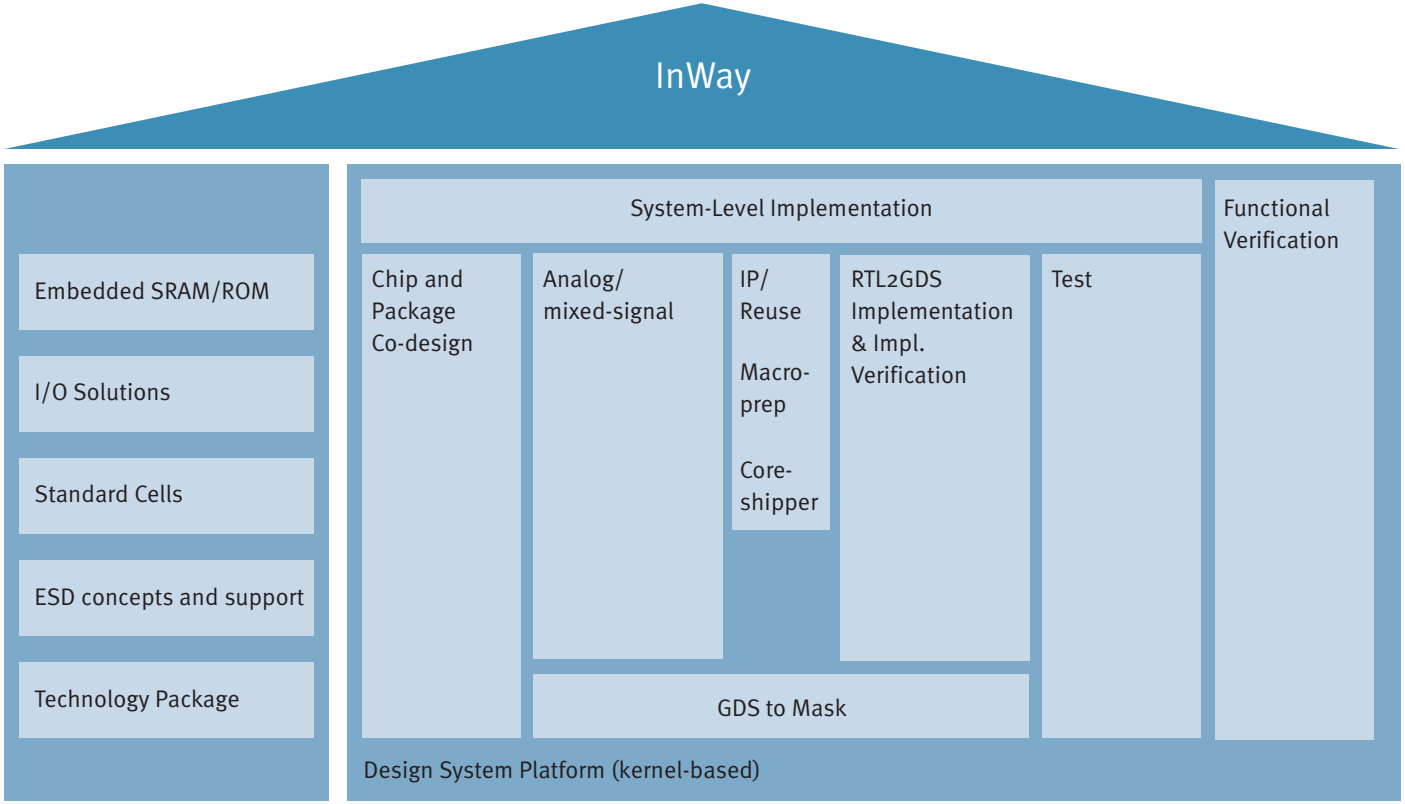
I/O Libraries

Features and Benefits

- Based on the widely automated view generation, dimensioning and verification method
- Fully adapted to InWay design flow
- Big set of standard IO cell libraries i.e. LVTTL incl. I^2C, HSTL, WS-Lib (80 µm pitch), FS-USB
- Universal low-swing MHz-oscillator and ultra low power, low voltage kHz-oscillator
- Extended range of standard I/O macros
  Project specific I/O solution on demand, e.g.
  - HDD specific IO macro ATA-100
  - USB-PHY
  - LVDS (1250 Mbit/s)
  - DDR-1
  - PCI-133
- Area efficient flip-chip concept
- Area saving separation and arrangement of probe pads and bond pads, flexible pitch 60 µm and 80 µm

Key Parameters	
Core signal voltage	1.5 V (1.2 V)
Standard bond pad pitch	60 µm (inline)
ESD hardness (HBM)	≥ 2 KV
Latchup immunity (EIA/JESD78)	100 mA
Number of metal layers	4 to 6
LVTTL	
– Standard driver strenghts	4 ... 24 mA
– Cell height (with overactive area bond pad)	138.5 µm
HSTL	
– Cell height (with overactive area bond pad)	190 µm
Low swing oscillator	
– Frequency range	4 ... 40 MHz
Ultra low power, low voltage oscillator	
– Frequency	32 kHz
– Voltage range	1.0 ... 3.3 V
– Current dissipation	1.5 µA

InWay – Infineon specific Design Environment



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