Power Semiconductors

Application Note

TLE 6220 / TLE 6230 / TLE 6240 GP

Quad, Octal and 16-fold Smart Power Low-Side Switches for Automotive Engine Management/Powertrain Applications

by Claus Preuschoff

Introduction

Modern Engine Management/Powertrain Systems call for high integrated intelligent Power Semiconductors under respect of today's and tomorrow's environmental and safety regulations. The enlarging number of loads - from a few milliamperes up to 100 A - must be driven in a intelligent way in combination with a real time fault monitoring. These requirements demand that protection and fault diagnostics be present in the module to keep emission levels and maintain system reliability.

The new Siemens chip set of multiple channel low-side switches covers all these requirements by embedded protection functions and diagnostic feedback via **S**erial **P**eripheral **I**nterface (SPI) in surface-mount packaging with integrated heat slug (Power SO Package)

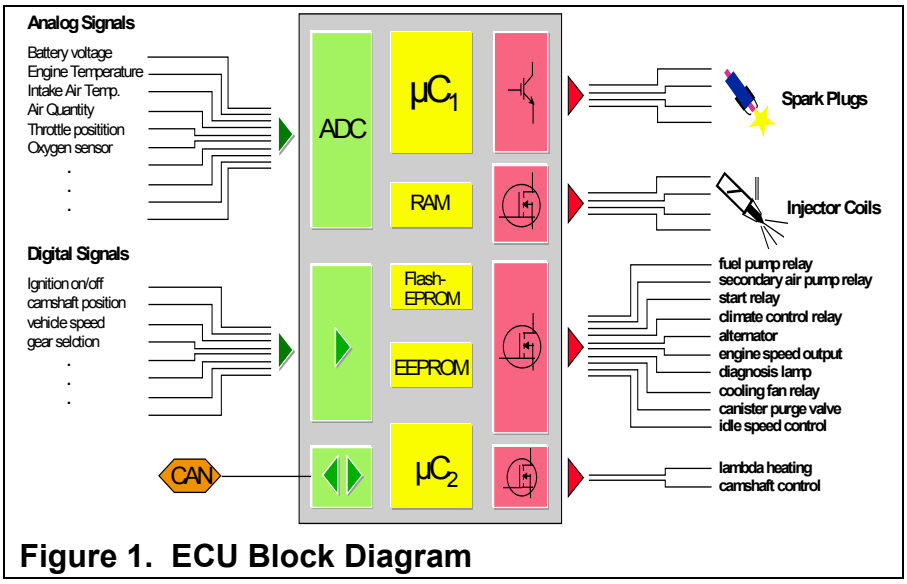


Figure 1. ECU Block Diagram

1 Overview

Modular concept
To fulfill the different platform requirements the design engineer needs a modular chip concept for ECU design in order to reduce the time to market. So the new Siemens chip set of multiple channel low-side switches follows one simple principle:

+ + + If you know one device you know all devices + + +

Coming out with a Quad-, Octal- and a 16-fold channel device with identical key features an adjustment to specific ECU needs is easily possible. The devices may be used like a construction set.

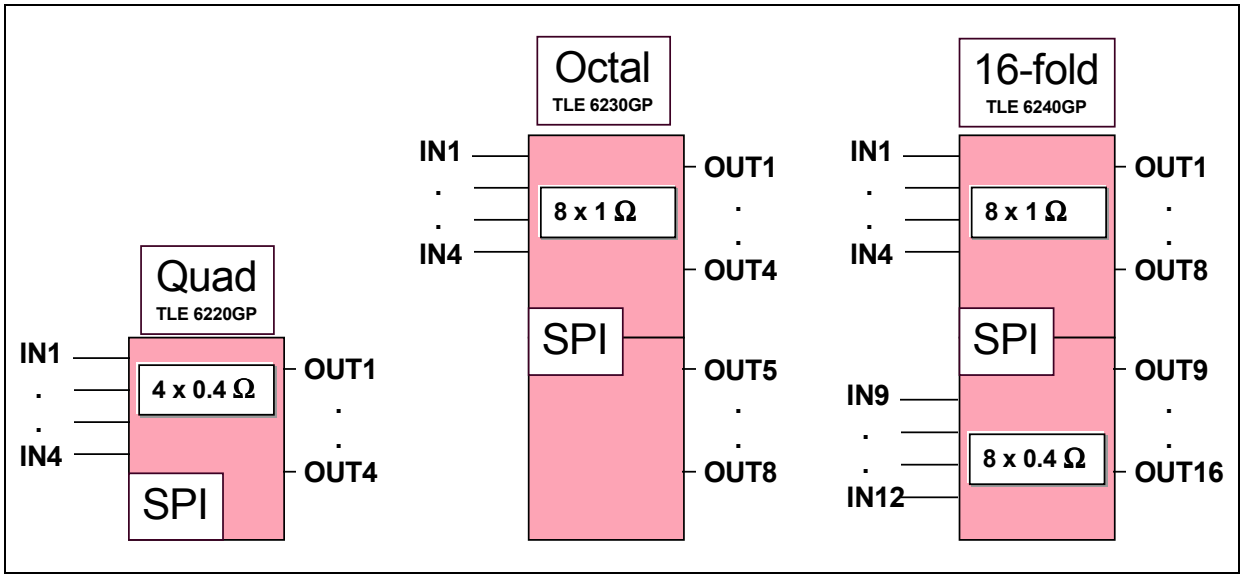
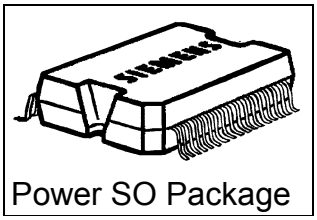
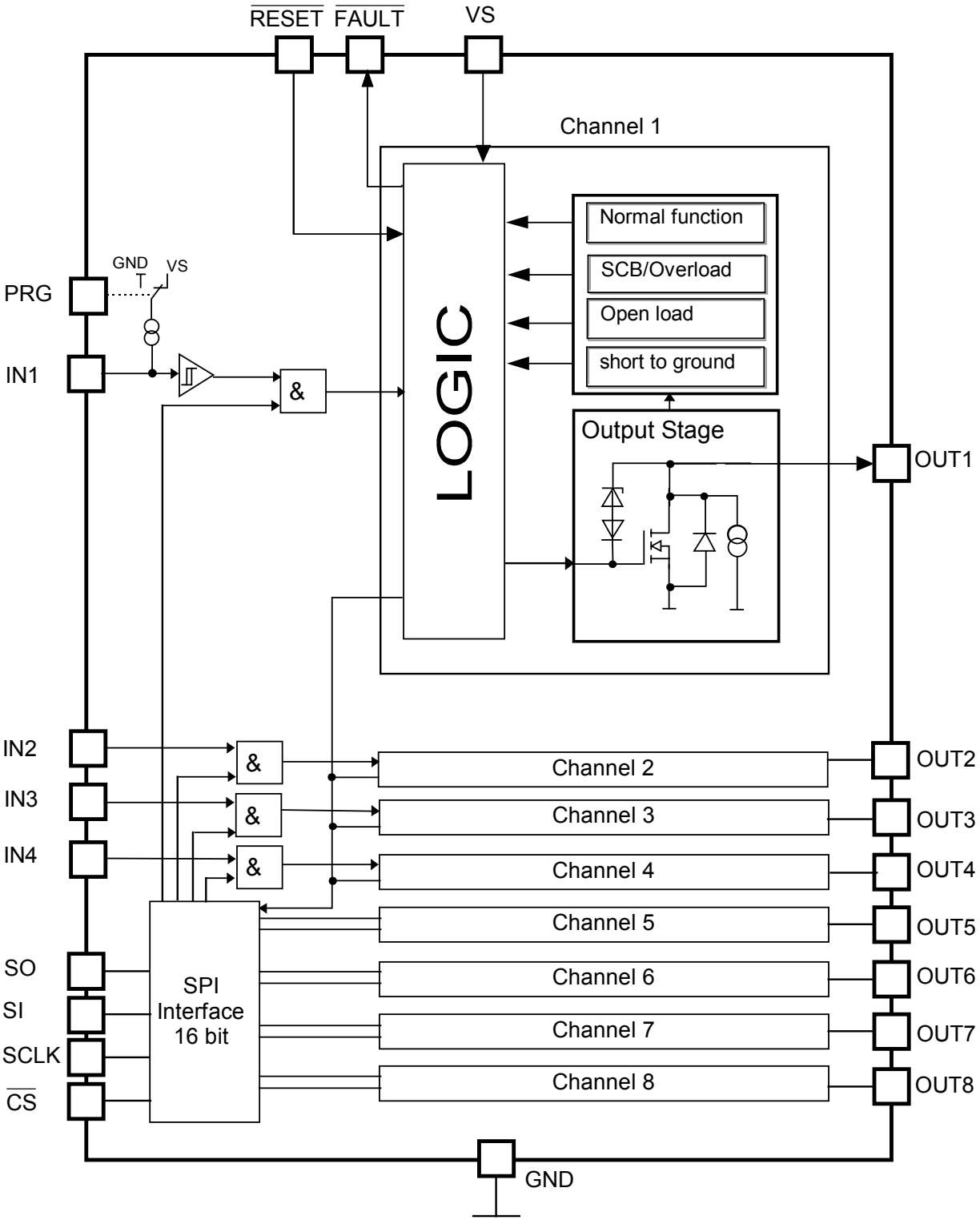


Figure 2 Modular Concept of TLE 62x0 GP Chip Set

Common Features


Power SO Package

- Short circuit protection
- Overtemperature protection (selective)
- Overvoltage protection
- Serial Interface for data input and diagnostic output (2 bit per channel according SPI protocol)
- In addition to the serial control of the outputs it is possible to control some channels direct in parallel for PWM applications (see figure 2)
- Parallel inputs high or low active programmable
- General fault flag
- Low quiescent current
- Compatible with 3,3V micro controllers
- **E**lecto**s**tatic **d**ischarge (ESD) protection



Detailed Block Diagram TLE 6230 GP

All channels can be controlled via serial interface (SPI). In addition to this serial control it is possible to control channel 1 to 4 direct in parallel with a separate input pin. The input pins are either high or low active (programmable via PRG-pin).

2 Protection Functions and Fault Detection

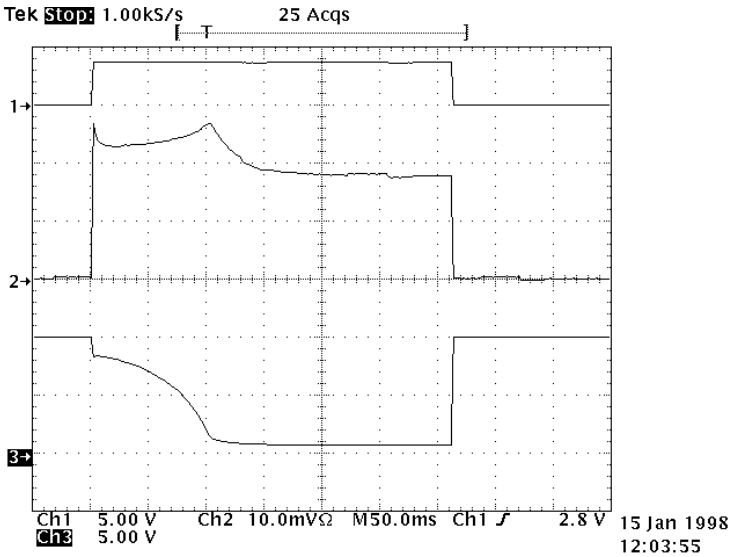
Each output is protected by embedded protection functions. Each of the output stages has its own zener clamp. This causes a overvoltage limitation at the power transistor during inductive load switch off transients. The outputs are provided with a current limitation set to minimum of 1A or 3A (TLE 6220 GP: 4 x 3A; TLE 6230 GP: 8 x 1A; TLE 6240 GP: 8 x 1A, 8 x 3A).

2.1 Overload, Short Circuit and Overtemperature Protection

A key design consideration is the device's ability to handle unsafe current levels. As with the existing HITFET®, the overload protection - which includes short circuit and overtemperature protection - acts in stages. This means that if the internal current limit $I_{D(lim)}$ is exceeded, the output stage is not switched off immediately, but the current is limited to $I_{D(lim)}$ and the corresponding bit combination (SPI register) is set (early warning).
The device thus operates in the analogue region, and the voltage between drain and source increases. This leads to a rise in the chip temperature due to the increasing power dissipation. To prevent the maximum junction temperature being exceeded, a temperature sensor of the affected channel switches off the output stage. Thus the device protects itself.

2.1.1 Driving a Lamp

For loads with capacitive behaviour, such as a lamp when being switched, the inrush current can be eight or ten times the steady state value. The TLE 62xx GP device are well suited for this applications because of its internal current limitation which increases lamp operating lifetime. Figure 3 shows the switching of a lamp with a nominal current of around 0.8 A. The ‘inrush current’ here is limited to around 1.3 A.



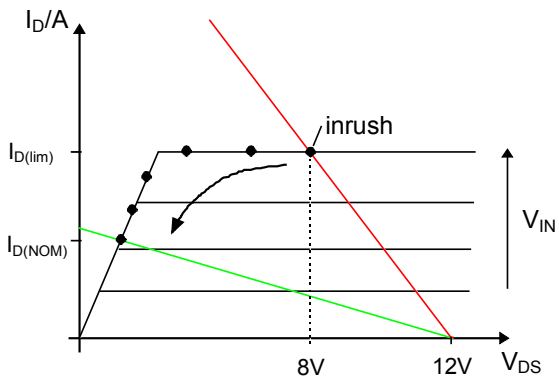


Figure 3 Switching of a Bulb

The bottom trace on the oscillogram shows the drain-source voltage during switching. Next to the oscillogram, the output characteristics are shown with the corresponding operating points during the switching operation. Initially the current is limited to $I_{D(lim)}$ for a voltage of $V_{DS} \approx 8V$ (inrush). The operating point then moves along the curve in the direction shown by the arrow, until the nominal current at $V_{DS} = I_{D(NOM)} \times R_{ON}$ is reached.

2.1.2 Short Circuit Protection

If there is a permanent short circuit and the channel is switched on, the current is only limited by the internal current limitation ($I_{D(lim)}$) of the device. This leads to an increasing chip temperature (depending on the cooling conditions). If the temperature of the chip rises to 170 °C (typ.), the device automatically switches itself off.
The device is designed as 'restart on cooling' type, i.e. the temperature needs only to fall 10 K (typ.) in order for the device to switch back on again. Each channel has its own temperature sensor, i.e. the others continue their operation.

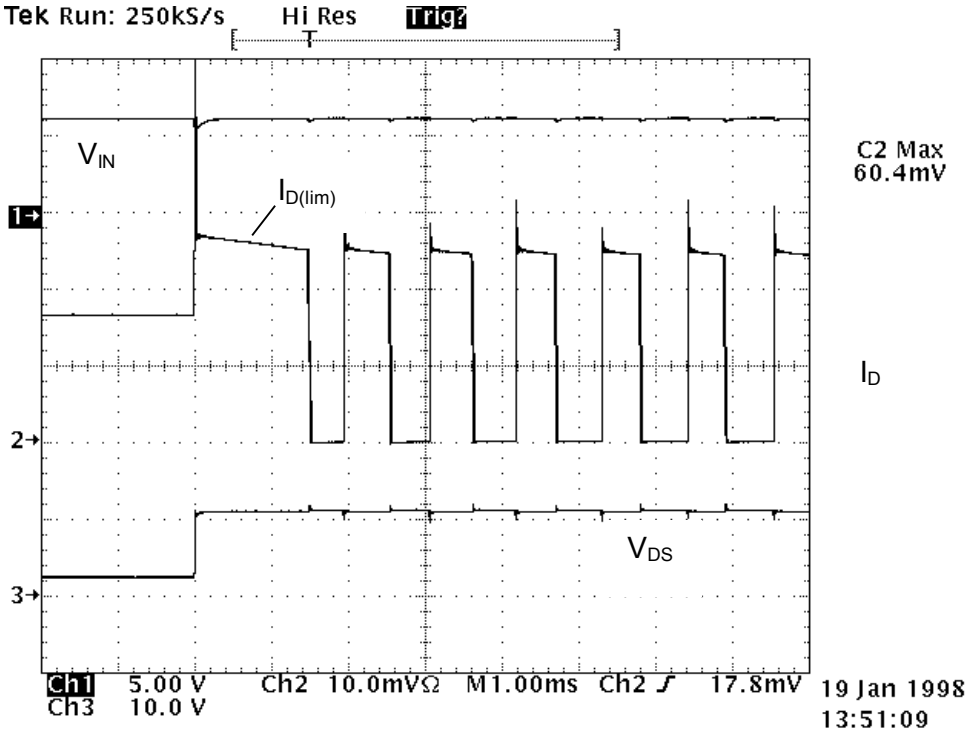


Figure 4 Short Circuit Condition

Figure 4 shows a transition from normal operation (0.8A) into short circuit condition. The current is limited to $I_{D(lim)}$ and the device shuts off after reaching the 170 °C junction temperature. After cooling down the device restarts automatically (V_{IN} permanent On).

2.2 Switching of Inductive Loads: Overvoltage Protection

Each channel has an active zener-diode clamp between drain and gate, in order to protect the device against overvoltage when using inductive loads (e.g. inductors, relays, motors). When the channel is switched off and the voltage across the inductive load rises above 45V, the zener diode will start to conduct and control the gate, so keeping the MOSFET on. Compared to Avalanche Breakdown, the switch-off energy in this case is considerably larger. Figure x displays the switching of a solenoid, clearly showing the point of switching (change of inductivity).

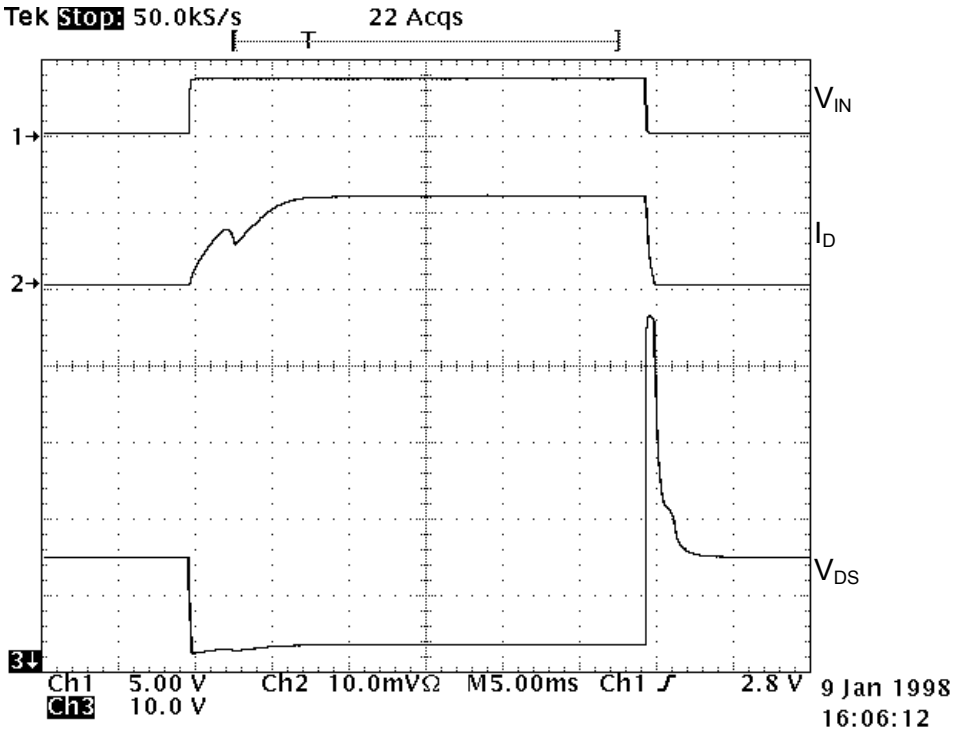


Figure 5 Switching of a Solenoid

A short switch-off time with a large di/dt exists with no chance of damage to the device, due to the active zener diode clamp.

Application Example:

The switching-off of a relay is a typical example for demonstrating the inductive overvoltage behaviour. If one channel is used to drive a relay, no external free-wheeling diode is necessary, as V_{DS} is limited by the device itself.
This overvoltage protection function does not require a supply voltage.

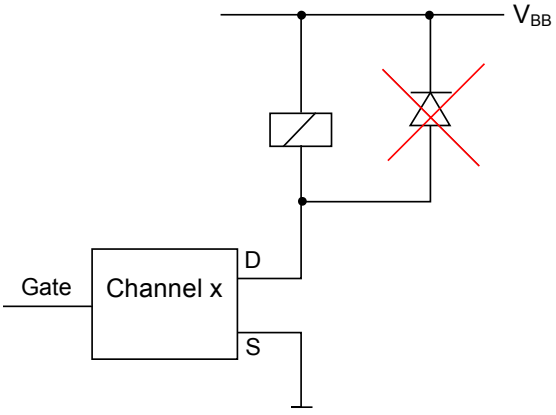


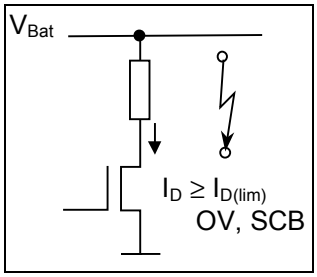
Figure 6 Driving a relay

The mentioned faults in the previous chapter (overload, short circuit, overtemperature) would influence the lifetime of the device, if there would be no protection against them.
There are other faults which may occur without stress for the device, but strong negative influence on the application and on emission levels. These faults are "open load" and "short circuit to ground".

3 Fault Detection

There are four different conditions each channel can work, which the driving microcontroller must be able to distinguish definitely.

3.1 Overload (OV), Short circuit to battery (SCB) or Overtemperature

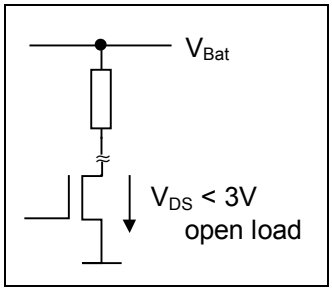


Overload or short to battery do only stress the device in ON-state. As soon as the current limit $I_{D(lim)}$ is reached the bit combination HL (s. diagnosis chapter) is set as an "early warning" for an operating condition, which may lead to an overtemperature.
I. e. when an incandescent load is switched on and the current is limited only temporarily, HL is reported as early warning. If there is a permanent overload or short circuit and the junction reached 170°C the device protects itself and switches the affected channel off until the junction temperature has decreased.

3.2 Open load (OL)

The open load test is performed in OFF-state. A current source is applied to the drain to pull the output below the threshold of the open load reference voltage which is typ. 3V according data sheet. LH bit combination is set.

Remark
If there is an open load condition and the channel is switched on, no fault is recognized.



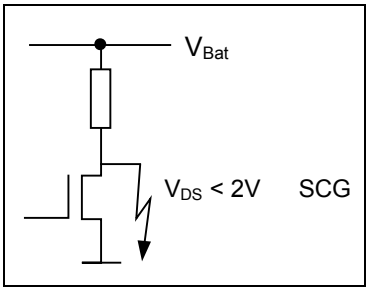
For ”open load” detection the respective channel has to be switched off for $t \geq t_{D(fault)}$ = 100µs typ.

3.3 Short to Ground (SCG)

Short to ground condition is also detected in off state.
If the mentioned current source pulls V_{DS} below a second threshold (2V typ.) SCG is detected and the respective bit combination LL is set.

Remark
If the channel is switched on during a SCG condition no fault is detected.

For SHG detection the respective channel has to be switched off for $t \geq t_{D(fault)}$ = 100µs typ.

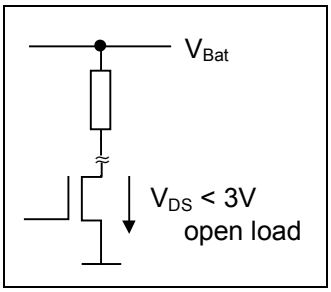


3.3.1 Open load and short to ground; Influence on the application

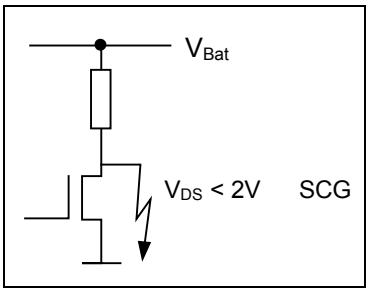
In off-state and normal condition (no fault) the drain-source voltage $V_{DS} = V_{Bat}$. So a decreasing drain-source voltage is an appropriate method for open load detection.
Using two different thresholds is a good idea for distinction. It is described in the following.

3.3.2 Influence on application

In Engine Management/Powertain application an injector is a typical load. The influence on the application at open load or short to ground condition is shown in the following figures.



No injection, neither in on-, nor in off-state
The engine operates with 3 cylinders,
”Limp-home to the workshop” is possible



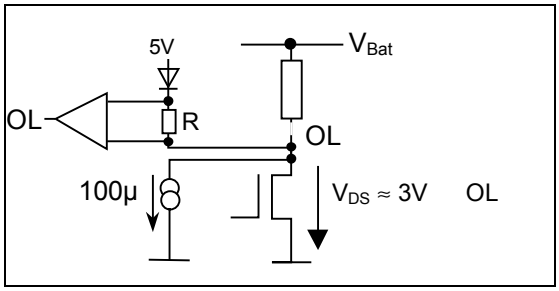
Injection in on- and off-state
danger of catalyst damage

It is evident, that a wrong fault detection in this application is not allowed, so another key design consideration is the device ability to distinguish definitely between open load and short to ground condition.

3.3.3 Realisation in practice

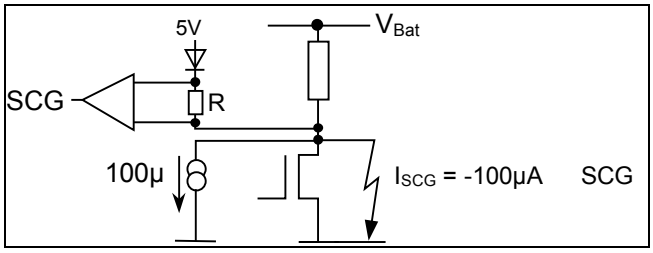
Open load

In case of an open load condition the drain voltage decreases so the diode starts to conduct and the internal current source is able to pull the drain down. This starting current flow causes a voltage drop at R. When the V_{DS} reaches the open load detection voltage $V_{DS(OL)}$ = 3V (typ.) open load is detected and latched into the fault register.



Short to ground

In difference to the open load condition the drain must be pulled down actively. This external short circuit must enable a current from at least -100 µA outside the drain. This short to ground detection current is measured internally and the corresponding fault register is set. When this current threshold is reached $V_{DS(SCG)}$ = 2V (typ.) is measurable at the drain.



3.4 Normal function

If there is no fault and the device is within its operational range, it works under normal function conditions. HH-bit combination is set in ON-state as well as in off-state.

Remark
Normal function is also reported, although there is an overload or short circuit condition, but the respective channel is switched off.

$I_{D(lim)}$ is not reached → no stress for the device

Normal function is also reported, although there is an open load or short to ground condition but the respective channel is switched on.

OL, SHG-condition are only recognised in off-state

Operation condition	Detection in		Bit combination
	Off-state	On-state	
Normal function	X with no fault	X with no fault	HH
	X with OV, SCB	X with OL, SCG	
Overload (OV), SCB, Overtemperature		X	HL
Open load (OL)	X		LH
Short to ground (SCG)	X		LL

Table 1 Status detection in different operation modes

4 Serial Peripheral Interface (SPI) for Output Stage Control and Diagnostic Feedback

The TLE 6220, 6230, 6240 GP provide a serial peripheral interface (SPI) to control the power DMOS switches, as well as diagnostic feedback.

The serial interface consists of a chip select ($\overline{CS}$), serial clock (SCLK), serial data input (SI) and a serial data output (SO). To enable serial data transfer, the $\overline{CS}$ is brought low while SCLK is low. At this time the current fault status (two bits per channel) are loaded into the shift register. As each of the consecutive rising edges of SCLK occurs, the state of the SI pin will be clocked into the device. Simultaneously at each rising clock, the diagnostic information is output on the SO pin. Figure 7 shows the cyclic serial data transfer.

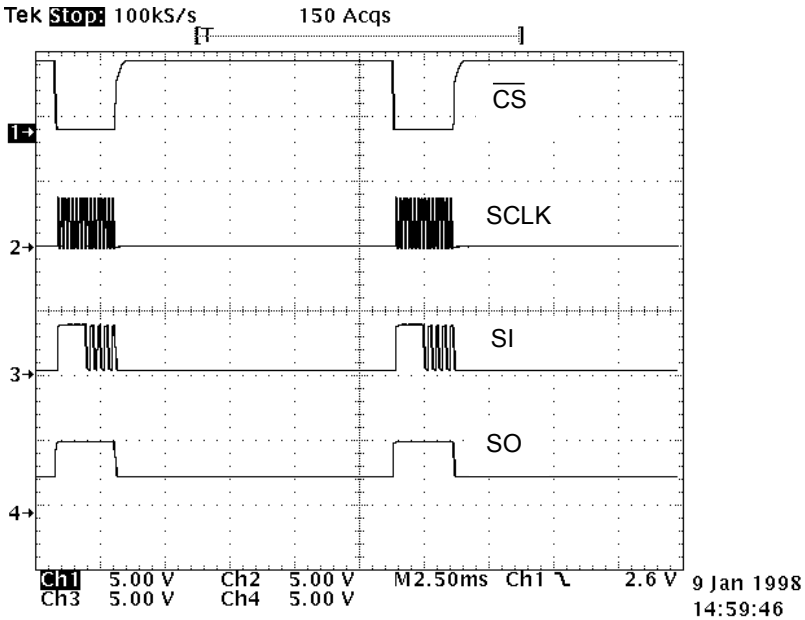


Figure 7 Cyclic serial data transfer via SPI

The features, the behaviour, protection function described up to now are valid for all three devices, the TLE 6220, 6230, 6240 GP.
The octal switch (TLE 6230 GP) is now used to describe the output stage control and the diagnostic feedback in principle.

4.1 Output Stage Control (TLE 6230 GP)

Each output is independently controlled by an output latch and a common reset line, which disables all outputs. The Serial Input (SI) is read on the falling edge of the serial clock. A logic high input 'data bit' turns the respective output channel ON, a logic low 'data bit' turns it OFF. $\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output control buffer.

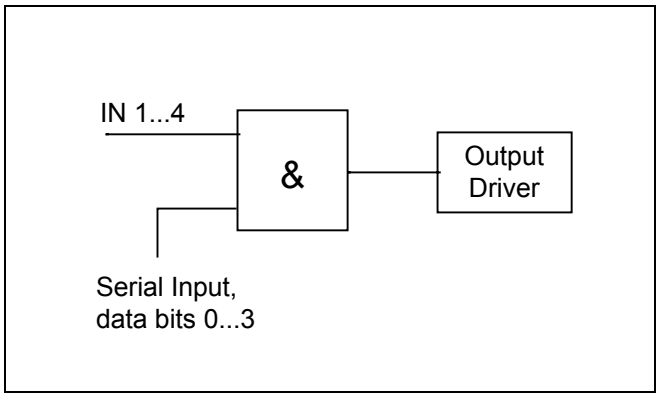
The input data consist of two bytes- a control byte and a data byte. The control byte is used to program the device, to operate it in a certain. The eight data bits contain the input information for the eight channels, and are high active.

4.1.1 Parallel Control for Channel 1 to 4

In addition to the serial control of the outputs it is possible to control channel 1 to 4 directly in parallel for PWM applications.
A Boolean **AND operation** is performed on each of the parallel inputs and respective SPI data bits, in order to determine the states of the respective outputs.
The parallel inputs are high or low active depending on the PRG pin. If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the outputs 1 to 4 are switched OFF. PRG pin itself is internally pulled up when it is not connected.

PRG - Program pin. PRG = High (V_S): Parallel inputs Channel 1 to 4 are high active
PRG = Low (GND): Parallel inputs Channel 1 to 4 are low active.

The AND operation implies that the output can be switched off by the SPI data bits, even if the corresponding parallel input is in the ON state.



SPI Priority for OFF-state

This also implies that the serial input data bit can only switch the output channel ON if the corresponding parallel input is in the ON state.

Due to the AND operation the respective serial data bits must be programmed to high level to enable parallel control.
Figure 8 shows the serial data transfer. Channel 5 to 8 are programmed off, channel 1 to 4 on.

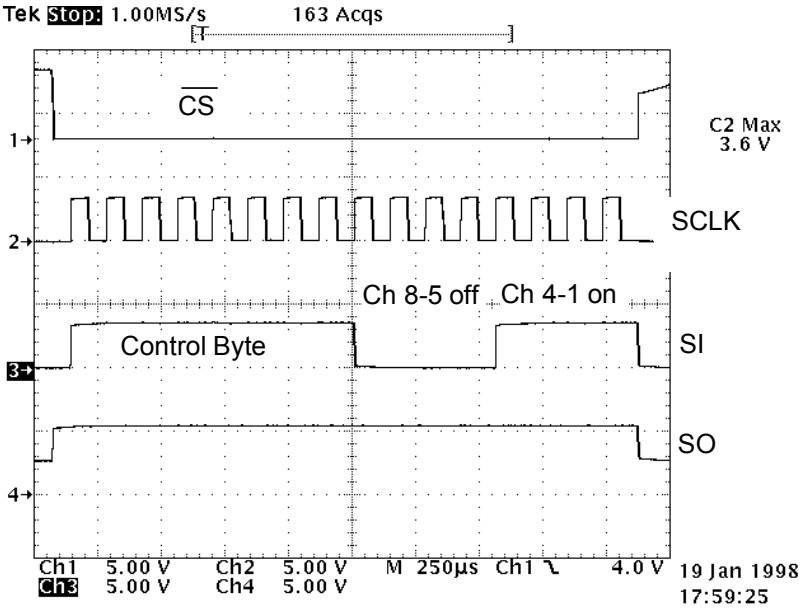


Figure 8 Data bits 0 to 3 are programmed high to enable the parallel control for channel 1 to 4.

Figure 9 shows the parallel control of channel 1 to 4 with the software tool of the evaluation board. Frequency and Duty Cycle are adjustable. In practice a µC-Port drives the four inputs to react in real time on different events.

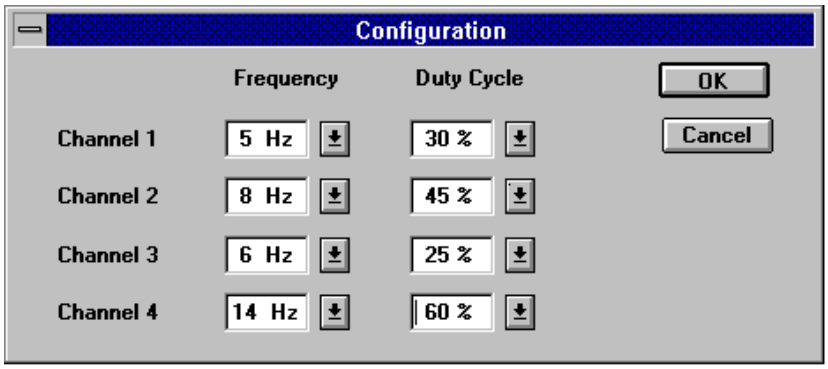


Figure 9 Parallel control via software tool

Figure 10 shows the output voltages of channel 1 to 4 during parallel control with inductive loads. The output voltage increases after shut off until the internal clamp gets active.

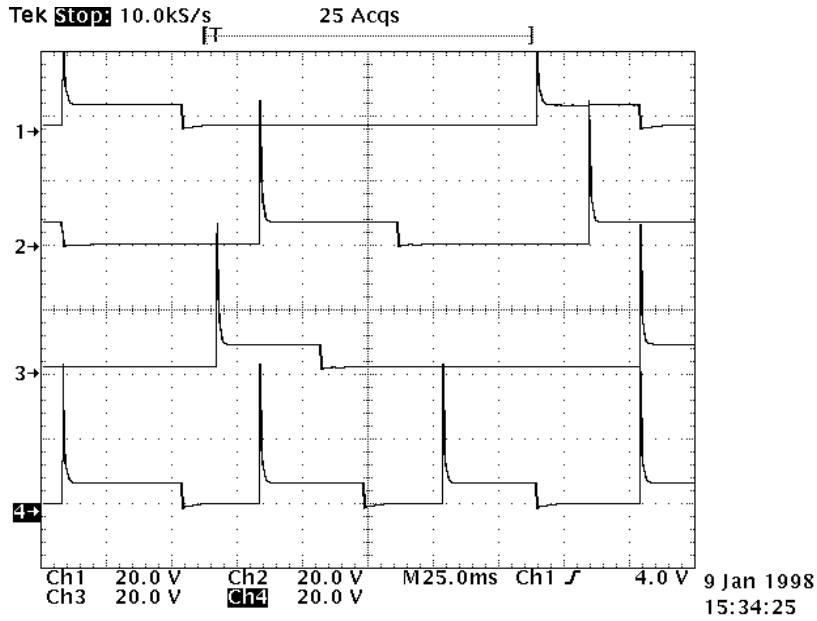


Figure 10 Output voltages of channel 1 to 4

4.1.2 Serial control of the outputs

As mentioned above, the serial input byte consists of a control byte and a data byte. Via the control word, the specific mode of the device is programmable.

MSB LSB

CCCCCCCC DDDDDDDD : Serial input byte

Control Bits Data Bits

Two specific control words are recognised (for TLE 6230 GP), having the following functions:

No.	Serial Input Byte	Function
1	LLLL LLLL XXXX XXXX	Only 'Full Diagnosis' performed. No change to output states.
2	HHHHHHHH DDDDDDDD	IN1...4 and serial data bits 'AND'ed. 'Full Diagnosis' performed.

Note: 'X' means 'don't care', because this bit will be ignored
'D' represents the data bit, either being H (=ON) or L (=OFF)

1. LLLLLLLL XXXXXXXX - Diagnosis only
By clocking in this control byte, it is possible to get pure diagnostic information (two bits per channel) in accordance with the diagnosis chapter. The data bits are ignored, so that the state of the outputs are not influenced. This command is only active once unless the next control command is again "Diagnosis only". Diagnostic information can be read out at any time with no change of the switching conditions.

2. HHHHHHHH DDDDDDDD - AND operation, and ‘full diagnosis’
With HHHHHHHH as the control word, each of the input signals IN1...IN4 are 'AND'ed with the corresponding data bits. Full diagnosis (2 bits per channel) is performed.

4.2 Diagnostics

As mentioned previously, the TLE 62x0 GP devices provide on-board diagnostics to identify load problems for detailed fault detection. The four operation conditions that can be detected are

- normal function
- overload/short to battery/overtemperature
- open load
- short to ground

As soon as an error occurs, the error information is latched into the diagnosis register and a falling edge is generated at the $\overline{\text{FAULT}}$ pin.

4.2.1 Diagnostic via $\overline{\text{FAULT}}$ - pin

The general fault pin (open drain) shows a high to low transition as soon as an error occurs for any one of the channels. This fault indication can be used to generate a µC interrupt. Therefore a 'diagnosis' interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.
For definite fault detection, an error must exist longer than $t_{d(fault)}$ = 100 µs (typ.). This fault delay time is necessary to filter spikes, transitions, ... in order to avoid false error detection. Figure 11 shows an arising open load condition at channel 1. The error is detected and latched, when it lasts longer than 100 µs. The previous oscillations - generated by a bouncing contact – are filtered and not detected. The arrow shows the real beginning of the open load condition.

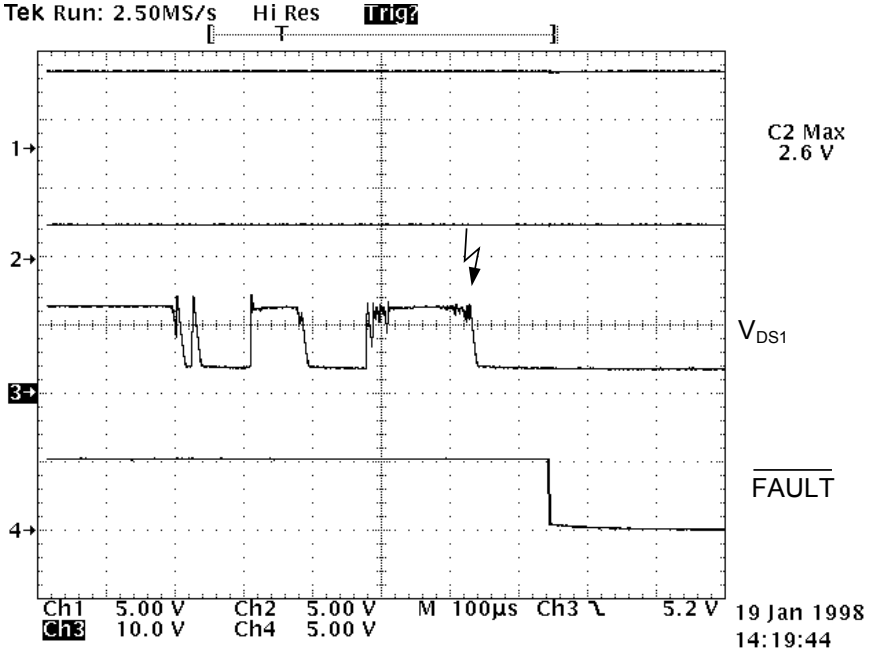


Figure 11 Fault detection via $\overline{\text{FAULT}}$ pin

Figure 12 shows the $\overline{FAULT}$ - signal during the occurrence of an open load condition (arrow) and the $\overline{CS}$ low to high transition. After the fault delay time $t_{d(fault)}$, the $\overline{FAULT}$ - signal transits to low until $\overline{CS}$ rising edge. The chip select low to high transition clears all error register and resets the $\overline{FAULT}$ - signal to high. The error is still present and is latched in the fault register. The $\overline{FAULT}$ - signal again goes to low.

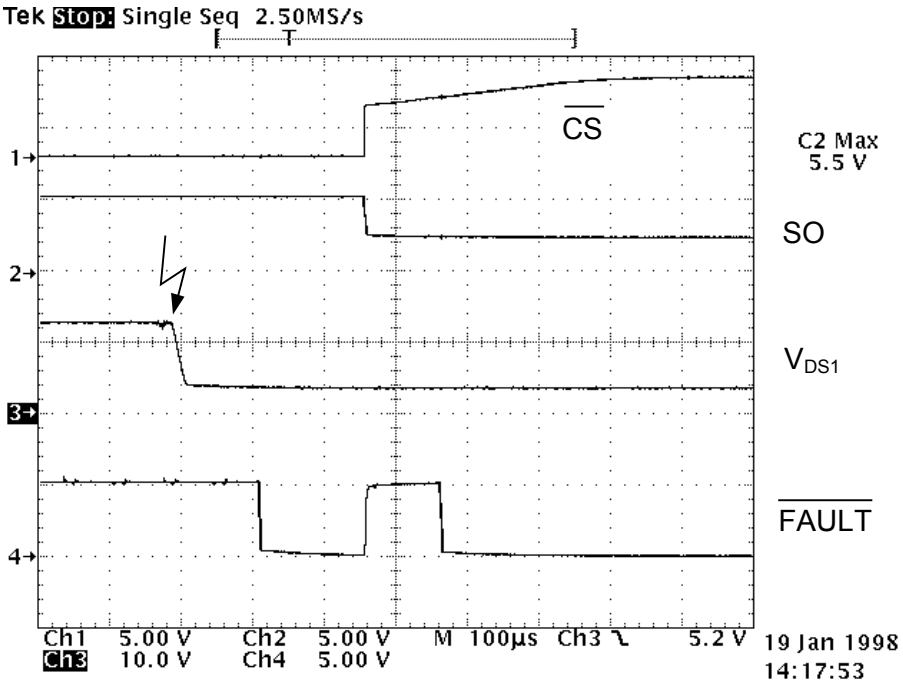


Figure 12
Fault detection via $\overline{FAULT}$ pin during $\overline{CS}$ rising edge

Remark:
The SO line shows the status information which was valid at $\overline{CS}$ falling edge. At that time there was no fault condition, so normal function for all channels was transferred into the shift register. The open load condition for channel 1 can be clocked out with the next $\overline{CS}$ cycle even when it disappears in the meantime.

A new error overwrites the old error report but normal function can't overwrite any existing error. Only the rising edge of $\overline{CS}$ resets the fault register.

4.2.2 Diagnostics via SO line

The FAULT line indicates the occurrence of an error. For a detailed analysis – under respect of emissions levels - the system microcontroller needs to know, which channel (load) is effected and what kind of error has occurred. This detailed diagnostic information is performed by the serial data output (SO) line according to Figure 13.

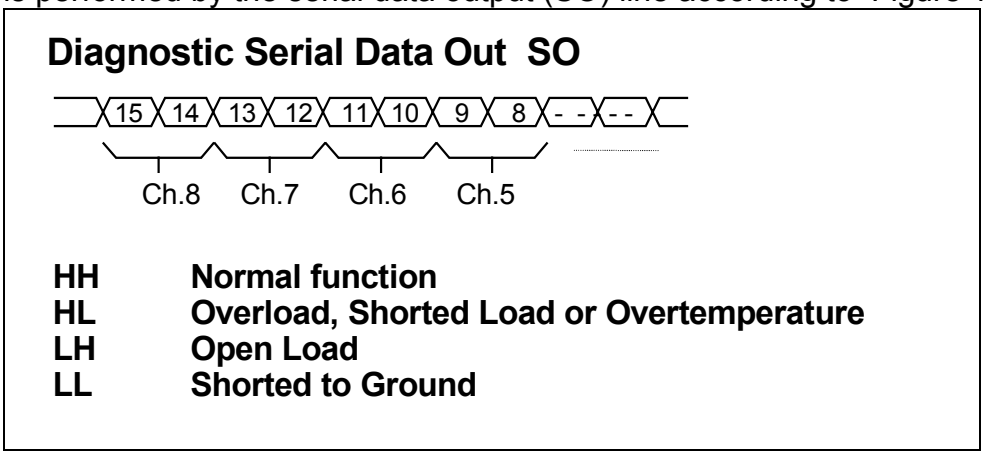
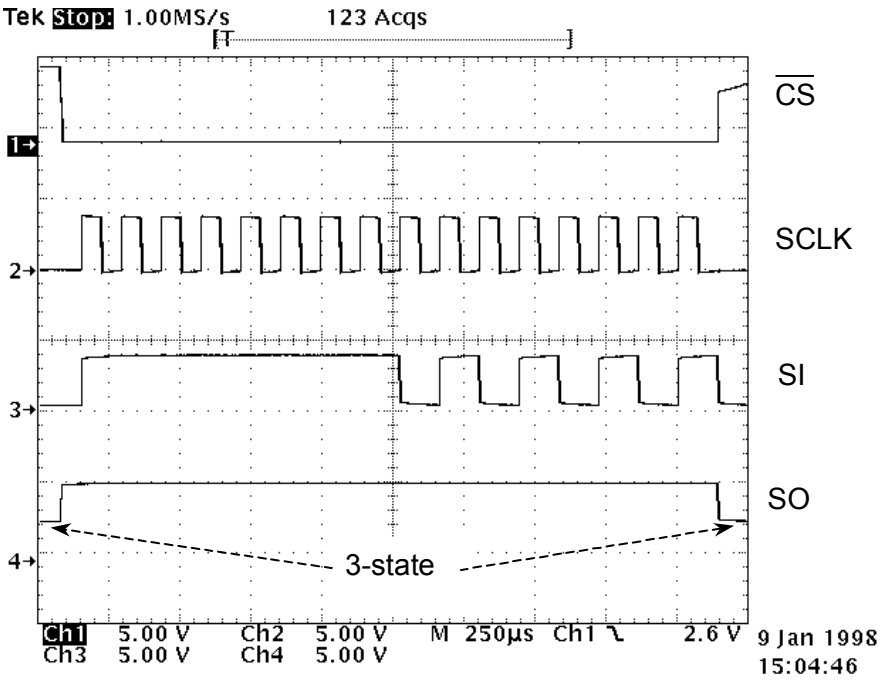


Figure 13 Two bits per channel diagnostic feedback

With the falling edge of $\overline{CS}$ the diagnostic status information is transferred into the shift register. Serial data out pin (SO) is in a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ receives a LOW signal, all diagnosis bits can be shifted out serially. The rising edge of $\overline{CS}$ will reset all error registers. Figure 14 shows the TLE 6230 GP controlled by the software tool of the evaluation board. The oscillogram shows the generated signals $\overline{CS}$, SCLK, SI and the SO-response of the device. The SO-line indicates normal function for all channels and is tri-stated before and after $\overline{CS}$ cycle.



The control byte is programmed to FFhex, i.e. AND operation and full diagnosis is performed. Due to the AND operation the parallel inputs must be set to high

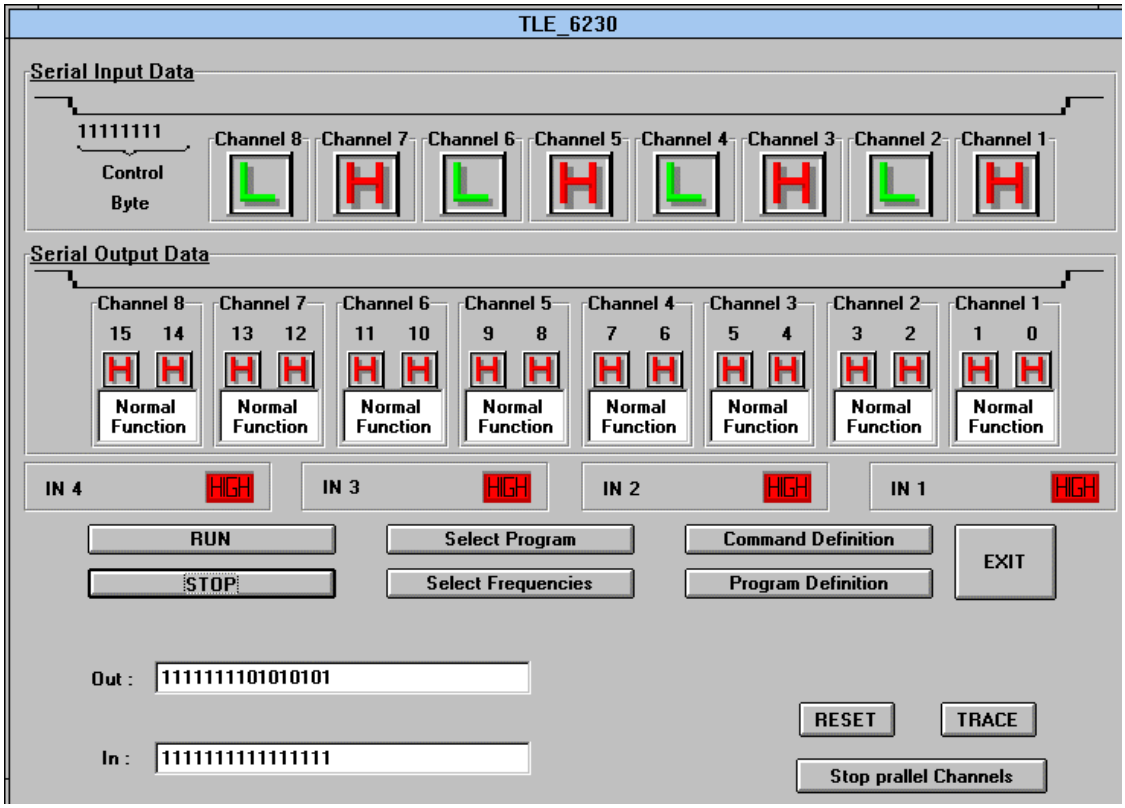
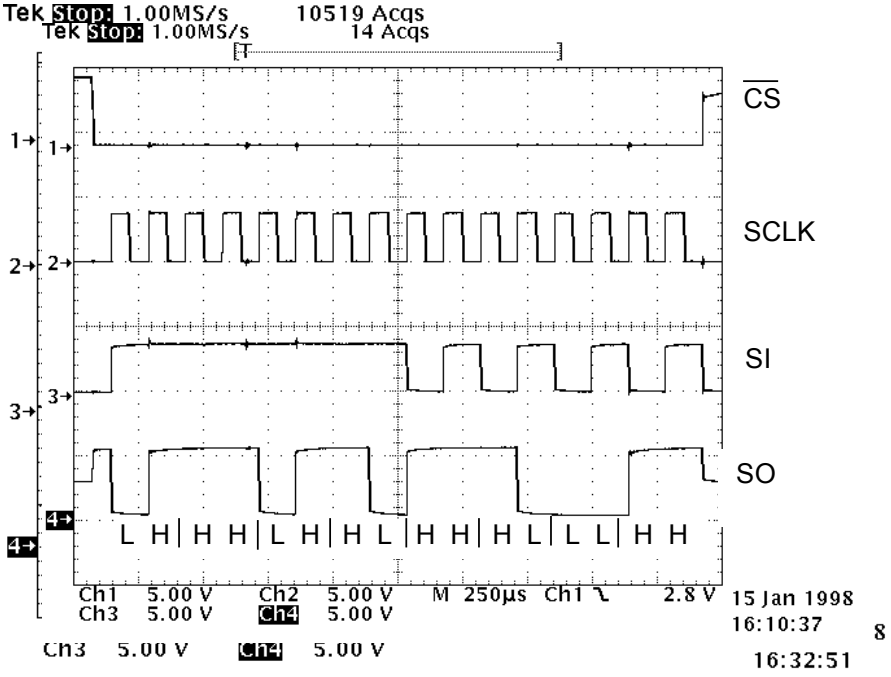


Figure 14 Oscillogram and software evaluation of serial control and diagnosis

(PRG-pin = high assumed) to enable the serial control for channel 1 to 4. The program illustrates SI and SO and the state of the parallel inputs. For every channel normal function is recognised.



Detection of different errors

Figure 15 shows the detection of different fault conditions. The input pattern is the same like before but only channel 1, 4 and 7 operate with normal function.
Channel 8, 6: open load
Channel 5, 3: overload
Channel 2:short to ground

These errors are detected and displayed accordingly.

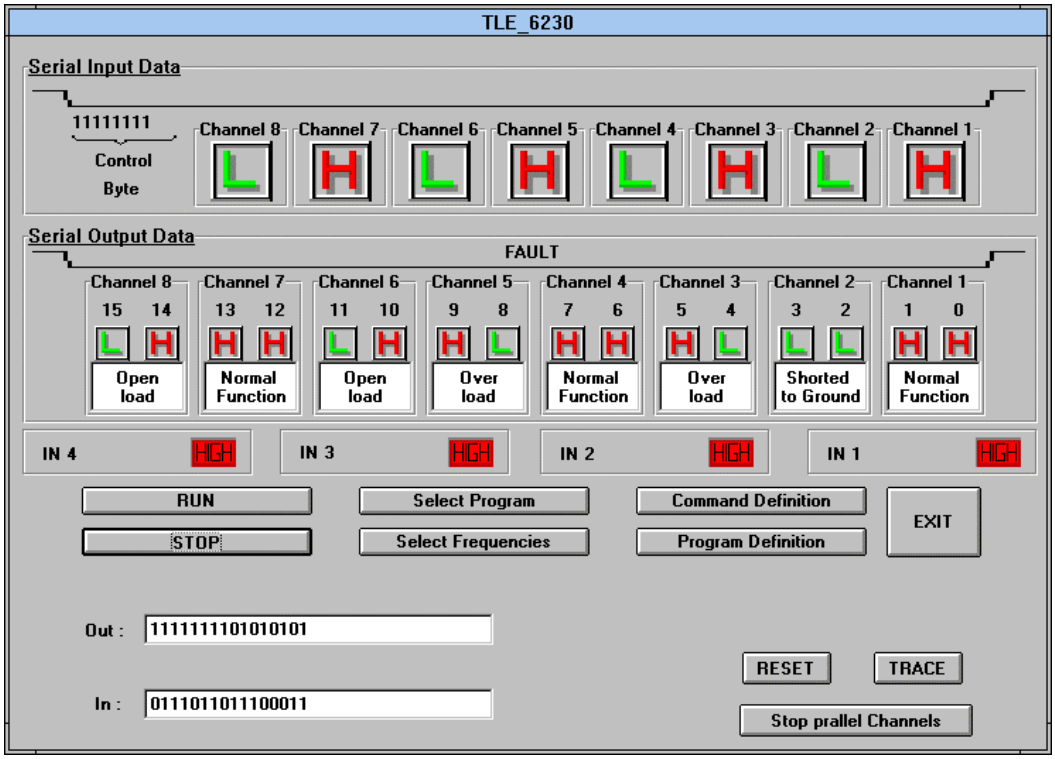


Figure 15 Oscillogram and software display of different errors

Diagnosis only

To check the diagnostic information of all channels with no change of its state, ”diagnosis only” can be programmed as control word. Then all data bits will be ignored, i.e. the state of channels 5 to 8 is not influenced, channels 1 to 4 can continue in PWM-mode depending on the parallel control inputs. Figure 16 illustrates this operation mode. The control byte is programmed to 00hex.
The visible data bits will be ignored.

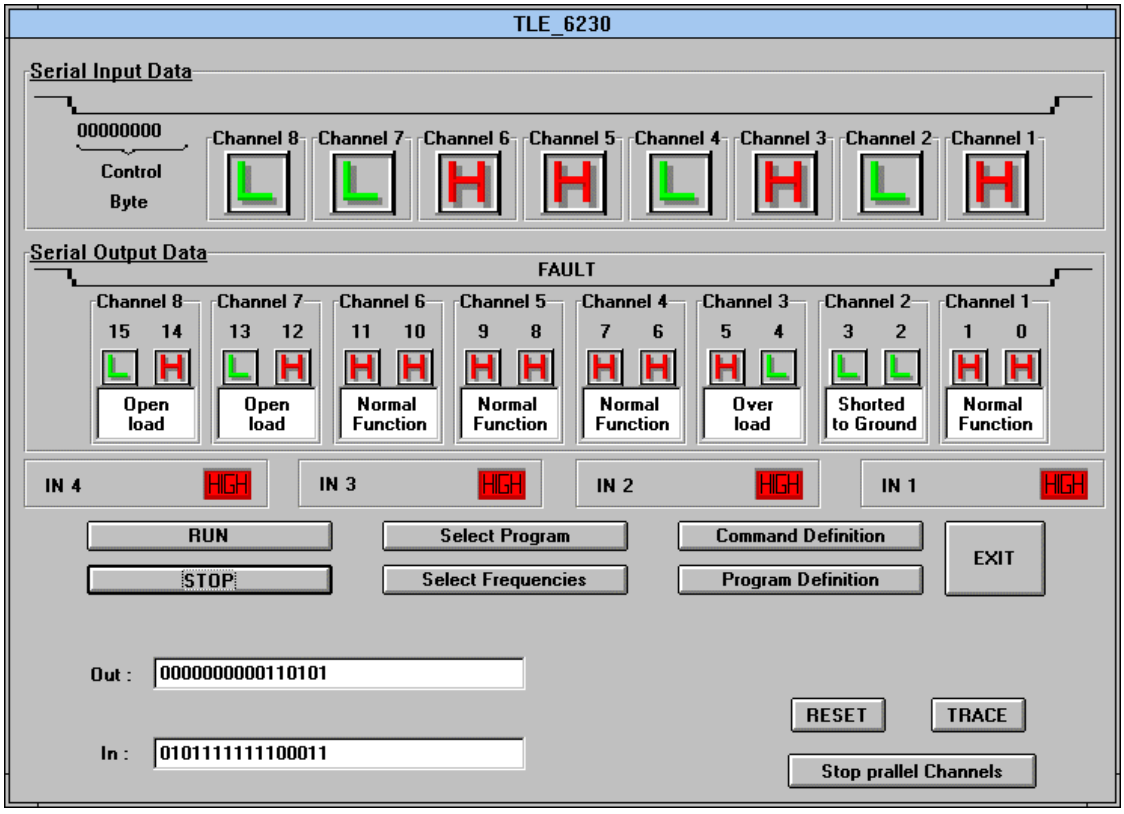


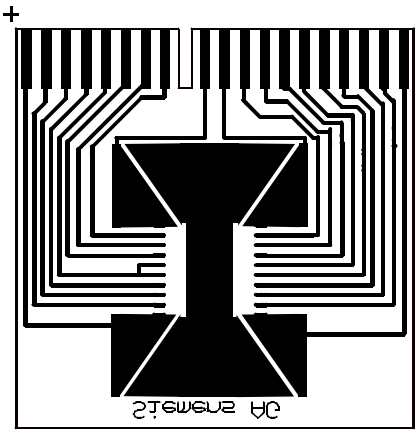
Figure 16 software display with diagnosis only command

5 Thermal and Power Considerations

The TLE 62x0 G family has demonstrated its effectiveness in serial data transfer and driving various types loads, serial as well as parallel. The thermal and power considerations are also of interest. The devices are available in surface-mount Power SO packages to reduce thermal resistance when mounted to a copper-clad circuit board. Using 6 cm^2 copper area a thermal resistance R_{thJA} of 35 K/W can be achieved.

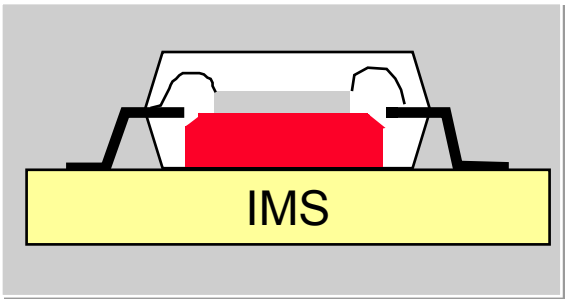
The maximum power dissipation for the device in this example is determined as follows: Assume a maximum ambient temperature (T_A) of 125 °C. Then with the maximum junction temperature (T_J) of 150 °C:

$P_D = (T_J - T_A)/R_{thJA} = 25/35 = 0.714$ W for the device.



If the devices are mounted on **I**solated **M**etal **S**ubstrate (IMS) a thermal resistance of 7 to 10 K/W can be achieved.

$P_D = (T_J - T_A)/R_{thJA} = 25/7 = 3.5$ W for the device



Power SO 36 mounted on IMS

R_{thJA} = 7 - 10 K/W

6 Engine Management Application

Figure 17 shows the TLE 6230 GP in combination with the TLE 6240 GP (16-fold switch) for relays and general purpose loads and the TLE 6220 GP (quad switch) to drive the injector valves. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 28 channels in sum 16 can be controlled di-

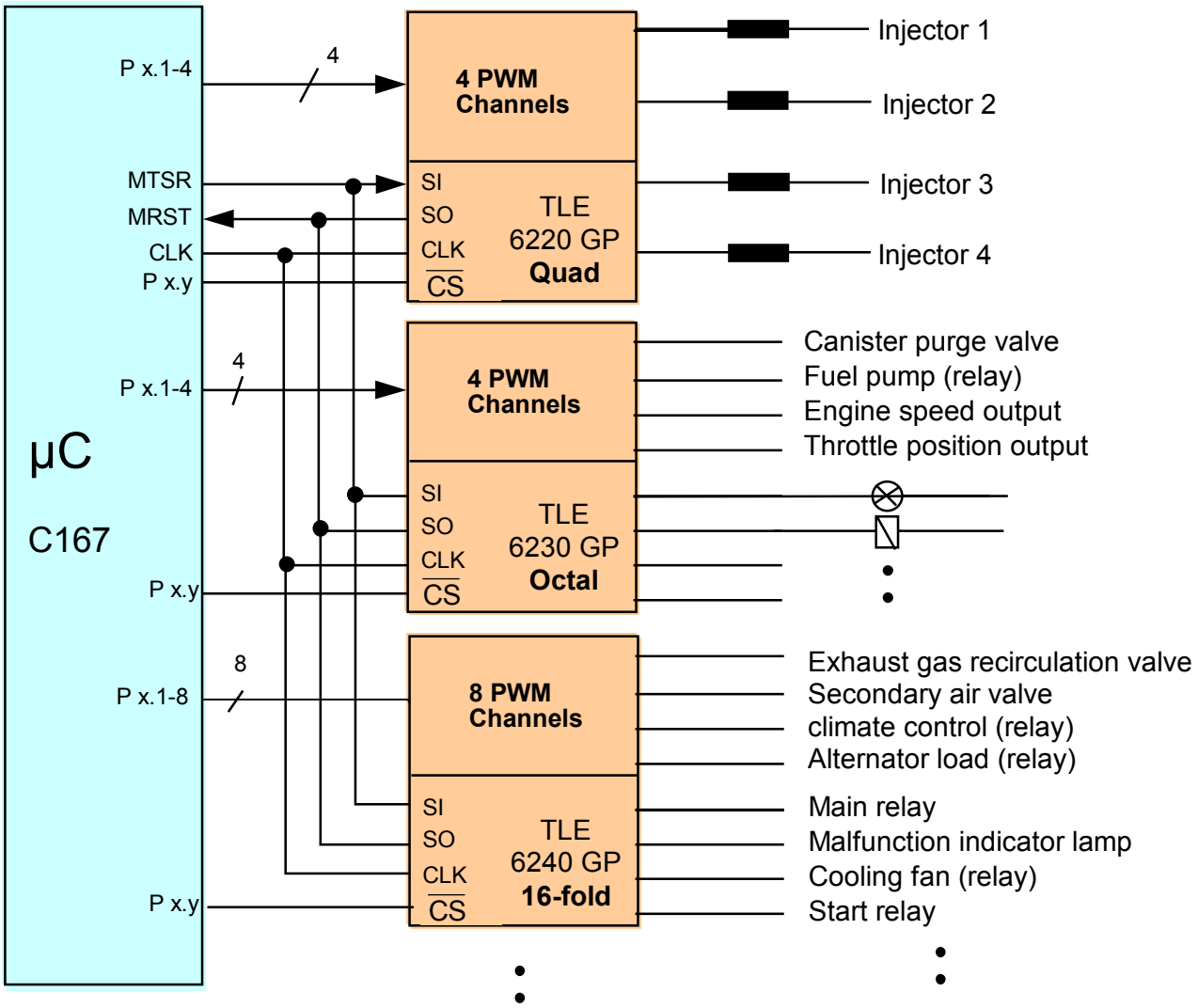


Figure 17 Engine Management Application with the TLE 6220/6230/6240 GP

rect in parallel for PWM applications.

7 Conclusion

The TLE 62x0 GP family are integrated multiple channel low-side switches which combine both; power and logic in a single package. In addition, the devices feature on-board fault diagnostics for detailed error detection (2 bit per channel) to reduce down time and increase system reliability. The thermally enhanced power package increases the power capability of the devices and the ”construction set” (4/8/16-fold) provides more flexibility for design engineers to incorporate the TLE 6220, 6230, 6240 GP into their system solution.