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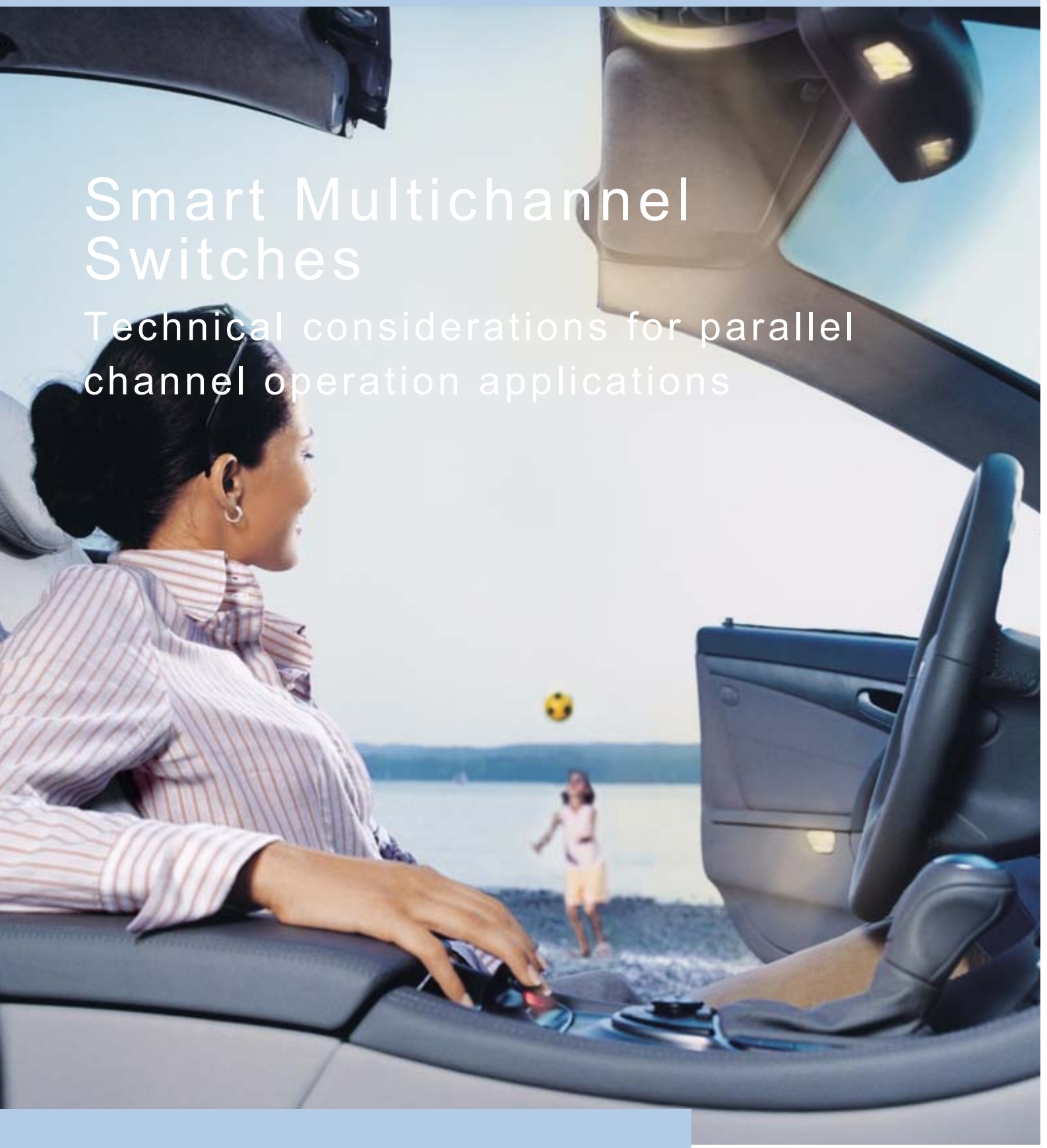

Smart Multichannel Switches

Technical considerations for parallel channel operation applications

Automotive Power

by Bernard Wang

Infineon technologies

Never stop thinking.

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Revision History: V1.2 V1.2

Previous Version:	1.1
Page	Subjects (major changes since last revision)
8	Added “Because thermal effects can cause a difference in $R_{DS(ON)}$ between different channels, asynchronous turn-on of multiple channels in parallel operation can result in current sharing imbalance (ie. the device turned on first will be warmer, and thus have a higher $R_{DS(ON)}$). “
8	Changed “A zener diode connects the gate to the drain” to “A zener diode connects the drain to the gate”

Previous Version:	1.0
Page	Subjects (major changes since last revision)
6	Changed “but is guaranteed” to “but typically is”
8	Added gate driver to Figure 1
15	Corrected from 5.75A to 2.75A
16	Added digital bit identity to Figures 7 and 8
All	Removed “Confidential: For Internal Use Only”

1 Overview

Infineon's Smart Multichannel Switches in Smart Power Technology (SPT) offer performance and reliability for a wide range of applications (ie. powertrain, safety and body in automotive applications). Because of its high level of design integration, the multichannel product family incorporates power, control, protection and diagnostic functions in one package. To further expand their flexibility, it is possible for the system designer to utilize multiple channels of the same IC in parallel. Since the load current and thermal power dissipation can be divided between paralleled channels, parallel operation of channels offers the benefit of increased current load capability. However, Smart Multichannel Switches are designed and tested only for individual channel operation. No specific measures are taken during the design and test process to guarantee symmetrical performance under parallel channel operation. Therefore, when considering Smart Multichannel Switches in parallel channel operation in their designs, system designers should be aware of three important restrictions, including load current capability, switching characteristics & clamping capability, and protection & diagnostic circuit functionality. The following sections will discuss these limitations in further detail and provide a design example with the TLE 6230GP.

It must be noted that, due to the greater potential for mismatches between different ICs, it is not advised to use channels from multiple ICs in parallel. Additionally, it is also not advisable to parallel different kinds of channels on the same IC. For example, on the TLE 6228GP, it is not advisable to parallel channels 1 or 2 (higher current capability) with 3 or 4 (lower current capability), since the two sets of channels are differently configured. This document will focus solely on design considerations when paralleling multiple channels of the same configuration of the same IC.

2 Current Capability

The primary benefit of parallel channel operation is an increase in current carrying capability. Two channels used in parallel offer reduced overall on-resistance $R_{DS(ON)}$ and distribute power dissipation across a larger area on the device. However, mismatches between two channels can cause an imperfect balance in current sharing applications, resulting in electrical and thermal stresses in the paralleled devices. Mismatches that affect current capability include current limit thresholds, overtemperature shutdown thresholds and the $R_{DS(ON)}$ values of individual channels.

A mismatch in overload current detection thresholds restricts the current capability of devices in parallel. For example, as specified on the TLE 6220GP datasheet, the current limit threshold $I_{D(LIM)}$ can vary between 3A and 6A. When calculating the current capability of two channels, the system designer should consider the worst-case scenario, which is if both channels have the lowest specified current limit threshold. Therefore, if two channels on the TLE 6220GP are utilized in parallel operation, based on the lower 3A current limit threshold, the system designer should consider no more than 6A to be the total current capability of both channels in parallel.

With regards to $R_{DS(ON)}$ and overtemperature shutdown thresholds, limitations in manufacturing and thermal conditions in the application can cause undesirable device behavior. Table 1 shows actual $R_{DS(ON)}$ values of different channels on the same TLE 6236G device at room temperature and T_J=150°C. As can be seen, the $R_{DS(ON)}$ value can vary between different channels on the same device. Also noteworthy is that $R_{DS(ON)}$ values change significantly with higher temperature. This means a thermal gradient on-chip can significantly affect the $R_{DS(ON)}$ difference between different channels. The overtemperature shutdown threshold is not measured during production and is not guaranteed to match between different channels, but typically is in the range of 170°C to 200°C. Any imbalance of $R_{DS(ON)}$ between channels in parallel will result in an imbalance in the sharing of the current load and, consequently, an imbalance in power dissipation. The imbalance in power dissipation can cause individual channels to prematurely reach thermal shutdown, requiring the remaining channels to take over the load current. With the increased load, the remaining devices will then heat up more quickly and will eventually reach thermal shutdown themselves. If configured for auto-restart after thermal shutdown, it is possible that different channels will alternate in thermal shutdown. Thermal shutdown cycling between multiple channels can result in an unstable load current and is therefore not advisable. Likewise, variation in overtemperature shutdown thresholds between different channels can also cause alternating thermal shutdown between channels. For example, even if the current load and $R_{DS(ON)}$ of different channels in parallel are the same, the channel with the lowest overtemperature shutdown threshold will reach thermal shutdown first. Remaining channels must then conduct the increased load, causing them to eventually reach thermal shutdown themselves. Therefore, it is prudent to include a thermal design

margin that would prevent the possibility of thermal shutdown between paralleled channels due to variations in $R_{DS(ON)}$ and overtemperature shutdown thresholds.

Table 1 Measured $R_{DS(ON)}$ values for different channels on the same TLE 6236GP device

Channel	$R_{DS(ON)}$ @ 25°C	$R_{DS(ON)}$ @ 150°C (Ohm)
1	1.662Ω	2.651Ω
2	1.599Ω	2.567Ω
3	1.598Ω	2.551Ω
4	1.664Ω	2.643Ω
5	1.669Ω	2.653Ω
6	1.604Ω	2.565Ω
7	1.597Ω	2.557Ω
8	1.667Ω	2.659Ω

For these reasons, the system designer must factor in design and engineering margin when considering the current capability of multiple channels in parallel operation. It is recommended to adequately derate the current capability of individual channels to avoid overload limitation and thermal shutdown.

3 Switching Characteristics and Clamping Capability

Two factors should be considered when multiple channels are switched on and off in parallel operation. First, the system designer should make sure that the activation signals for parallel channels occur at the same time. This can be realized either by controlling the channels through the parallel inputs or by setting the corresponding bits in the SPI register. Channels used in parallel operation should NOT be asynchronously activated. Because thermal effects can cause a difference in $R_{DS(ON)}$ between different channels, asynchronous turn-on of multiple channels in parallel operation can result in current sharing imbalance (ie. the device turned on first will be warmer, and thus have a higher $R_{DS(ON)}$).

The second factor that should be considered is the clamp energy capability of channels in parallel operation. This is not a consideration if the paralleled channels conduct current from a resistive load. It is also not a consideration with inductive loads if a freewheeling diode is utilized in the circuit design to absorb the energy of the inductive load after the channels are turned off. However, in applications with inductive loads without a freewheeling diode, each channel will limit the resulting inductive voltage spike by activation of the integrated clamping circuit. Figure 1 shows the typical active zener clamping circuit integrated into each DMOS channel. A zener diode connects the drain to the gate to turn on the DMOS in the event of a voltage spike at the drain of the device. The output clamping voltage $V_{DS(AZ)}$ is the drain voltage threshold where the channel begins to conduct. Table 2 shows actual measured values of $V_{DS(AZ)}$ for different channels on the same TLE 7230G device at room temperature. As can be seen, channel 8 has a clearly lower clamp voltage compared to the other channels. In output clamping situations with channels in parallel operation, the switch with the lowest $V_{DS(AZ)}$ threshold voltage will always clamp before its counterparts, absorbing most, if not all, the energy of the inductive load. Requiring an individual channel to dissipate inductive energy in excess of its rated maximum can cause overheating and premature failure. Thus in parallel operation, system designers should consider the maximum clamping capability of multiple channels in parallel to be no more than that of a single channel.

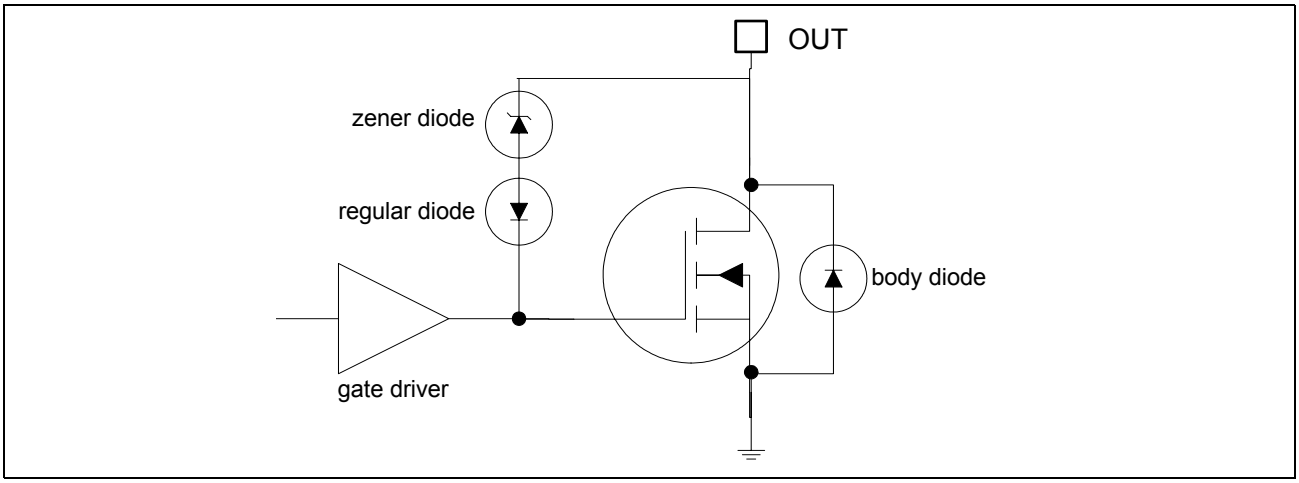

Figure 1 Typical active clamping circuitry integrated into each DMOS channel

Table 2 Measured output clamping voltages for different channels on the same TLE 7230G device

Channel	$V_{DS(AZ)}$ @ 25°C
1	52.404 V
2	52.401 V
3	52.526 V
4	52.521 V
5	52.449 V
6	52.451 V
7	52.413 V
8	52.093 V

Additionally, poor PCB layouts that introduce different parasitics to different channels can also affect the voltage seen by the different devices in parallel. For example, a channel that is poorly routed to the load will experience more parasitics than its counterparts and see a different voltage at its drain, thereby affecting its output voltage clamp threshold.

For these reasons, the system designer should not expect channels in parallel configuration to be able to distribute the output clamping energy evenly among all the channels. This will help to protect the switch that has the lowest output clamping voltage threshold from absorbing more than the maximum rated output clamping energy.

4 Diagnostic Circuitry Considerations

Diagnostic circuits on Infineon's Smart Multichannel Switches are designed to correctly report the status and faults of individual channels. Fault conditions are reported through an on-board FAULT output or are accessible via an SPI bus. Although the diagnostic circuits are independent for each channel, even in parallel channel operation, they will generally report the same, correct result. This is because, in general, the signals used by all channels to detect fault conditions will clearly fall into a specified fault domain. However, problems arise when the signal used to detect fault conditions has a value that lies on different sides of the detection threshold for different channels. Due to design and manufacturing limitations, the diagnostic circuit thresholds on different channels of the same chip cannot be guaranteed to be exactly alike. It is therefore possible that different channels connected in parallel can report different diagnostic results. System designers should take both the OFF-state and ON-state diagnostic functions into account when using the integrated fault detection features in parallel channel configuration.

Figure 2 shows a typical OFF-state diagnostic circuitry integrated in each individual DMOS switch and its corresponding I-V curve. It consists of two comparators and an amplifier that controls two current sources. Depending on the voltage at the drain of the DMOS, the amplifier controlling the current sources will either generate a pullup or pulldown current. The DMOS drain voltage is then detected by the open load and short to ground comparators, which reports a fault if either the open load voltage threshold $V_{DS(OL)}$ or short to ground voltage threshold $V_{DS(SG)}$ are crossed. Table 3 shows actual measured values of open load and short to ground fault detection thresholds for different channels on the same TLE 6214L device at room temperature. In general, the drain voltage that results from a fault condition will fall within the area of one of the three domains. This would then result in the same reported diagnostic result by all channels. However, if the measured drain voltage falls on different sides of the diagnostic threshold of different channels, then different channels will report different diagnostic results. For example, in Table 3, it can be seen that, if channels 1 and 2 on this particular chip are connected in parallel and the drain voltage V_{DS} is 2.98V, then channel 1 would report normal operation while channel 2 would report open load. Likewise, if the drain voltage V_{DS} is 2.01V, then channel 1 would report open load while channel 2 would report short to ground.

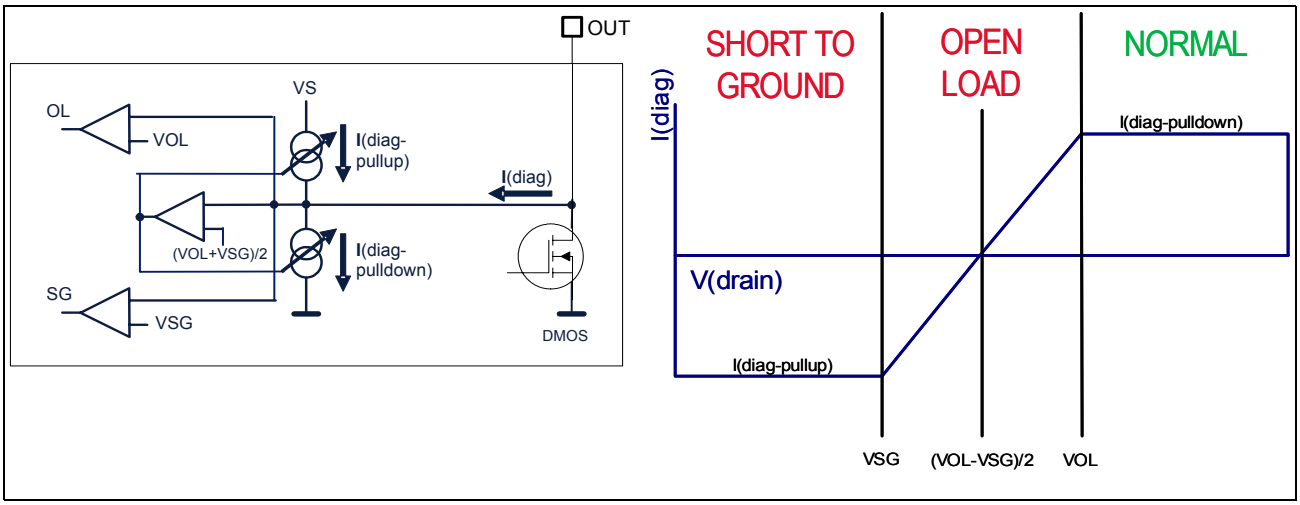

Figure 2 **Typical OFF-state diagnostic circuitry integrated in each individual DMOS switch and its corresponding I-V curve**

Table 3 **Measured Open Load and Short to Ground thresholds for the diagnostic circuits of individual channels on the same TLE 6214L device**

Channel	$V_{DS(OL)}$ @ 25°C	$V_{DS(SG)}$ @ 25°C
1	2.95 V	1.99 V
2	3.01 V	2.03 V

Figure 3 shows the typical ON-state diagnostic circuitry integrated within each individual DMOS switch. The current limit comparator measures the current using the voltage across a sense resistor in series with a sense DMOS and compares this to an on-chip reference voltage. Table 4 shows actual measured values of the current limit detection threshold $I_{D(LIM)}$ at room temperature for different channels on the same TLE 6214L device. As mentioned previously, current limit detection thresholds can vary across different channels. It can be seen from Table 4 that, if channels 1 and 2 are used in parallel operation and a load current of 14A is distributed between the two channels (7.1A in channel 1 and 6.9A in channel 2), then channel 1 would report normal operation and channel 2 would report overload.

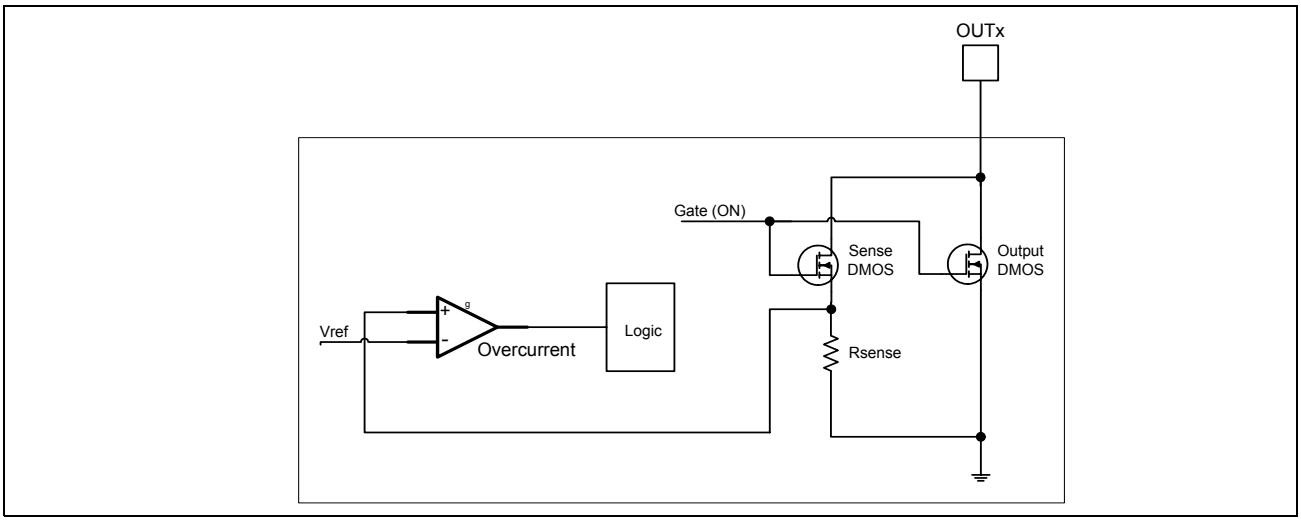

Figure 3 **Typical ON-state diagnostic circuitry integrated in each individual DMOS switch**

Table 4 **Measured Shorted Load and Overload thresholds for the diagnostic circuits of individual channels on the same TLE 6214L device**

Channel	Current Limit Threshold $I_{D(LIM)}$ @ 25°C
1	7.2 A
2	6.9 A

In most fault situations, the signals used to detect fault conditions will fall in the domain of a known fault condition and the diagnostic circuits of different channels connected in parallel will report the same results. However, due to differences in the thresholds of the fault detection comparators, it is possible that different channels connected in parallel will report different results. It is recommended for the system designer to keep this possibility in mind when reading diagnostic information of channels in parallel operation.

5 Design Example

As a design example, consider multiple channels on a TLE 6230GP device being used together in parallel. To properly utilize channels in parallel, they should be switched on and off simultaneously either with the same parallel input or by setting the corresponding bits in the SPI register. Channels 1 and 2 are ideal candidates for parallel implementation due to their neighboring output and control pins, simplifying routing during PCB design. Figure 4 shows the activation and shutdown of channels 1 and 2 in parallel configuration on the same TLE 6230GP device and the resulting drain voltage and drain current waveforms.

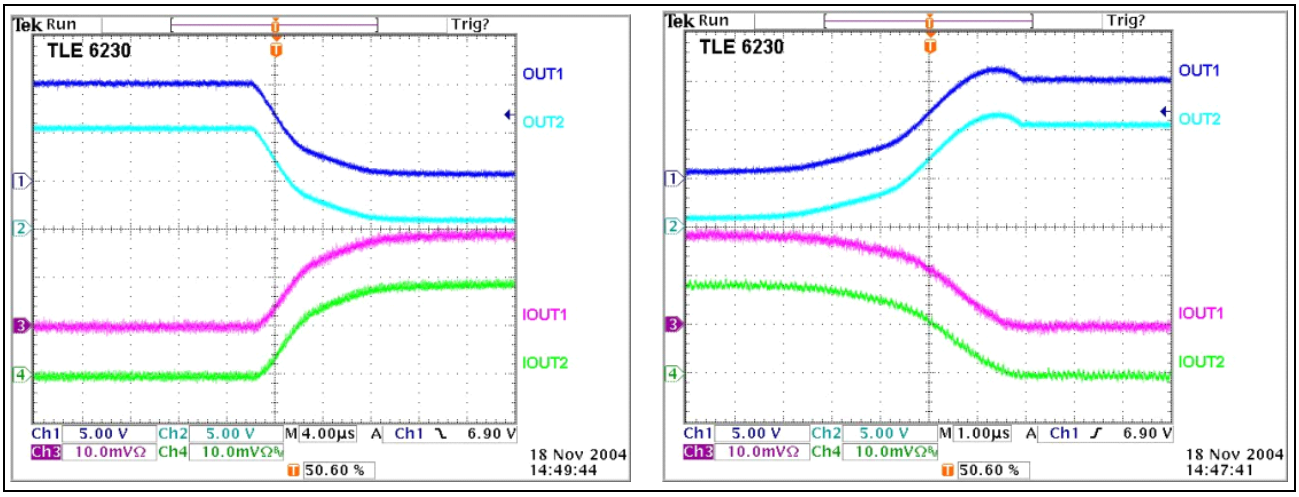

Figure 4 Simultaneous turn-on and turn-off of channels 1 and 2 on a TLE 6230GP device. Note: the scale of the current waveforms is 500mA per 10mV.

The TLE 6230GP has eight identical channels with a maximum RDS(ON) value of 1.7Ω at 150°C and a minimum current limit value of 1A each. Based on these values, for channels 1 and 2 in parallel, the system designer should design for a maximum combined RDS(ON) value of 0.85Ω and a combined current capability of 2A. Additionally, since the two channels in parallel operation will simultaneously generate heat on the IC, attention must be paid so that the chip does not exceed thermal limitations. This helps to avoid the possibility of alternating thermal shutdown of the paralleled channels. Figure 5 shows examples of undesired thermal shutdown conditions. The first scope capture shows what occurs if channel 1 reaches thermal shutdown before channel 2. After channel 1 turns off due to thermal shutdown, channel 2 must then absorb the entire load current, which causes it to reach overload limitation before eventually reaching thermal shutdown itself. The second capture shows the two channels in an alternating thermal shutdown cycling condition. Since only one channel emerges from overtemperature shutdown at any given time, the single active channel must conduct the entire load current. As can be seen from the current waveforms, both scenarios cause instability in the output current.

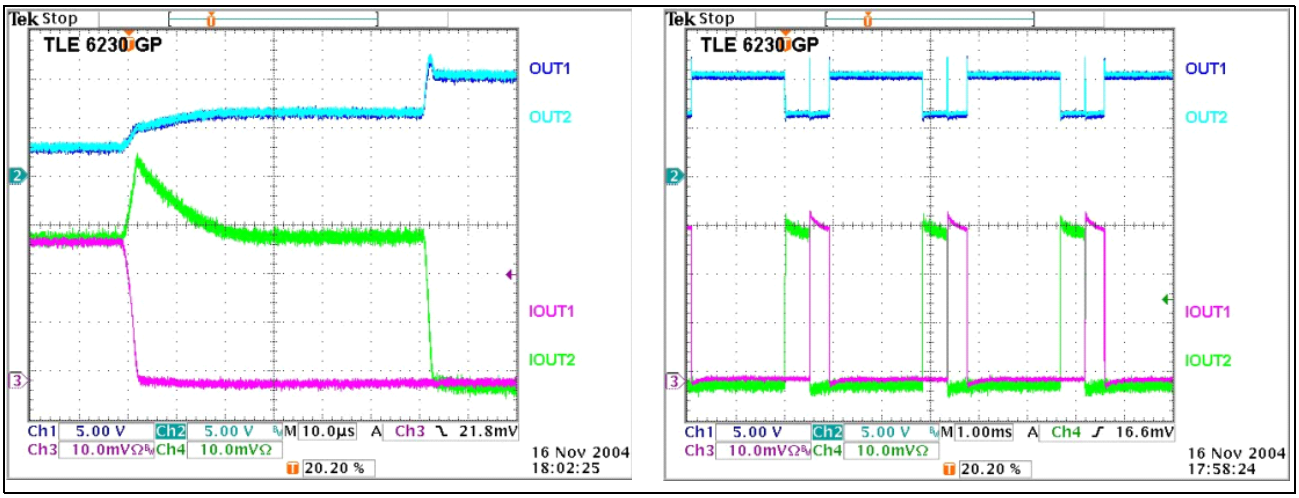

Figure 5 Scope captures of thermal shutdown conditions on the TLE 6230GP. The left figure shows what occurs when channel 1 reaches thermal shutdown before channel 2. The right figure shows alternating thermal shutdown between the two channels. Note: the scale of the current waveforms is 500mA per 10mV.

Additionally, each channel is rated to handle up to 50mJ of output clamping energy (0.5A, single pulse). Output clamping energy capability is not a concern with purely resistive loads or inductive loads with a freewheeling diode. With inductive loads and no freewheeling diode, the combined maximum output clamping energy capability should be considered to be 50mJ (0.5A, single pulse), the output clamping energy capability of a single channel. This is due to potential mismatches in the output clamping threshold $V_{DS(AZ)}$. Poor signal routing to the paralleled channels can also cause parasitic differences, potentially resulting in output clamping imbalance. Figure 6 shows an example of output clamping imbalance between channels 1 and 2 on the TLE 6230GP due to poor signal routing. Note that, even though both channels conduct approximately the same amount of output current in ON state, when the channels are turned off, channel 1 absorbs significantly more of the output clamping energy. In extreme cases, it could even be possible for one channel to absorb all the clamping energy from all other channels connected in parallel. To prevent such output clamping imbalances from causing device damage and failure in parallel channel applications, system designers should not exceed the output clamping energy rating of one individual channel.

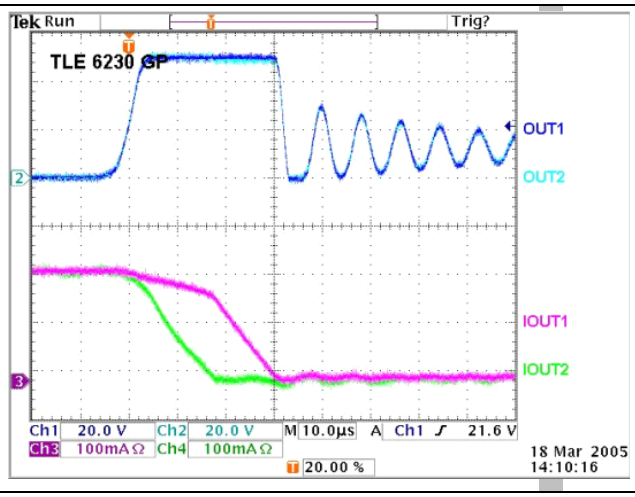

Figure 6 Scope capture of output clamping imbalance on the TLE 6230GP due to poor signal routing. In this scenario, channel 1 absorbs the majority of the output clamping energy. Note: the scale of the current waveforms is 100mA per division.

Each channel on the TLE 6230GP has its own independent OFF-state diagnostics (open load, short to ground) and ON-state diagnostics (overload, overtemperature), creating the possibility of contradictory diagnostic reporting between channels in parallel operation. Figure 7 and 8 show examples of such diagnostic circuit mismatches. Figure 8 shows the test circuit used to show open load diagnostic threshold mismatches and the waveform of the resulting SPI response. (For a more detailed description of the TLE 6230GP SPI functionality, please refer to the TLE 6230GP datasheet). The TLE 6230GP dedicates two bits to report the condition of each channel. For example, if an open load condition is detected on a specific channel, the SPI diagnostic output reports "01" for the corresponding channel. The scope capture shows that when a voltage (3.02V) near the open load diagnostic threshold voltage is applied to all 8 outputs of a TLE 6230GP device, the resulting SPI diagnostic output indicates an open load fault condition only on channels 1-5. The diagnostic outputs for channels 6-8 continue to report "11", indicating normal operation. The result demonstrates that the open load detection threshold for each channel can vary independently. Figure 8 shows a mismatch between the overload detection thresholds of channels 1 and 2. Channels 1 and 2 are configured in parallel operation to share a total load current of 2.75A. If an overload condition is detected on a specific channel, the SPI output reports "10" for the corresponding channel. In the scope capture, channel 1 conducts 1.35A and the SPI diagnostic output indicates it has reached its overload threshold. Channel 2 conducts 1.4A, yet the SPI diagnostic output indicates normal operation. This shows that the overload detection threshold for each channel can vary independently. These two examples show that, under certain conditions, it is possible for diagnostic circuits of different channels connected in parallel to report different results.

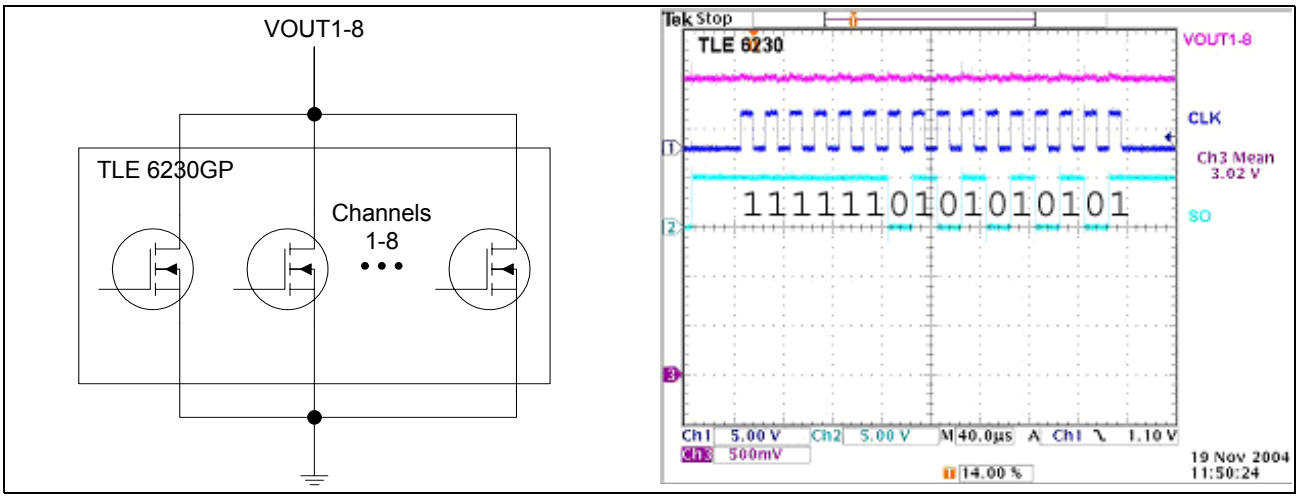

Figure 7 **Test circuit and scope capture of differing open load diagnostic reporting between all 8 channels on a TLE 6230GP device. When all outputs are subject to 3.02V, only channels 1-5 recognize an open load condition.**

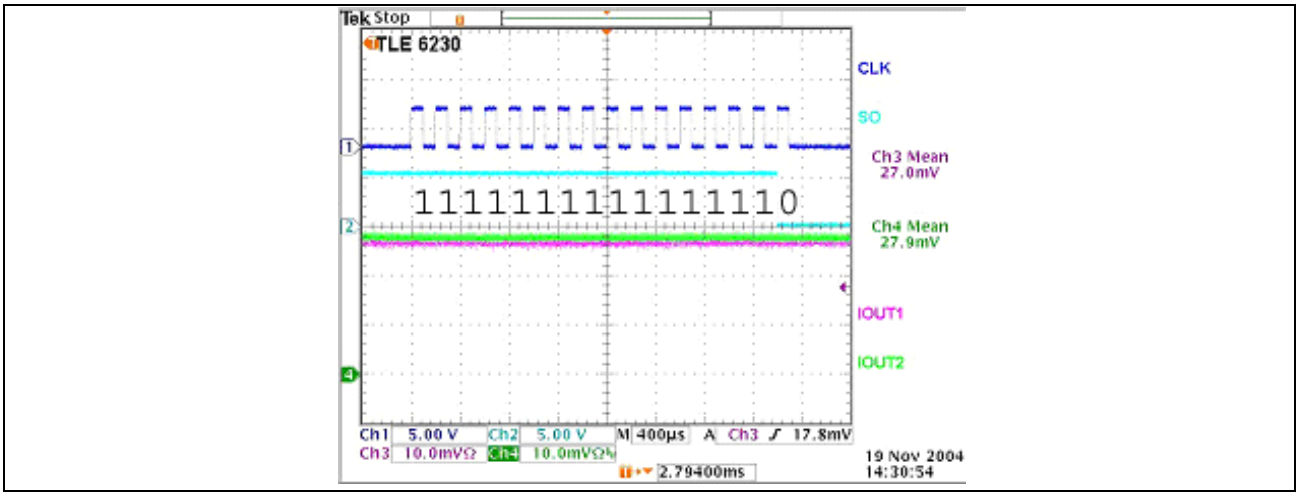

Figure 8 **Scope capture of differing overload diagnostic reporting between channels 1 and 2. Channel 1 conducts 1.35A and reports an overload condition and channel 2 conducts 1.4A but does not report an overload condition. Note: the scale of the current waveforms is 500mA per 10mV.**

6 Summary

Although it is possible to utilize multiple channels on the same integrated multichannel low-side switch in parallel channel operation, system designers should keep in mind three important considerations:

- First, due to manufacturing limitations and environmental conditions, it cannot be assumed that all channels have the same current and thermal capability. This can be taken into account by making adequate current and thermal deratings.
- Second, differences in the output clamping voltage threshold between channels should be taken into account for applications with inductive loads without a freewheeling diode. To prevent damaging devices, the maximum clamping capability of channels in parallel operation should not exceed the maximum clamping capability of an individual channel.
- Third, because it is not guaranteed that diagnostic circuits of all channels have exactly the same fault detection thresholds, it is possible in specific situations for individual channels connected in parallel to report different diagnostic results. System designers should be aware of the possibility when reading diagnostic information of channels in parallel operation.

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