PowerBond^{TM} Technology for High-Current Automotive Power MOSFETs

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Automotive Power

N e v e r   s t o p   t h i n k i n g .

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1 Abstract

This Application Note introduces Infineon Technologies' PowerBond™, an improved bond wire technology for automotive power MOSFETs, and discusses the features and benefits of this technology. It will be show that an increase in the bond wire diameter enables the device to carry more current, to decrease sometime dramatically the Rds(on) and also to increase the reliability of the application. Furthermore, the PowerBond™ III enabled the unprecedented current levels in D^2PAK, DPAK and in through-hole components.

2 What is PowerBond™?

PowerBond™ is an improved bond wire technology from Infineon Technologies. It consists of 500 µm diameter bond wire, 40% thicker than standard 350 µm diameter bond wire. The number of bond wires used is dependent on the package chosen. Depending on the desired current a different interconnection between bond wires and the chip (single stitch or a double stitch approach) can be used. This approach led to the unique current capability of true 180A in D^2PAK and 90A in DPAK. Both of these variants are qualified according to AEC-Q101. They are available as engineering samples since November 2006 and are in mass production since February 2007. Also unique with the PowerBond™ is the 120A current capability in TO-220 and TO-262 package.

3 Why PowerBond™?

PowerBond™ was developed to respond to the increasing demand of current needs in high power applications like for example Electrical Power Steering (EPS).
PowerBond™ also contributes to lower overall package resistance. This is especially important for new power MOSFET technologies. Today the package resistance is about 20% of the total MOSFET resistance. The other 80% are the chip contribution. In the near future with further decreasing of the specific on-resistances of a power MOSFET (Rds(on) x Area), the package share would be easily 50% without further development in assembly technology.

4 What are the Customer Benefits of PowerBond™?

4.1 Rds(on) Reduction

The total Rds(on) of a MOSFET is comprised of chip resistance, (dependent on technology and die size), and package resistance (dependent on quantity of bond wires, diameter, length, pin section etc).
By increasing the amount of bond wires and/or the bond wire's diameter the package influence and thus the total Rds(on) can be reduced. Improvement in the interconnect technology with the introduction of a double stitch bonding led to the further reduction of the package influence on Rds(on). Figure 1 shows the historical development of the PowerBond™. Together with the highest achieved currents, the package resistance is shown for the D2PAK (TO-263), TO-220/TO-262 and DPAK. Figure 2 shows an example of a true 180A part (IPB180N04S3-02), having a total Rds(on) of 1.5mΩ.

4.2 Increase of the Current Capability

In usual molding compounds decomposition occurs if temperature exceeds about 220 °C. This temperature limit restricts the permissible current.

Depending on the bonding configuration the current rating of a MOSFET is limited either by the chip itself or by the bonding
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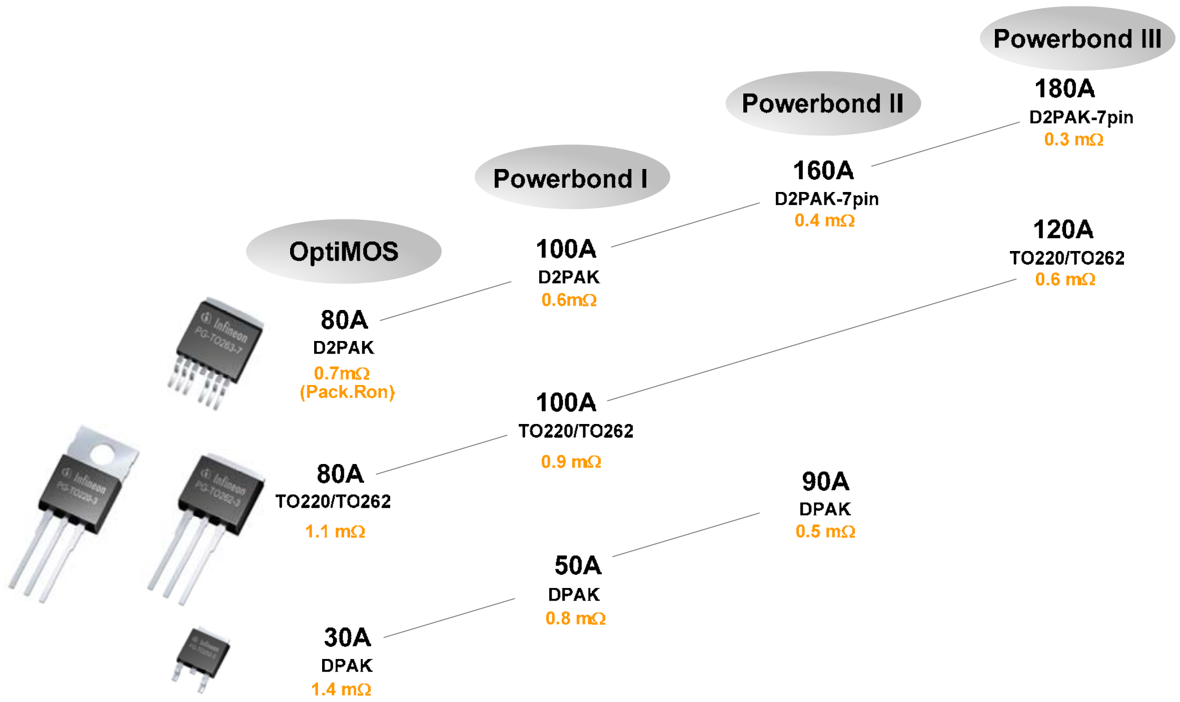

Figure 1 PowerBond™ Generations

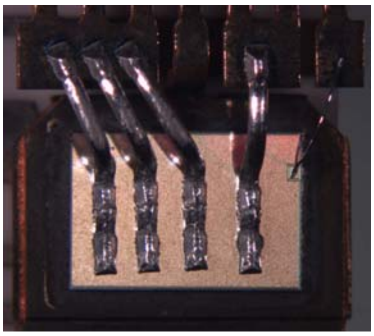

Figure 2 Example of PowerBond™ III (IPB180N04S3-02)

4.2.1 Chip Limitation

The chip current rating of a MOSFET is historically defined at a case temperature of 25°C and by taking into account the static losses, i.e. Rds(on)xId². This power has to be dissipated by the MOSFET via the thermal path.

The maximum power dissipation is defined by:

$$Ptot = \frac{T_{J\_\max} - T_C}{Rth_{JC}} \tag{1}$$

The chip current rating is the current Ids which leads to a temperature rise from Tc to Tj_max:

$$Id = \sqrt{\frac{T_{J\_\max} - T_C}{R_{ds(on)\ \_T_{J\_\max}} \times Rth_{JC}}} = \sqrt{\frac{175°C - T_C}{R_{ds(on)\_175°C} \times Rth_{JC}}} \tag{2}$$

where
Id: drain current
Tj_max: max. junction temperature
Tc: case temperature
Rds(on): max. Rds(on)@Tj_max
RthJC: thermal junction to case resistance

For example in the case of the IPB180N04S3-02, the chip limitation @ 25°C is:

$$Id = \sqrt{\frac{175°C - 25°C}{2.9m\Omega \times 0.5K/W}} = 321A \quad (3)$$

The current capability of the MOSFET is more often limited by the bonding. In the next paragraph it will be shown how to define the current capability of the bonding wires.

4.2.2 Bonding Limitation

In order to calculate this limitation a model including a number of bond wires, a number of stitches, wire diameter, wire length, geometry of the lead frame, of the pins, etc was used. Also a maximum allowed temperature of the bond wires, which is limited by the wire temperature influence on the mold compound material, was defined. In usual molding compounds decomposition occurs if temperature exceeds about 220 °C. This temperature limit restricts the permissible current and the worst point is the top of the wire arc. This temperature combined with the temperature of the chip and of the source pin (or board temperature) defines the current capability of the power MOSFET.

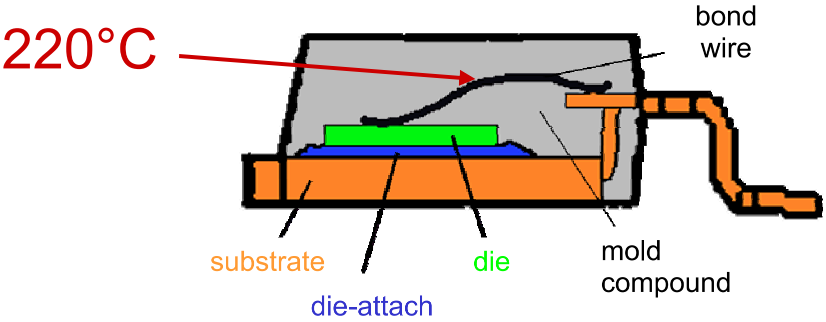

Figure 3 Defining a Max. Temperature of a Bonding Wire

The rated bond wire's current capability for a given package geometry is defined as follows:

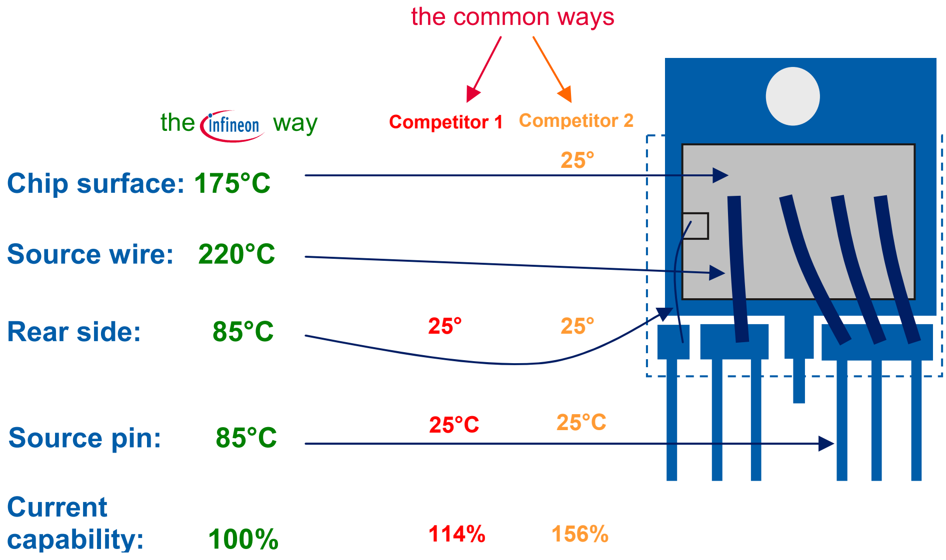

Figure 4 Influence of temperature definition on the current capability of bond wires

It is very important to be aware of the influence of the temperature definition on the bond wire current capability. By simply changing the temperature conditions you could achieve very high current ratings which are unrealistic for any application, as the MOSFET never stays at these low temperatures. Thus, Infineon defines a chip temperature as 175°C and the leadframe (and source pin) temperature as 85°C. Figure 4 shows in green the Infineon way of defining the temperatures used for the current rating. Red and orange colors show the common way to define these temperatures. One way (in red) achieves 14% more current by

defining the leadframe temperature to 25°C and the other way (in orange) achieves 56% more current by defining the chip temperature to 25°C. These definitions can be very dangerous since they do not take into account the realistic application conditions.
When putting the chip and the bond wire's limitation in one diagram the improvement in current capability due to thicker and/or more bond wires in a package can clearly be seen. Figure 5 shows some examples of the current capability vs. single pulse time of a 3.4 mΩ MOSFET (solid lines @85°C and @125°C) and of the bond wires (dotted lines with 2x 500µm, 3x 500µm and 4x500µm) in a TO-263 with ideal cooling. The use of a double stitch increases the current capability of 4x500um bond wires from 160A to 180A. Figure 6 shows the same with a 6.7 mΩ chip (solid lines @85°C and @125°C) and the bond wires (dotted lines with 1x 350µm, 1x 500µm and 2x 500µm) in a TO-252.

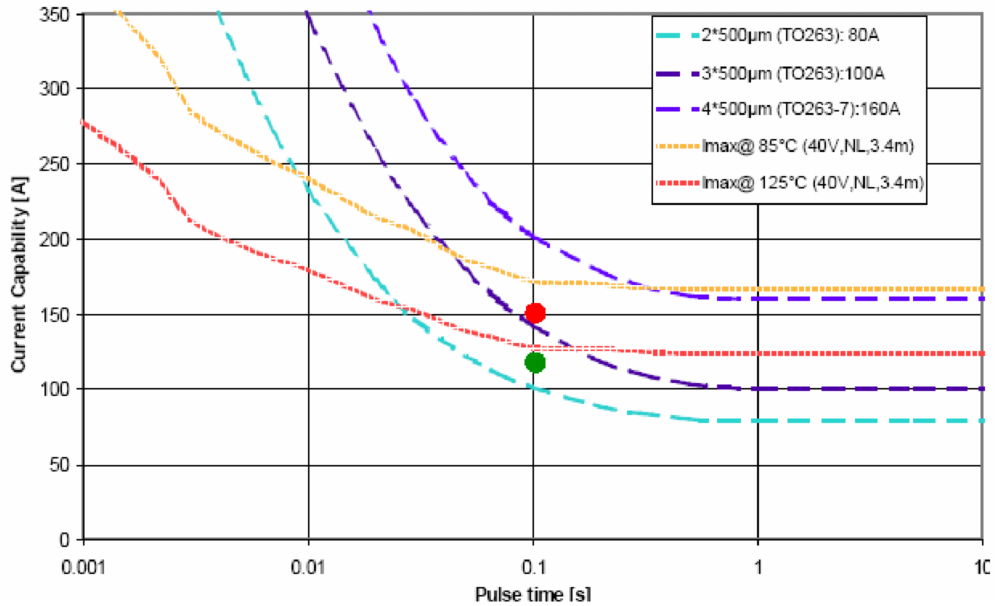

Figure 5 IDS capability vs. single pulse TO-263

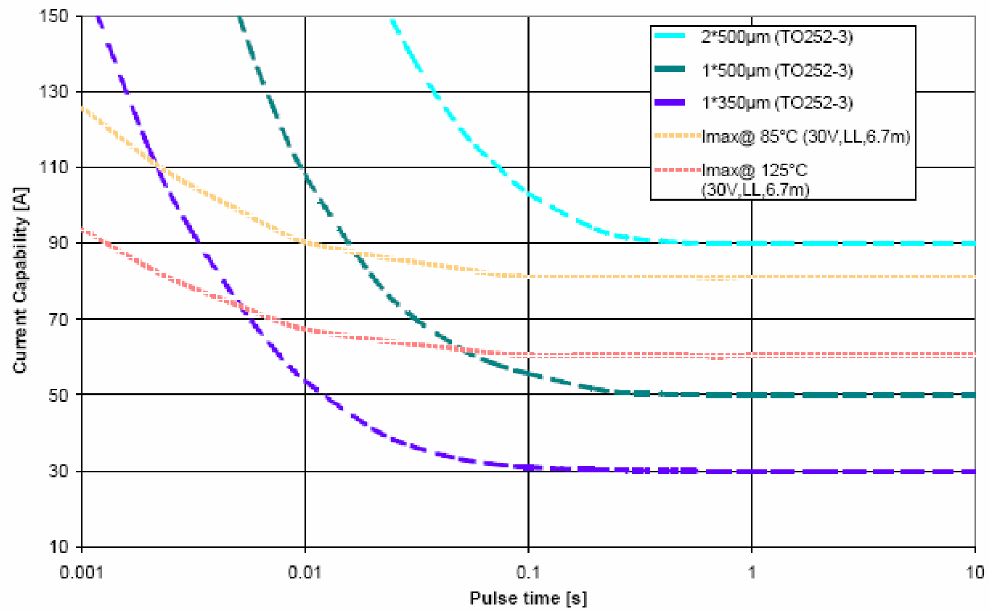

Figure 6 IDS capability vs. single pulse TO-252

4.2.3 Datasheet Current Rating

The datasheet current rating is the minimum value of either bond wire or chip limitation as calculated in both previous paragraphs. For example in the case of the IPB180N04S3-02, the chip current rating is 321A. However, for this part 4x500µm bond wires with double stitch are used, limiting the current to 180A and thus is the DC current rating of this MOSFET 180A.

4.3 Replacing a D2PAK with a DPAK

Up to now, all automotive applications with the drain currents above 50A were reserved for D2PAK. With the second and a third generation of the PowerBond™, a true 90A current capability in a DPAK was reached. Therefore, for the same Rdson (the same chip inside the package) as in D2PAK, it is possible to replace a D2PAK with a DPAK. This brings an enormous advantage to the customers, since the board space which is used can be drastically reduced, leading to less cost and volume of the whole ECU.

Therefore, the full benefit of replacing a D2PAK with a DPAK: the same true current capability with the same Rdson and the needed board space for power MOSFETs is cut in half.

5 How does PowerBond™ Increase the Reliability of Your Application?

In figure 5, the solid lines represent the chip limitation, i.e. the current necessary to increase the case temperature Tc to the maximum junction temperature of 175°C. This means that if for one pulse you are above the limit at a given Tc you will reach a junction temperature over 175°C and thus are out of specification. The same applies for the bonding with the dotted lines. If for a certain pulse length and a given bonding you are above the line you will reach bond temperatures over 220°C.
Consider the green point in figure 5: With a standard bonding of 2x 500µm and a pulse of 0.1s MOSFET can carry up to 100 A. These 100A are the bond limitation as the chip could carry more current. If the application requires 125 A (green point), a bond wires temperature of above 220°C will be reached and therefore the reliability of the MOSFET will be reduced.
Figure 7 shows the bond wire temperature reached for a 100A pulse vs. pulse length. PowerBond™ products will clearly stay at 220°C max. where a standard 80A device will reach wire temperature of 290°C. This temperature could crack the mould compound and would lead to contamination and corrosion of chip and bond wire meaning again dramatic reduced life time.
By taking our PowerBond™ device both the chip and the bond wires stay within their ratings and thus will increase the reliability of the application.
For the 150A pulse (red point) the 4 x 500µm device combined with a 7 pin package should be taken in order not to exceed the maximum temperature. The 180A device in PowerBond™ III technology increases the reliability even further.

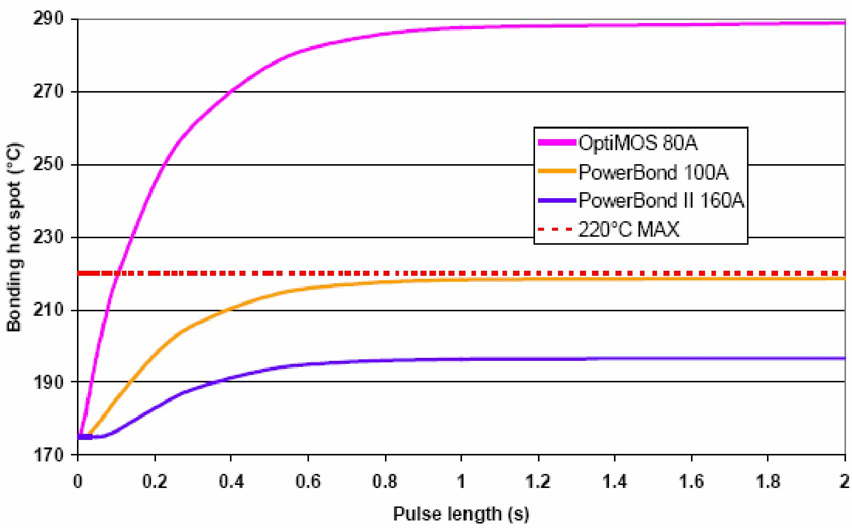

Figure 7 Bond wire temperature for 100A pulse

6 Conclusion

In this Application Note Infineon's PowerBond^{TM} was presented and showed the benefits in terms of lower Rds(on), higher current capability and increased reliability of the application. PowerBond^{TM} has still not reached the end of its development. PowerBond^{TM} III is the solution for applications with even higher current demand in a standard package without having to switch to modules or to larger and more expensive packages. It also permits the ECU designers to gain board space by replacing TO-263 with standard TO-252.

The method of calculation of the current capability of the bond wires, strongly dependent on temperature definition, was also presented. Since there is no standard way of defining and rating the current capability of MOSFET, a great care has to taken when comparing current ratings from different datasheet to be sure to have a realistic comparison.

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