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AP16088

XC16x

EBC timing Tool for XC16x microcontrollers

Microcontrollers

Infineon technologies

Never stop thinking.

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1 Introduction

The EBC Timing Calculation Tool is an Excel based tool, which offers an easy way of evaluation the timing conditions on the bus between an Infineon XC166 microcontroller derivative and an external device (e g an external memory). Just the most essential parameters are viewed and the tool will guide the user in his first determination of the timing capabilities of his design.

It is assumed that the user has the accurate Data Sheets available – for the XC166 device in question as well as for the external devices he or she intend to connect to the microcontroller EBC (External Bus Controller).

The tool has futhermore not the ambition to generate SFR programming code. For such purposes the Infineon Dave Tool can be used.

The main objective is to support the designer's first steps in performance evaluation and optimization of the targetted design.

The way of working with the sheets is *itterative* – in the sense that the user will find out the appropriate clock frequency and parameter conditions by testing different settings 'by his own head' and check for 'acceptance" from the tool. The tool is able to consider all conditions that have to be taken care of – even for an application that is using a mix of different memories with different timing qualities, e g a mix of Flash and SRAM.

Note: This application note cannot cover all relevant topics. It can only give hints for a success EBC Timing Calculation by the aid of the dedicated 'Timing Calc XLS Sheet. The intention of this document is to give a structured guideline on how to handle timing issues and should help to avoid general mistakes.

2 EBC Timing Basics

2.1 The External Bus Controller (EBC)

External accesses are performed by the External Bus Controller (EBC) dynamically, depending on the selected Address Range and chosen Chip Select Line to one of four possible Addressing Modes:

- 16- up to 24-Bit Addresses, 16-Bit data, Demultiplexed (DEMUX)
- 16- up to 24-Bit Addresses, 16-Bit data, Multiplexed (MUX)
- 16- up to 24-Bit Addresses, 8-Bit data, Demultiplexed (DEMUX)
- 16- up to 24-Bit Addresses, 8-Bit data, Multiplexed (MUX)

2.2 Basic Timing Principles (simplified)

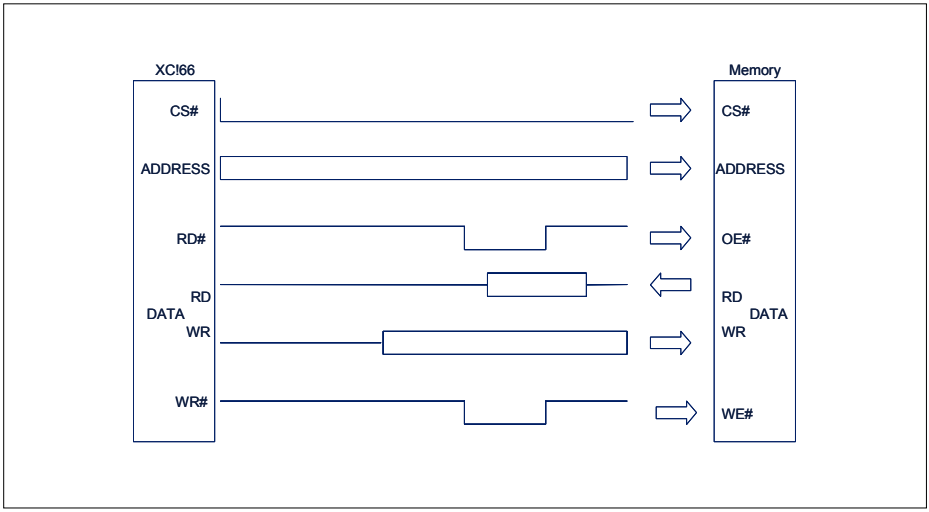


Figure 1 The basic, Intel style DEMUX protocol to External Memory

CS#	Chip Select (Active Low)
ADDRESS	Address Bus (16..24 Bit), see above
RD#	Read strobe (Active Low) for every read access.
DATA	Data Bus (8-/16-Bit)
WR#	Write strobe (Active Low) for every write access

ALE Address Latch Enable for MUX access (is not shown here)

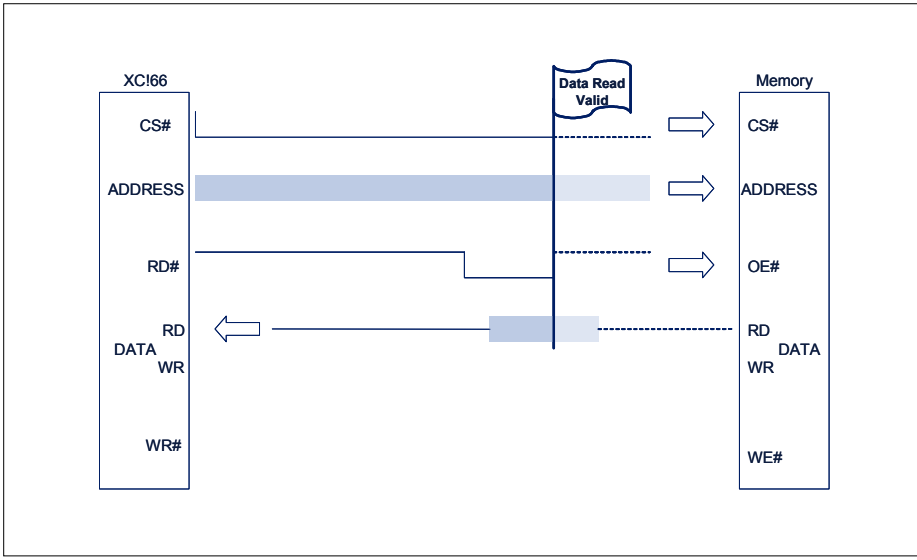


Figure 2 Example: Read Cycle – Data Read Valid

Read Command is performed by the internal Master Clock ($\mathbf{f_{CM}}$) at that edge by which it ends the Read Strobe (RD#) output signal.

2.3 XC166 Basic Bus Cycle Protocols

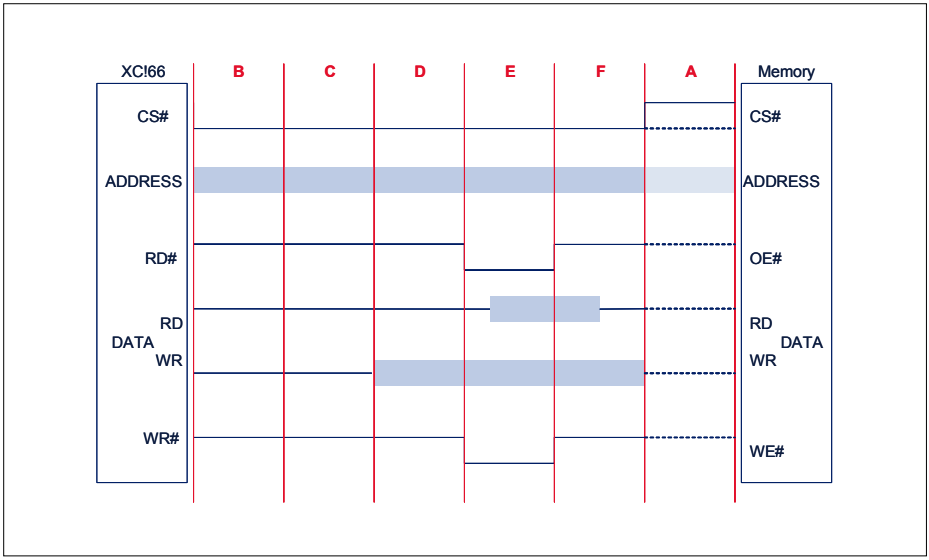


Figure 3 The XC166 External Bus Timing Phases (A-F)

The external bus timing of the XC166 devices consists of 6 Phases (A to F), which in turn are derived from the Master Clock (f_{MC}) in time slot lengths of 0 TCM up to individually programmable lengths of TCM (TCM=Master Clock Period). By these means the designer can adjust lengths and positions of the wait states in each Bus Cycle Protocol appropriately to the timing characteristics of the external devices in his application.

Phase A is only used to tri-state the output bus drivers during a chip select switch - to ensure that no conflicts will occur on the data bus lines by the data from a previously addressed device before any next device is accessed! From the 'next device' point of view the Phase A is the *first phase* of its bus cycle – and the addressing lines $A_{23..0}$, $CS#_n$, BHE# etc (depending on design) will go active at the beginning of its phase A.

However, Phase A has to be regarded as the *last phase* in a bus cycle when calculating the time width – because the calculation is depending on the timing parameters of the device that was accessed before a chip select switch! (See next figure).

2.4 XC166 Principle of Bus Cycle Wait States Distribution

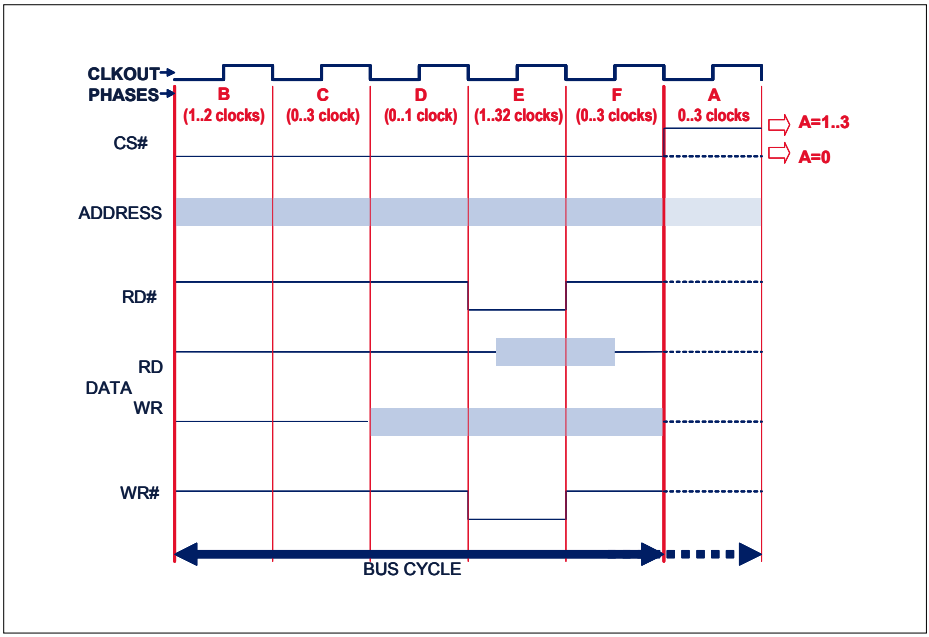


Figure 4 Clock Out (CLKOUT) and adjustable lengths of the phases A..F.

A phase: Addresses valid, (ALE high),
no Command. CS switch (tri-state wait states)

B phase: Addresses valid, (ALE high),
no Command. ALE length

C phase: Addresses valid, (ALE low),
no Command. R/W delay

D phase: Write data valid, (ALE low),.
no Command, Data valid for Write cycles

E phase: Command (read or write) active. Access time

F phase: Command inactive, Address hold.
Read data tristate time,
Write data hold time

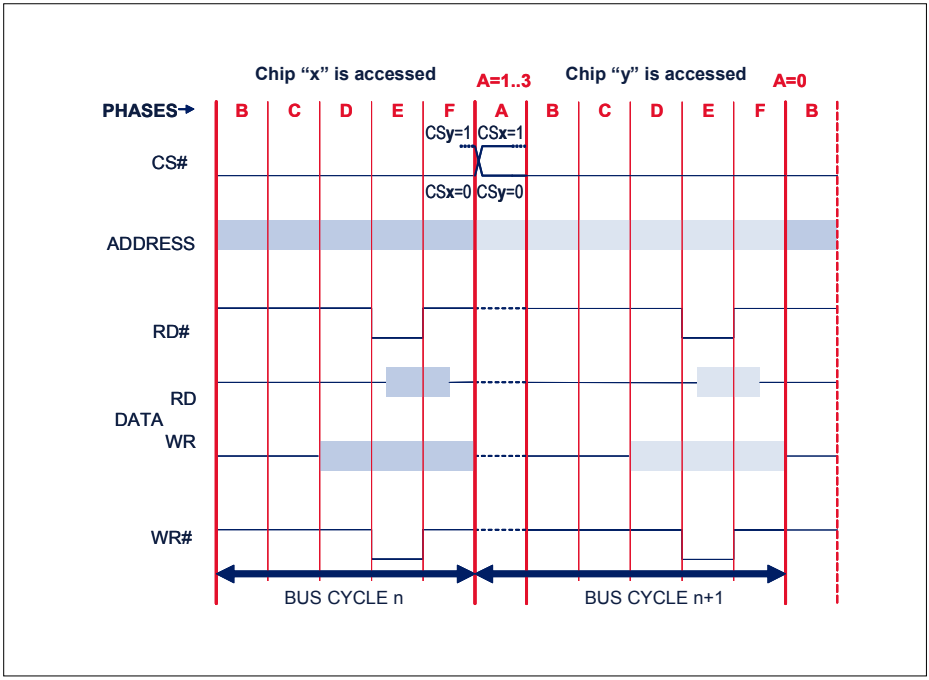


Figure 5 Demo example showing implementation of Phase A at a CS switch.

3 Timing Calculations Using DEMUX mode

The time base for all AC characteristics in the XC166 EBC system and control buses are not referred to the internal CPU Clock but to the Clock Output signal (**CLKOUT**), which makes test measurements with externally connected analyzers adequate.

Clock Out (**CLKOUT**) is derived form the internal Master Clock (f_{MC}), so the period length of CLKOUT is = 1 TCM. That defines the resolution in positioning and length setting of wait states in the Bus Cycle Protocol.

3.1 Access Times and Delays in DEMUX Mode (Ideal case)

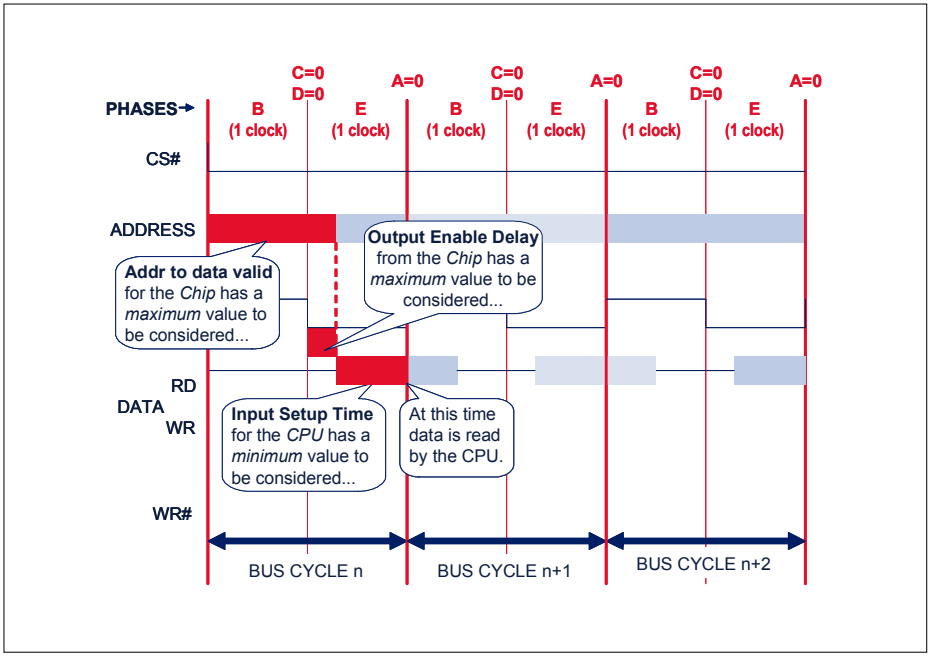


Figure 6 Address Access and Data Read Delays

3.1.1 Address Valid to Data Output Valid Delay

There's a certain time the address has to be hold valid by the CPU before the external device recognizes the address. This time parameter ($\mathbf{t}_{acc}$) is specified by the data sheet of the external device.

3.1.2 Output Enable to Output Data Valid Delay

There's a certain time the read strobe has to be hold active (low) by the CPU before the external device will recognize the read command and deliver the data on the bus. This delay (t_{oe}) is specified by the data sheet of the external device.

3.1.3 Input Setup Time Delay

There's a certain time the data has to be hold valid by the external device before the CPU is prepared to recognize the data by its read command. This delay (tc_{30}) is specified by the data sheet of the CPU.

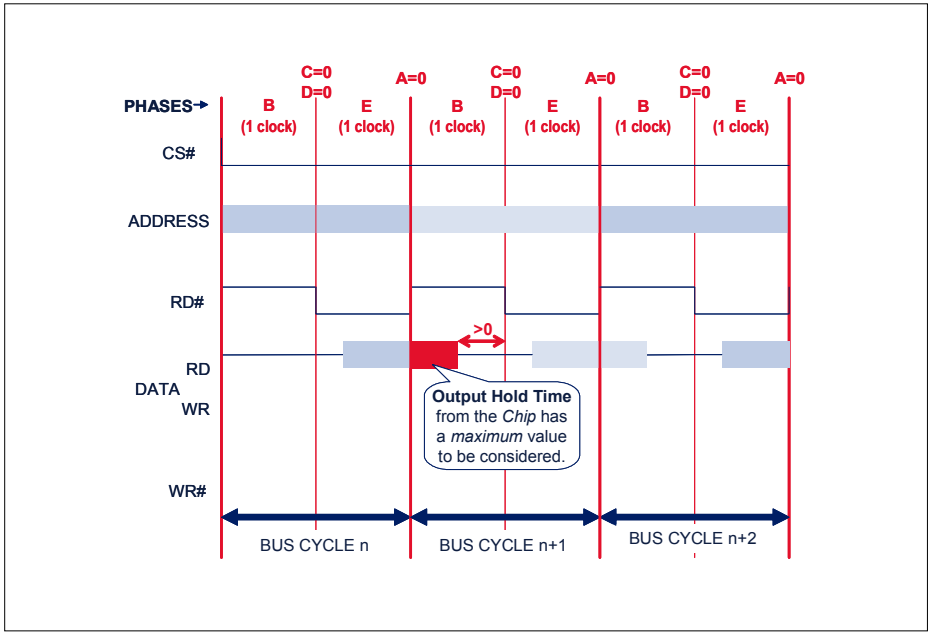


Figure 7 Output Hold Time to Tristate Delay by the External Device.

3.1.4 Output Hold Time Delay

There's a certain time (t_{hoz}) the external device will need to tristate its data output drivers after the the disable command from the read strobe. This delay is specified by the data sheet of the external device.

3.2 Access Times and Delays in DEMUX Mode (Real case)

In the real case even the *rise* and *fall* times for all signal level shifts within the bus protocol have to be taken into account when calculating the timings on the bus lines..

In addition to that even the jitter caused by the PLL, if used, has to be considered!

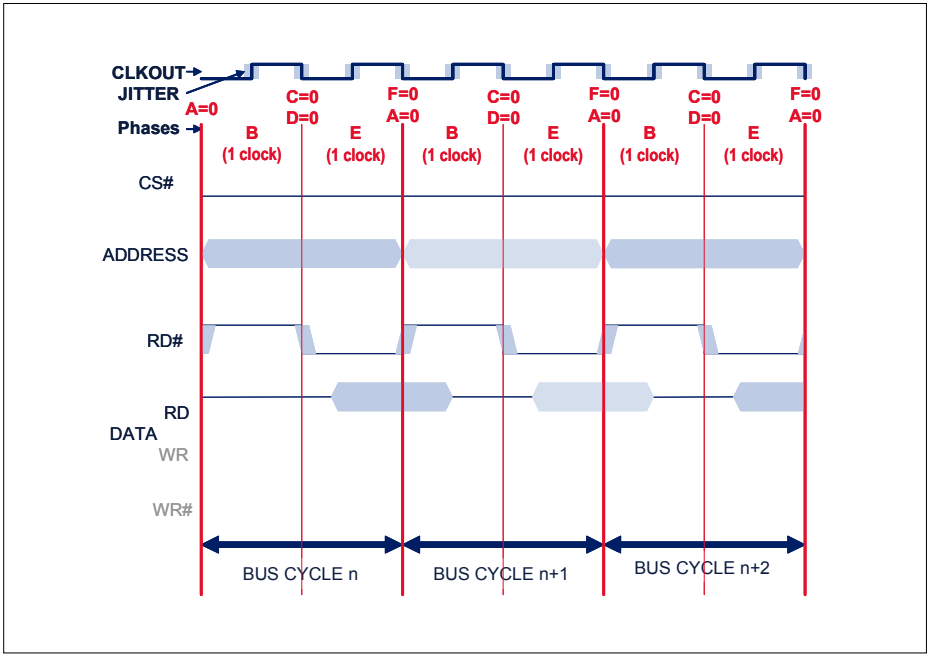


Figure 8 Impact on Timings by Rise and Fall Times and Jitter (if PLL is used).

The jitter amplitude [in ns] can be of the same magnitude as the AC parameters! Jitter is normally irrelevant for longer time periods, say around 100 master clock periods or more – but for a few periods, as is the case within the Bus Cycle, jitter may have significance.

Note: Read Users Manual chapter "PLL Operation" or in the Data Sheet chapter about "Timing Parameters" and the section "Phase Locked Loop (PLL)"!

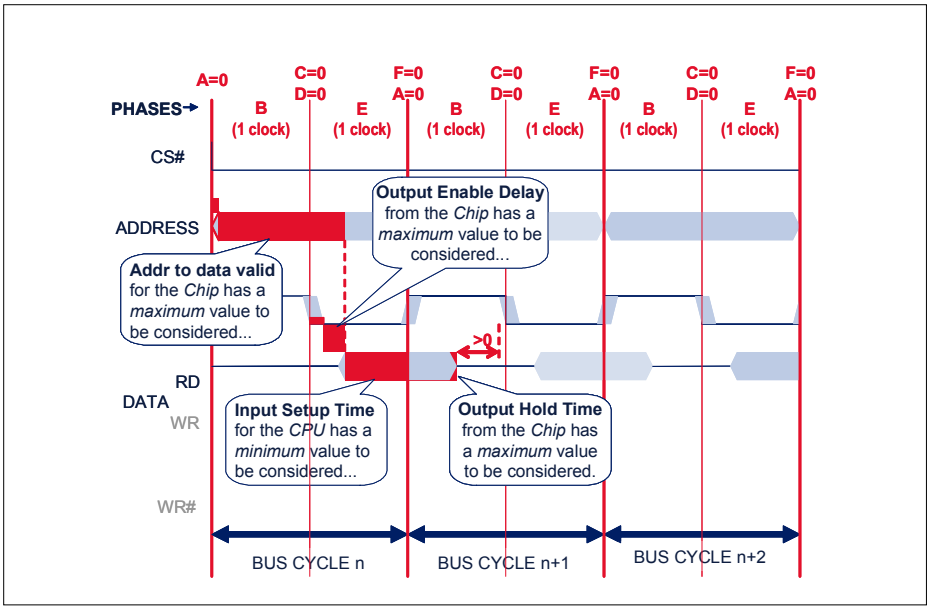


Figure 9 Timing in DEMUX Mode when considering all AC components

3.3 Access and Delay Calculations in DEMUX Mode

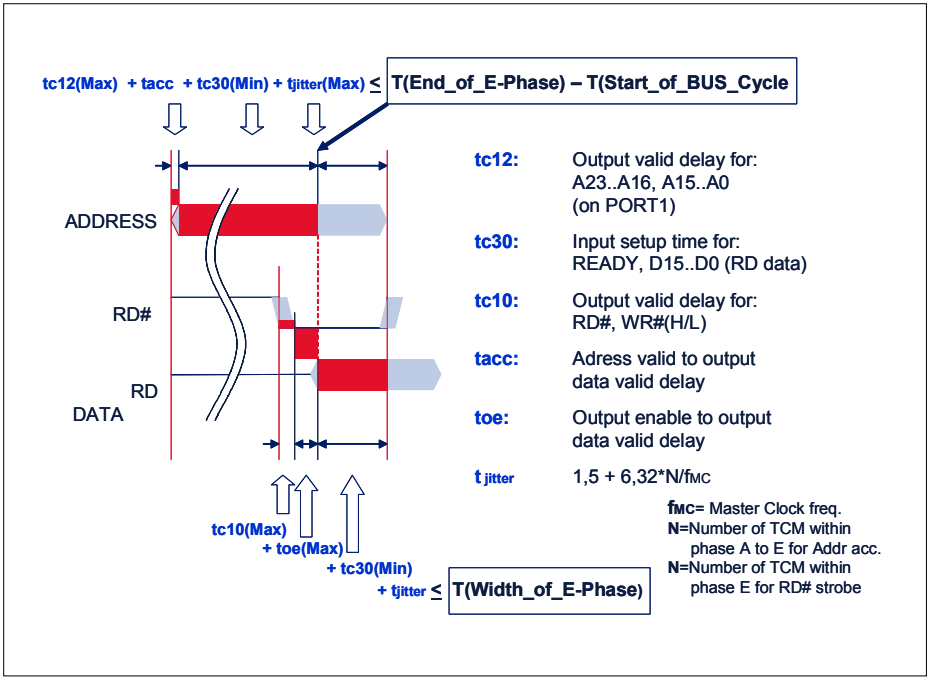


Figure 10 Access and Delay formulas for DEMUX Mode timing calculations

4 The EBC Timing Calculation Tool

The EBC Timing Calculation Tool is an XLS-sheet, which offers an easy way of evalution the timing conditions on the bus between an XC166 derivative and the external device. Just the most essential parameters are viewed and the tool will guide the user in his first determination of the timing capabilities of his design.

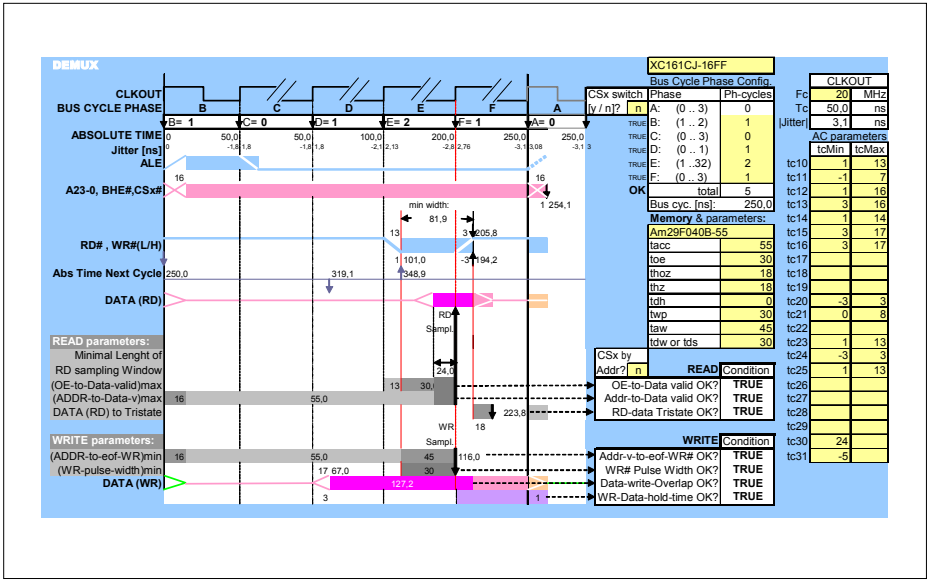


Figure 11 Sheet Layout for Timing Calculations in DEMUX Mode.

There's one worksheet for applications working in DEMUX (Demultiplex) Mode and another one that can deal with MUX (Multiplex) Mode is a similar way.

4.1 How to work with the Timing Calculation Tool

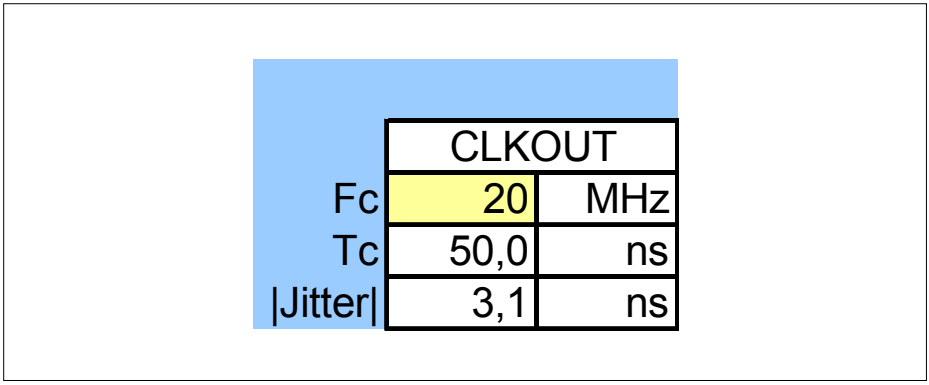
You will have to type in all the essential data into the Sheet Input Data boxes, as for example Clock Out frequency, CS switch condition, Phase lenghts and AC parameters of all the devices.

Note: You can only manipulate cells with yellow bottom color!

Output data is comments such as *'TRUE', 'FALSE', 'OK', 'NOT OK'* reflecting how successful you have been in your approach of setting the data in the input data boxes.

4.2 Sheet Input Data

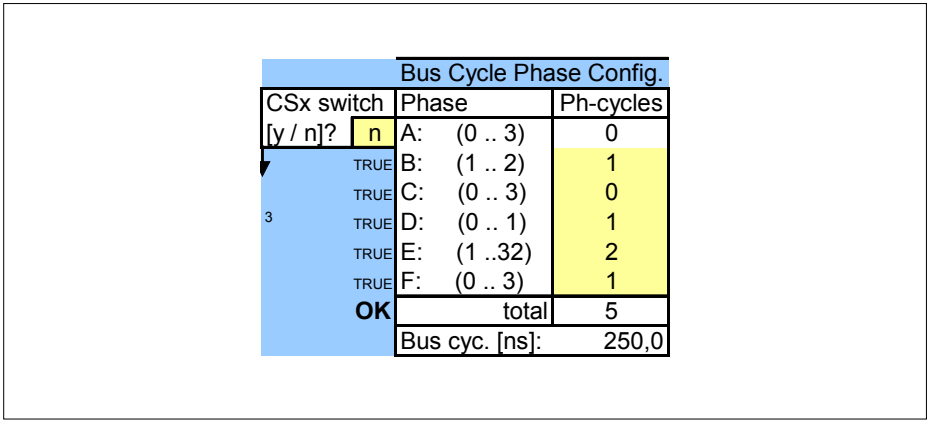
- Fill in Clock Out Frequency (**CLKOUT**), which is equal to the internal Master Clock.



	CLKOUT	
Fc	20	MHz
Tc	50,0	ns
|Jitter|	3,1	ns

Figure 12 Where you put in CLKOUT frequency

- Fill in all the **Phase B..F** values, which will set the respective number of Master Clock periods (TCM) for each phase. The values have to be within the respective ranges that are hinted within brackets for each phase. Extending any range will be indicated with a “FALSE” sign and a “NOT OK” sign for the total bus cycle length.
- **Phase A=0** and can not be filled in by the user. It will be calculated by the sheet automatically, if the user wants that a Chip Select switch should be considered. This mode can be selected by filling in “y” (=yes). Default is “n” (=”no”).



		Bus Cycle Phase Config.	
CSx switch [y / n]?	n	Phase	Ph-cycles
	TRUE	A: (0 .. 3)	0
	TRUE	B: (1 .. 2)	1
	TRUE	C: (0 .. 3)	0
3	TRUE	D: (0 .. 1)	1
	TRUE	E: (1 ..32)	2
	TRUE	F: (0 .. 3)	1
	OK	total	5
		Bus cyc. [ns]:	250,0

Figure 13 Where you put in the Phase lengths

- Fill in the relevant **AC Parameters** of the **External Device** (e g Memory)

Memory & parameters:	
Am29F040B-55	
tacc	55
toe	30
thoz	18
thz	18
tdh	0
twp	30
taw	45
tdw or tds	30

Figure 14 Where you put in External Device AC Parameters

Fill in the relevant **AC Parameters** of the **XC166 derivative** (e g XC161CJ-16FF)

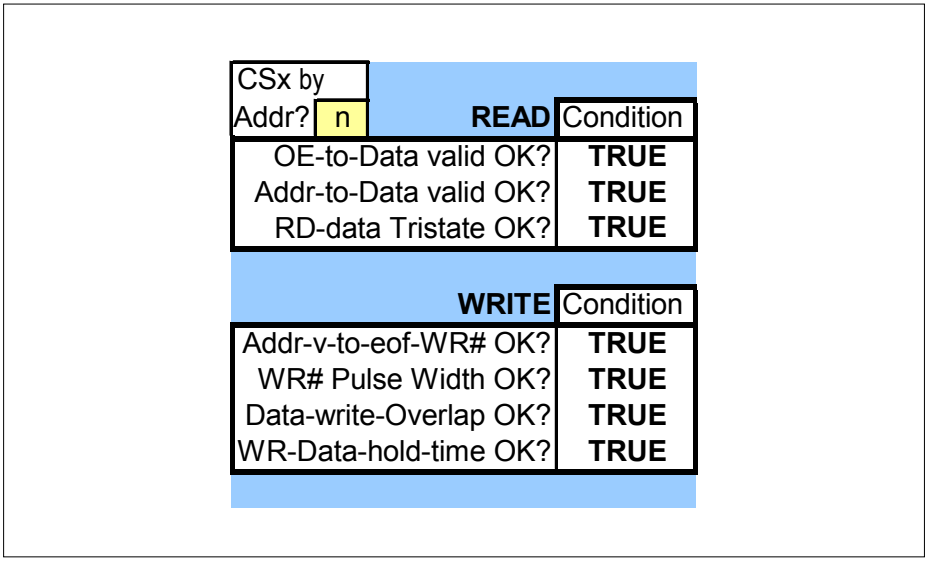
	AC parameters	
	tcMin	tcMax
tc10	1	13
tc11	-1	7
tc12	1	16
tc13	3	16
tc14	1	14
tc15	3	17
tc16	3	17
tc17		
tc18		
tc19		
tc20	-3	3
tc21	0	8
tc22		
tc23	1	13
tc24	-3	3
tc25	1	13
tc26		
tc27		
tc28		
tc29		
tc30	24	
tc31	-5	

Figure 15 Where you put in Microcontroller AC Parameters

All parameters listed in the XLS worksheet are explained by comments in the respective cells – but can also, of course, be found and clarified in the Data Sheets.

4.3 Sheet Output Data

In the Outpot Box of the XLS Sheet, the success from setting up the the different timing conditions in the Sheet Input Data boxes is disclosed by simple ‘TRUE’ or ‘FALSE’ statements.



CSx by Addr?	n	READ	Condition
OE-to-Data valid OK?			TRUE
Addr-to-Data valid OK?			TRUE
RD-data Tristate OK?			TRUE

WRITE	Condition
Addr-v-to-eof-WR# OK?	TRUE
WR# Pulse Width OK?	TRUE
Data-write-Overlap OK?	TRUE
WR-Data-hold-time OK?	TRUE

Figure 16 Output Data

Note that even an additional option can to be found in the Sheet Ouput Box; namely using an Address Line as Chip Select line in the user application! If the user has implemented such an opportunity, he should mark this condition by writing “y” (=yes) where this question appears in the output box. (Default setting is “n” (=no).

5 Using MUX mode

The worksheet for MUX Mode timing evaluations looks quite similar to the one for the DEMUX mode – except for the AC parameter for the Adress Latch that is used to store the Low Address during each bus cycle (and the ALE strobe AC parameters, of course)

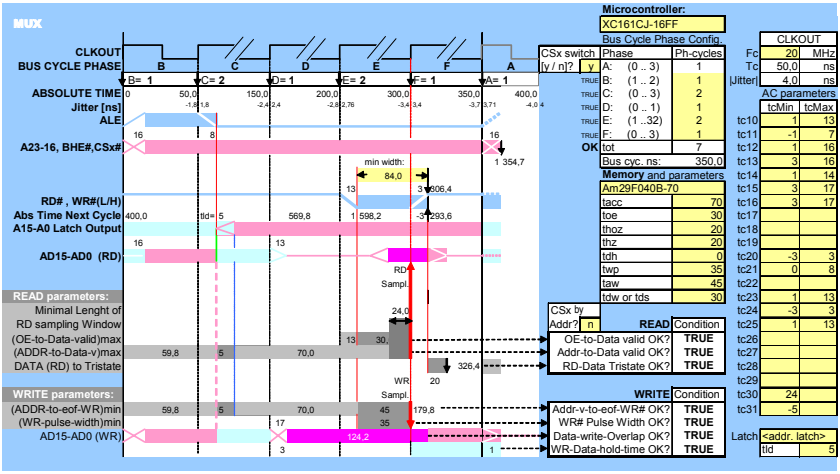


Figure 17 Sheet Layout for Timing Calculations in MUX Mode.

5.1 Sheet input Data

- Fill in accordingly to the description shown for the DEMUX Mode
- Fill in appropriate **ALE length** by the number of Clock Cycles for **Phase B**
- Fill in Address Latch Output Valid Delay (t_{ld})

5.2 Sheet Output Data

The success from setting all relevant input data is shown by ‘TRUE’ or ‘FALSE’ in the Sheet Output Box (similar to the description for the DEMUX Mode).

6 Last words…

Note: All documents like datasheets, user's manuals or addendums for the selected device should be crosschecked in all aspects regarding new functions or deviations to former versions and the latest documents should always be used.

The latest XC16x related documents can be found by the following link:

http://www.infineon.com/XC166-Family

In case for any reason this link does not work you can find such information by the links:

Infineon home page: http://www.infineon.com

Infineon microcontroller home page: http://www.infineon.com/microcontrollers

http://www.infineon.com

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