Infineon

Product Info Package V1.0

AUDO-NG TC1762

Never stop thinking.

Fast. Innovative. TriCore.
AUDO Next Generation TC1762

+ **Extension** of the award winning AUDO Architecture
+ **40-60MHz** high performance 32-bit TriCore™
+ **1 MByte** embedded Flash
+ **52 KByte** SRAM
+ **Triple Bus Structure**
+ **Saving efforts**
  in software and system costs
+ **Speeding up**
  software development with
  complete toolchain
+ **Ground-breaking** peripherals e.g.
  MSC: save I/O pins = system costs
  FADC: waive external DSP ASICs
  GPTA: realize scalable eMotor control
  MLI: build up multi processor systems
  and eliminate expensive DPRAM

Never stop thinking.

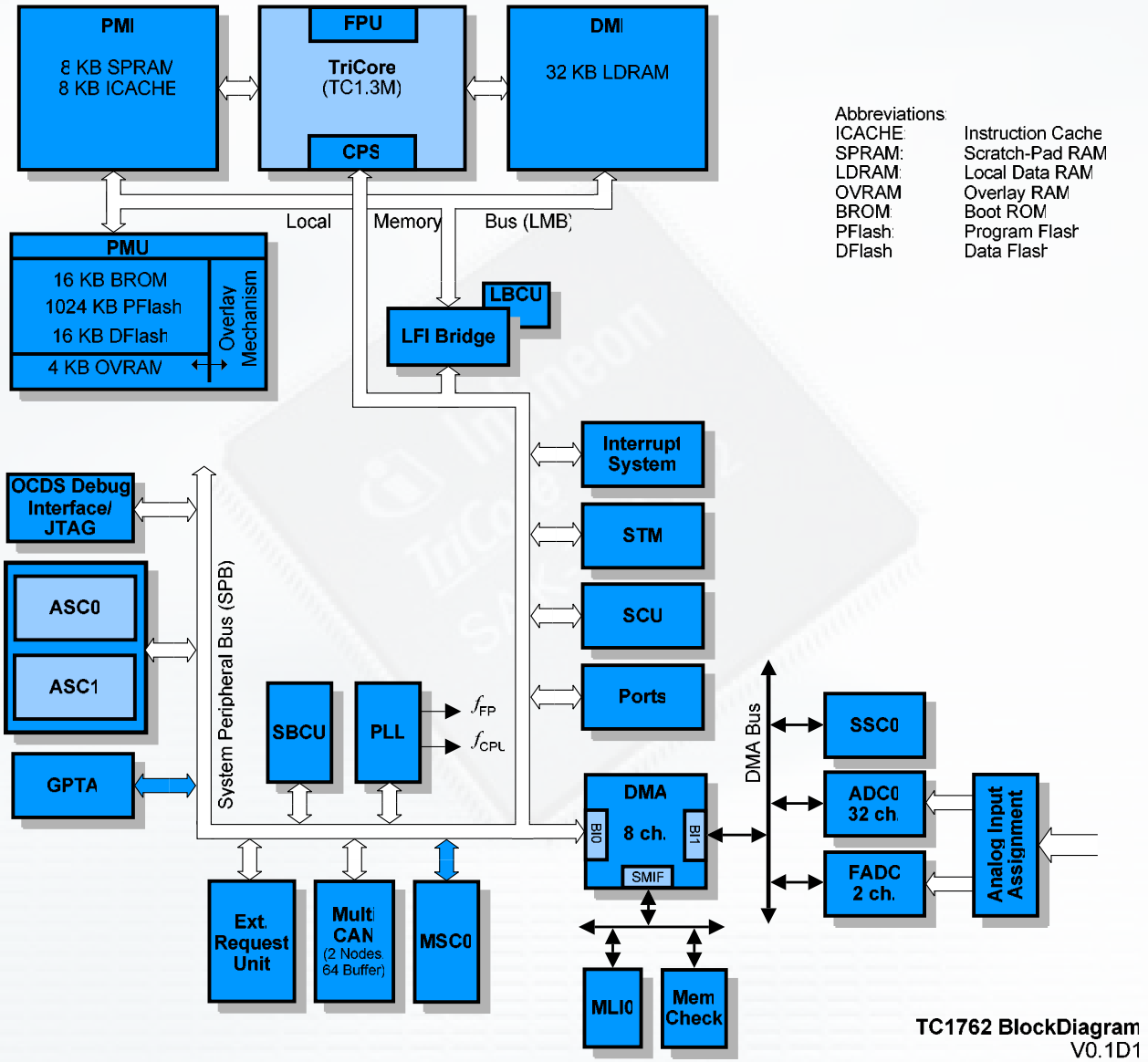
AUDO Next Generation TC1762
Info Package Overview

Content

- TC1762 – at first sight
- Block Diagram
- Feature Overview

- misc. 'going into detail..'
  - Core Concept
  - Code Size
  - Key Peripherals
  - Tool Support

AUDO Next Generation TC1762
Block Diagram



AUDO Next Generation TC1762
Feature Overview (1/5)

- **High Performance 32-Bit CPU**
  - 32-bit architecture with 4 GBytes unified data, program, and input/output address space
  - Fast automatic context-switch
  - Multiply-accumulate unit
  - Single-precision Floating point unit
  - Saturating integer arithmetic
  - High performance on-chip peripheral bus (FPI Bus)
  - Register based design with multiple variable register banks
  - Bit handling
  - Packed data operations
  - Zero overhead loop
  - Precise exceptions
  - Flexible power management

- **Instruction Set with High Efficiency**
  - 16/32-bit instructions for reduced code size
  - Data types include: Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double word integers, and IEEE-754 single precision floating-point
  - Data formats include: Bit, 8-bit byte, 16-bit half word, 32-bit word, and 64-bit double word data formats
  - Powerful instruction set
  - Flexible and efficient addressing mode for high code density

AUDO Next Generation TC1762
Feature Overview (2/5)

- **Integrated On-Chip Memories**
  - Code memory:
    - 1 MByte on-chip Program Flash (PFLASH)
    - 8 KByte Scratch-pad RAM (SPRAM)
    - 8 KByte Instruction Cache (ICACHE)
    - 16 KByte Boot ROM (BROM)
  - Data memory
    - 32 KByte Data Memory (SRAM)
    - 4 kByte Overlay Memory (OVRAM)
    - 16 KByte on-chip Data Flash (DFLASH)

AUDO Next Generation TC1762
Feature Overview (3/5)

- **Interrupt System**
  - In total 85 Service Request Nodes (SRNs)
  - Flexible interrupt prioritizing scheme with 256 interrupt priority levels
  - Fast interrupt response
  - Service requests are serviced by CPU

AUDO Next Generation TC1762
Feature Overview (4/5)

- **DMA Controller**
  - 8 independent DMA channels
  - Programmable priority of the DMA sub-blocks on the bus interfaces
  - Buffer capability for move actions on the buses (min. 1 move per bus is buffered).
  - Individually programmable operation modes for each DMA channel
  - Full 32-bit addressing capability of each DMA channel
  - Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
  - Micro Link bus interface support
  - One register set for each DMA channel
  - Flexible interrupt generation
  - DMA Controller operates as bus bridge between System Peripheral Bus and DMA Bus

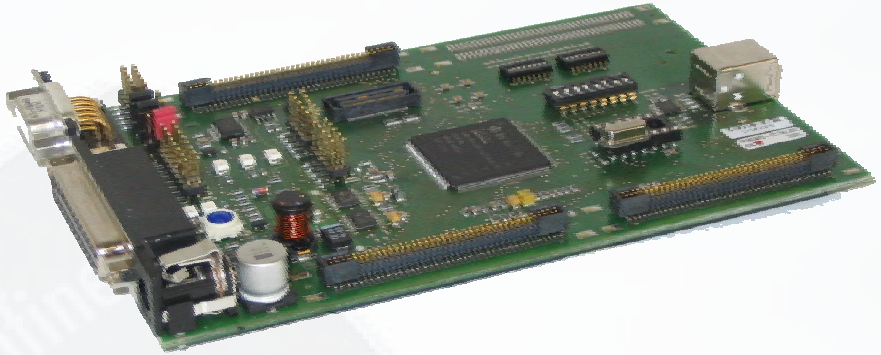
- **Parallel I/O Ports**
  - 81 digital general purpose input/output (GPIO) port lines
  - Input/output functionality individually programmable for each port line
  - Programmable input characteristics (pull-up, pull-down, no pull device)
  - Programmable output driver strength for EMI minimization (weak, medium, strong)
  - Programmable output characteristics (push-pull, open drain)
  - Programmable alternate output functions
  - Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

AUDO Next Generation TC1762
Feature Overview (5/5)

- **On-chip Peripheral Units**
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud-rate generator, parity, framing and overrun error detection
  - One Synchronous Serial Channel (SSC) with programmable data length and shift direction
  - One Micro Second Channel Interface (MSC) for serial communication
  - One CAN Module with two CAN nodes (MultiCAN) for high efficiency data handling via FIFO buffering and gateway data transfer
  - One Micro Link Serial Bus Interfaces (MLI) for inter-processor communication
  - One General Purpose Timer Array (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One medium speed Analog-to-Digital Converter Unit (ADC) with 8-bit, 10-bit, or 12-bit resolution and sixteen analog input each
  - One fast Analog-to-Digital Converter Unit (FADC)
- **Package**
  - LQFP-176 package, 0,5 mm pitch
- **Clock Frequencies**
  - Maximum CPU Clock Frequency: 40-60MHz
  - Maximum System Clock Frequency: 40-60MHz
- **Temperature Rnage**
  - Ambient temperature: -40 ° to +125 °C

AUDO Next Generation TC1762
Starter Kit Details

- **Infineon TC1762 Starter Kit includes:**
  - TC1762 TriBoard
  - StarterKit CD with all device and board information as PDF as well Getting Started Software and a Hands-On-Training for self-study
  - DAvE (e.g. for generating peripheral initialization code)
  - Demo CD of third party compiler and debugger vendors
  - GNU C-Compiler full version
  - Parallel cable for direct connection to the PCs LPT interface
  - Extension Board for easy measurement of HW signals with a scope or a logic-analyzer



TC176x Starterkit

- **Order Information:** www.infineon.com/mc-starterkits
  - Order Number:

    TC176x B158-H8539-G1-0-7600

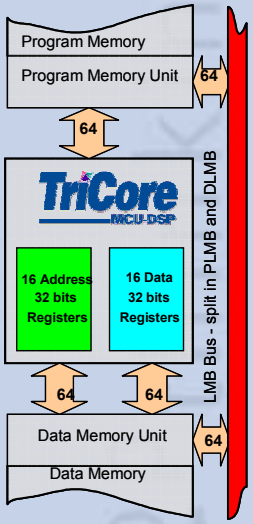
Infineon

going into detail..

TC1762 – Core Concept

Never stop thinking.

AUDO-NG – Outperforming Core Concept
TriCore Architecture – Key Features and Benefits (1/2)



Combining the the best of three worlds: RISC (MCU), DSP and µ-Controller together in a single core - TriCore offers maximum system performance for embedded real-time applications

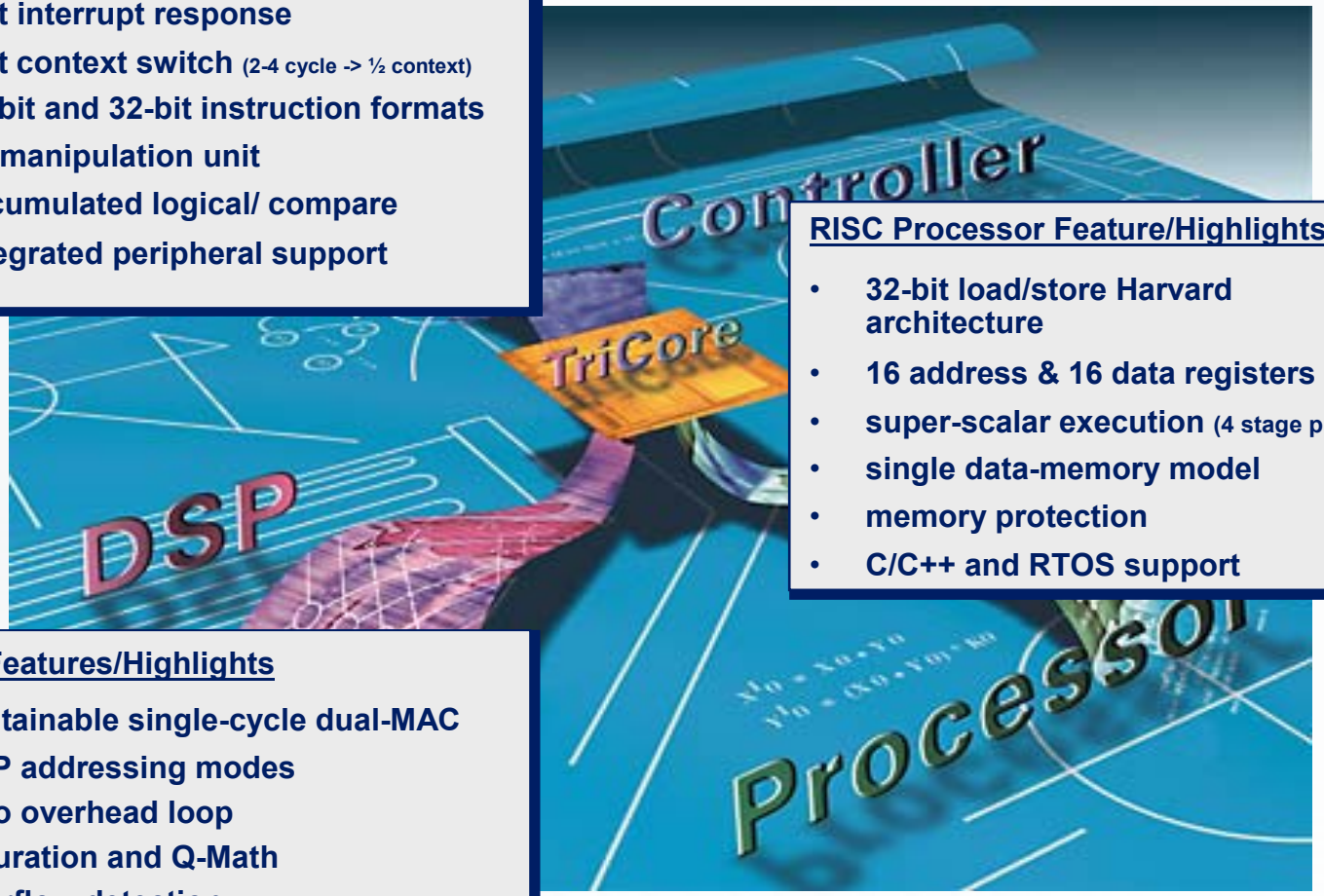
Key Features	Key Benefits
■ **High Performance 32-bit TriCore CPU** (TC v1.3) with 4-stage pipeline and triple issue super-scalar implementation (f_{CPU} = 40-60MHz) *	■ Optimized chip-size to performance ratio for real-time critical embedded systems.
■ **Register sets** – 2x16 address/data 32 bits registers – Switch upper shadowed half context in 2/4 cycles (the lower half in 4 cycles)	
■ **Local Memory Bus (LMB)** – 64 bits data – separated busses used for program and data (PLMB and DLMB)	■ Separated instruction and data busses speed up the system performance due avoided arbitration conflict on a common bus
■ **mixed 16/32 bit instruction format**	■ compressed Code-Density optimized for embedded FLASH memory usage

* referring to TC1762

The Infineon 32-bit TriCore

Microcontroller Features/Highlights

- fast interrupt response
- fast context switch (2-4 cycle -> ½ context)
- 16-bit and 32-bit instruction formats
- bit manipulation unit
- accumulated logical/ compare
- integrated peripheral support



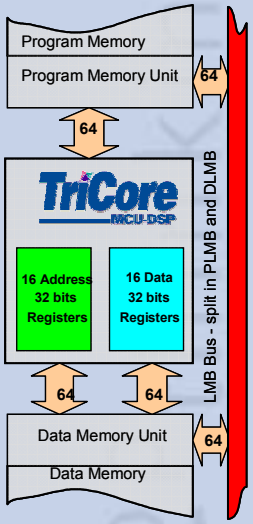
RISC Processor Feature/Highlights

- 32-bit load/store Harvard architecture
- 16 address & 16 data registers
- super-scalar execution (4 stage pipeline)
- single data-memory model
- memory protection
- C/C++ and RTOS support

DSP Features/Highlights

- sustainable single-cycle dual-MAC
- DSP addressing modes
- zero overhead loop
- saturation and Q-Math
- overflow detection
- rounding

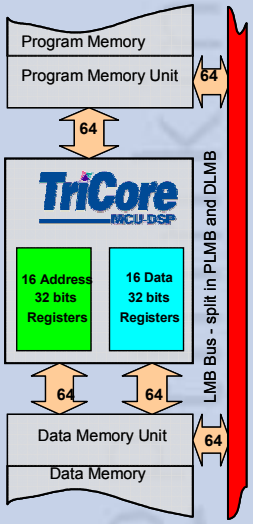
AUDO-NG – Outperforming Core Concept
TriCore Architecture – Key Features and Benefits (1/2)



Combining the the best of three worlds: RISC (MCU), DSP and µ-Controller together in a single core - TriCore offers maximum system performance for embedded real-time applications

Key Features	Key Benefits
■ **High Performance 32-bit TriCore CPU** (TC v1.3) with 4-stage pipeline and triple issue super-scalar implementation (f_{CPU} = 40-60MHz) ■ **Register sets** – 2x16 address/data 32 bits registers – Switch upper shadowed half context in 2/4 cycles (the lower half in 4 cycles)	■ Optimized chip-size to performance ratio for real-time critical embedded systems.
■ **Local Memory Bus (LMB)** – 64 bits data – separated busses used for program and data (PLMB and DLMB)	■ Separated instruction and data busses speed up the system performance due avoided arbitration conflict on a common bus
■ **mixed 16/32 bit instruction format**	■ compressed Code-Density optimized for embedded FLASH memory usage

AUDO-NG – Outperforming Core Concept
TriCore Architecture – Key Features and Benefits (2/2)



Key Features

Key Benefits

- **Interrupt System**
  - Flexible multi-master interrupt system (interrupts serviced by CPU or DMA)
  - Hardware controlled context switch
  - Hardware Interrupt Priority arbitration with 255 priority levels
  - very fast interrupt response time resp. **< 250 ns** @ 40-60MHz)

- sophisticated interrupt system with up to 255 HW arbitrated sources and very fast response times is optimized for realtime sensitive embedded applications

- **powerful MAC unit** supports circular buffer, No data overflow faults due to saturating arithmetic and bit-reverse addressing modes for DSP algorithms

- given scalability approach due to MCU and DSP function merged in one core. Only one tool set for development and emulation

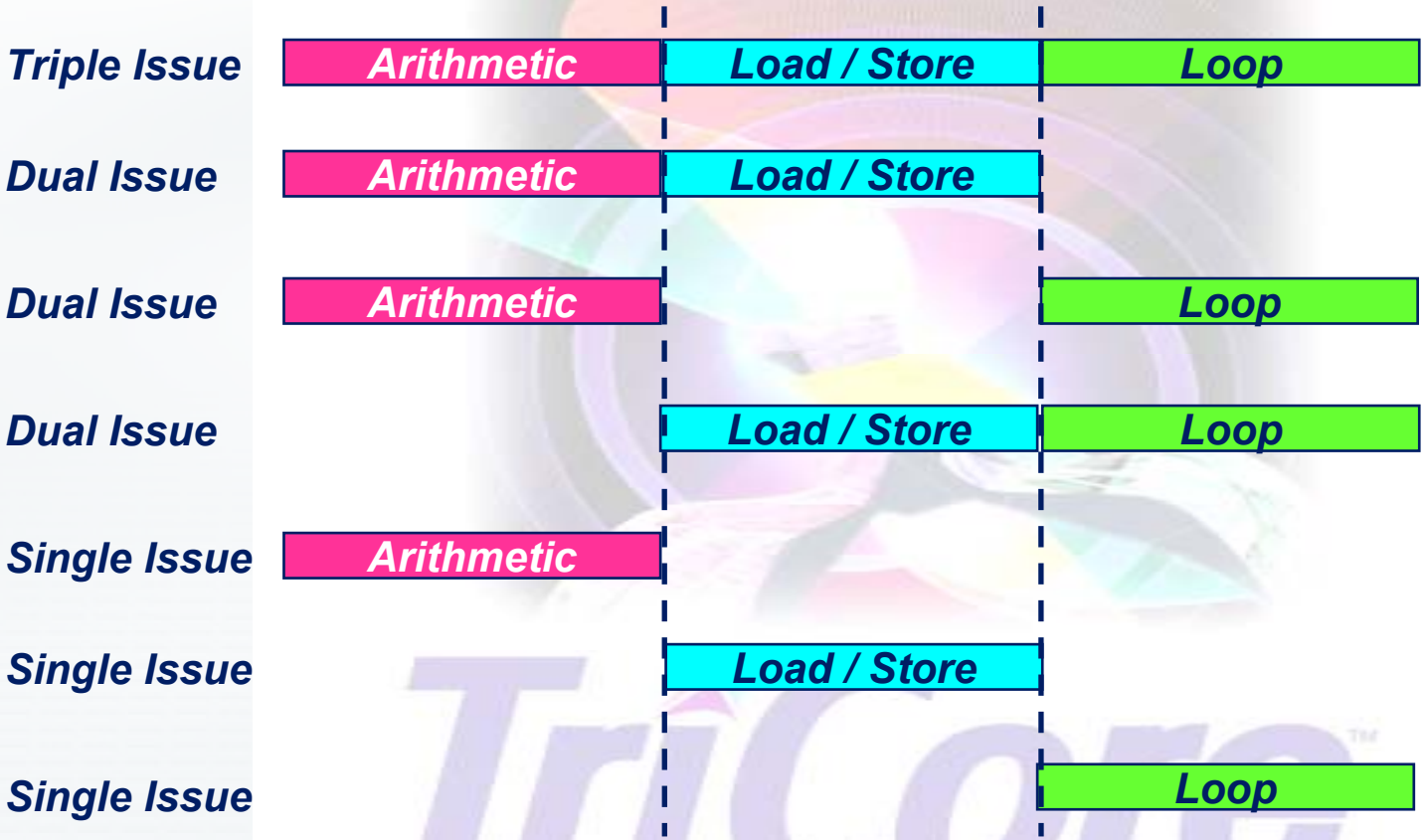
- **single precision Floating Point Unit** (FPU) with integrated interrupt capability for exception handling

- tightly coupled coprocessor FPU support with single precision IEEE-754 data format compromises acceptable physical precision demands with increased real time behaviour (unaltered fast 2 cycle context switch) and reduced storage memory for FPU variables

TriCore Architecture –
Super-scalar Execution

Triple / Dual / Single Issue

~1.3 instr/cycle



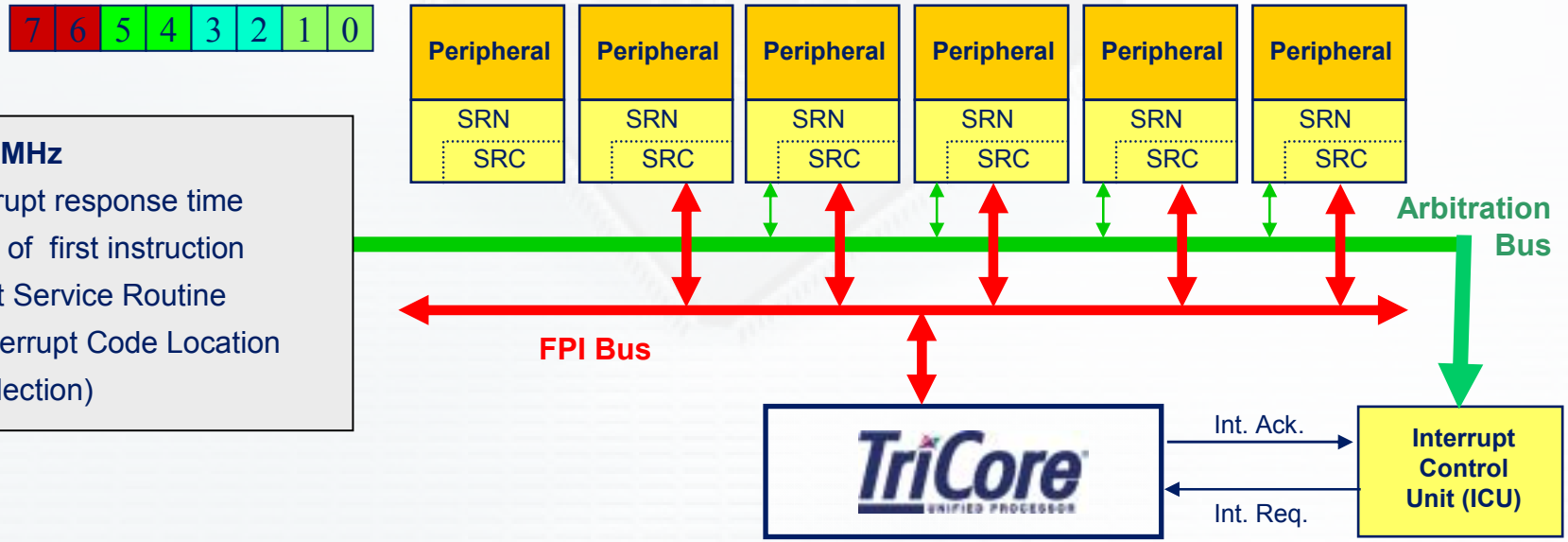
TriCore Architecture –
Powerful Interrupt Service System

Features

- Up to 4 x 255 request nodes (SRN), concurrently supported
- Parallel Arbiter HW to select highest interrupt & clear when accepted
- Automatic context save during branch to interrupt routine
- Interrupt table - no jumps needed

Benefits

- Meets real-time requirements
- Zero Software overhead
- Ease of programming, High flexibility
- Large Number of SRNs
- Flexible grouping of request into priority groups

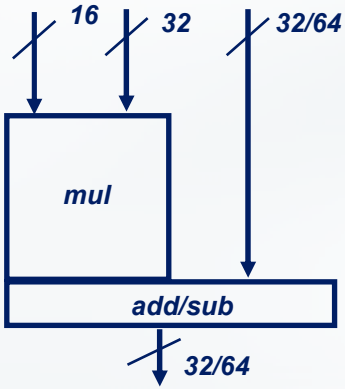


TC1762 @ 40-60MHz

- **< 250 ns** interrupt response time until execution of first instruction within Interrupt Service Routine (depending Interrupt Code Location and priority selection)

TriCore Architecture –
DSP Some Results

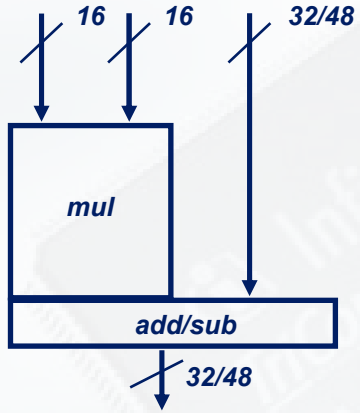
MUL MADD MSUB
32 +/- 16x32
64 +/- 16x32



Choice of register half
Left-alignment
*8000*8000 -> 7FFF FFFF*
Rounding
Sat

thru-put = 1 cycle

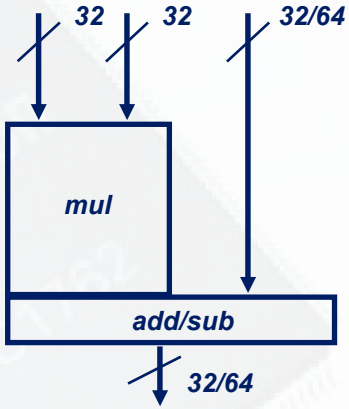
MUL MADD MSUB
32 +/- 16x16
48 +/- 16x16



choice of register half
Left-alignment
Sat

thru-put = 1 cycle

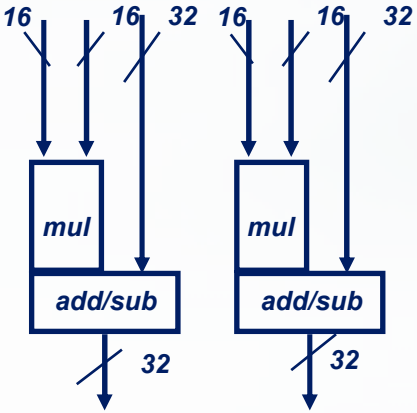
MUL MADD MSUB
32 +/- 32x32
64 +/- 32x32



Left-alignment
Sat

thru-put = 2 cycles

MUL MADD MSUB
32 +/- 16x16 ||
32 +/- 16x16



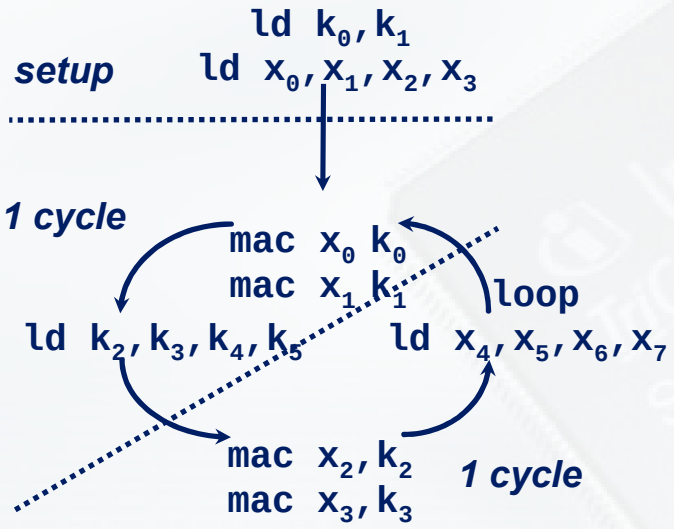
choice in register half
left-alignment
*8000*8000 -> 7FFF FFFF*
add/sub or sub/add
Rounding
Sat
Packing 2 32bit into 1 32bit

thru-put = 1 cycle

TriCore Architecture – Supported DSP Operations

Two MACs per cycle:

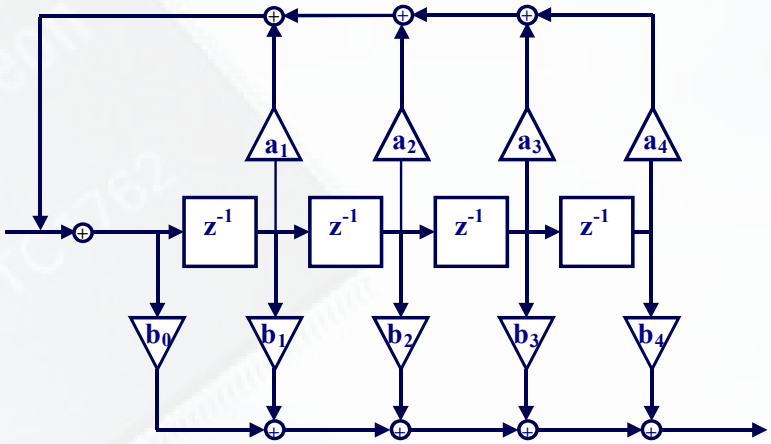
Matrix calculus



- Dual 16x16 hardware MAC
- Packed data
- Parallel load
- Mac-load-(loop) per cycle

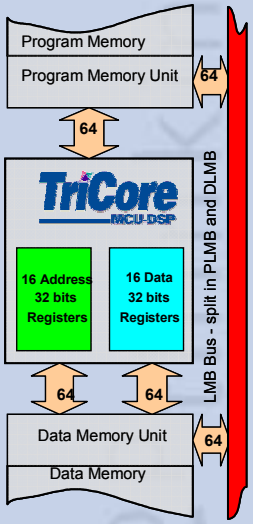
Sensors signal processing:

FIR, IIR, DFT, FFT,

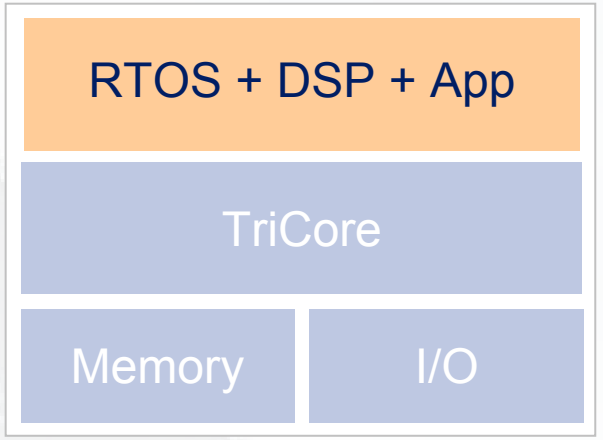


- Zero overhead loop
- Bit reverse addressing

TriCore Architecture –
Reducing Cost and Complexity by merging MCU and DSP



- Control and DSP development and integration/debug can all be done with the same development tools
- Optimized DSP library algorithms can be used out of the box
- Easy adaptation of DSP functions integrated in Automatic Code Generation tool package
- Devices can quickly be adapted to new market requirements
- smaller silicon



TriCore™ → **one CPU**
one Tool
one RTOS → **Fast Time to Market**
New Features
Lower Cost

Infineon
Technologies AG
10.2005

Infineon

going into detail..

TC1762 – Code Size

Never stop thinking.

TriCore Architecture – Code Size

With an Instruction Set tailored to real-time embedded control applications TriCore offers the best combination for optimized code performance and optimized code size:

Key Features	Key Benefits
■ **16 & 32-bit instruction format**	■ can be intermixed freely without setting mode bits 40% better code size vs. 32 bit instructions only
■ **Dual & Triple operand instructions**	■ well suited for C compiler, reduced overhead for temporary operand loads/stores
■ **Bit handling instructions**	■ cover control-oriented requirements, efficient in control tasks and peripheral register access, allow efficient SW state machine implementation
■ **Accumulated Logical/Compare**	■ efficient code in state machine programming
■ **Saturation Arithmetic and Rounding/MIN/MAX instructions**	■ cuts off overhead for immediate result verification, done in HW by saturating math instructions (e.g. extensive lookup table algorithms)
■ **Embedded DSP instructions**	■ specific data formats and addressing modes, no overhead by additional instructions for operand handling (e.g. digital filter algorithm for knock detection

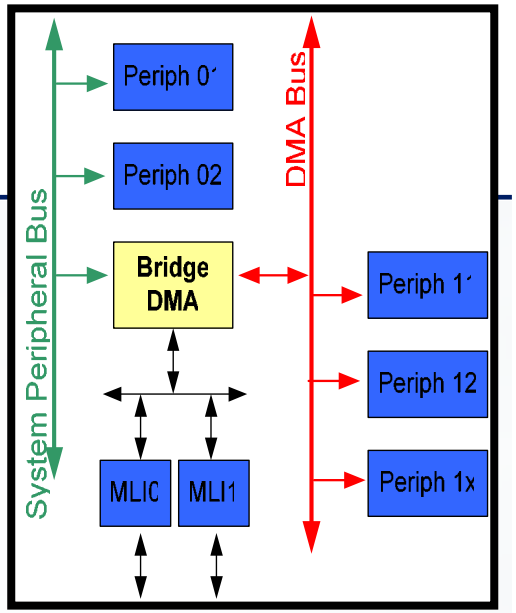
Infineon

going into detail..

TC1762 – Key Peripherals

Never stop thinking.

TC1762 Peripherals – DMA
Direct Memory Access Controller



Capabilities

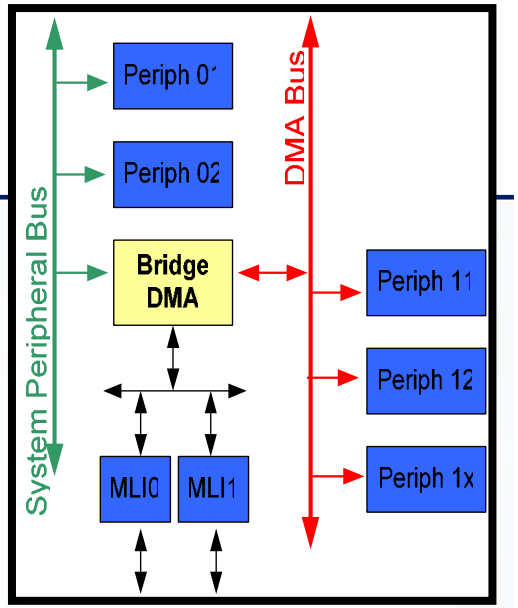
The DMA (single move engine) supports 8 independent channels for high flexible memory or peripheral transfer operations. It additionally supports MLI operations and bridge functionality between the System Peripheral Bus (SPB) and the DMA bus.

Structure and Benefits

By mapping simple data transportation tasks to the DMA controller, the TriCore CPU is significantly released and might focus on its application and low level driver task.

- **flexible usage** for **single event or continuous transfer operation** including **programmable data width** for 8/16 or 32 bit memory transfer transactions covers a wide range of feasible customer application requirements
- **flexible interrupt generation** from up to 18 different interrupt sources (e.g. data pattern recognition) fulfills clear hierarchical separation of HW driven data transfers and needed SW interaction
- **programmable request wiring matrix** of up to 8 hardwired possible inputs for each DMA channel supports maximum adaptation flexibility to the customer
- combination of **hardwired channel priority** with **programmable SW priority** for each individual DMA channel offers maximum adaptation to application demands

TC1762 Peripherals – Memory Checker



Capabilities

Check dedicated memory portions (e.g. program memory flash) in background for correctness (e.g. to be able to determine code corruption)

Structure and Benefits

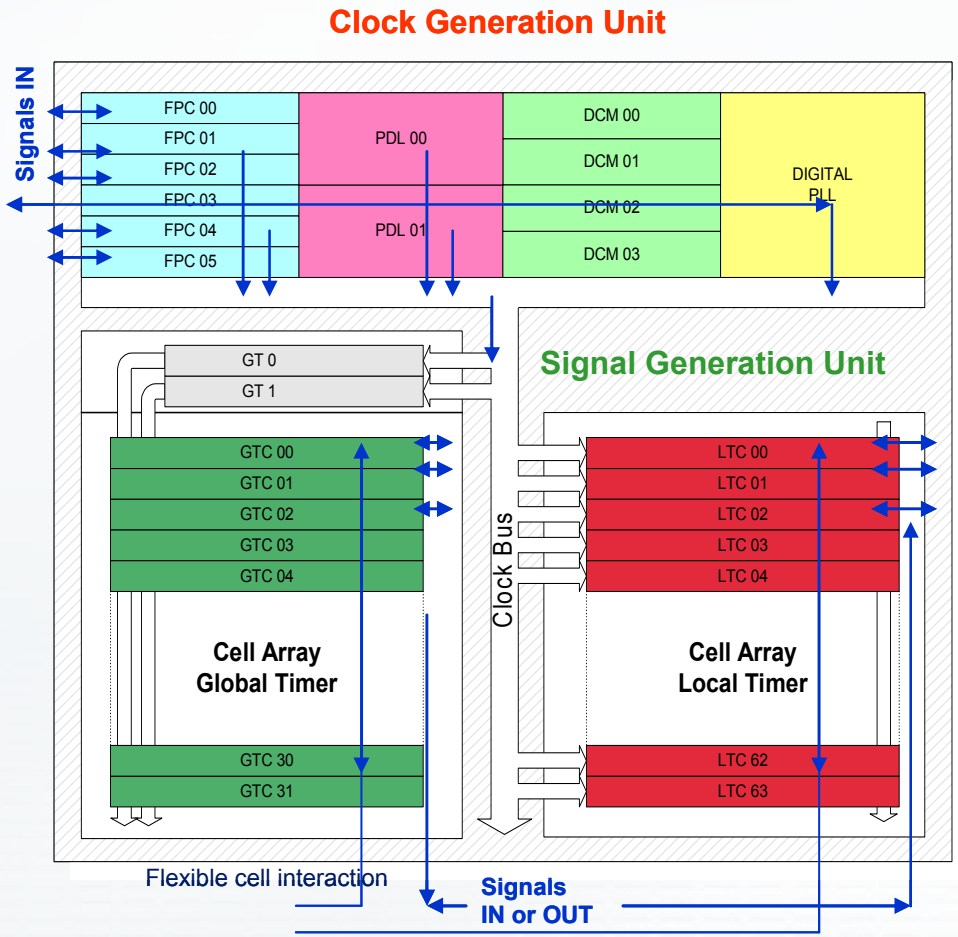
The memory checker has implemented a polynomial generator which equals to the standard used within Ethernet:

$$G^{32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

Any bus master (TriCore CPU, PCP or DMA controller) might serve the memory checker located on the SMIF interface of the DMA module.

- checking a memory portion is feasible by a **sequential move** (read operation followed by a write operation) of dedicated memory portion to a a single address of the memory checker located on the SMIF interface
- **simple compare function** is needed to fell a decision whether calculated memory checker result matches to the pre-calculated expected result stored somewhere in the FLASH area
- using a **DMA channel** offloads TriCore CPU. Only READ operations are seen on the System Peripheral Bus (SPB) or the DMA Bus. The write operation to the memory checker by the move engine is hidden within the DMA (routed to SMIF interface) and does not require any bandwidth of the other buses

TC1762 Peripherals – GPTA
Functional Block Diagram



Clock Generation Unit:

FPC Filter and Prescaler Cell
amount of cells: 6

PDL Phase Discrimination Logic
amount of cells: 2

DCM Duty cycle Measurement Cell
amount of cells: 4

PLL Phase Locked Loop
amount of cells: 1

Clock Distribution Bus
amount of clock lines: 8

Signal Generation Unit:

GT Global Timer (24bit)
amount of cells: 2

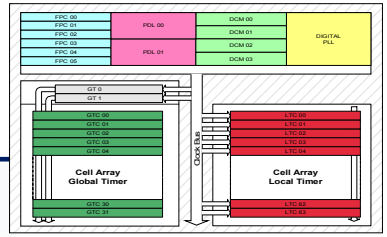
GTC Global Timer Cell (24bit)
amount of cells: 32

LTC Local timer Cell (16bit)
amount of cells: 64

Signal Cross Connection:

- via the Clock Bus
- Pad connections to and between the FPC/GT/GTC/LTC cells

TC1762 Peripherals – GPTA
General Purpose Timer Array (1/2)



Capabilities

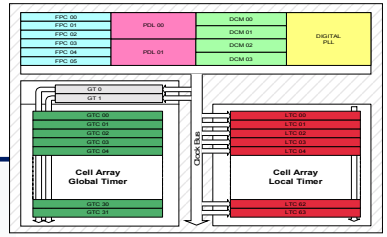
The GPTA offers very flexible filtering and high resolution signal acquisition, a digital PLL used for the generation of a higher resolution of input signals and due to its universal cell structure all kinds of enhanced counting, capture compare and PWM functionality.

Structure and Benefits (1/2)

perfect adaptation to target application by non-static modular cell approach compared to timer implementations of the competition:

- **very flexible digital input filtering** can be achieved by the usage of the implemented Filter Prescaler Cells (FPC). Flexible strategies between delayed and immediate debounce filtering are possible (e.g. for input filtering of the flywheel or the camshaft signals)
- **tracking of all kind of rotating shafts** (e.g. within a gearbox system) including the encoding of the signals for the forward and backward position can be easily achieved by usage of the Phase Discrimination Logic (PDL) cells which supports the decoding of 2 and 3 sensor input signals
- **scalable high resolution** for the generation of optimal distributed microticks as an angle reference counter signal for the engine position can be easily achieved by usage of the implemented digital PLL module

TC1762 Peripherals – GPTA
General Purpose Timer Array (2/2)



Structure and Benefits (2/2)

perfect adaptation to target application by non-static modular cell approach compared to timer implementations of the competition:

- **independent access to time and angle domain** by two global timers (GT0/GT1) with corresponding Global Timer Cell (GTC) array
  - optimal support for capture/compare interaction corresponding to time or angle counters (e.g. injection or ignition for gasoline engines)
- **all kinds of PWM generation** are supported by the usage of the Local Timer Cell (LTC) array. Hereby all kind of desirable scalability in terms of
  - **autonomous full coherent high speed PWM generation** from 0-100% duty cycle with five LTC cells driven completely in HW down to
  - **SW supported PWM generation** from 10-90% duty cycle with minimum on one LTC cell of used GPTA resources can be easily implemented
- **optimal application driven balance** between precise HW driven event generation (e.g. HW driven start of ignition on pre-calculated engine angle) and SW driven interrupt tasks (e.g. reconfiguration of the compare value for next ignition start)
- **In field test and repair** feasible due to dynamic reconfigurable in/out multiplexer and array of replaceable blocks

TC1762 Peripherals – ADC/Fast ADC
Aanalog to Digital Converters ADC and Fast ADC

Capabilities

AUDO-NG incorporates two different implementations for ADC peripherals using successive approximation conversion principle:

- **one ADC module** with programmable resolution 8/10/12 bit and conversion time of 2,5 µs @ 10bit
  with a sophisticated feature set for autonomous analog/digital data acquisition
- **one Fast ADC** module with 10 bit resolution and a minimum conversion time of 320 ns resp. (corresponding to 3 Msamples) including a data reduction filter with moving average
- **auto-calibration** mechanism build in at power up

FADC targeted application segments are knock detection and dynamic control of ignition by ion current measurement

Structure and Benefits Fast ADC

unique solution for knock detection without external ASICs or dedicated DSP

- **reduced SW load** for FIR-Filter by usage of integrated decimation comb filter (e.g. data reduction by factor 6 from 1200 to 200 ksamples)
- **quick adaptation of the overall filter quality** to the application demands by programmable adaptation of data rate used for the FIR filter
- **increase of ADC accuracy** by data reduction filter and moving averaging filter (e.g. from 10 bit to 11 bit by selected oversampling factor of 4)

TC1762 Peripherals – MLI
Multiprocessor Link Interface

Capabilities

AUDO-NG incorporates two MLI modules which are used for a serial high speed inter processor connection to other AUDO-NG family members.

Structure and Benefits MLI

- **serial high speed interface** up to $f_{MLI}/2$ (i.e. 33 Mbaud for TC1762) which is used for **inter-processor communication** between the AUDO_NG family members and therefore offers the possibility of scalable processing power within an application
- parallel memory accesses to up to **four memory windows** automatically will be converted to serial high speed MLI protocol and vice versa at the other MLI device
- capability of posting up to **four interrupts** to the second processor on the other side by sending a command frame
- **high efficient data transfer bandwidth** supported (up to 33 MBaud) by special protocol for data, address offset or data and address offset
- for security reasons **MLI interface is locked after HW reset** and first has to be unlocked by the device itself

TC1762 Peripherals – MSC
Introduction of the Advanced Micro Second Bus

Evolution	Parallel Input parallel Status	Parallel Input SPI Interface	SPI + µs -Bus	Advanced Micro Second Bus
Pins / IO	16 + 16 = 32	16 + 4 = 20	4 + 3 = 7	6
performance	PWM	PWM configurability	PWM configurability	PWM configurabilit
diagnostic	1 bit / channel no memory	2 bit / channel fault memory	2 bit / channel fault memory	2 bit / channel fault memory
interface	parallel	parallel + duplex bus	duplex bus + point - point	point - point + async . upstream

time

TC1762 Peripherals – MSC
Micro Second Channel

Capabilities

purpose of the MSC module is to set a new open standard for the serial high speed communication to power ASIC modules, like multi-switches (i.e. for ignition or injection drivers) including transfer of command frames, data frames and asynchronous diagnosis feedback from the device

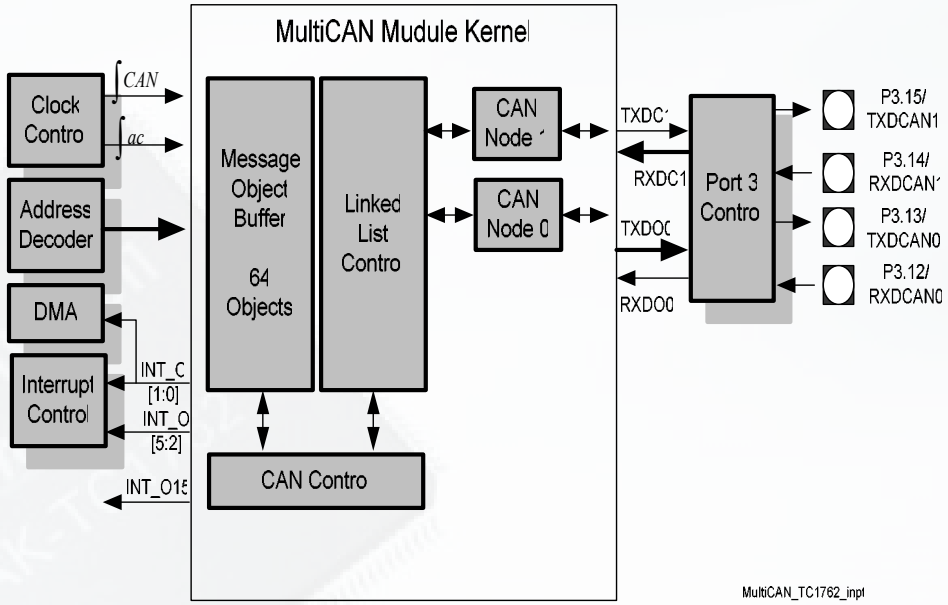
Structure and Benefits MSC

Design goals for the new approach has been:

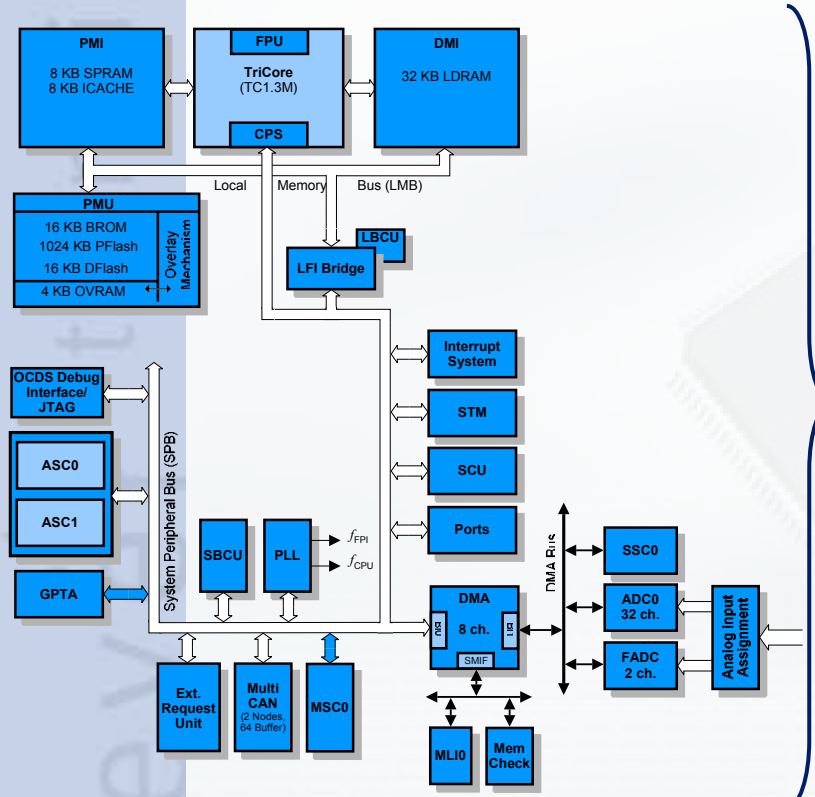
- parallel high speed **PWM channels** generated by the General Purpose Timer Array (GPTA) are serialized via MSC module and transferred to the corresponding MSC module within the connected power ASIC device without any additional SW load
- maximum resolution for transferred PWM data is 400 kHz or 2,5µs period length
- 2x2 signal wires **Low-Voltage Differential Signals** (LVDS) drivers implemented for high speed downstream signals (CLK and Data) for lower EMI
- **asynchronous upstream channel** implemented for diagnosis data for getting rid of SPI used polling mechanism
- 6 wires used to connect up to 32 high speed PWM channels instead of the standard SPI approach with 36; **saving of up to 30 package pins** on the MC and power asic side offers ability of smaller pin counts on packages for microcontroller and power asic and therefore saves system costs
- **scalable approach** supported for the connection of up to four MSC power devices to one module
- **standard SPI protocol alternatively supported** for high speed downstream channel

TC1762 Peripherals – MultiCAN
Feature Set and Module

- CAN functionality conform to **CAN specification V2.0 B active** for each CAN node (compliant to ISO 11898)
- **2** independent **CAN nodes** available
- **64** independent **message objects** (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to **1MBaud**, individual programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Automatic **gateway mode** support
- **6** individually programmable **interrupt nodes**
- **CAN Analyzer Mode** for bus monitoring



TC1762 Peripherals – System Benefits
Summary – Peripheral Support



TriCore Architecture

combining three worlds of µProcessor, µController and DSP results in scalable HW resources optimized for embedded Powertrain applications

optimized Bus Architecture

Three layer SW concept simplifies clear hierarchical separation of e.g. "Branding Application SW" based on the IP of the OEM and standard Low Level Driver SW delivered by the TIER1

AUDO-NG Peripheral Support and Connectivity

Enhanced Peripheral Modules helps to lower system costs by:

- **saving package pins of the µC through serialization (e.g. µs-Bus for external Power ASSP)**
- **porting external ASIC function to AUDO-NG (e.g. saving external Knock-ASIC by FADC usage)**
- **scalable system performance (e.g. connecting family members of AUDO-NG through MLI bus)**

Extensive Development Support

World Leading Tool partners supporting all phases of development within the V-Cycle

Infineon

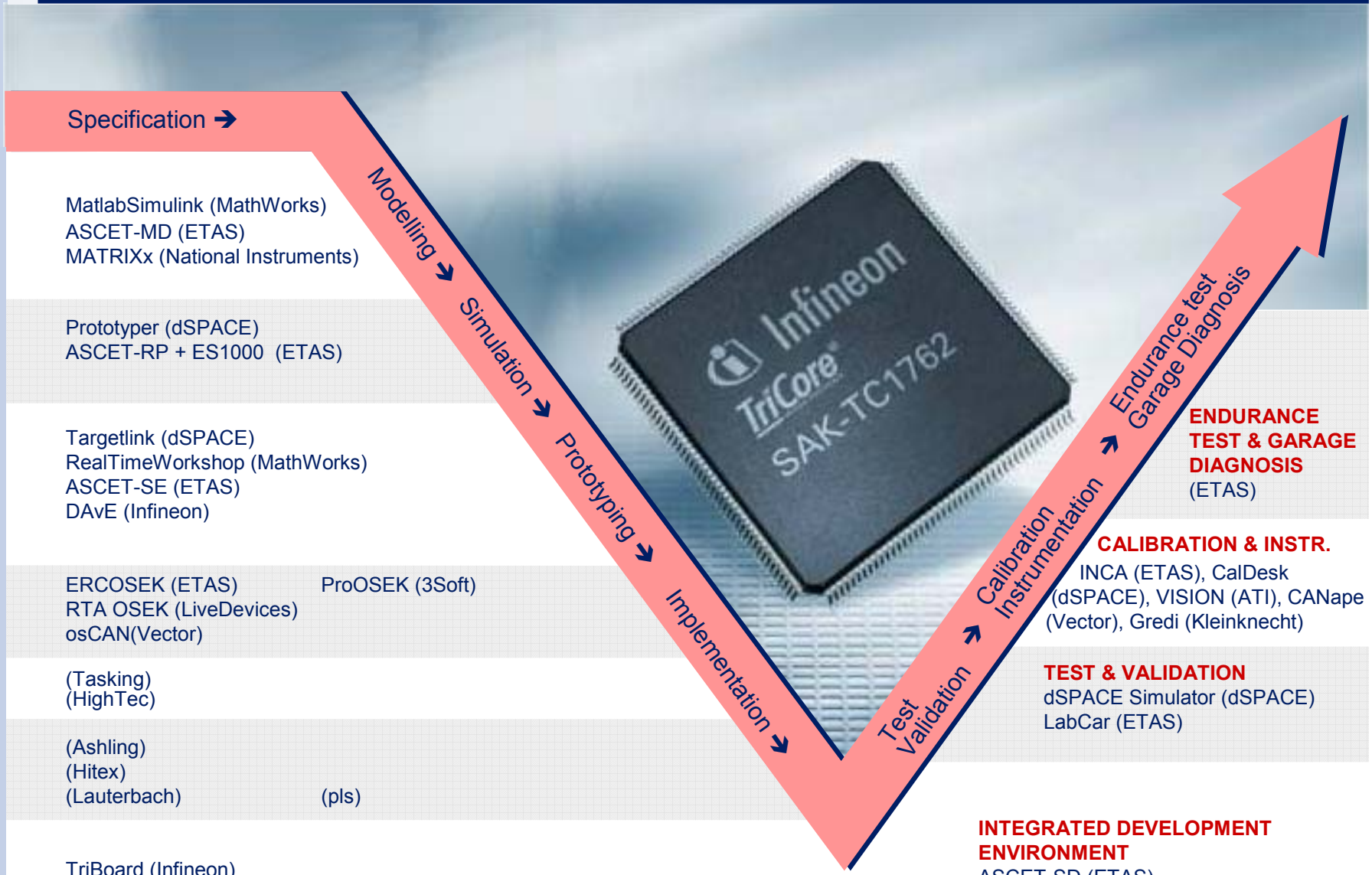
going into detail..

TC1762 – Tool Support

Never stop thinking.

Complete Tool Environment for System Development
Toolpartners for AUDO-NG Support

AUDO-NG
automotive UnifieD prOcessor
Next Generation



MODELING SIMULATION
MatlabSimulink (MathWorks)
ASCET-MD (ETAS)
MATRIXx (National Instruments)

PROTOTYPING
Prototyper (dSPACE)
ASCET-RP + ES1000 (ETAS)

AUTOMATIC CODE GENERATION
Targetlink (dSPACE)
RealTimeWorkshop (MathWorks)
ASCET-SE (ETAS)
DAvE (Infineon)

OPERATING SYSTEM
ERCOSEK (ETAS) ProOSEK (3Soft)
RTA OSEK (LiveDevices)
osCAN(Vector)

COMPILER DEBUGGER
(Tasking)
(HighTec)

EMULATOR DEBUGGER
(Ashling)
(Hitex)
(Lauterbach) (pls)

DEVELOPMENT BOARD
TriBoard (Infineon)
Low-Level Driver, Libraries, AppNotes (Infineon)

ENDURANCE TEST & GARAGE DIAGNOSIS
(ETAS)

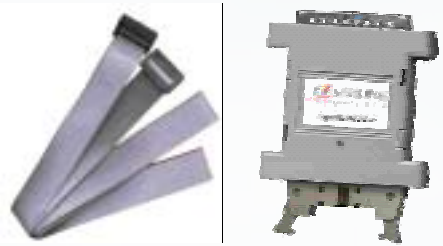
CALIBRATION & INSTR.
INCA (ETAS), CalDesk (dSPACE), VISION (ATI), CANape (Vector), Gredi (Kleinknecht)

TEST & VALIDATION
dSPACE Simulator (dSPACE)
LabCar (ETAS)

INTEGRATED DEVELOPMENT ENVIRONMENT
ASCET-SD (ETAS)
MATLAB/Simulink… (MathWorks)

Complete Tool Environment for System Development
Scalable OCDS (L1&L2) Debug Support

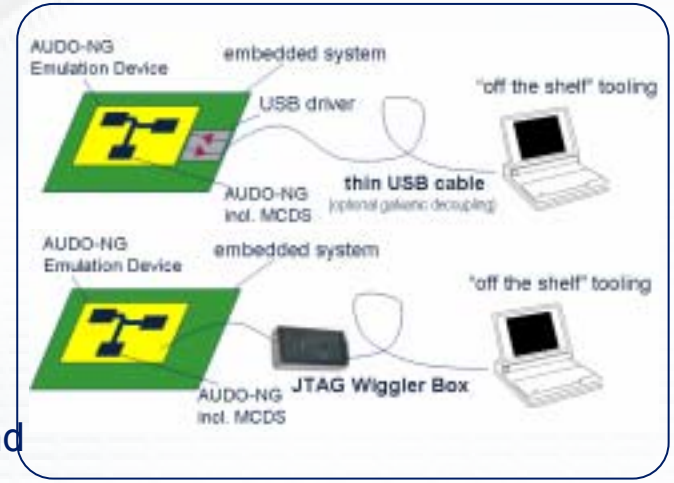
- **JTAG/ OCDS-L1 support (On Chip Debug Support):**
  - Run Control (Start, Stop, Breakpoints)
  - Program Download
  - Memory Read and Write Access at runtime
  - Data Visibility
  - Calibration



JTAG / OCDS-1 Debug Cable and Wiggler

- **OCDS-L2 support:**
  - Program Trace (via 16-bit Port) (TriCore **only**)

- **OCDS-L3 support** (available by a separate Emulation Devices)
  - Full system level trace (bus transactions and core execution)
  - Minimal HW investment (USB or JTAG to target only)
  - On-Chip resources for trace capture
  - Additional event logic to allow intelligent filtering and data capture.



Complete Tool Environment for System Development
TC1762 Debugger and RTOS Support

Compilers + Assembler

Availability

	TCv1.3	PCP2 Assembler	FPU	SFR sup.
Tasking	now	now	now	now
HighTec	now	now	now	now

ICEs + Debugger

	OCDS L1	OCDS L2	PCP 2 L1	PCP 2 L2
Ashling	now	pending		
Hitex	now.	L2 trace available for 40-60MHz		
Lauterbach	now	L2 trace available for 40-60MHz		
pls	now	L2 trace available for 40-60MHz		
Tasking	now			
HighTec	now			

RTOS (using enhanced System Timer as standard OSEK peripheral)

ETAS	ERCOSEK	
Vector	osCAN tbd	AUDO-NG support available
3-Soft	ProOSEK tbd	
LiveDevices (ETAS)	Realogy Real-Time Architect	


Infineon
technologies
We create
Semiconductor Solutions,
enabling the Technology
Lifestyle of the Individual
in the 21st Century.
Never stop thinking.