XMC4000

Microcontroller Series
for Industrial Applications

PCB Design

✓ Guidelines

Application Guide

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Microcontrollers

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Revision History

Page or Item	Subjects (major changes since previous revision)
V1.0, 2013-11	

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Guidelines

1 Introduction

The XMC4000 family is an ARM® Cortex™-M4 based 32-bit microcontroller family available in VQFN-48, LQFP-64/100/144 and LGBGA-144 pin packages. This application guide helps to design a PCB with respect to:

- electromagnetic compatibility
- power supply system
- performance of analog peripherals
- thermal management

In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rules for PCB design, some product-specific recommendations and guidelines for the XMC4000 family are provided in this document.

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by the customer, based on dedicated implementation choices. Other design implementations can also be applied.

2 General Information

The XM4000 family has four different power domains:

- Pad Domain (VDDP, 3.3V, supplied externally)
- Analog Domain (VDDA, 3.3V, supplied externally)
- Core Domain (VDDC, 1.3V, generated internally)
- Hibernate Domain (VBAT, 2.0-3.6V, supplied externally)

The Pad Domain VDDP and the Analog Domain VDDA with a nominal voltage of 3.3V must be supplied and decoupled externally.

The Core Domain supply with a nominal voltage of 1.3V is generated out of the Pad Domain supply by an on-chip EVR (Embedded Voltage Regulator). The VDDC pins are the output of the EVR and must be stabilized and decoupled with external decoupling capacitors on the PCB.

The supply pin VBAT of the Hibernate Domain can be connected to a battery coin cell or large capacitor. Even if the hibernate features are not used, the VBAT pin must always be connected to a power supply, when VDDP is supplied.

Note: The VBAT pin must always be supplied, when VDDP is supplied. Tie the VBAT pin directly to VDDP, if no other circuitry for VBAT is destined.

3 PCB Design Recommendations

3.1 Clock Output

To minimize the EMI radiation on the PCB some measures have to be considered if the external clock output feature via the clock pin EXTCLK (P0.8 or P1.15) is used:

- Reduced the driver strength of the pin if possible by choosing a weak pad drive mode (register P0_PDR0 or P1_PDR15 respectively)
- Route this signal with adjacent ground reference and avoid signal and reference layer changes
- Route it as short as possible
- Routing ground on each side can help to reduce coupling to the other signals (crosstalk)

3.2 Unused Pins

For unused pins the measures listed in Table 1 should be considered.

Table 1 Measures for unused pins

Unused Function / Unused Pin	Recommended measure if pin is not used
Power Supply Pins (VDDP, VDDA, VDDC, VBAT, VSS including exposed pad, VSSA, VSSO, VAGND)	• These pins **must always** be connected to an appropriate power supply or power circuitry!
Reference Voltage of the ADC (VAREF)	• Leave VAREF open (ADC cannot be used, digital input function of P14 and P15 is still working)
Port Pins (P0-P15)	• Pins should be configured as “direct input” with an “internal pull-up [or pull-down] device active” via the register Pn_IOCR • Pins should be left open and should not be connected to any other net (layout isolated PCB pad, for soldering only)
External oscillator pins (XTAL1, XTAL2, RTC_XTAL1, RTC_XTAL2)	• Leave XTAL1 / RTC_XTAL1 open if the corresponding oscillator is in dower-down • Connect a pull-down resistor to XTAL1 / RTC_XTAL1 or tie directly to GND (VSS) if the corresponding oscillator is **not** in dower-down • Leave XTAL2 / RTC_XTAL2 open
USB Pins (USB_DP, USB_DM, VBUS)	• Leave USB_DP, USB_DM and VBUS open
Serial Wire Debug Pins (TMS, TCK)	• Leave TMS and TCK open
Reset Pin (PORST#)	• Leave PORST# open
Hibernate Pins (HIB_IO_0, HIB_IO_1)	• Leave HIB_IO_0 open (after reset this pin is driving a low level) • Leave HIB_IO_1 open if the Hibernate domain is **not** enabled (SCU_PWRSTAT.HIBEN == 0) • Leave HIB_IO_1 open and configure as “Direct input, Input pull-down device connected” (HDCR.HIBIO1SEL = 0001_B) if the Hibernate domain is enabled (SCU_PWRSTAT.HIBEN == 1)

3.3 Main Oscillator (XTAL1 / XTAL2)

To reduce the radiation / coupling from the main oscillator circuit, a separated ground island on the GND layer should be designed (see Figure 1). This ground island can be connected at one point to the GND layer. Ideally this point is close to the VSSO pin (not available in all packages). This helps to keep the noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSO should also be connected to this island. Traces for load capacitors and Crystal should be as short as possible.

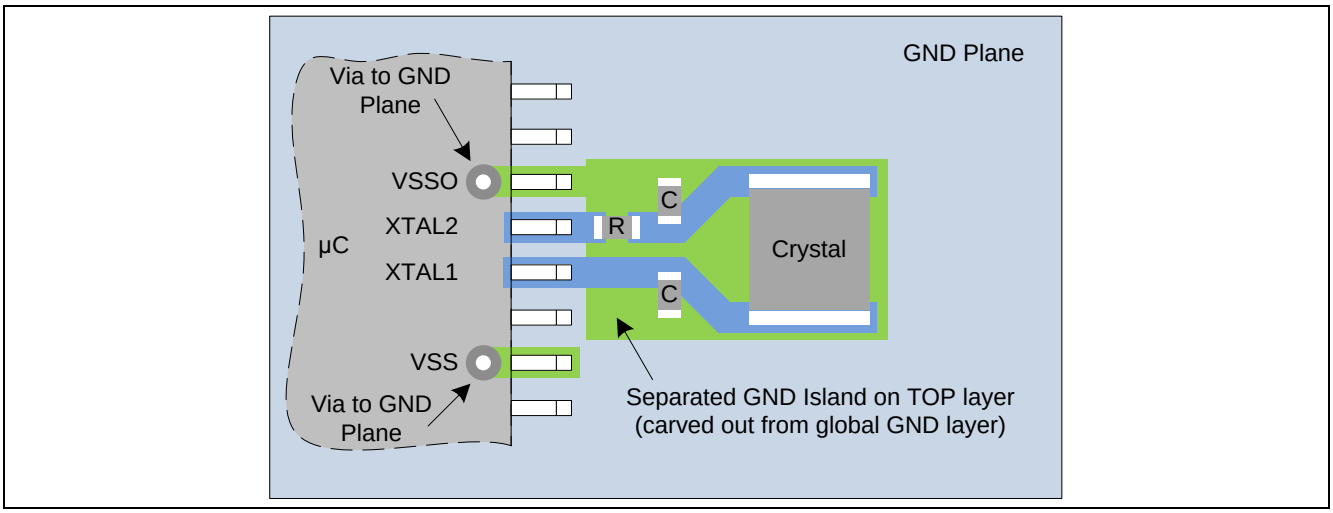


Figure 1 Separated Ground Island for the Main Ocsillator

3.4 Power Supply Domains

- All VDDC pins must be connected to one net on the PCB, even if they are internally connected by each other, because the impedance of the external connection is much lower than the internal connection.
- A low inductance value for the connection of decoupling capacitors to the supply pins is required. Therefor place the decoupling capacitors close to the corresponding power supply pin group.
- All supply domains should be decoupled separately with Low ESR and Low ESL capacitors (ceramic multilayer capacitors preferably)
- Use the capacitors values for decoupling/stabilization as shown in Table 2.

Table 2 Decoupling / Stabilization Capacitor Values

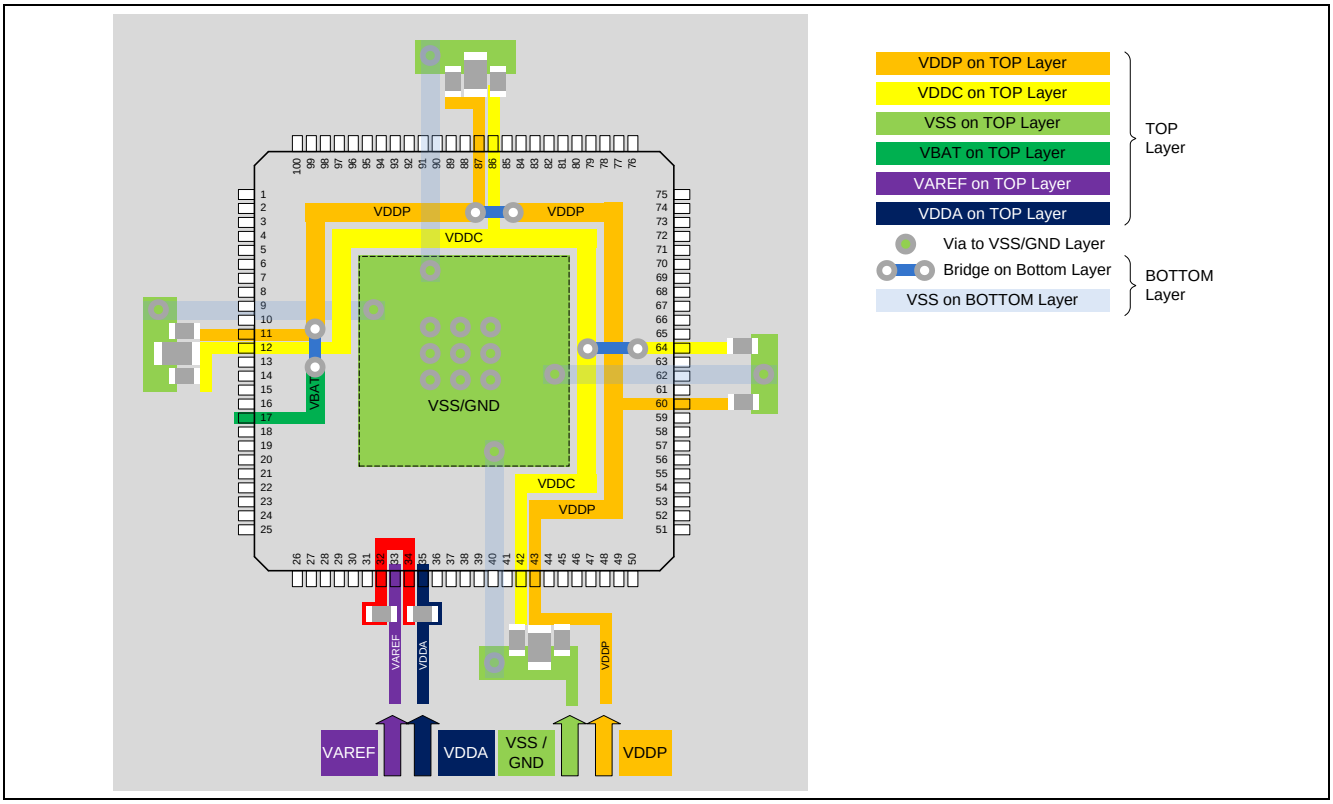
Power Supply Domain	Number and Sizes of Decoupling / Stabilization capacitors
Pad Domain VDDP/VSS	100 nF to each VDDP pin, 20 µF or higher to one pin
Analog Domain VDDA/VSSA	100 nF to VDDA pin
Core Domain VDDC/VSS	XMC4500: 100 nF to each VDDC pin, 10 µF ±10% X7R to one pin XMC4400/XMC4200: 100 nF to each VDDC pin, 4.7 µF ±10% X7R to one pin
Hibernate Domain VBAT	Any value, depends on hibernate time

- All power supply pins (supplied from a voltage regulator) should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power supply planes
- All VSS pins should be connected to the GND layer
- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).

- Inductance/ferrite beads in the range L ~5-10µH should be inserted in the supply paths at the regulator output.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.
- Depending on power dissipation (refer to the Data Sheet) the exposed pad should be connected to sufficient GND area on all layers.

A power-plane/grounding concept example for the XMC4000 microcontrollers can be found in Figure 2.

Figure 2 2-layer PCB Layout Example for Decoupling of XMC4000 (single sided assembly)



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