

A large, light blue decorative graphic consisting of a thick, curved line that forms a partial circle. A small, solid light blue circle is positioned on the upper left part of the curve.

TC172x

AP32181

Design Guideline for TC172x Microcontroller Board Layout

Application Note

V1.2 2012-02

Microcontrollers

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Device1

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Page	Subjects (major changes since last revision)
10	Figure 4 changed.

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Table of Contents

1	Overview	5
1.1	General Information	5
1.2	Pinout of TC172X.....	5
2	PCB Design Recommendations	5
2.1	Decoupling	7
2.2	Decoupling Capacitor List:	11
2.2.1	External supply generation mode:.....	11
2.2.2	Embedded voltage regulator mode (internal or external passdevice):	11

1 Overview

The TC172X is a 32-Bit microcontroller in LQFP-176 and LQFP-144 packages, which requires a PCB carefully designed for electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for the TC172x are discussed here.

1.1 General Information

The microcontroller has three supply domains (VDD=1.3V for Core, VDDP=3.3V for I/O Pad, VDDM=3.3V or 5V for ADC) and an external supply for the EVR (5V) which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC172X

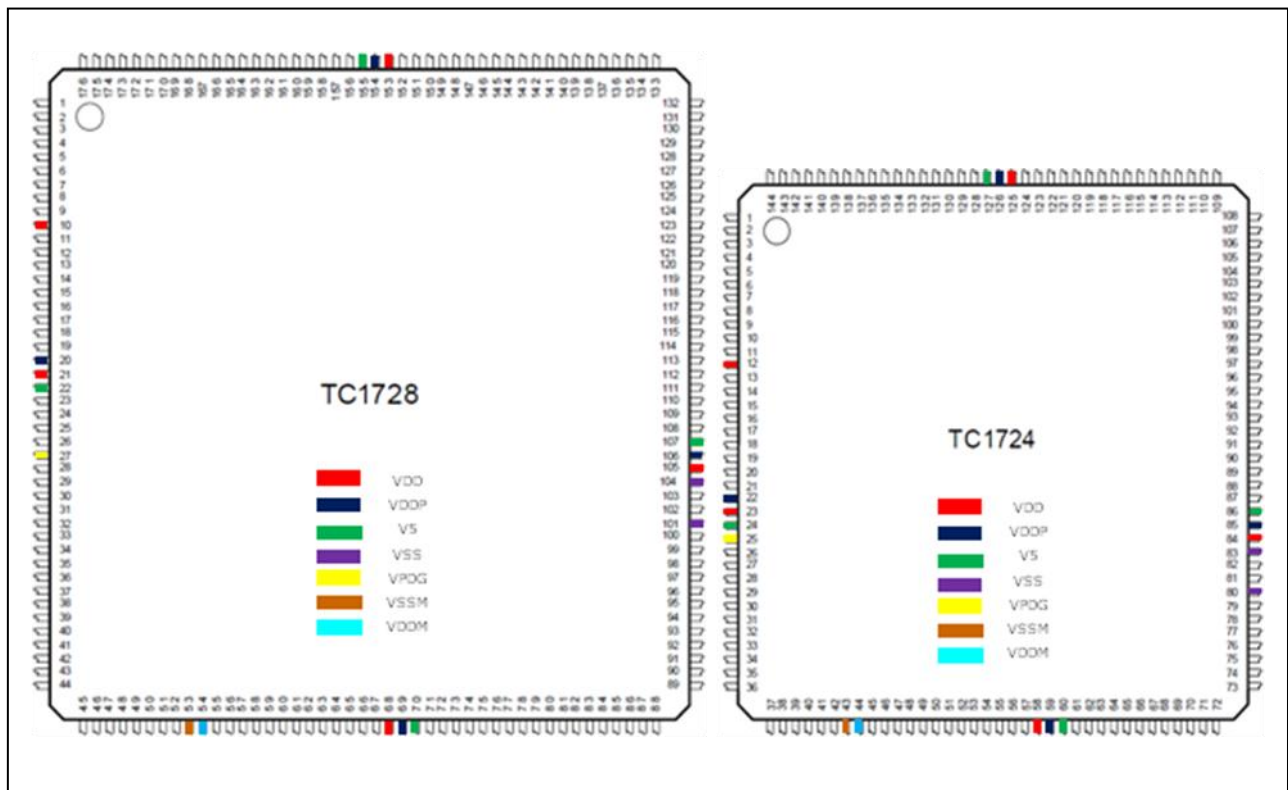


Figure 1 Pinout of TC1724 (TQFP-144) and TC1728 (LQFP-176).

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
 - LVDS Pins
 - MLI Pins
 - MSC Pins

PCB Design Recommendations

- ERAY Pins
- Supply Pins

Route these signals with adjacent ground reference and avoid signal and reference layer changes.

Route them as short as possible.

Routing ground on each side can help to reduce coupling to other signals.

- For unused **“Output, Supply, Input and I/O “** pins following points must be considered:

1. Supply Pins (Modules)	<ul style="list-style-type: none"> • See the User’s Manual.
2. I/O-Pins	<ul style="list-style-type: none"> • Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins including LVDS	<ul style="list-style-type: none"> • Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4. Input Pins without internal pull device	<ul style="list-style-type: none"> • For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device	<ul style="list-style-type: none"> • For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User’s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:

- Separate analog and digital grounds.
- The analog ground must be separated into two groups:
 1. Ground for OSC.
 2. Ground for ADC (VSSM for VDDM) as common star point.

- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground

PCB Design Recommendations

connections of the load capacitors and VSS(-OSC) should also be connected to this island. Traces for the load capacitors and Xtal should be as short as possible.

The purpose of this isolated oscillator GND island is to prevent osc noise from propagating into the global GND plane. Vice versa any noisy power or switching signals should be moved away from this local osc GND to prevent osc/pll disturbance. This local osc GND should only serve as current return path of the osc driver/crystal circuit. Restrict the layers under this island to digital GND or uncritical digital signals, but avoid power-related signal or pwr/GND routing. Also no signals from the connector which are subject to global disturbances (pulses, ESD) should be routed close to this osc GND Island.

- The power distribution from the regulator to each power plane should be made over filters.
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDM. Using inductance or ferrite beads (5 – 10 μ H) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~ 10 dB μ V on the related supply net.
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32111).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

2.1 Decoupling

- All supply domains of TC172x should be decoupled separately (see decoupling placement examples in Figure 2 & 3).
- Type of capacitors:
 - Values: 47 nF, 100 nF, 220nF, 330 nF
 - X7R Ceramic Multilayer (low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and POWER/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

In Figure 2 & 3 shown examples are based on device power supply concept and implementation. Alternative implementations are also acceptable and must be evaluated within application by customer.

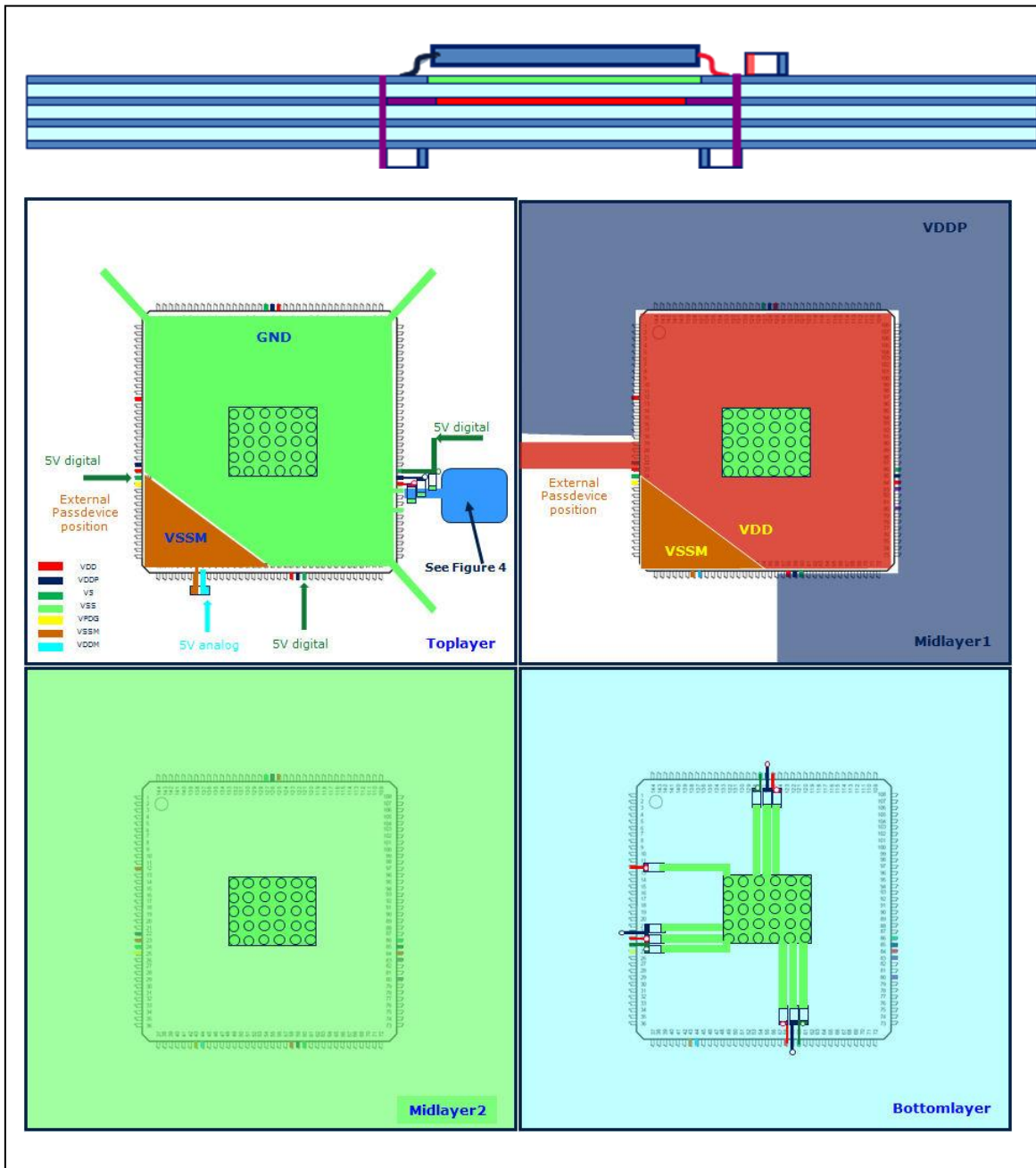


Figure 2 Capacitor Placement Example for Decoupling of TC1724 (TQFP-144) on a four layer board

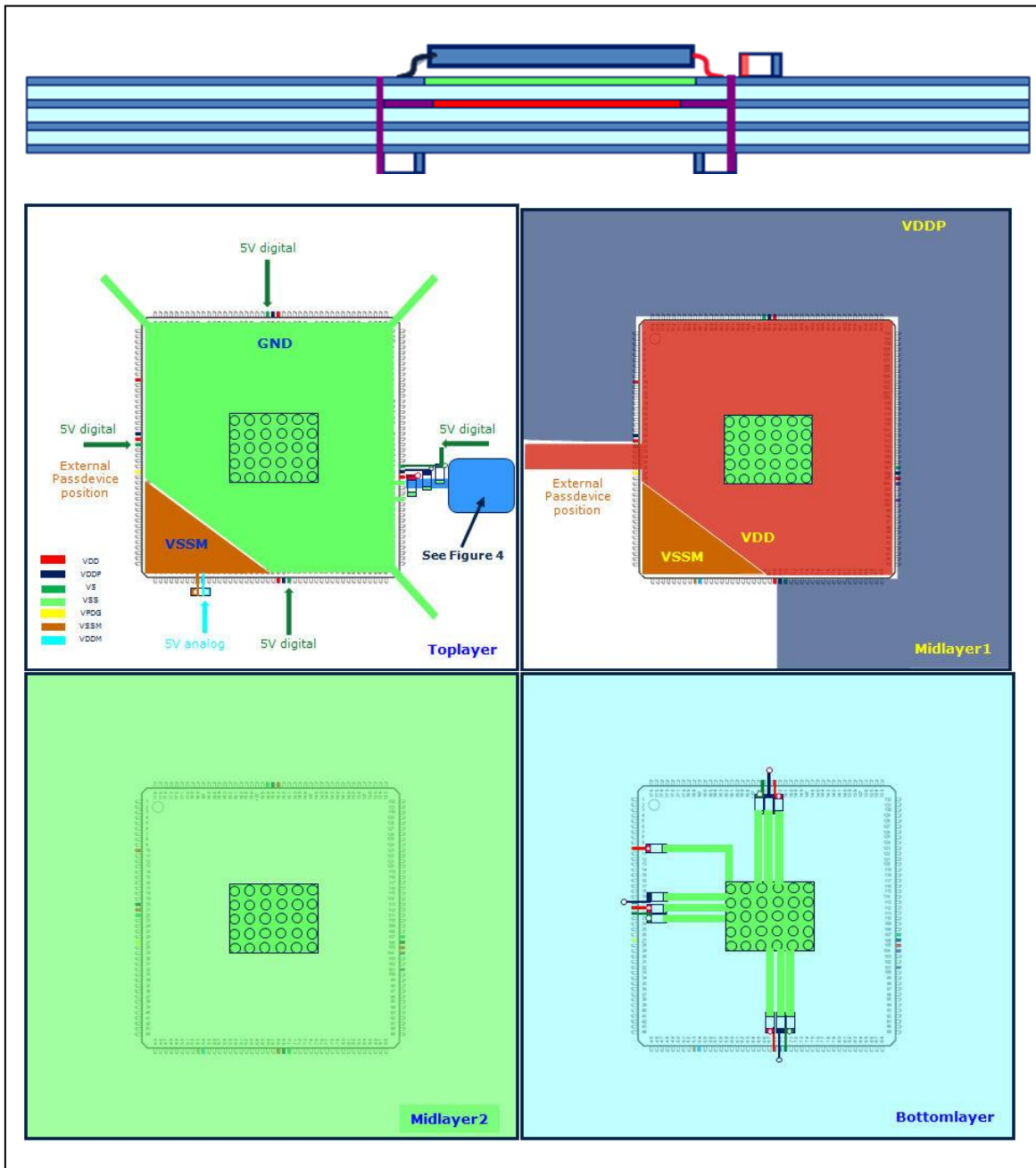


Figure 3 Capacitor Placement Example for Decoupling of TC1728 (TQFP-176) on a four layer board

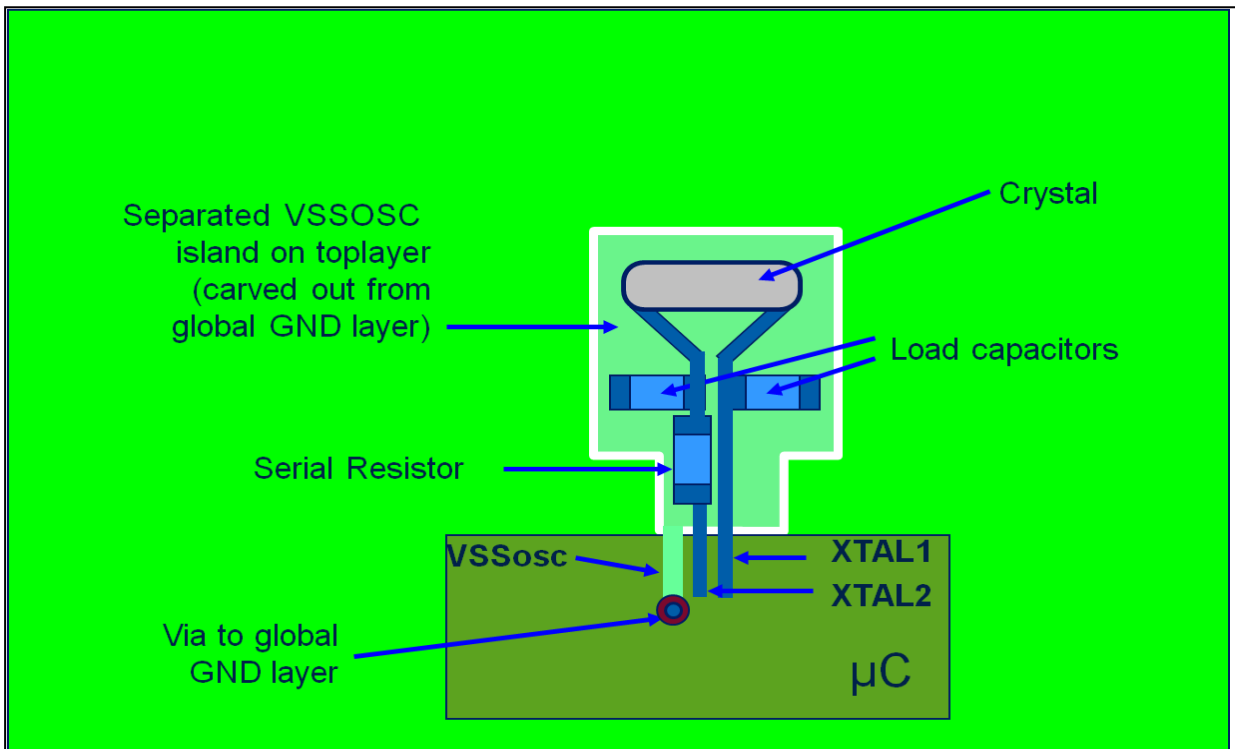


Figure 4 Layout Proposal Oscillator Circuit

2.2 Decoupling Capacitor List:

2.2.1 External supply generation mode:

Capacitor	Supply	Pins (TQFP-144)	Pins (TQFP-176)
47nF or 100nF	VDD	12	10
47nF or 100nF	VDD	58	68
47nF or 100nF	VDD	84	105
47nF or 100nF	VDD	125	153
47nF or 100nF	VDD	23	21
100nF	VDDP	22	20
100nF	VDDP	59	69
100nF	VDDP	85	106
100nF	VDDP	126	154
100nF	5V	24	22
100nF	5V	60	70
100nF	5V	86	107
100nF	5V	127	155
220 nF	VDDM	44	54

2.2.2 Embedded voltage regulator mode (internal or external passdevice):

Capacitor	Supply	Pins (TQFP-144)	Pins (TQFP-176)
220nF	VDD	12	10
220nF	VDD	58	68
220nF	VDD	84	105
220nF	VDD	125	153
220nF	VDD	23	21
4.7µF @80MHz 10µF @133MHz	VDD	Close to Chip	Close to Chip
220nF or 330nF	VDDP	22	20
220nF or 330nF	VDDP	59	69
220nF or 330nF	VDDP	85	106
220nF or 330nF	VDDP	126	154
4.7µF @80MHz 10µF @133MHz	VDDP	Close to Chip	Close to Chip
100nF	5V	24	22
100nF	5V	60	70
100nF	5V	86	107
100nF	5V	127	155
4.7µF	5V	At VR output	At VR output
220 nF	VDDM	44	54

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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