Never stop thinking

TC1782

AP32145

Design Guideline for TC1782 Microcontroller Board Layout

Application Note

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Microcontrollers

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Device1

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10	Figure-4 update

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1 Overview

The TC1782 is a 32-Bit microcontroller in LQFP176-pin package, which requires a carefully designed PCB concerning electromagnetic compatibility. In additionl to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for TC1782 are discussed here.

1.1 General Informations:

The microcontroller has three supply domains (VDD = 1.3V for Core, VDDP = 3.3V for I/O Pad, VDDM =3.3V- 5V for ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1782

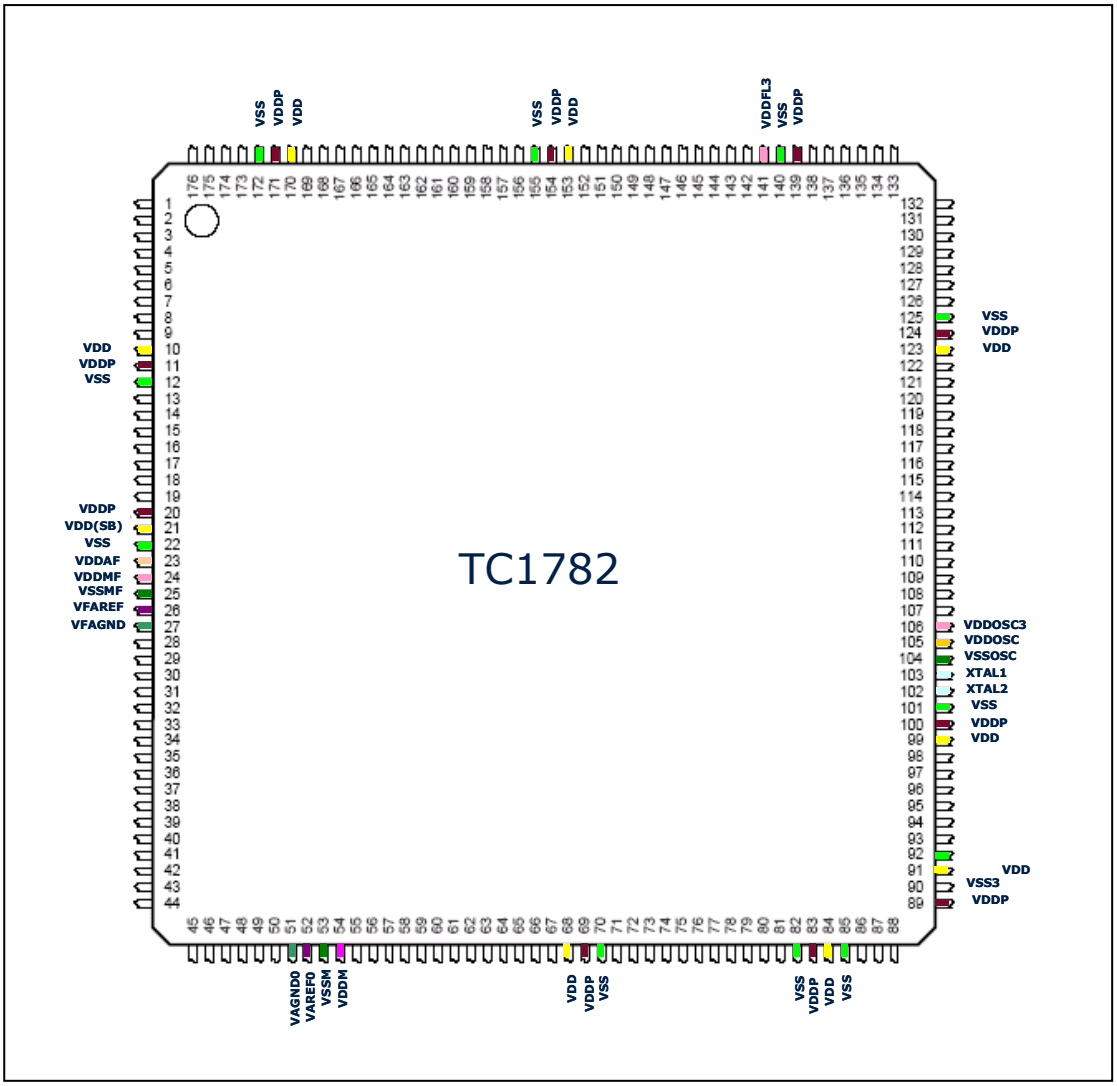

Figure 1 Pinout of TC1782 (LQFP-176):

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
  - SYSCLK: System clock output
  - Supply pins

  Route these signals with adjacent ground reference and avoid signal and reference layer changes.

  Route them as short as possible.

  Routing ground on each side can help to reduce coupling to other signals.

- For unused **"Output, Supply, Input and I/O "** pins following points must be considered:

1. Supply Pins (Modules) :	• See the User´s Manual.
2. I/O-Pins:	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins :	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4.Input Pins without internal pull device:	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device:	• For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:

  - Separate analog and digital grounds.

  - The analog ground must be separated into two groups:

    1. Ground for OSC and PLL (VSSOSC for VDDOSC and VDDOSC3) as common star point.
    2. Ground for ADC (VSSM for VDDM, VSSMF for VDDMF/VDDAF) as common star point.

PCB Design Recommendations

- To reduce the radiation / coupling from oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSOSC should also be connected to this island. Traces for load capacitors and Xtal should be as short as possible.
- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3, VDDM, VDDMF, and VDDAF. Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dBµV on the related supply net. (See Figure 2).
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32146).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

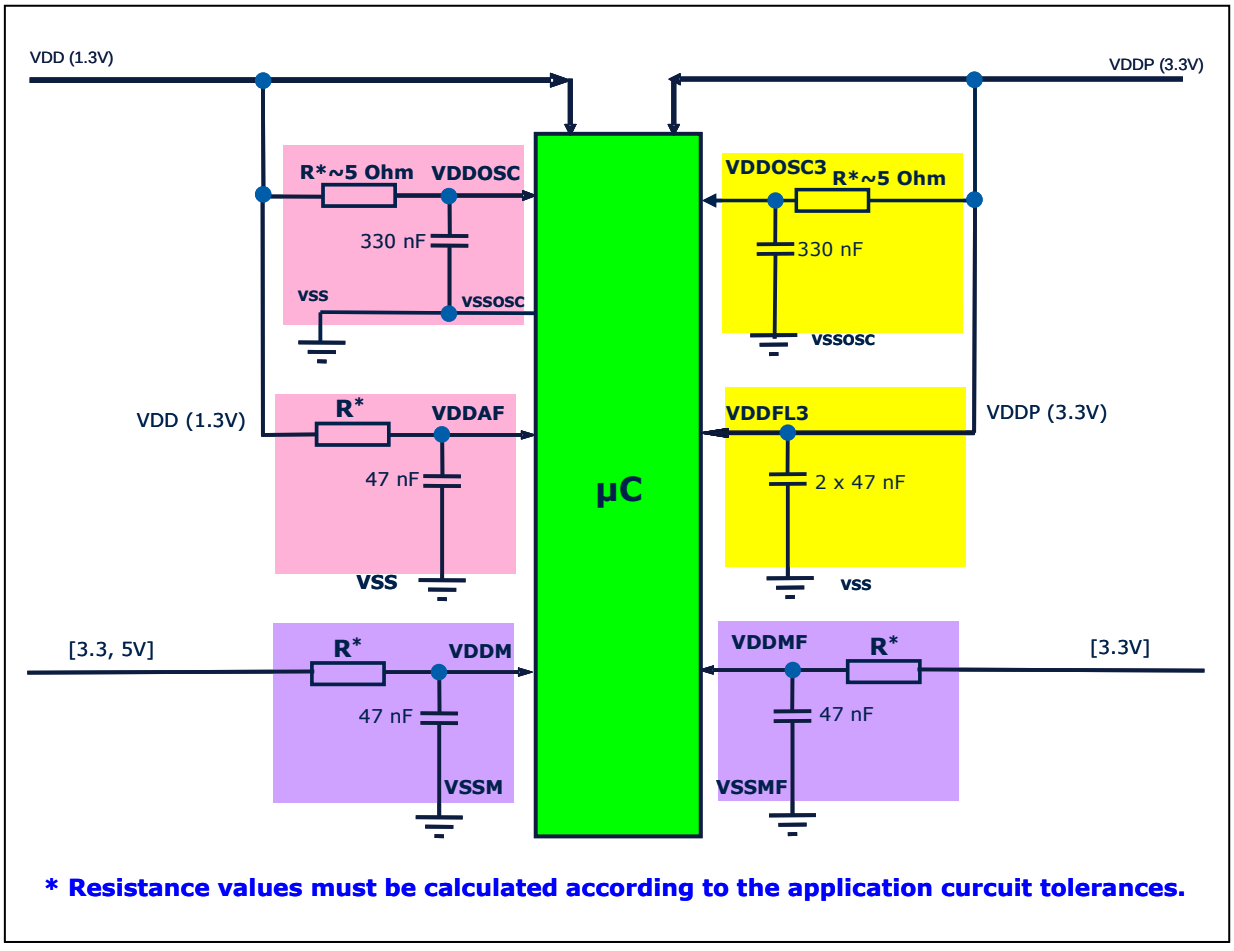

Figure 2 Filtering of VDDOSC, VDDOSC3, VDDFL3, VDDM, VDDMF, VDDAF supply pins

2.1 Decoupling

- The two supply domains VDD and VDDP of TC1782 should be decoupled separately. Figure 3 shows an example placement of decoupling capacitors. The decoupling capacitors for VDDC domain should be referenced to the GND area of exposed pad in order to get a smaller current loop. The remaining decoupling capacitors for VDDP should be referenced to GND-Leads of the package. (See decoupling layout example in Figure 3).
- If it is required to reduce the count of the capacitors, 100nF can be used instead of 47nF for the pins where two capacitors are connected (see capacitor list on page 11). The total value of decoupling capacitors for the supply domains shall not below 600nF for VDD and 700nF for VDDP.
- Type of capacitors:
  - Values: 47 nF (or 100 nF), 330 nF
  - X7R Ceramic Multilayer (Low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND layer.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and power/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.
- Please note that pin 21 and pin 170 are the Vddsb (stand-by RAM supply) pins of the TC1782ED Emulation Device. If a higher parasitic inductance the stand-by power supply can't be avoided (e.g. connected over a cable), it is mandatory to increase the size of this capacitors C18 and C19 (see decoupling capacitor list) to a value of 330nF or larger.

A power-plane/grounding concept example for a 32-bit microcontroller like TC1782 with LQFP-176 package can be seen in Figure 3. Alternative implementations are also acceptable and must be evaluated within application by customer.

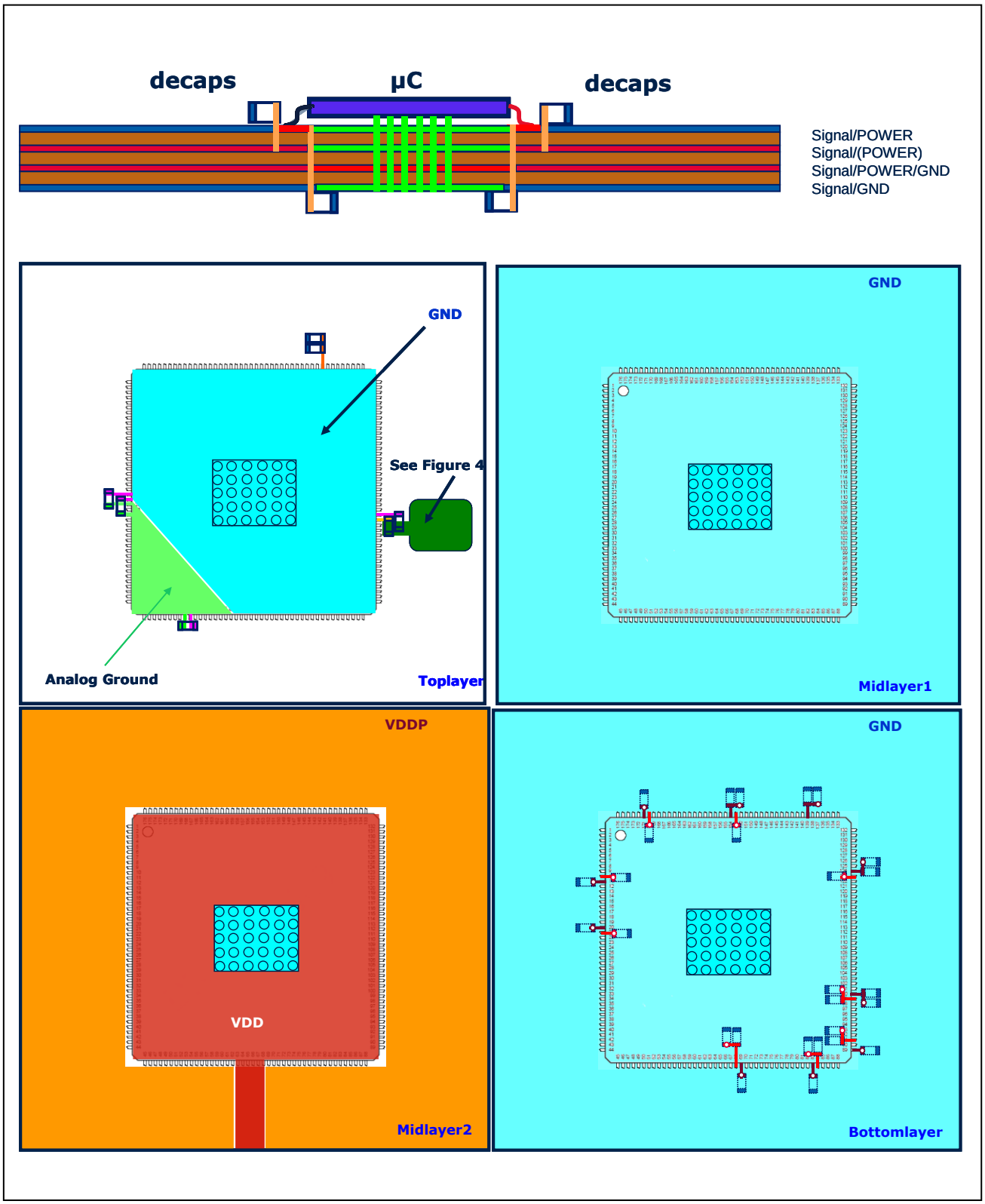

Figure 3 Layout example for decoupling of TC1782 (LQFP-176)

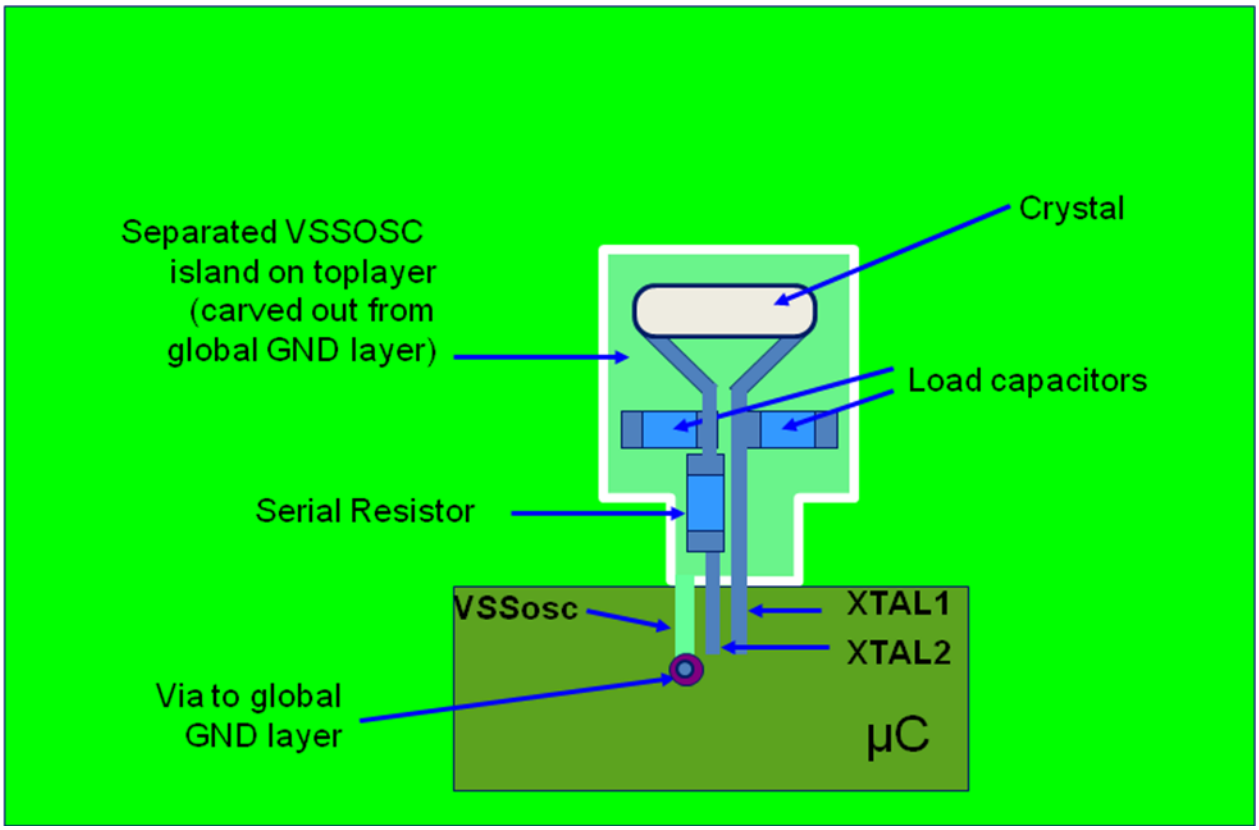

Figure 4 Layout proposal oscillator circuit

2.2 Decoupling Capacitor List:

Number	Capacitor	Supply	Pins(LQFP-176)	Comments
C1	47nF	VDDP	11	
C2	47nF	VDDP	20	
C3	47nF	VDDP	69	
C4	47nF	VDDP	83	
C5	47nF	VDDP	89	
C6	47nF	VDDP	100	1x100nF can be used for C6 & C6-1
C6-1	47nF	VDDP	100	
C7	47nF	VDDP	124	1x100nF can be used for C7 & C7-1
C7-1	47nF	VDDP	124	
C8	47nF	VDDP	139	1x100nF can be used for C8 & C8-1
C8-1	47nF	VDDP	139	
C9	47nF	VDDP	154	1x100nF can be used for C9 & C9-1
C9-1	47nF	VDDP	154	
C10	47nF	VDDP	171	
C11	47nF	VDD	10	
C12	47nF	VDD	68	1x100nF can be used for C12 & C12-1
C12-1	47nF	VDD	68	
C13	47nF	VDD	84	1x100nF can be used for C13 & C13-1
C13-1	47nF	VDD	84	
C14	47nF	VDD	91	1x100nF can be used for C14 & C14-1
C14-1	47nF	VDD	91	
C15	47nF	VDD	99	1x100nF can be used for C15 & C15-1
C15-1	47nF	VDD	99	
C16	47nF	VDD	123	
C17	47nF	VDD	153	
C18	47nF	VDD	170	
C19	47nF	VDD	21	
C20	47nF	VDDFL3	141	1x100nF can be used for C20 & C20-1
C20-1	47nF	VDDFL3	141	
C21	330 nF	VDDOSC	105	
C22	330 nF	VDDOSC3	106	
C23	47 nF	VDDAF	23	
C24	47 nF	VDDMF	24	
C25	47 nF	VDDM	54	

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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