

AP32137

TC1736

Design Guideline for TC1736 Microcontroller Board Layout

Microcontrollers



Never stop thinking

Edition 2008-12-18

**Published by
Infineon Technologies AG
81726 München, Germany**

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1 Overview

The TC1736 is a 32-Bit microcontroller in TQFP-144-pin package, which requires a carefully designed PCB concerning electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for TC1736 are discussed here.

1.1 General Informations:

The microcontroller has three supply domains (VDD = 1.5V for Core, VDDP = 3.3V for I/O Pad, VDDM = 3.3V or 5V for ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1736

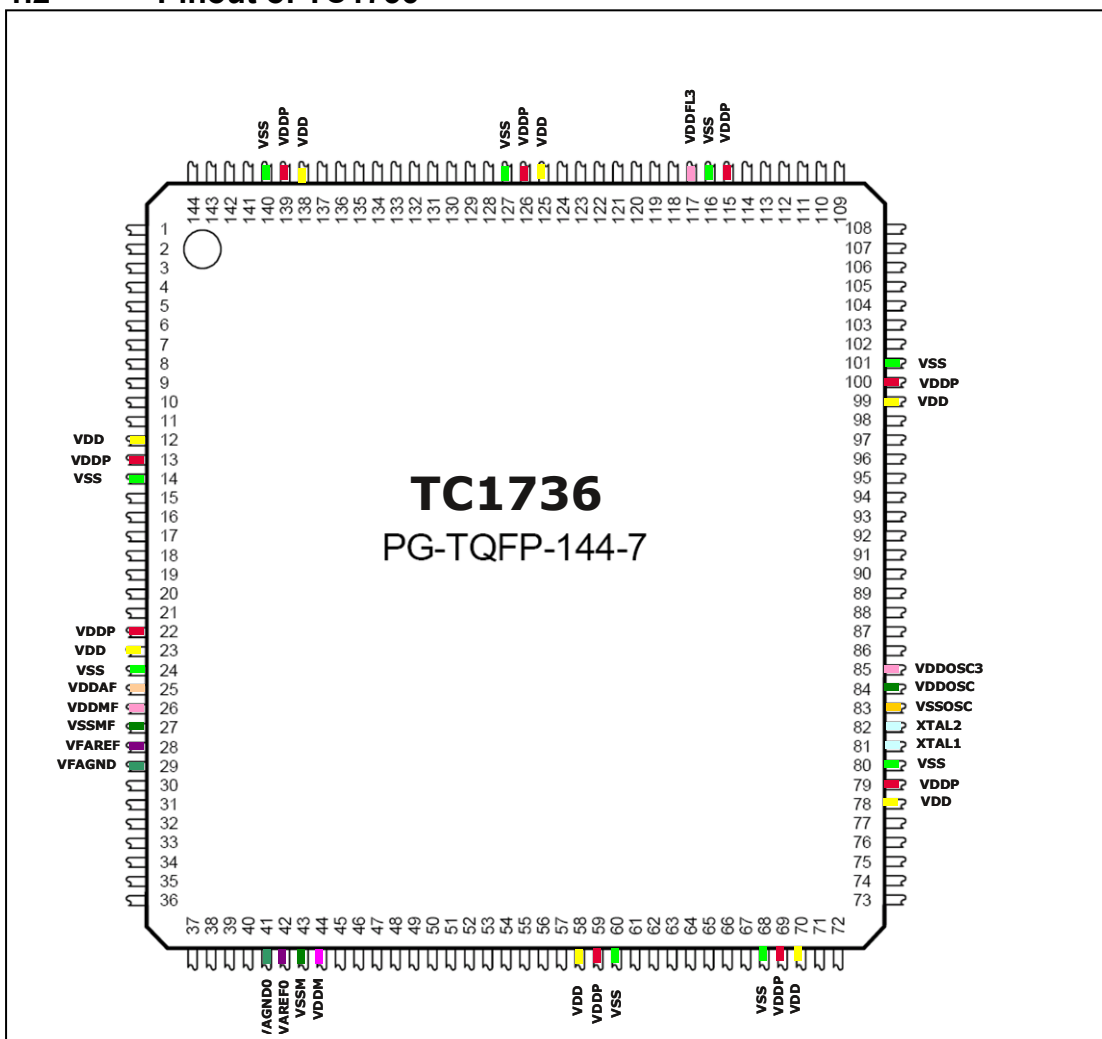


Figure 1 Pinout of TC1736 (TQFP-144):

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
 - SYSCLK: System clock output
 - Supply pins

Route these signals with adjacent ground reference and avoid signal and reference layer changes.

Route them as short as possible.

Routing ground on each side can help to reduce coupling to other signals.

- For unused **“Output, Supply, Input and I/O”** pins following points must be considered:

1. Supply Pins (Modules) :	<ul style="list-style-type: none"> • See the User’s Manual.
2. I/O-Pins:	<ul style="list-style-type: none"> • Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins :	<ul style="list-style-type: none"> • Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4. Input Pins without internal pull device:	<ul style="list-style-type: none"> • For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device:	<ul style="list-style-type: none"> • For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User’s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:
 - Separate analog and digital grounds.
 - The analog ground must be separated into two groups:
 1. Ground for OSC and PLL (VSSOSC for VDDOSC and VDDOSC3) as common star point.
 2. Ground for ADC (VSSM for VDDM, VSSMF for VDDMF/VDDAF) as common star point.
- To reduce the radiation / coupling from oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the

load capacitors and VSSOSC should also be connected to this island. Traces for load capacitors and Xtal should be as short as possible.

- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3, VDDMF, and VDDAF. Using inductance or ferrite beads (5 – 10 μ H) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dB μ V on the related supply net. (See Figure 2).
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32111).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

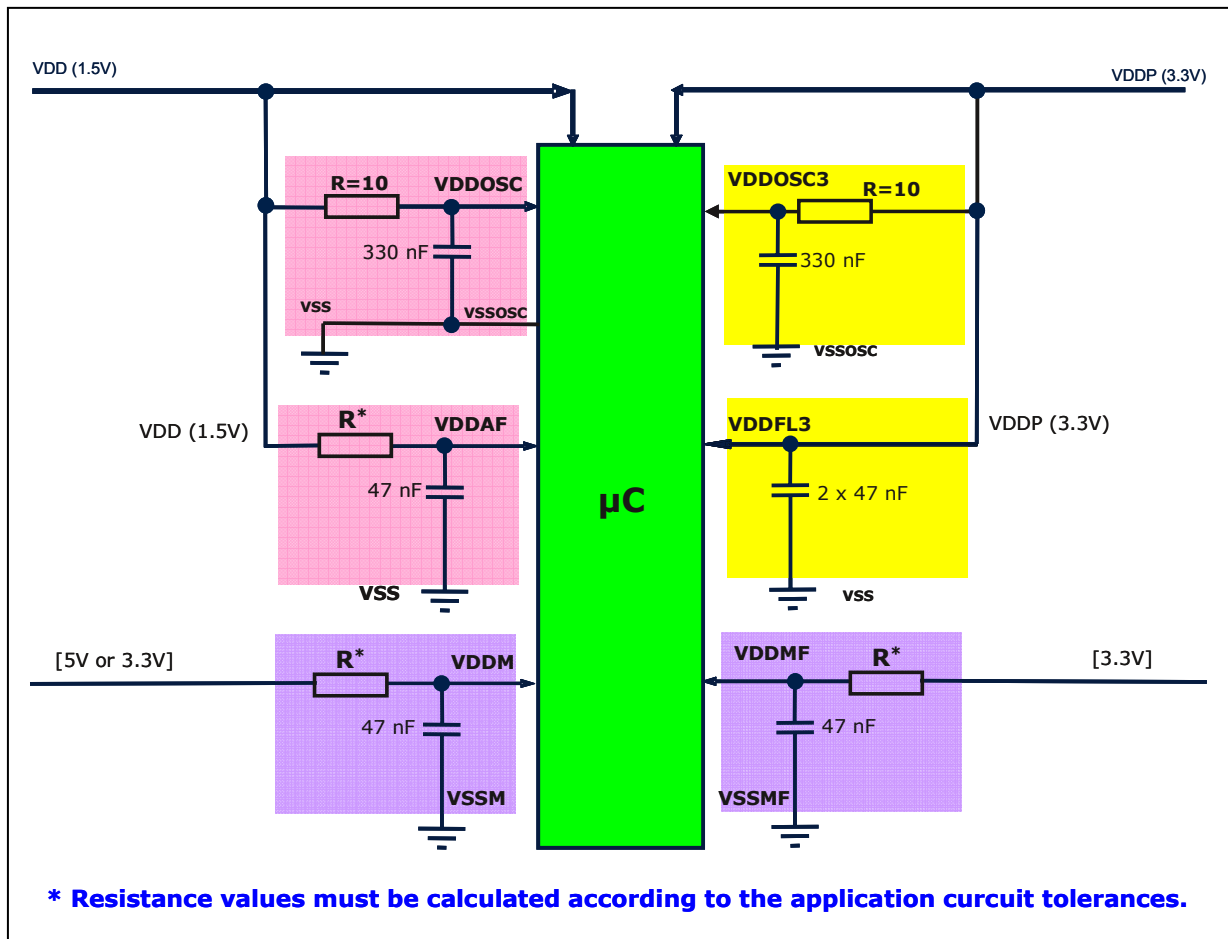


Figure 2 Filtering of VDDOSC, VDDOSC3, VDDFL3, VDDDM, VDDMF, VDDAF supply pins

2.1 Decoupling

- The two supply domains VDD and VDDP of TC1736 should be decoupled separately (see decoupling layout example in Figure 3).
- Type of capacitors:
 - Values: 47 nF, 330 nF
 - X7R Ceramic Multilayer (Low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND layer.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and power/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

A power-plane/grounding concept example for a 32-bit microcontroller like TC1736 with TQFP-144 package can be seen in Figure 3. Alternative implementations are also acceptable and must be evaluated within application by customer.

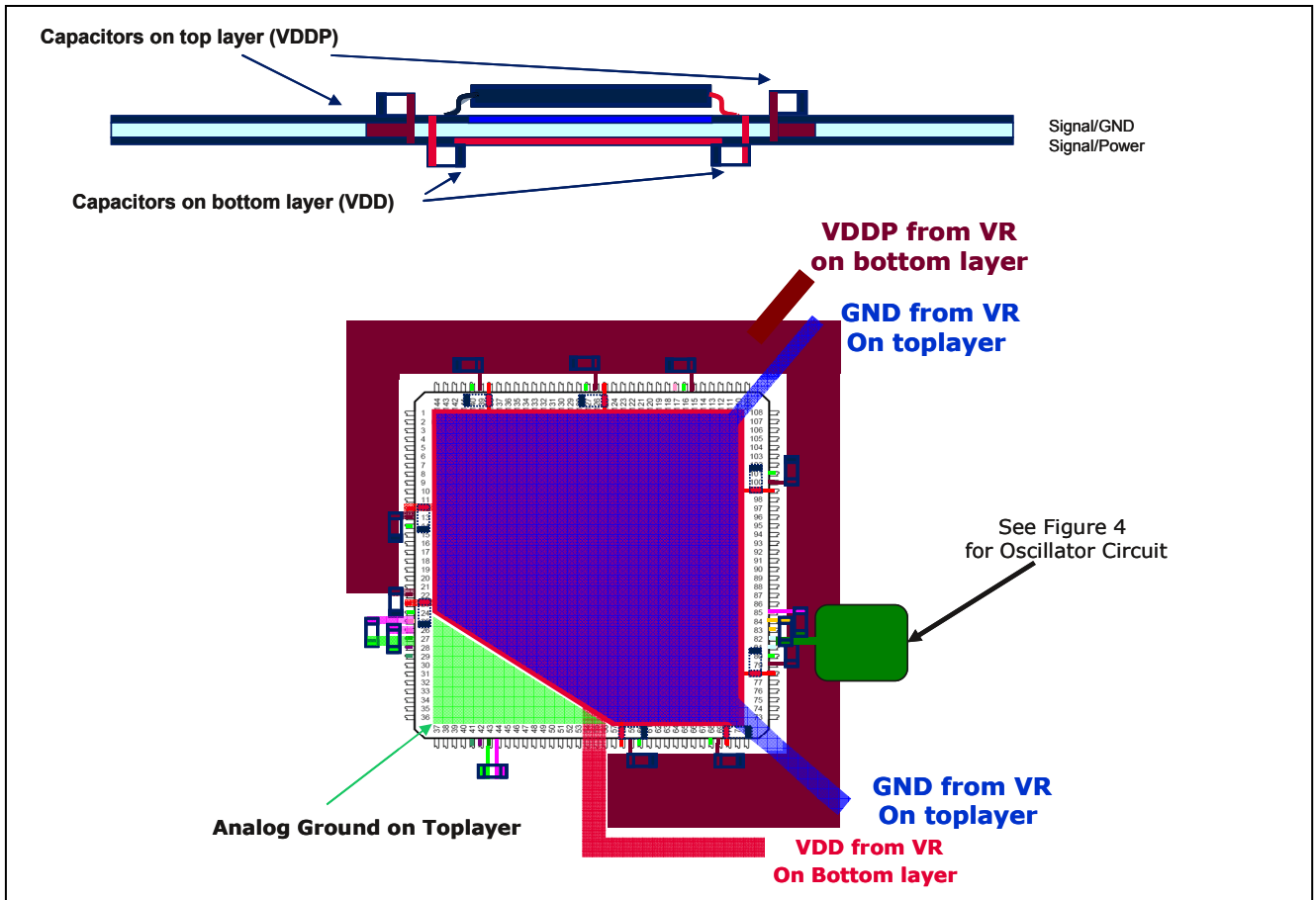


Figure 3 Layout example for decoupling of TC1736 (LQFP-176)

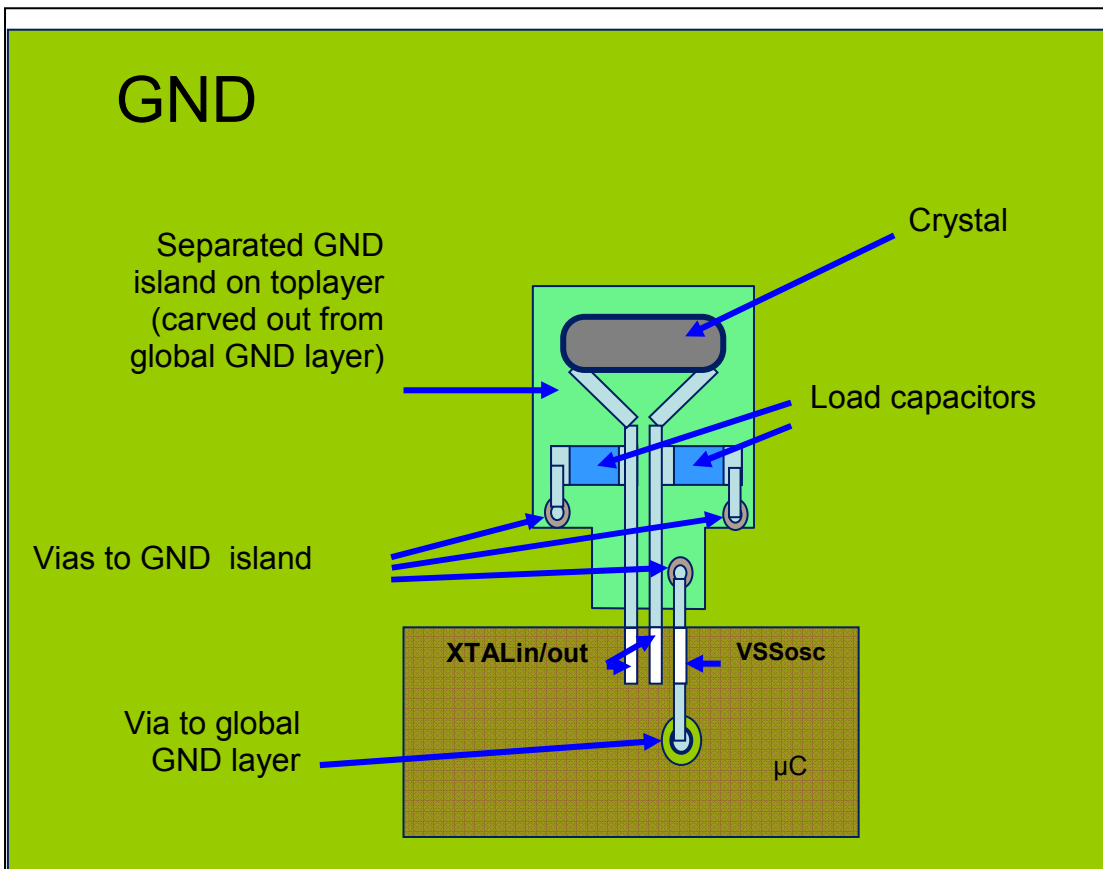


Figure 4 Layout proposal oscillator circuit

2.2 Decoupling Capacitor List:

Capacitor	Supply	Pins(TQFP-144)
47nF	VDDP	13
47nF	VDDP	22
47nF	VDDP	59
47nF	VDDP	69
47nF	VDDP	79
47nF	VDDP	100
47nF	VDDP	115
47nF	VDDP	126
47nF	VDDP	139
47nF	VDD	12
47nF	VDD	23
47nF	VDD	58
47nF	VDD	70
47nF	VDD	78
47nF	VDD	99
47nF	VDD	125
47nF	VDD	138
47nF	VDDFL3	117
330 nF	VDDOSC	84
330 nF	VDDOSC3	85
47 nF	VDDAF	25
47 nF	VDDMF	26
47 nF	VDDM	44

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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