Application Note, V1.1, September 2006

AP32111

Scalable Pads

Electrical Specification of Scalable Output Drivers in 130nm CMOS Technology

Valid for Microcontrollers:
TC1766, TC1767, TC1796, TC1797

Microcontrollers

Never stop thinking.

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all	Added TC1767 & TC1797 to scope of appnote; valid for Audo-NG & Audo-Future	

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1 Preface

Output driver scaling, also referred to as „slew rate control“, is an effective technique to reduce the electromagnetic emission of an integrated circuit by reducing the driver strength and/or smoothing the rising and falling edges of one or more pad output drivers.

Output driver scaling makes sense only when a certain margin regarding signal frequency and/or capacitive output load is available. Any driver scaling must maintain proper signal integrity.

This application note presents a huge set of output driver characterization data which shall enable the system designers to select proper driver settings to reduce the electromagnetic emission caused by the driver switching while maintaining the desired signal integrity. Parameters under consideration are switching frequency, capacitive output load and ambient temperature.

Chapter 2 introduces physical basics behind the scaling.

Chapter 3 provides a set of measured rise/fall times under various conditions.

Chapter 4 documents rise/fall time simulations performed on PCB models of different signal routing structures.

Chapter 5 shows a set of measured electromagnetic emission under various conditions.

Chapter 6 shows a set of simulated electromagnetic emission under various conditions.

Chapter 7 recommends useful settings for the drivers by introducing signal categories and giving lots of decision tables and graphs.

The application note ends with a glossary.

The information given in this application note is valid for Infineon Audo-NG and Audo-Future microcontrollers of the TriCore family, fabricated in 130nm CMOS technology.

All measurement data are derived from a center lot device of the TC1796-BD step, using the same pad library as all other Audo-NG and Audo-Future microcontrollers.

Please note that all numbers given in this application note are no specification values. They are guaranteed by design without being monitored during the IC fabrication process. The numbers are based on timing measurements performed on center lot devices. Thus all values are subject to ca. 10% offset depending on parameter variations like fabrication process and pad supply voltages different from nominal conditions. The final selection of driver settings in system applications should consider this offset.

General note: Whenever Class B2 drivers are referenced, the same data is valid for Class B1 drivers. Reason is that the physical designs of Class B1 and Class B2 drivers are similar.

2 Introduction

Output driver scaling, also referred to as „slew rate control“, is an effective technique to reduce the electromagnetic emission of an integrated circuit by smoothing the rising and falling edges of one or more pad output drivers. This scaling is introduced by setting corresponding control bits in registers. Fig. 1 shows an example of a pad driver control register, taken from the XC161 specification. While the location and function of the control bits may differ among the available Infineon microcontrollers, the electrical effects caused by these bits remain similar for a given technology.

2.1 Pad driver scaling in detail

2.1.1 Driver characteristics

Basically, we distinguish between driver control and edge control. Driver control bits set the general DC driving capability of the respective driver. Reducing the driver strength increases the output's internal resistance which attenuates noise that is imported/exported via the output line.

For a given external load, charging and discharging time varies with the driver strength, thus the rise/fall times will change accordingly. For driving LEDs or power transistors, however, a stable high output current may still be required independent of low toggle rates which would normally allow to decide for weak drivers due to their low transitions and thus low noise emission.

The controllable output drivers of the microcontroller pins feature three differently sized transistors (strong, medium, and weak) for each direction (push and pull). The time of activating/deactivating these transistors determines the output characteristics of the respective port driver.

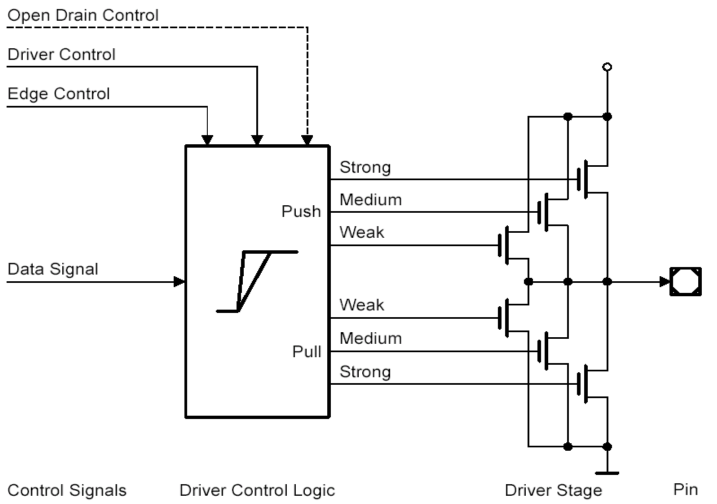


Figure 1: Pad output driver schematic

The strength of the driver can be selected to adapt the driver characteristics to the application's requirements:

In **Strong Driver Mode**, the medium and strong transistors are activated. In this mode the driver provides maximum output current even after the target signal level is reached. Strong drivers are only implemented in the Class A2/B2 drivers. Class A1 drivers offer only medium and weak drivers.

In **Medium Driver Mode**, only the medium transistor is activated while the other transistors remain off.

In **Weak Driver Mode**, only the weak transistor is activated while the other transistors remain off. This results in smooth transitions with low current peaks (and reduced susceptibility for noise) on the cost of increased transition times, i.e. slower edges, depending on the capacitive load, and low static current.

Selection of the Driver Characteristics for Class A1 drivers

PDx.2	PDx.1	PDx.0	Functionality
X	X	0	medium driver
X	X	1	weak driver

Selection of the Driver Characteristics for Class A2 drivers

PDx.2	PDx.1	PDx.0	Functionality
0	0	0	strong driver, sharp edge
0	0	1	strong driver, medium edge
0	1	0	strong driver, soft edge
0	1	1	weak driver
1	0	0	medium driver
1	0	1	medium driver
1	1	0	medium driver
1	1	1	weak driver

Figure 2: Port output control bit settings

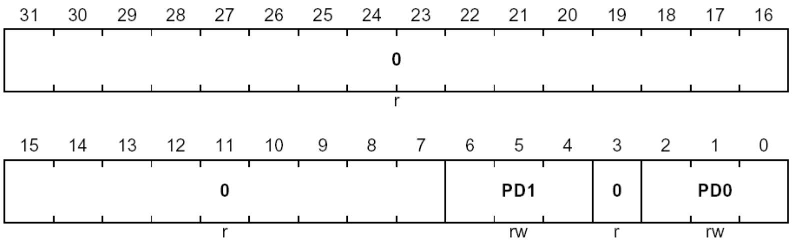
2.1.2 Edge Characteristics

This defines the rise/fall time for the respective output, i.e. the output transition time. Soft edges reduce the peak currents that are drawn when changing the voltage

level of an external capacitive load. For a bus interface, however, sharp edges may still be required. Edge characteristic effects the pre-driver which controls the final output driver stage.

The Port Output Control registers Px_PDR provide the corresponding control bits. A 4-bit control field configures the driver strength and the edge shape. Word ports consume four control nibbles each, byte ports consume two control nibbles each, where each control nibble controls 4 pins of the respective port. Fig. 2 shows the allocation of control bit fields and port pins. Fig. 3 gives an example of a Px_PDR register.

P0_PDR
Port 0 Pad Driver Mode Register **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
PD0	[2:0]	rw	**Pad Driver Mode for P0.[7:0]**
PD1	[6:4]	rw	**Pad Driver Mode for P0.[15:8]**
0	3, [31:7]	r	**Reserved;** read as 0; should be written with 0.

Figure 3: ***Control register example for Port0***

In this guideline, the scaling effects of output drivers fabricated in 130nm CMOS technology is described. It serves as a reference addendum to the respective microcontroller product specifications where the individual bit settings can be found.

2.2 Physical basics

Two main constraints have to be met when deciding for a certain clock driver setting: signal integrity and power integrity. Both issues will be discussed after a general introduction to capacitive load charging.

2.2.1 Load charging

Generally, a switching transistor output stage delivers charge to its corresponding load capacitor during rising edge and draws charge from its load capacitor during falling edge. Timing diagrams normally show the signal's voltage over time characteristics. However, the resulting timing is a result of the electrical charge transfer described above. Charge is transferred by flowing current.

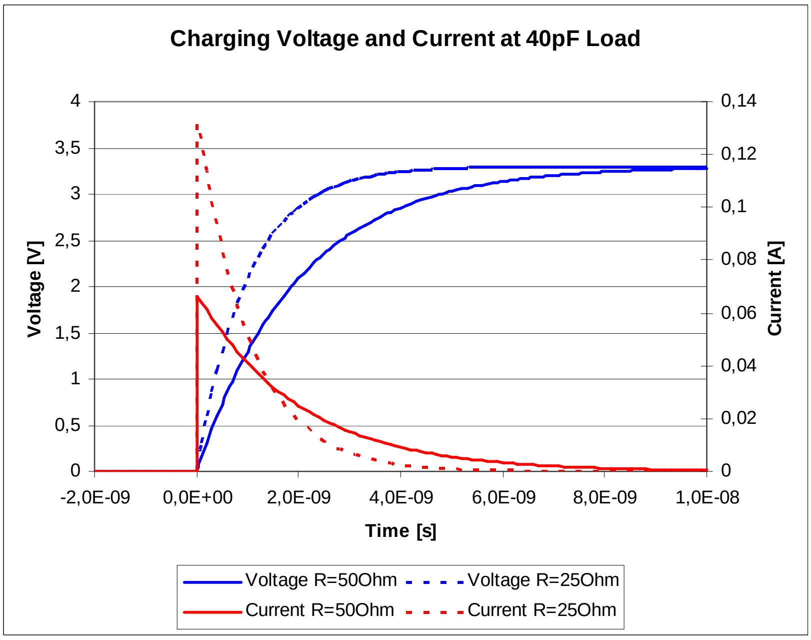


Figure 4: Current-/voltage charging curves for different driver strengths

A bigger pad driver means a smaller resistance in the loading path of the external load. Fig. 4 shows the load current and voltage of two examples of pad drivers connected to a load of C=40pF. The strong driver has on output resistance of 25Ω, the weak driver 50Ω. For times t<0, the output voltage is 0V. At t=0, the load capacitor C is connected to the target output voltage U=3.3V via the respective driver pullup transistor. As a reaction, the load current steps immediately to the value I=U/R. I is bigger for smaller values of R. This means that the strong driver generates a bigger current jump and charges the load capacitor in a shorter time.

In time domain this leads to bigger reflections for not adapted driver impedances. Since typical trace impedances range from 60 to 120Ω , a strong driver with Z=10Ω is poorly adapted and may cause

big voltage over- and undershoots. A weak driver with Z=100Ω may fit perfectly and generate a clean voltage switching signal without over- or undershoots. These effects are discussed in chapter 2.2.2.

In frequency domain, the current peak which is resulting from the charging of the load capacitor and from the over- or undershoots, causes significant RF energy and thus electromagnetic emission on the pad power supply. These effects are discussed in chapter 2.2.3.

Not only the pad driver impedance, but also the connected capacitive load determines the electromagnetic emission amplitudes. Fig. 5 illustrates the differences in charging current and voltage between a capacitive load of 40pF and one of 20pF. In both cases, the driver impedance is set to 50Ω.

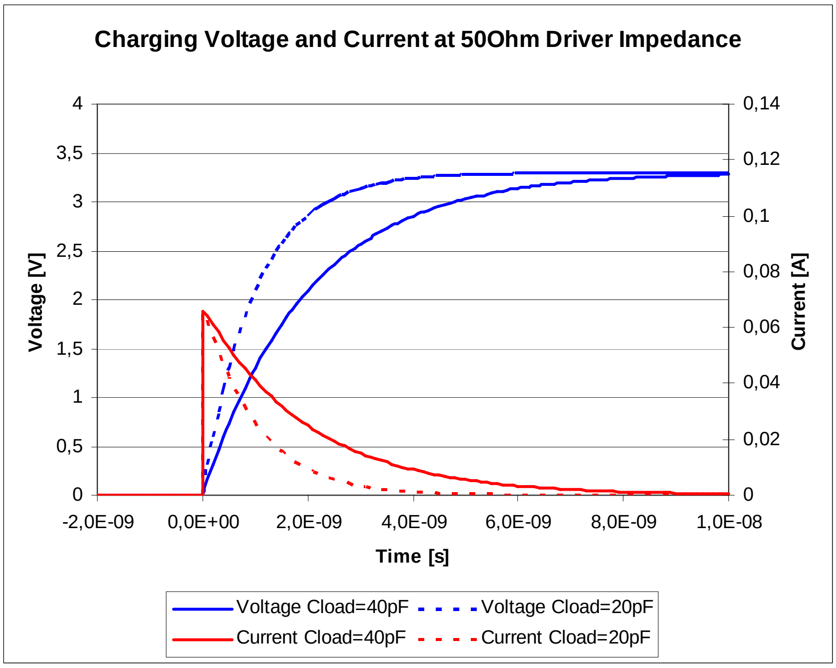


Figure 5: Current-/voltage charging curves for different capacitive loads

As expected, the charging voltage increases faster for a smaller load. However, the starting value of the charging current is only determined by the driver impedance and is thus load-independent. The load affects only the speed of load current decrease. It decreases faster if the load is smaller. This means on the other hand a bigger di/dt for smaller loads, resulting in higer emission for smaller loads.

This disadvantage can be compensated by chosing a smaller pad driver, i.e. a weaker driver setting, causing bigger driver impedance and thus smaller di/dt for the charging current.

The selection of a weaker driver setting slows down the pad switching time, so care must be taken to maintain the required signal integrity.

2.2.2 Signal integrity

Maintaining signal integrity means to select the rise/fall times such that all signal handshaking and data communication timing and levels are ensured for proper system operation. This means the data interchange between the microcontroller and external ICs like Flash memory, line drivers, receivers and transmitters etc. runs properly.

Therefore, it has to be taken into account that CMOS transistors become slower with rising temperature. Thus the timing of a critical signal has to be matched for proper operation at highest ambient temperature. Depending on the application, common temperature ranges are up to 85°C or up to 125°C. Several automotive control units specify an ambient temperature range from

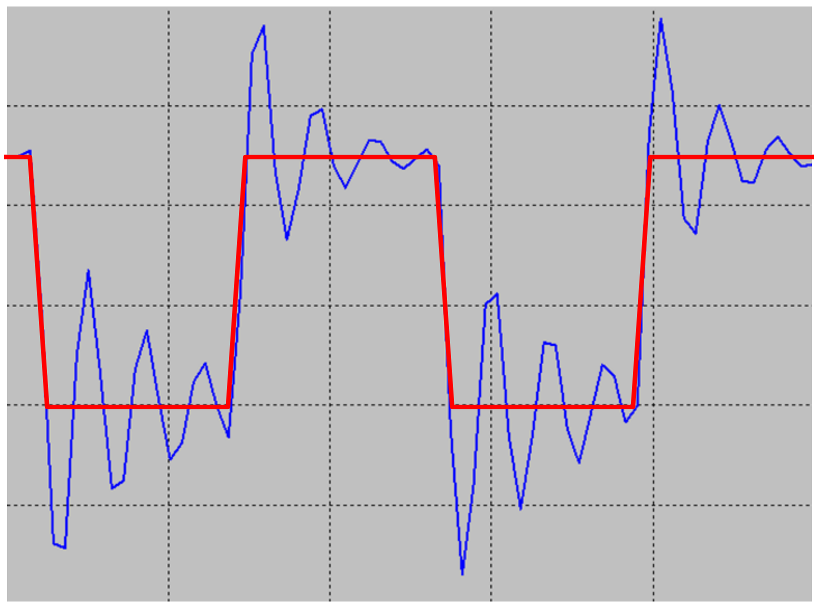


Figure 6: Signal over- and undershoots

-40°C up to 125°C. The die temperature may reach values up to 150°C during operation.

Rules:

- Choose driver characteristics to meet the DC driving requirements. Make sure that the DC current provided by the microcontroller's pad drivers is sufficient to drive actuators into the desired logic state.
- Choose edge settings to meet system timing constraints at the highest system temperature. Avoid selection of driver settings which are "too strong" for the signal timing and load capacitance. Otherwise unnecessarily fast signal edges would result, causing two disadvantages regarding electromagnetic emission: (1) The slopes are too fast and cause undesired high emission energy at higher frequencies; (2) Over- and undershoot appears with the danger of power/ground bounce affecting the accuracy of analog modules.
- If system timing requires short signal rise/fall times, series termination is recommended to avoid over-/undershoot at signal transitions, see Fig. 5. The value of the termination resistor has to be chosen identical to the signal line impedance.

2.2.3 Power integrity / Electromagnetic emission

Any switching between low and high voltage levels generates RF noise. This happens whenever the switching voltage or the switching current has no sinusoidal shape. Switching currents are mainly responsible for electromagnetic emission because of the voltage drop across line inductances such as bond wires and lead frames. Any shapes other than sinusoidal are composed by the overlay of multiple frequencies, also known as harmonics. To reach a significantly steep edge of a trapezoidal voltage of a clock signal, short current pulses during the edges are required. These switching currents are outlined as nearly triangular peaks which are composed from the base frequency and a set of odd and even harmonics, depending on the exact pulse shape.

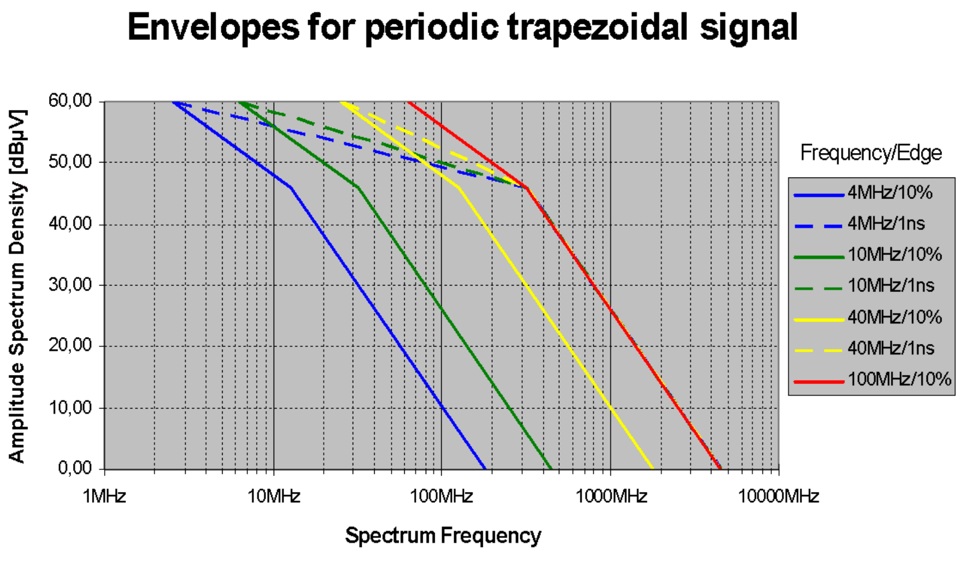


Figure 7: Spectrum envelope for different clocks and edges

The steeper a switching pulse is, the higher frequencies are required to form the rising and falling edges. A rise time of 1ns leads to a spectrum composed from harmonics up to at least 500 MHz.

A typical clock signal consists of 10% rise time, 40% high level, 10% fall time and 40% low level. Operating at 100MHz – equal to 10ns period time – this clock signal already generates at least harmonics up to 500MHz.

Unfortunately not the clock frequency, but the rise/fall times determine the resulting RF spectrum. Even if a clock driver operates at a relatively low toggle rate, it may generate the same RF spectrum as if it would operate at a significantly higher toggle rate – as long as its rise/fall times are not adjusted to the lower toggle rate by slowing down the transitions. For example, if the mentioned 100MHz clock driver operates at only 10 MHz, its rise/fall times should be extended from 1 ns to 10 ns, still maintaining the 10% ratio relatively to the clock period time. Fig. 6 illustrates that behaviour.

Rule:

- Choose driver and edge characteristics to result in lowest electromagnetic emission while meeting all system timing requirements at highest system temperature.

3 Measured Timings

3.1 Load conditions and ambient temperatures

The Audo-NG and Audo-Future microcontrollers use several classes of pad drivers: Class A drivers are operated at VDDP=3.3V (nominal) and Class B drivers are operated at VDDE (EBU) in the range between 2.5V and 3.3V (nominal).

3.1.1 Measurement conditions used in this document

- A temperature range from T_A=-40°C to T_A=125°C is covered for the timings. Timings were measured at temperatures -40°C, 0°C, 30°C, 85°C, 110°C and 125°C. Please note that even if signal integrity looks fine at higher temperature, over- or undershoot resulting from improper impedance matching between pad drivers and external load may increase at lower temperature.
- If the user is interested in rise/fall time values at other temperatures, a linear interpolation can be done.
- Electromagnetic emission is always measured at T_A=25°C.
- The supply voltage for Class A pad drivers is 3.30V for measurements at T_A=30°C.
- The supply voltage for Class A pad drivers is 3.13V for measurements at T_A>30°C to match worst-case conditions.
- The supply voltage for Class A pad drivers is 3.47V for measurements at T_A<30°C.
- Class B pad driver timings have not been measured, but only simulated.

Load capacitors are selected in a way that together with the measurement probe capacitance of 8pF total capacitance values of 18pF up to 55pF are reached. Table 1 shows the reference between real loads and numbers given in the result diagrams. For easy reading, these capacitances are referred to as 20, 30, 40 and 50 pF in the result diagrams.

Probe capacitance	SMD load capacitor	Resulting physical capacitance	Referred capacitance
8 pF	10 pF	18 pF	20 pF
8 pF	22 pF	30 pF	30 pF
8 pF	33 pF	41 pF	40 pF
8 pF	47 pF	55 pF	50 pF

Table 1: Overview of capacitive loads used for timing measurements

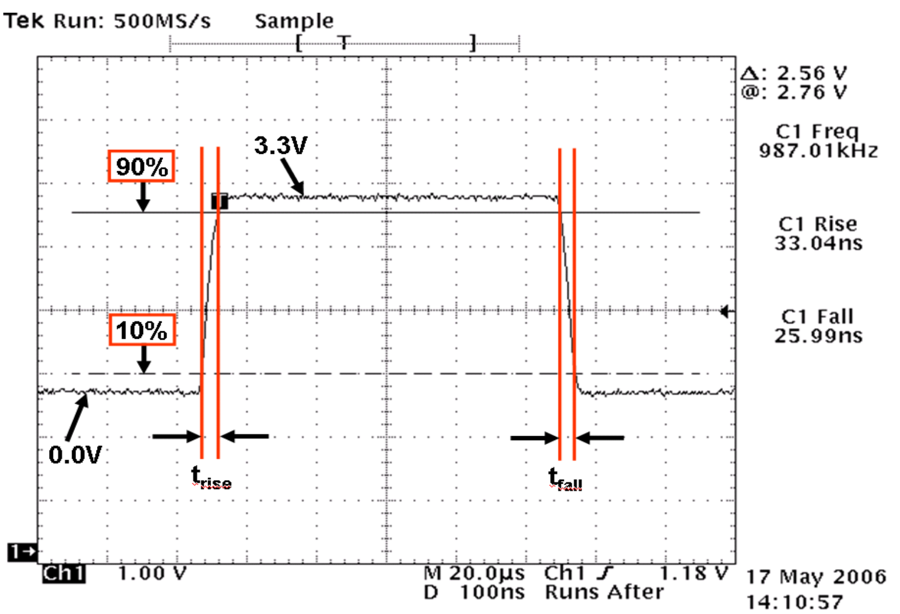


Figure 8: Voltage level references for Class A timing measurements

The result diagrams show the simulated rising and falling edge timing using an oscilloscope probe of 8pF||1MΩ. The reference points are 10% and 90% as indicated in Fig. 8 for Class A2 pads (VDDP = 3.3V).

For measurements at T_A=30°C, the pad supply voltage VDDP has been set to 3.30V (nominal VDDP). Thus the voltage levels references for timing measurements at T_A=30°C are: 0.33V (low reference) and 2.97V (high reference).

For measurements at T_A>30°C, the pad supply

voltage VDDP has been decreased to 3.13V (nominal VDDP minus 5%). Thus the voltage levels references for timing measurements at T_A>30°C are: 0.31V (low reference) and 2.82V (high reference).

For measurements at T_A<30°C, the pad supply voltage VDDP has been increased to 3.47V (nominal VDDP plus 5%). Thus the voltage levels references for timing measurements at T_A<30°C are: 0.35V (low reference) and 3.12V (high reference).

The probing point for timing measurements is connected to the pin under test via a straight 3 cm long 50 Ohm trace without via contacts.

3.1.2 Measured rise and fall times

Fig. 9-38 show the measured 10-90% rise times and 90-10% fall times of all Class A2 driver strengths at T_A=-40°C, 0°C, 30°C, 85°C, 110°C and 125°C. The physically connected load capacitor values are according the "Referred capacitances" listed in Table 1. The abbreviations used for driver strength and load description are listed in Table 2. The respective load capacitor is connected close to the driver pin. It is connected from the pin to GND. GPIO measurements have been done at Port 2.2 of the TC1796 and are valid for all other Class A2 pins of the Audo-NG and Audo-Future microcontrollers fabricated in 0.13µm CMOS technology.

Table 3 lists the measured rise and fall times for all Class A2 driver settings at various ambient temperatures for two different capacitive loads. Fig. 9-38 show the waveforms of these measured rise and fall times.

Fig. 39-40 present the rise and fall times as a function of driver settings for ambient temperatures of 30°C and 125°C.

Fig. 41-45 present the rise and fall times as a function of ambient temperature for every driver setting with various capacitive loads.

Abbreviation	Driver strength	Resulting physical capacitance
SSH-20pF	Strong-sharp	18 pF
SSH-30pF	Strong-sharp	30 pF
SSH-40pF	Strong-sharp	41 pF
SSH-50pF	Strong-sharp	55 pF
SME-20pF	Strong-medium	18 pF
SME-30pF	Strong-medium	30 pF
SME-40pF	Strong-medium	41 pF
SME-50pF	Strong-medium	55 pF
SSO-20pF	Strong-soft	18 pF
SSO-30pF	Strong-soft	30 pF
SSO-40pF	Strong-soft	41 pF
SSO-50pF	Strong-soft	55 pF
MED-20pF	Medium	18 pF
MED-30pF	Medium	30 pF
MED-40pF	Medium	41 pF
MED-50pF	Medium	55 pF
WEA-20pF	Weak	18 pF
WEA-30pF	Weak	30 pF
WEA-40pF	Weak	41 pF
WEA-50pF	Weak	55 pF

Table 2: Abbreviations used in the timing result diagrams

20pF Load

Strong-Sharp

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	0.714	0.628
0	0.751	0.644
30	0.838	0.735
85	0.908	0.706
110	0.902	0.718
125	0.913	0.758

Strong-Medium

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	1.377	1.543
0	1.652	1.777
30	1.875	2.167
85	2.584	2.767
110	2.721	2.835
125	2.801	2.940

Strong-Soft

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	4.48	5.76
0	4.93	6.75
30	5.85	7.69
85	6.94	9.74
110	7.19	9.99
125	7.65	10.17

Medium

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	10.38	10.92
0	10.9	11.77
30	12.24	13.23
85	14.69	17.64
110	14.98	17.84
125	15.06	17.48

Weak

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	48.64	54.32
0	51.56	64.32
30	59.99	70.16
85	69.69	91.34
110	73.41	95.67
125	72.76	97.67

40pF Load

Strong-Sharp

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	1.626	1.503
0	1.66	1.494
30	1.733	1.495
85	1.866	1.549
110	2.041	1.605
125	2.038	1.607

Strong-Medium

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	2.577	3.083
0	3.016	3.384
30	3.53	3.82
85	4.303	4.667
110	4.767	4.912
125	4.587	5.176

Strong-Soft

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	6.23	9.84
0	6.74	9.94
30	7.52	12.41
85	9.33	15.05
110	9.93	16.57
125	10.85	17.88

Medium

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	28.02	19.38
0	33.56	21.33
30	33.04	25.99
85	42.97	30.91
110	45.79	33.26
125	45.12	36.24

Weak

Temperature(°C)	Rise Time(ns)	Fall Time(ns)
-40	130.64	118.67
0	143.67	123.32
30	147.99	131.59
85	172.91	165.06
110	187.52	179.5
125	194.91	191.5

Table 3: Measured rise and fall times for 20pF and 40pF capacitive load

3.1.3 Measured Rise/ Fall Time Waveforms

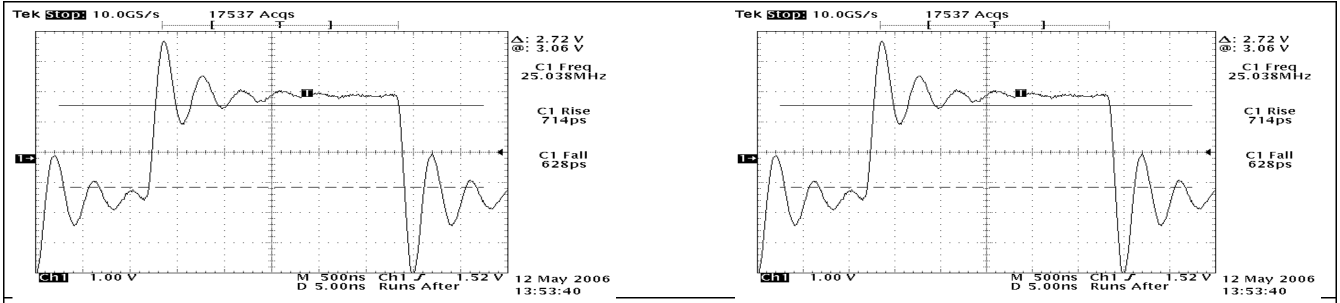


Figure 9: Waveforms Class A2 “Strong-Sharp” at -40°C ambient temperature

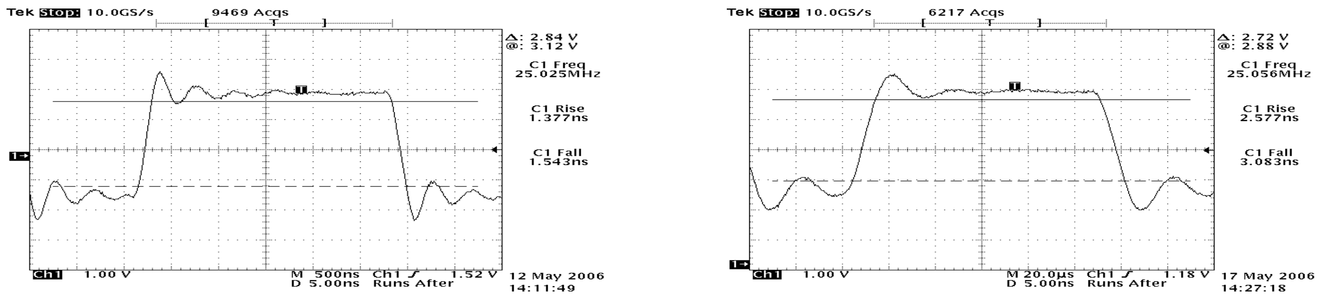


Figure 10: Waveforms Class A2 “Strong-Medium” at -40°C ambient temperature

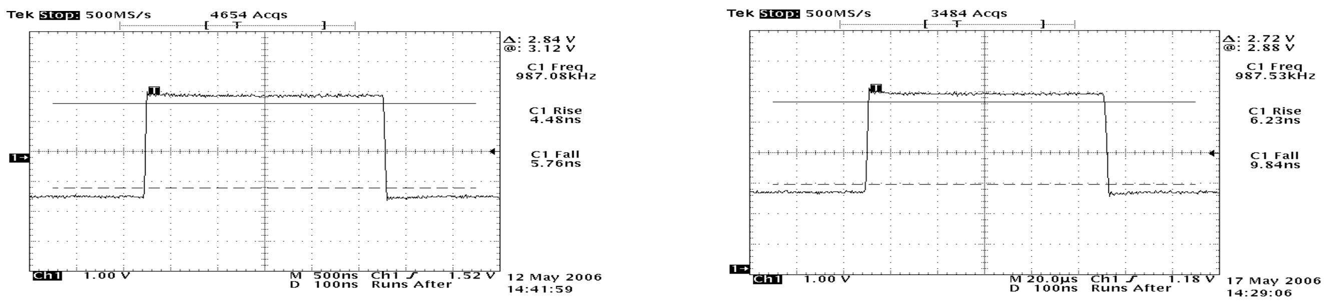


Figure 11: Waveforms Class A2 “Strong-Soft” at -40°C ambient temperature

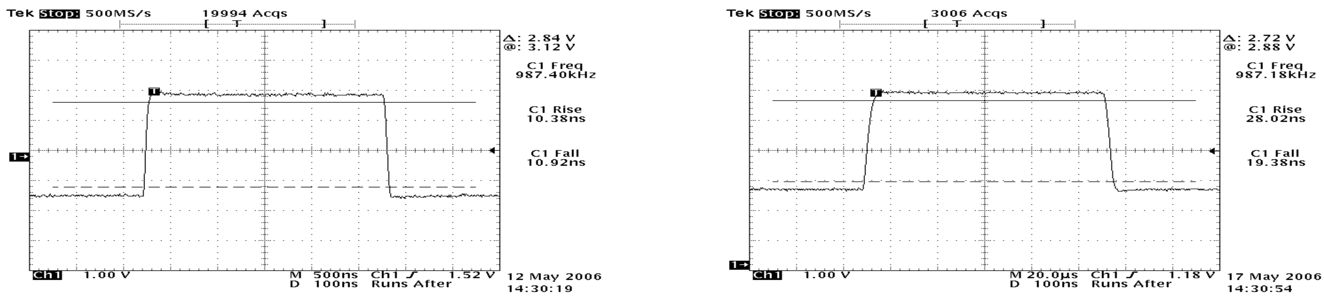


Figure 12: Waveforms Class A2 “Medium” at -40°C ambient temperature

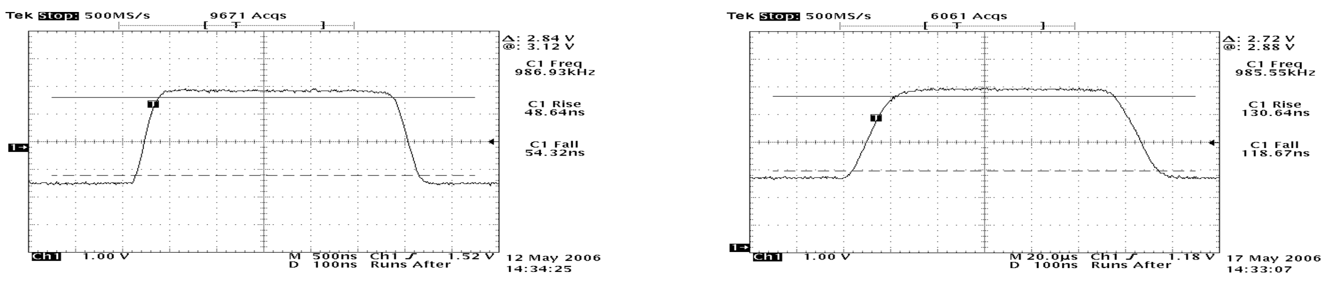


Figure 13: Waveforms Class A2 “Weak” at -40°C ambient temperature

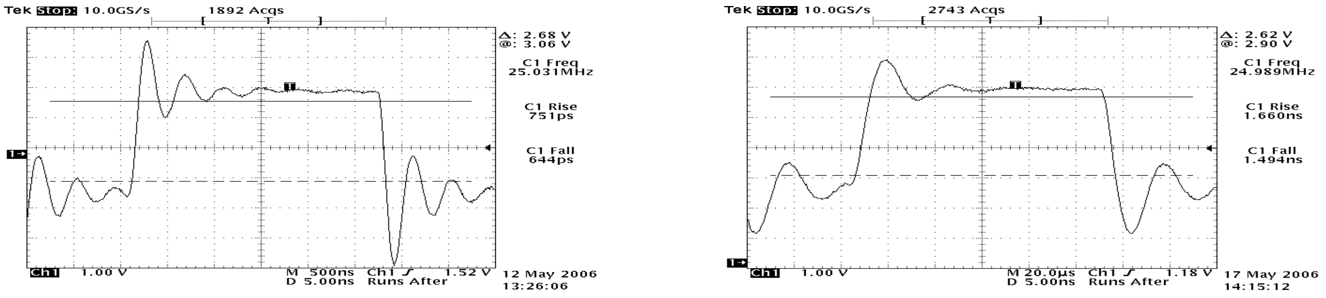


Figure 14: Waveforms Class A2 “Strong-Sharp” at 0°C ambient temperature

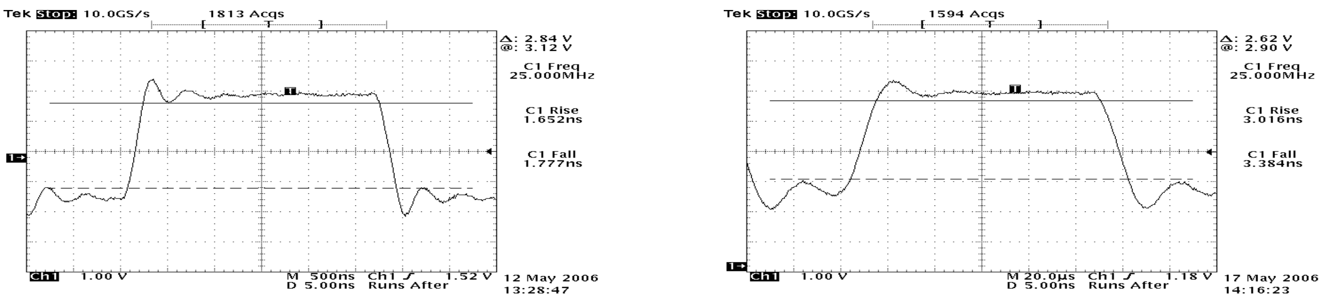


Figure 15: Waveforms Class A2 “Strong-Medium” at 0°C ambient temperature

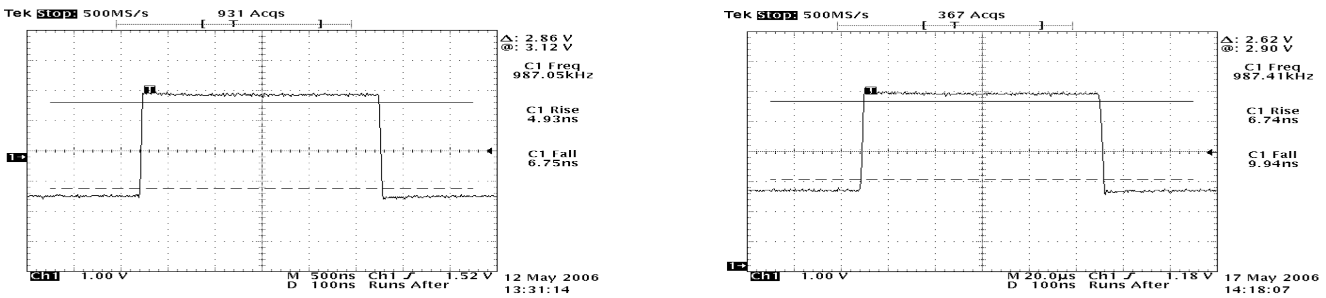


Figure 16: Waveforms Class A2 “Strong-Soft” at 0°C ambient temperature

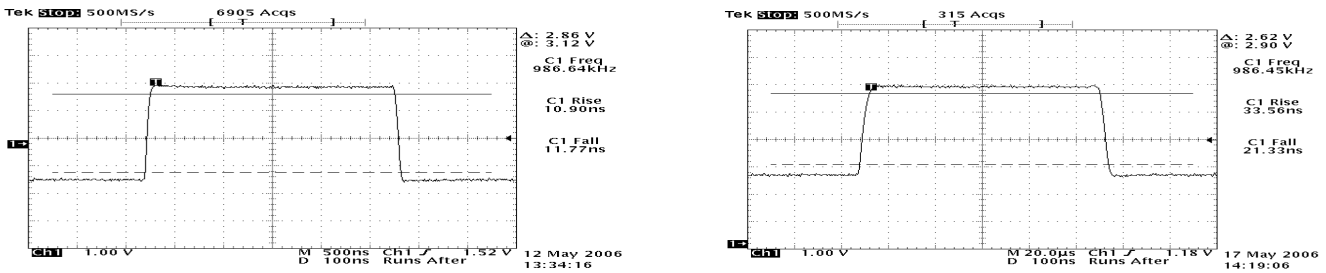


Figure 17: Waveforms Class A2 “Medium” at 0°C ambient temperature

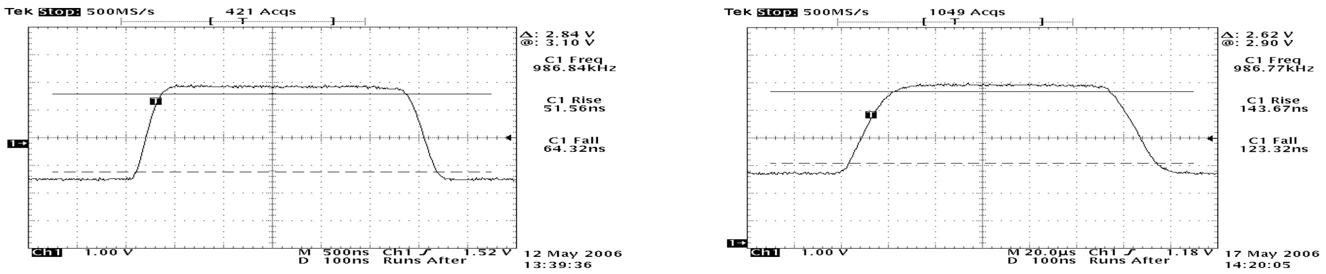


Figure 18: Waveforms Class A2 “Weak” at 0°C ambient temperature

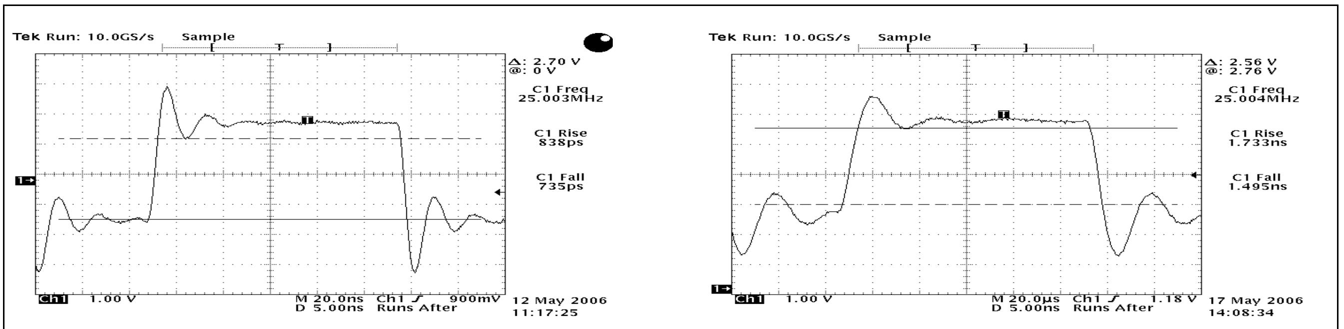


Figure 19: Waveforms Class A2 “Strong-Sharp” at 30°C ambient temperature

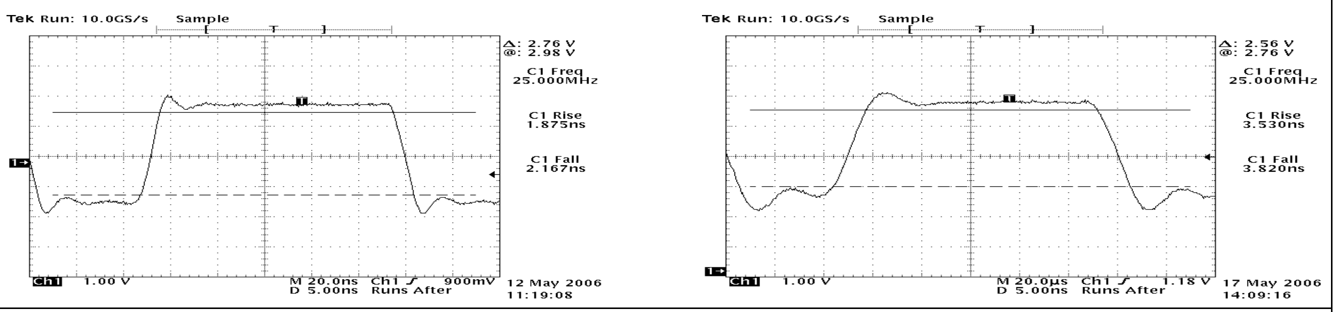


Figure 20: Waveforms Class A2 “Strong-Medium” at 30°C ambient temperature

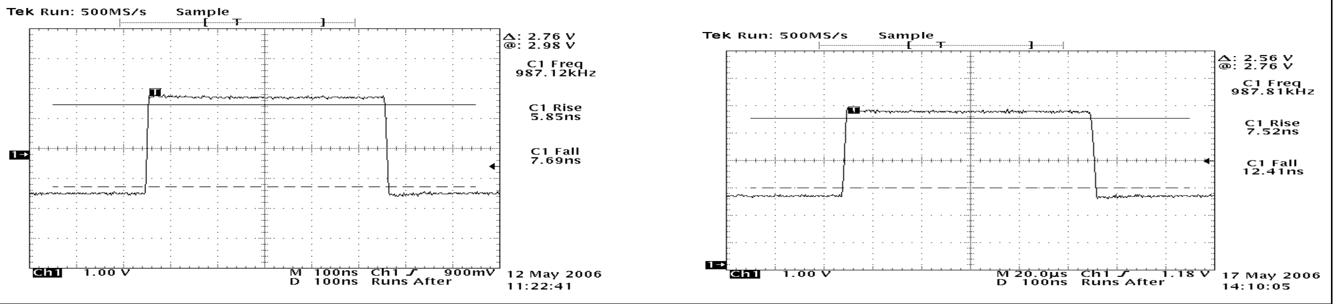


Figure 21: Waveforms Class A2 “Strong-Soft” at 30°C ambient temperature

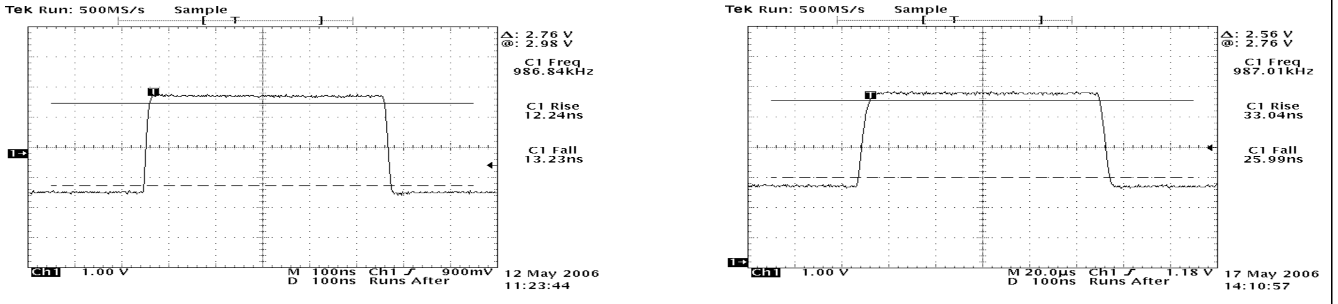


Figure 22: Waveforms Class A2 “Medium” at 30°C ambient temperature

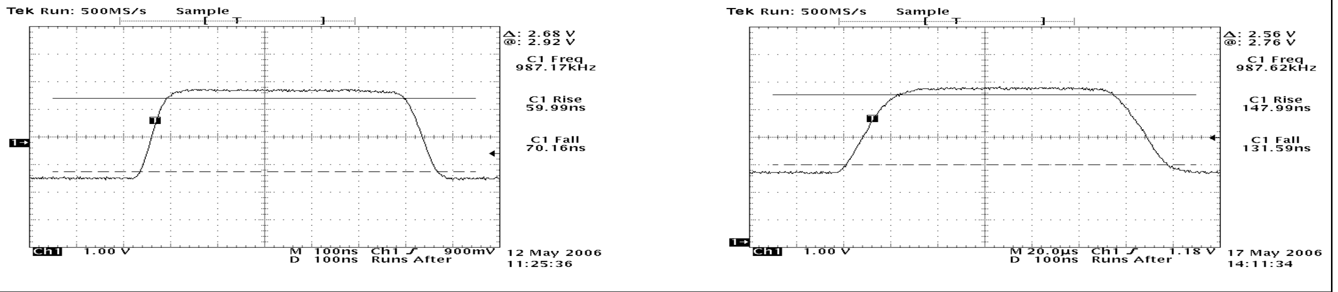


Figure 23: Waveforms Class A2 “Weak” at 30°C ambient temperature

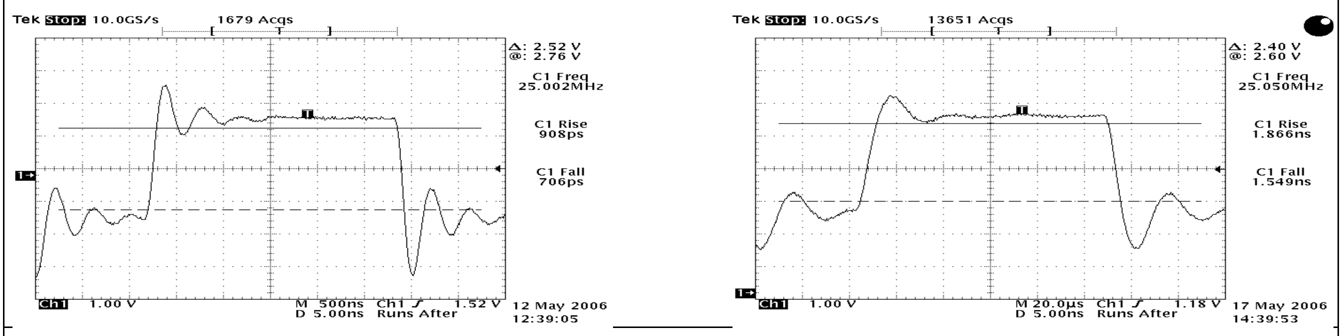


Figure 24: Waveforms Class A2 "Strong-Sharp" at 85°C ambient temperature

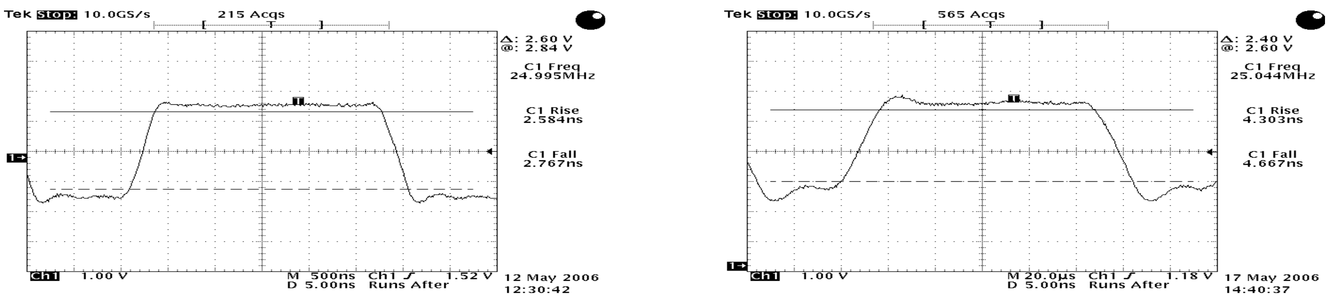


Figure 25: Waveforms Class A2 "Strong-Medium" at 85°C ambient temperature

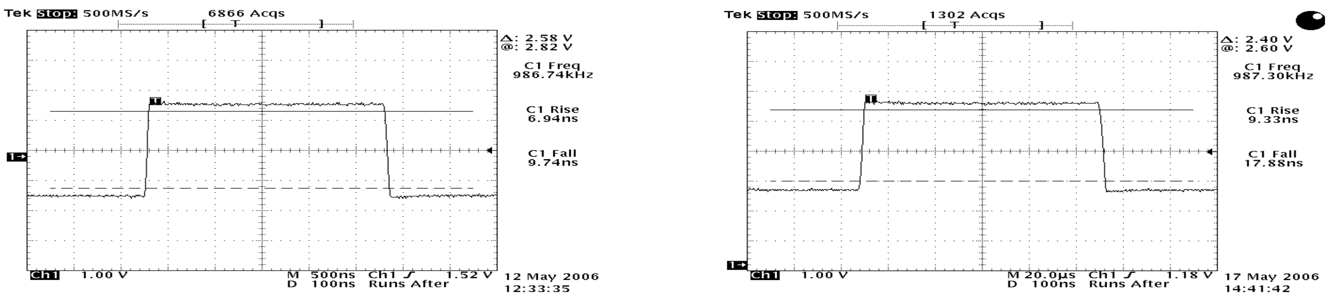


Figure 26: Waveforms Class A2 "Strong-Soft" at 85°C ambient temperature

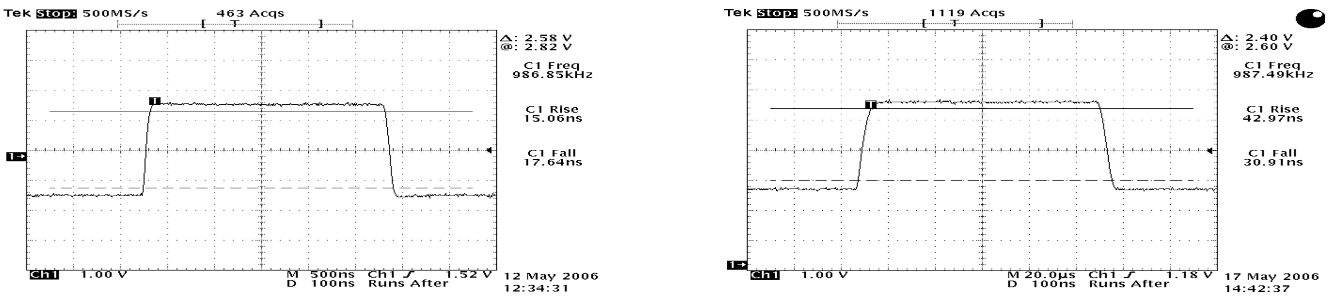


Figure 27: Waveforms Class A2 "Medium" at 85°C ambient temperature

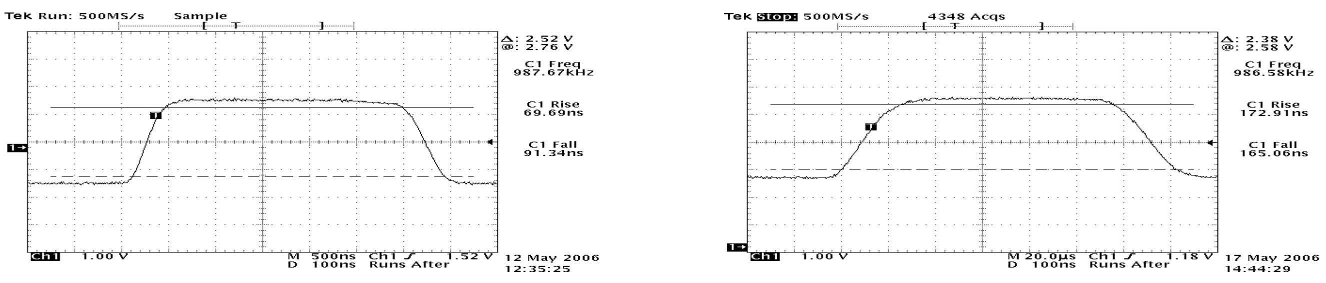


Figure 28: Waveforms Class A2 "Weak" at 85°C ambient temperature

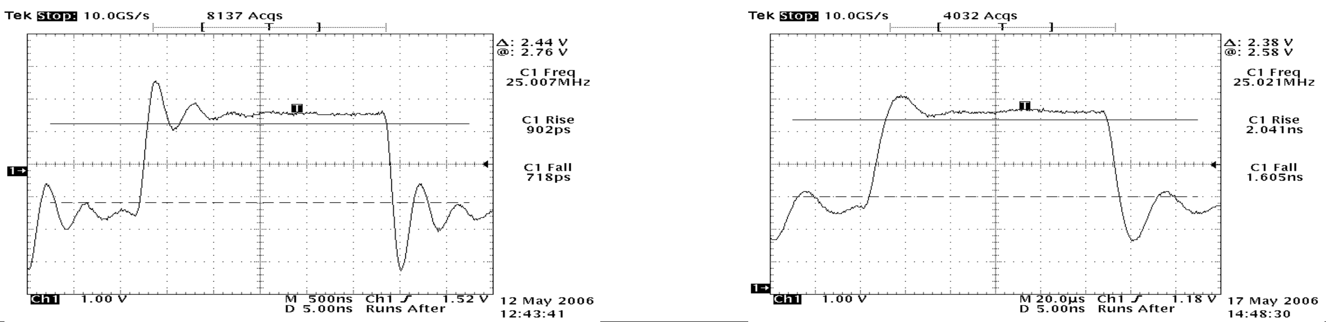


Figure 29: Waveforms Class A2 "Strong-Sharp" at 110°C ambient temperature

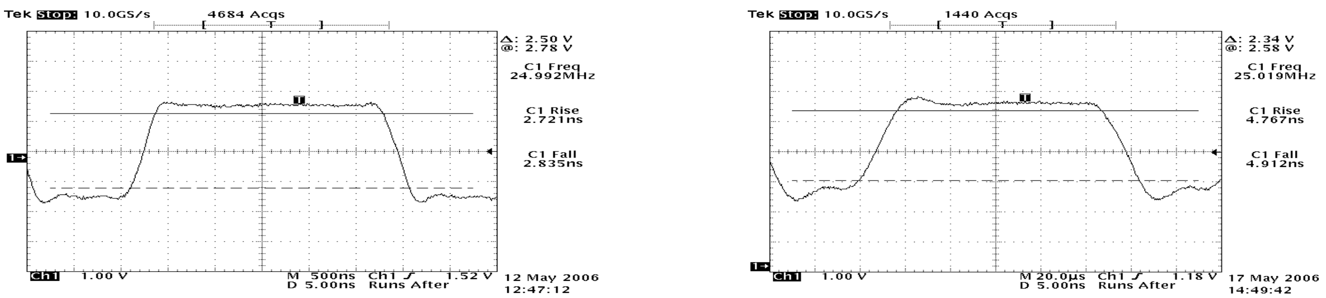


Figure 30: Waveforms Class A2 "Strong-Medium" at 110°C ambient temperature

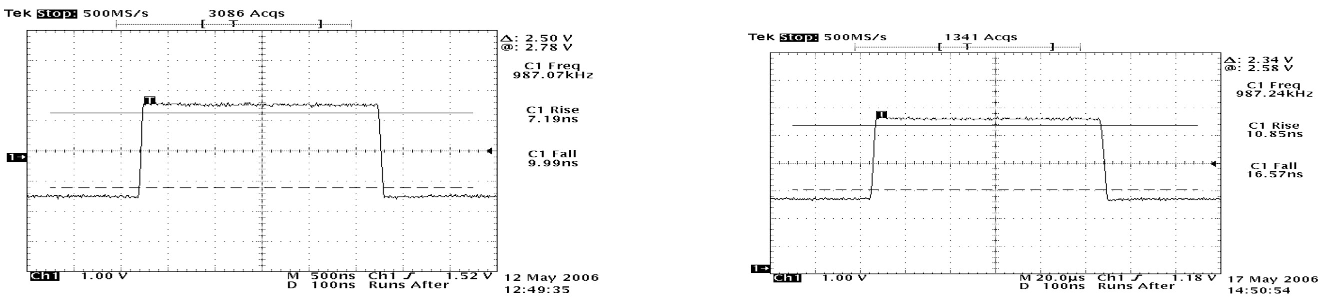


Figure 31: Waveforms Class A2 "Strong-Soft" at 110°C ambient temperature

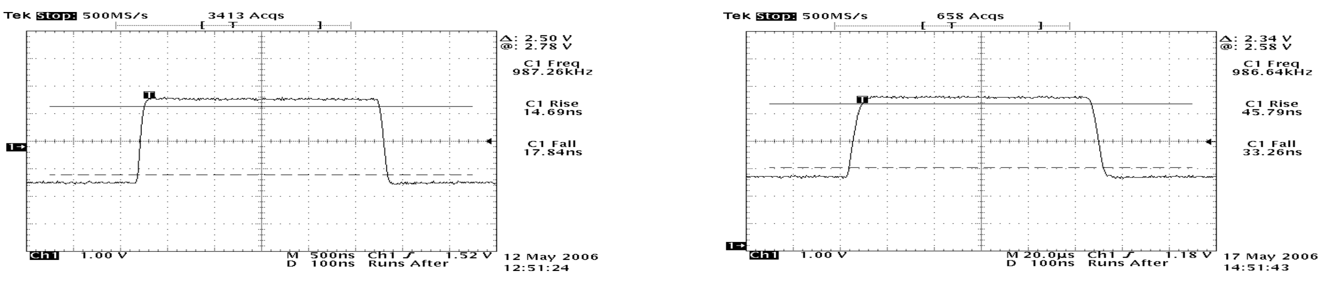


Figure 32: Waveforms Class A2 "Medium" at 110°C ambient temperature

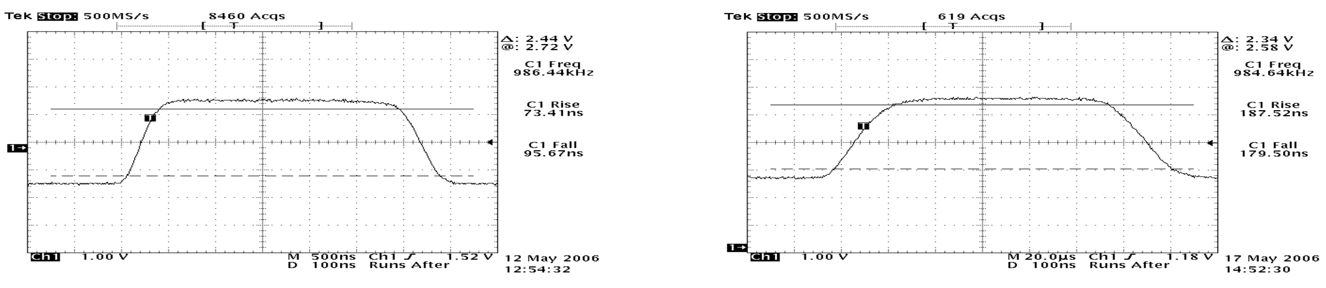


Figure 33: Waveforms Class A2 "Weak" at 110°C ambient temperature

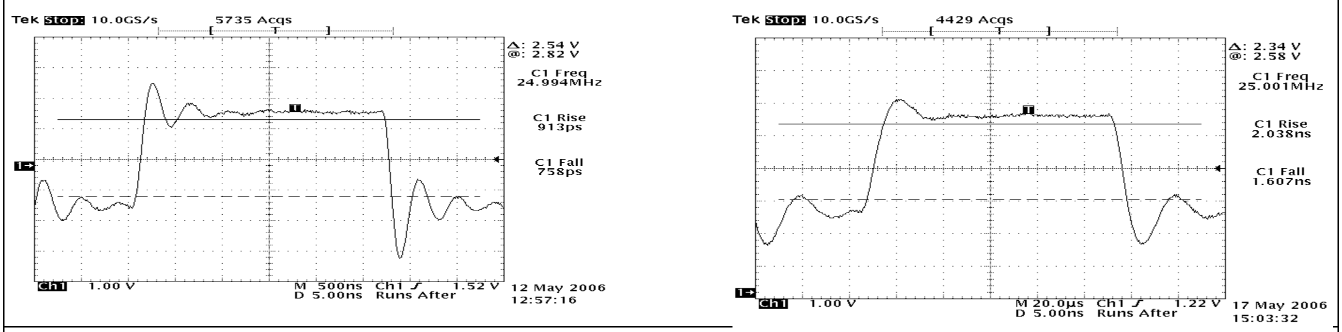


Figure 34: Waveforms Class A2 "Strong-Sharp" at 125°C ambient temperature

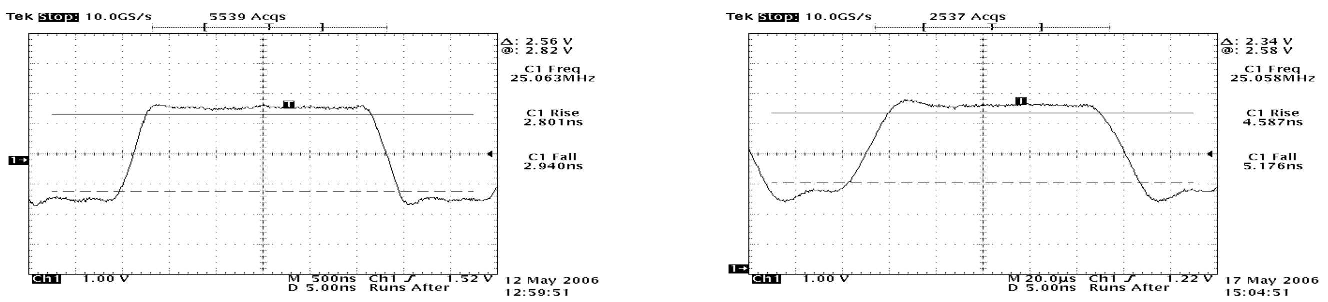


Figure 35: Waveforms Class A2 "Strong-Medium" at 125°C ambient temperature

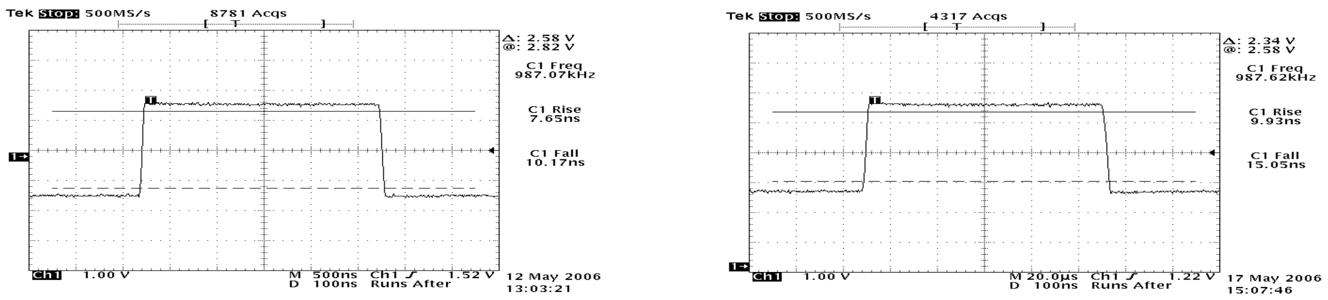


Figure 36: Waveforms Class A2 "Strong-Soft" at 125°C ambient temperature

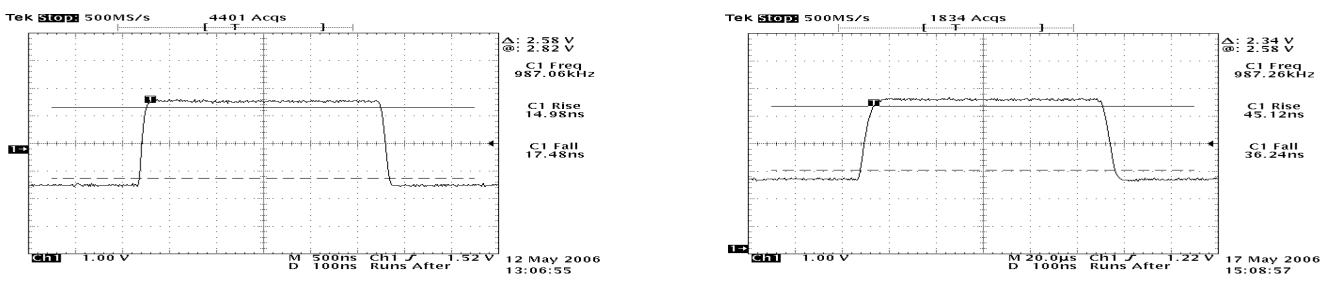


Figure 37: Waveforms Class A2 "Medium" at 125°C ambient temperature

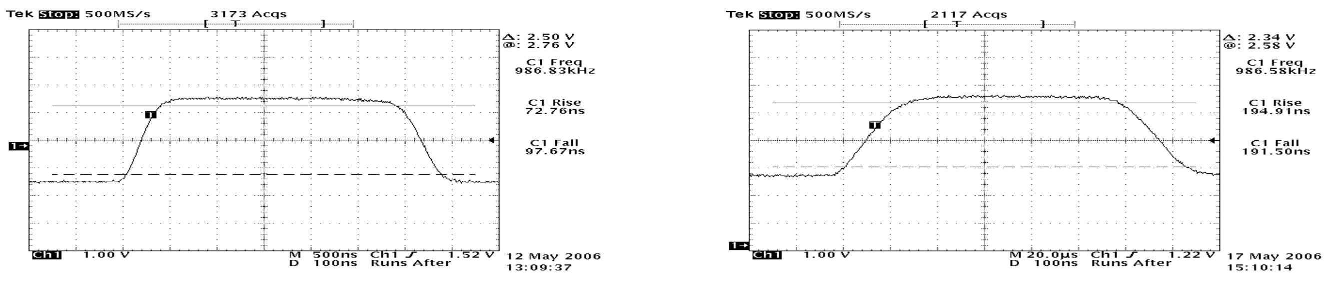


Figure 38: Waveforms Class A2 "Weak" at 125°C ambient temperature

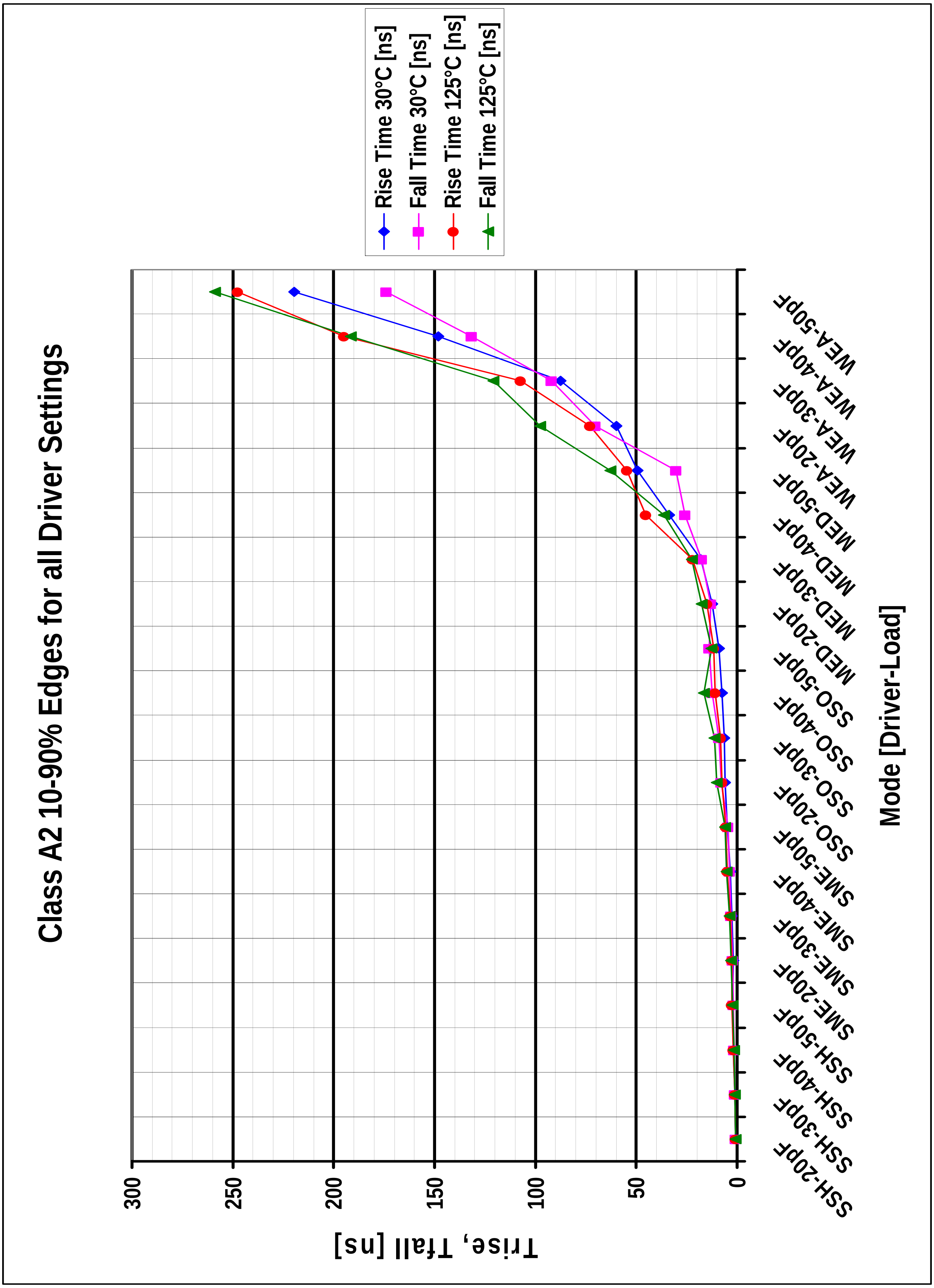


Figure 39: Timings Class A2 for all driver settings

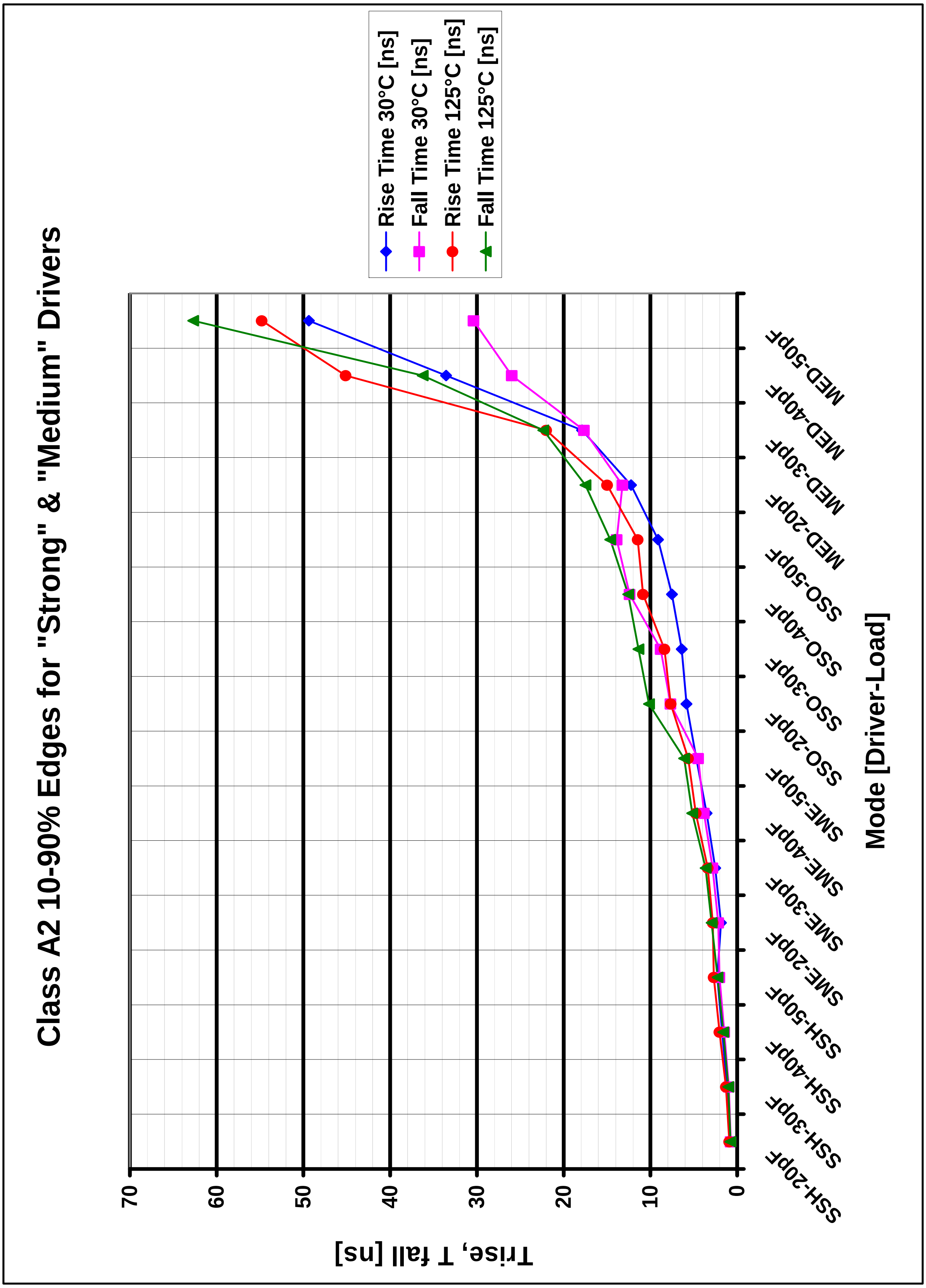


Figure 40: Zoomed timings Class A2 for strong and medium driver settings

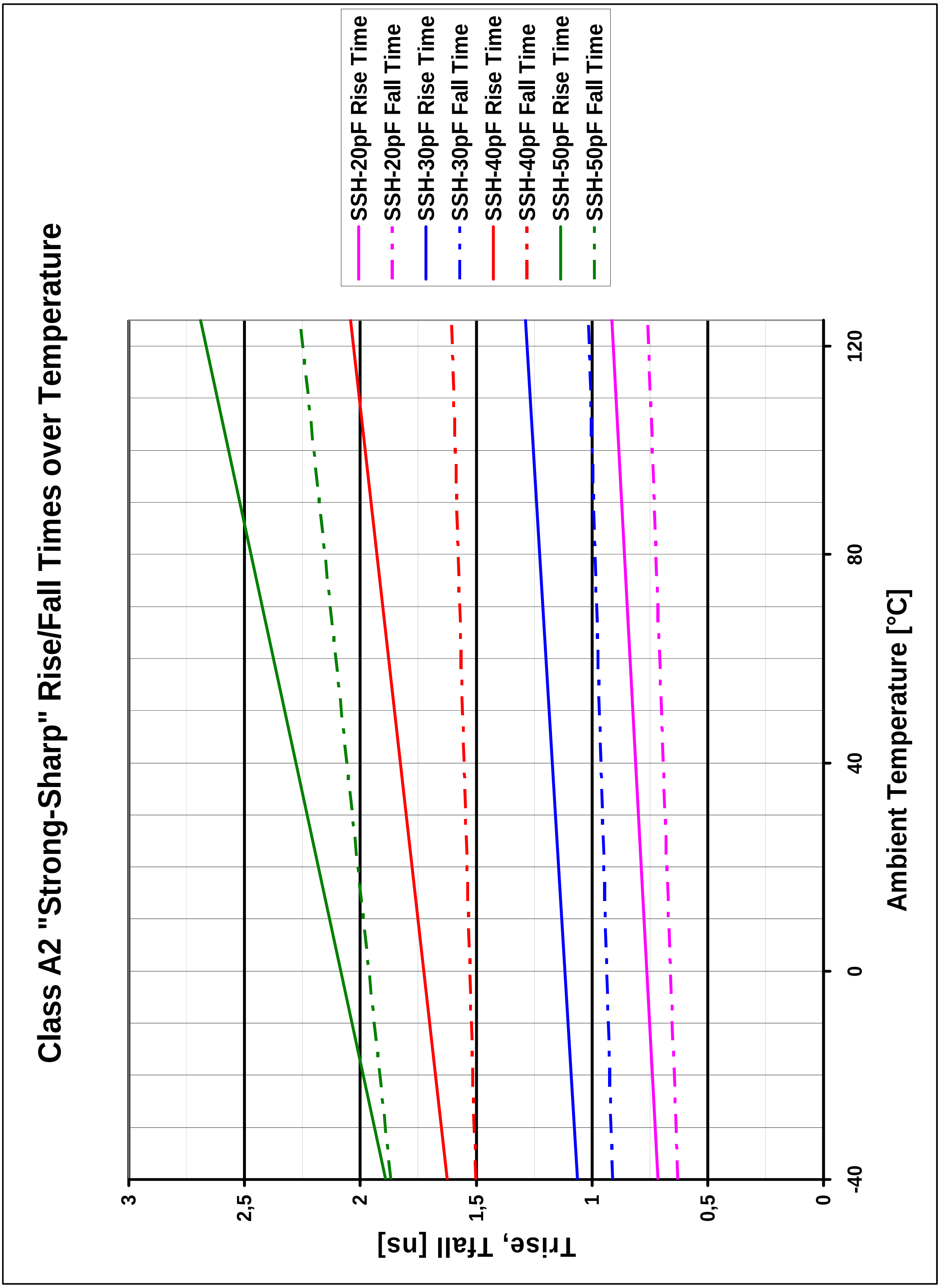


Figure 41: Class A2 “strong-sharp” driver rise/fall times over full ambient temperature range

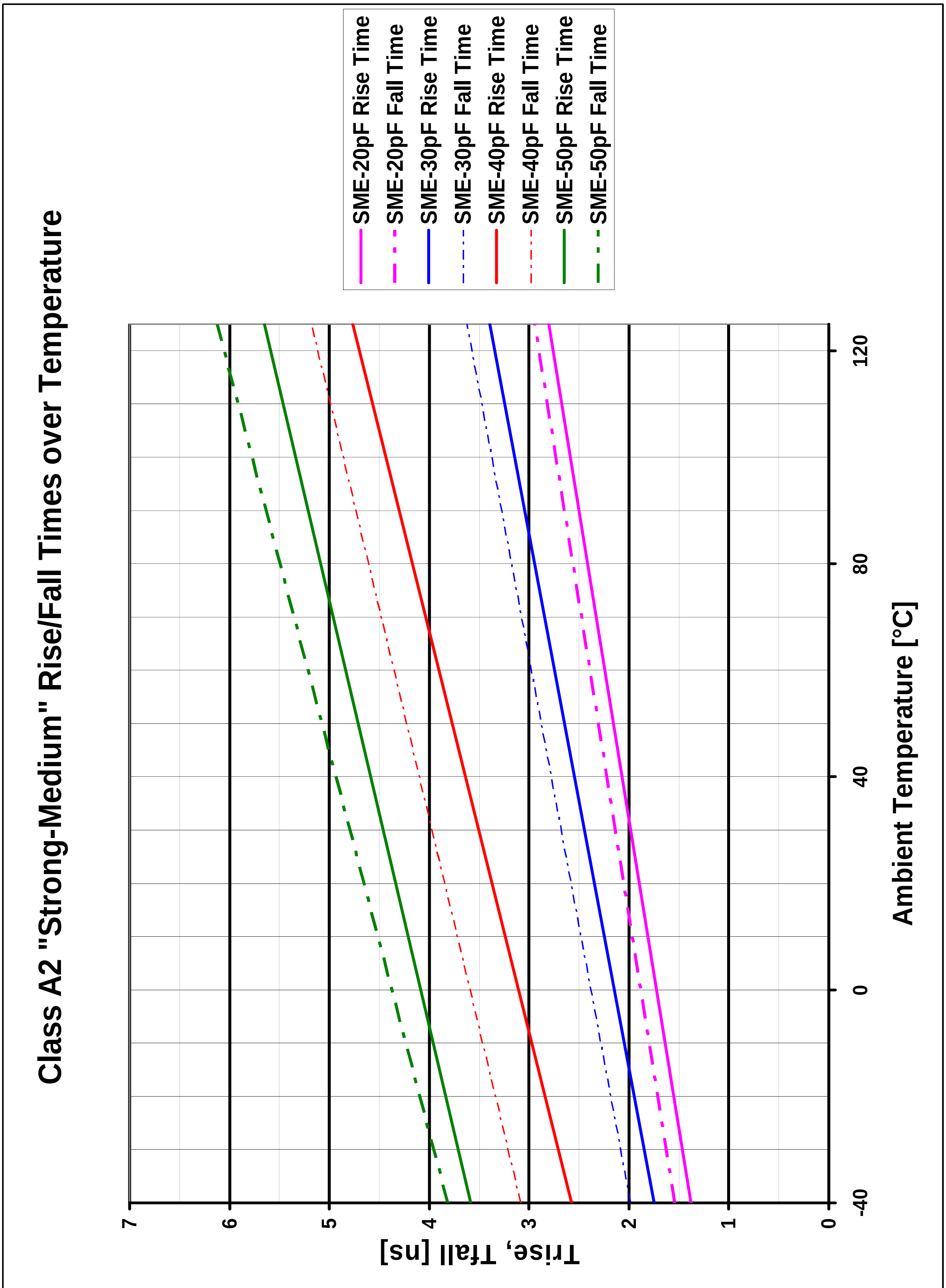


Figure 42: Class A2 “strong-med” driver rise/fall times over full ambient temperature range

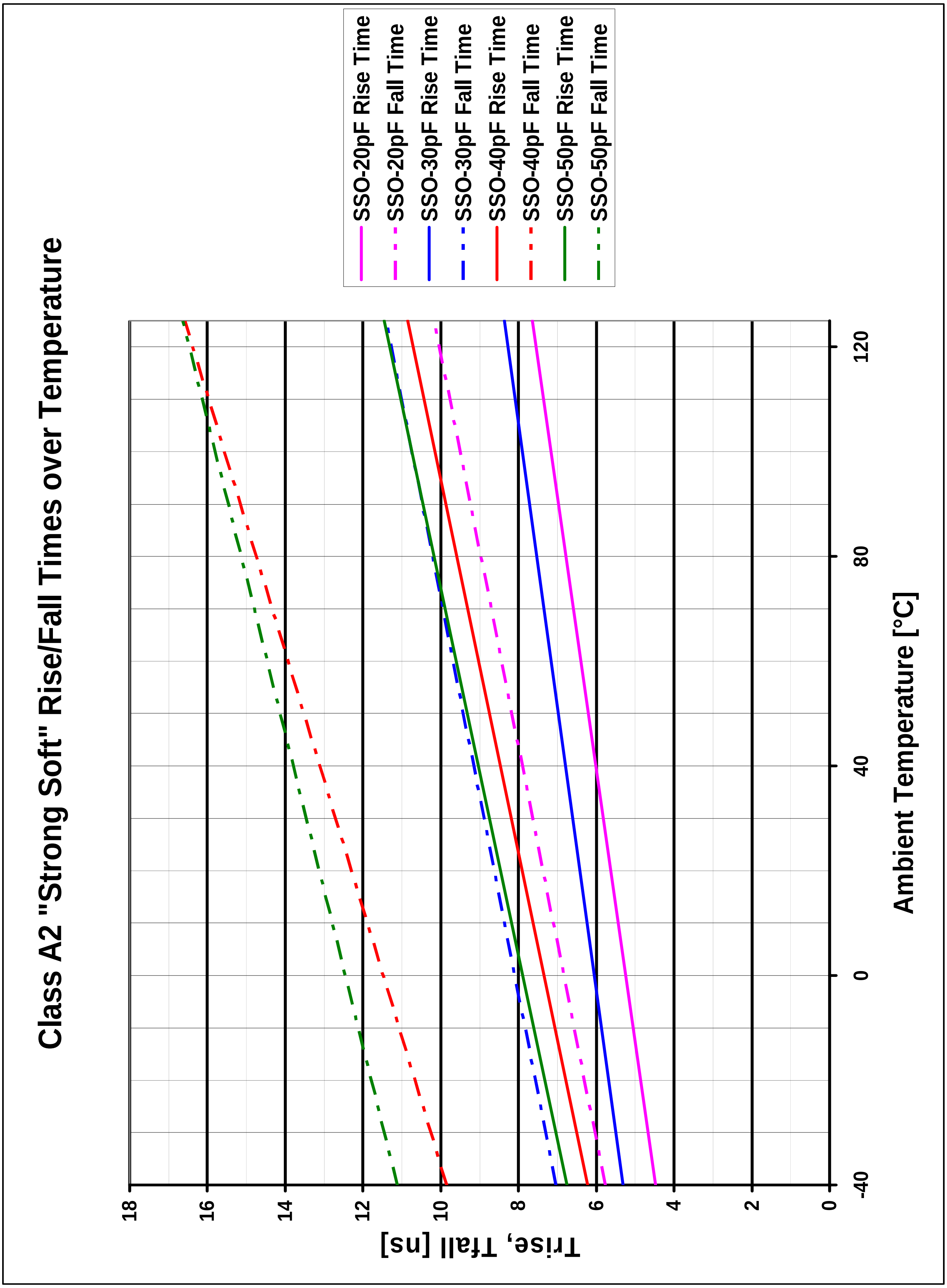


Figure 43: Class A2 "strong-soft" driver rise/fall times over full ambient temperature range

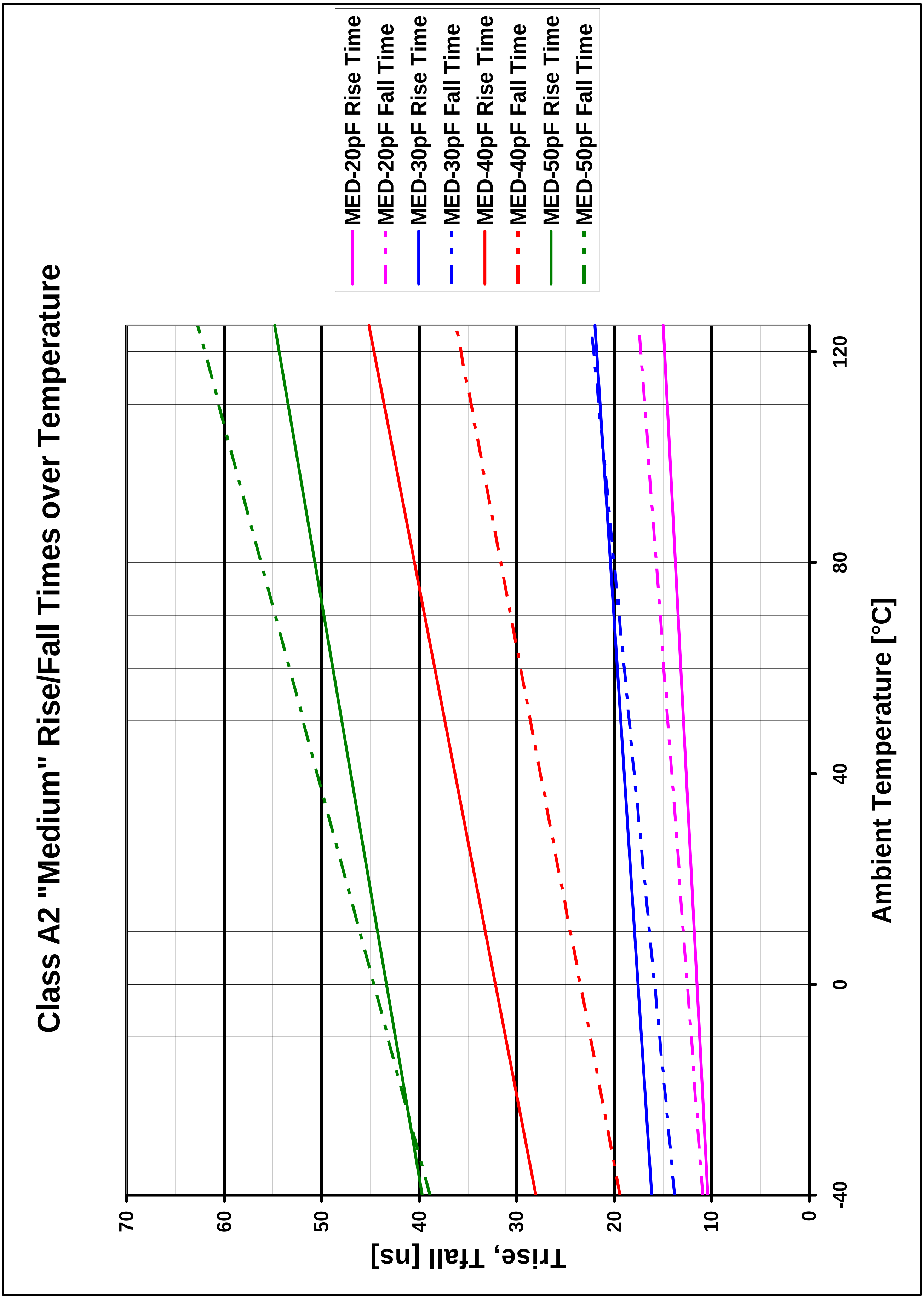


Figure 44: Class A2 “Medium” driver rise/fall times over full ambient temperature range

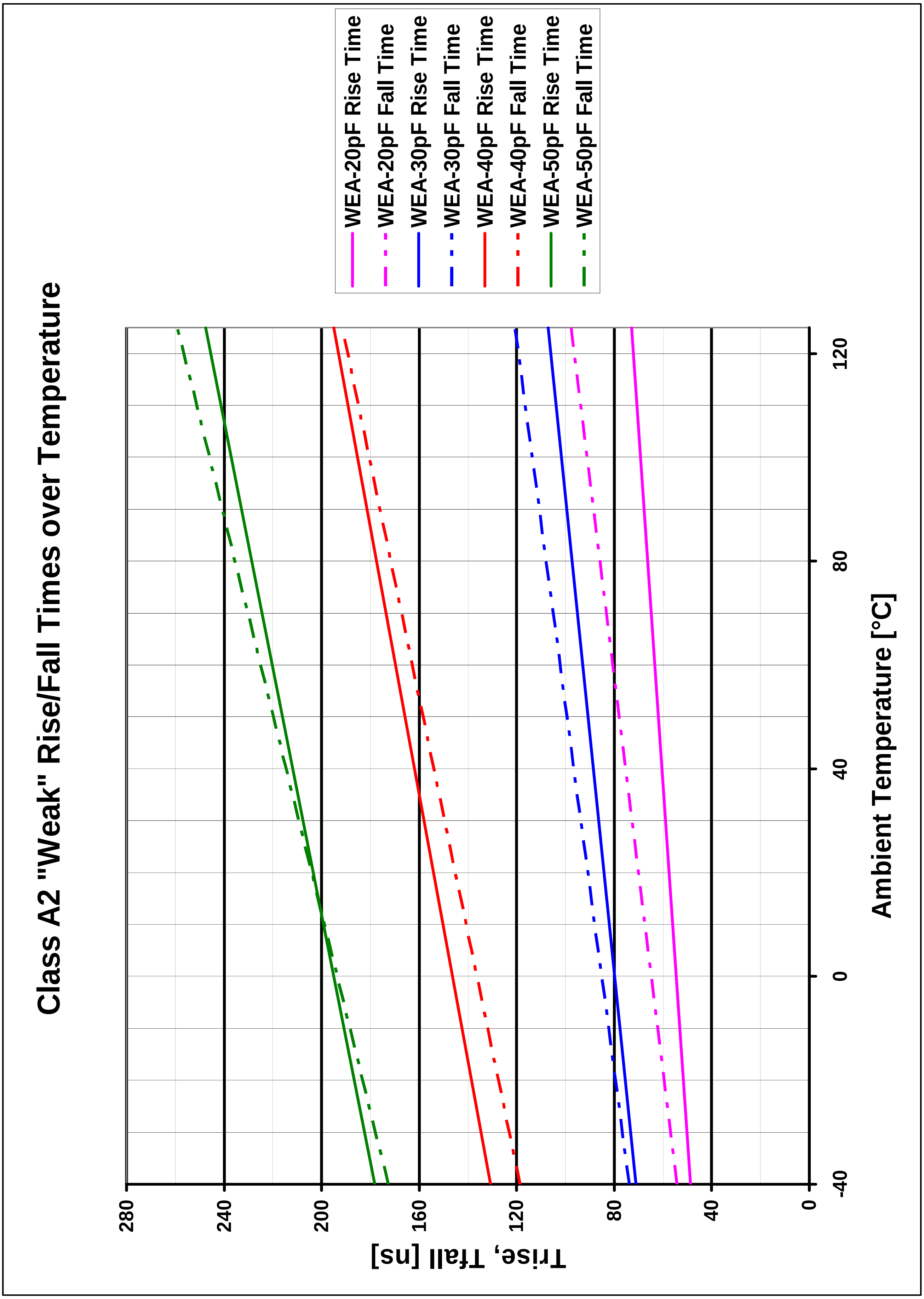


Figure 45: Class A2 “Weak” driver rise/fall times over full ambient temperature range

4 Simulated Timings

4.1 Simulated timings on selected PCB trace structures

4.1.1 Description of structures

A temperature range from T_A=25°C to T_A=150°C is covered for the timings. Please note that in addition to the measured timings, which use discrete load capacitors, it is interesting to compare timing waveforms for various PCB structures. This overview provides a good guess on the impact of serial termination, the use of via contacts, and the shape of trace structures connected to a pad driver.

We use 4 different structures, shown in Fig. 46:

(a) Point-to-Point,

(b) Bus,

(c) Star,

(d) Tree.

Each of the structures was drawn in 4 versions and simulated with Sigrity Speed2000™. The 4 versions are:

(1) no vias, no series termination,

(2) no vias, series termination at transmitter,

(3) vias, no series termination,

(4) vias, series termination.

In case of no vias, all traces are routed on the top PCB layer where transmitter and receivers are soldered. In case of vias, the red traces in Fig. 46 are routed on the bottom PCB layer. In case of series termination, a 51Ω resistor R_t is connected directly at the transmitter output in the data line.

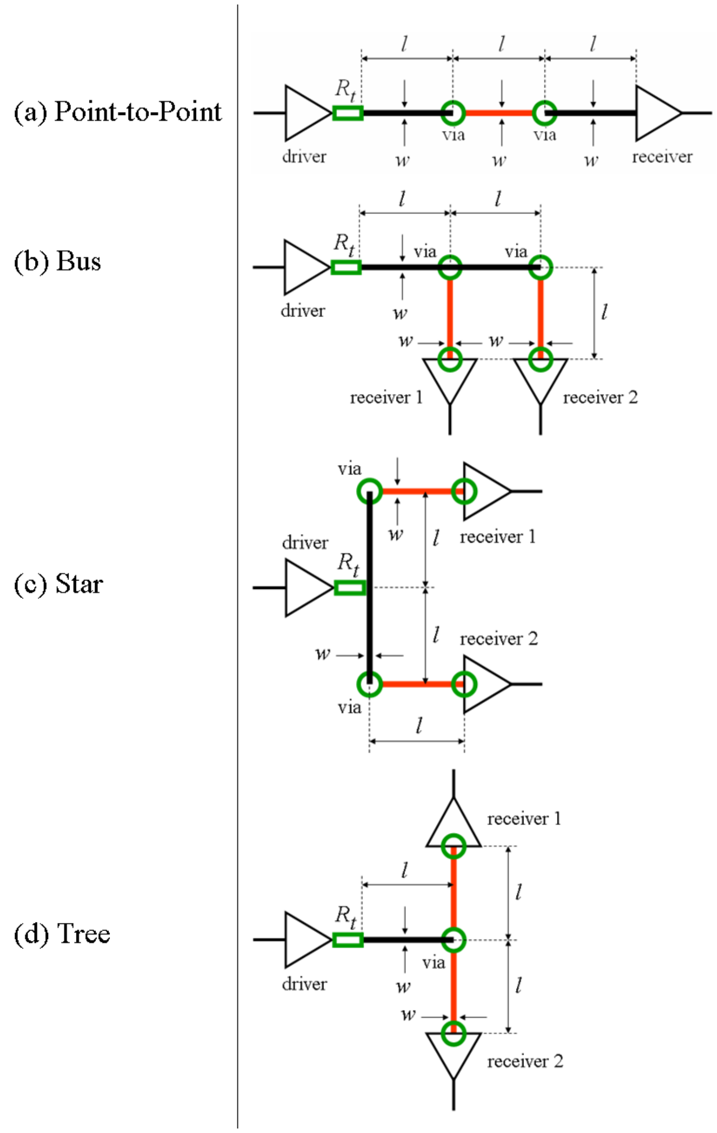


Figure 46: Set of PCB trace structures

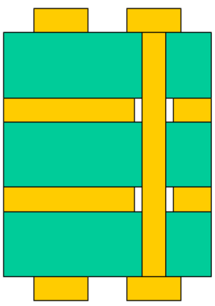
The layer stack of the printed circuit board model is shown in Fig. 47. It consists of 4 layers in standard FR4 material in the order signal-GND-VCC-signal.

300µm trace width results in a 57Ω trace impedance.

The capacitance per unit length is 1pF/cm.

An input capacitance of 5pF per CMOS receiver input is assumed.

The driver is represented by the IBIS model listed in Appendix A. The driver strength can be selected to be “strong-sharp”, “strong-medium”, “strong-soft”, “medium” and “weak”.



Top layer	Signal	w=300µm	h=36µm
Dielectricum 1		ε_r=4.0	h=500µm
Mid layer 1	GND		h=36µm
Dielectricum 2		ε_r=4.0	h=500µm
Mid layer 2	VCC		h=36µm
Dielectricum 3		ε_r=4.0	h=500µm
Bottom layer	Signal	w=300µm	h=36µm

Figure 47: PCB layer stack

The length of each trace piece marked “*l*” in Fig. 46 has been dimensioned such that the resulting total trace capacitance plus the receiver gate capacitances are 20pF, 30pF, 40pF and 50pF. Table 4 lists the resulting trace lengths. The via contacts connect signals on the top layer with signals on the bottom layer.

Fig. 50-110 show the simulated rise and fall times as a function of PCB structures with different capacitive loads. In each diagram, the measured timings and the simulated timings with ideal capacitive load are given for reference.

To keep a better overview, one diagram contains only the curves for one structure operating at one temperature. The parameters varied in one diagram are the load capacitance and the driver settings. The abbreviations are as defined in Table 2.

Structure	Load	Length “*l*”	Width “*w*”
Point-to-Point	20 pF	5.1 cm	300 µm
	30 pF	8.5 cm	300 µm
	40pF	11.9 cm	300 µm
	50 pF	15.3 cm	300 µm
Bus	20 pF	4.4 cm	300 µm
	30 pF	7.9 cm	300 µm
	40 pF	12.5 cm	300 µm
	50 pF	16.8 cm	300 µm
Star	20 pF	4.2 cm	300 µm
	30 pF	8.1 cm	300 µm
	40 pF	12.2 cm	300 µm
	50 pF	16.9 cm	300 µm
Tree	20 pF	5.9 cm	300 µm
	30 pF	11.4 cm	300 µm
	40 pF	17.2 cm	300 µm
	50 pF	21.3 cm	300 µm

Table 4: Dimensions of PCB structures

4.1.2 Rise/fall time diagrams

All rise/fall times refer to the 10-90% rising edge and to the 90-10% falling edge of the transmitter output voltage. Details are identical to the measured timings and levels described in chapter 3.1.1.

Weak driver strength has not been simulated because of the very low rise and fall times. Main purpose is to show the influence of via contacts which are placed on the traces, and series termination resistors placed at the driver outputs.

The 4 via/termination combinations are marked in the diagrams as follows:

“Vias No Term No” = no via contacts, no termination resistor

“Vias Yes Term No” = via contacts, but no termination resistor

“Vias No Term Yes” = no via contacts, but termination resistor

“Vias Yes Term Yes” = via contacts and termination resistor

The result diagrams show the simulated rising and falling edge timing using an oscilloscope probe of 8pF||1MΩ. The reference points are 10% and 90% as indicated in Fig. 7 for Class A2 pads (VDDP = 3.3V) and in Fig. 8 for Class B2 pads (VDDE = 2.5V).

For simulations at T_A=150°C, the pad supply voltage VDDP has been decreased to 3.13V (nominal VDDP minus 5%). Thus the voltage levels references for timing simulations at T_A=150°C are: 0.31V (low reference) and 2.82V (high reference).

For simulations at T_A=150°C, the EBU supply voltage VDDE has been decreased to 2.38V (nominal VDDE minus 5%). Thus the voltage levels references for timing simulations at T_A=150°C are: 0.24V (low reference) and 2.14V (high reference).

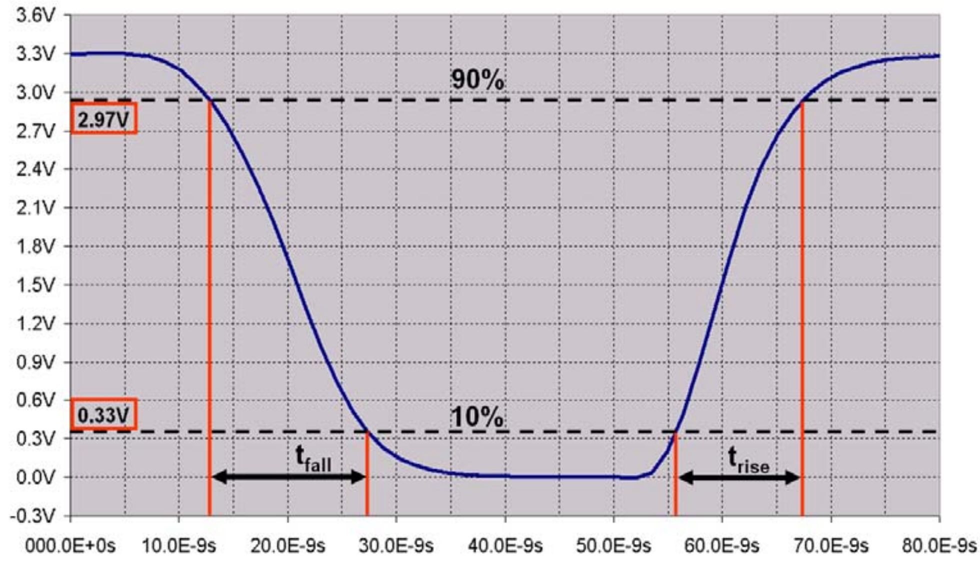


Figure 48: Voltage level references for Class A timing measurements

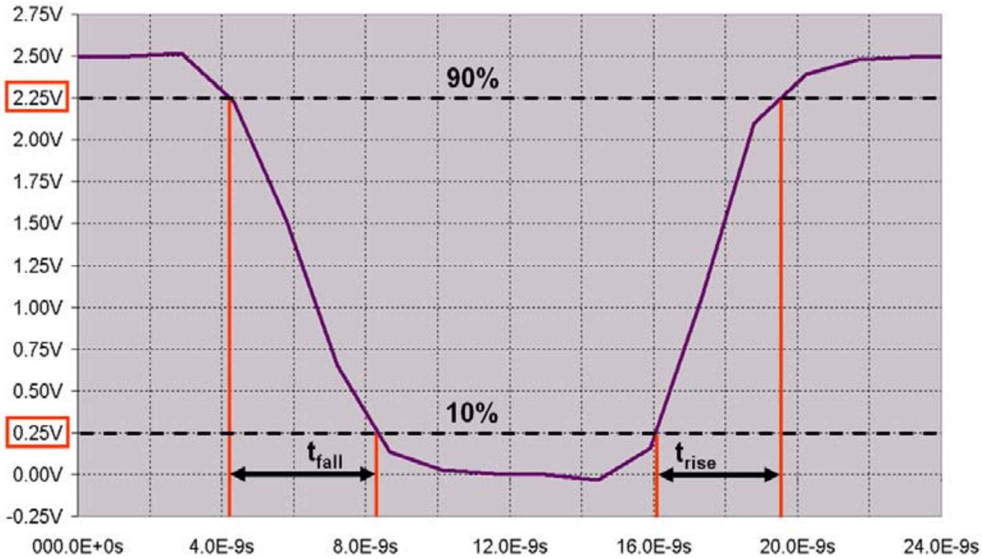


Figure 49: Voltage level references for Class B timing measurements

4.1.2.1 Rise/fall times of driver/load settings, sorted by layout structures

Fig. 50-113 show the rise/fall times – 10/90% margins as described above – for selected driver/load combinations as listed in Table 2, for the four layout structures under investigation. One diagram contains the results for the four vias/termination combinations explained above plus the measured values. The diagram title indicates the structure under investigation, the driver class (A2 or B2) and in case of class B2 the supply voltage (2.5V or 3.3V).

Note that Class B1 drivers are similar to the Class B2 drivers. Thus all timings given for Class B2 are also valid for Class B1.

All diagrams for class A2 drivers assume 3.3V supply voltage. At high temperature (150°C ambient temperature), the supply voltages have been decreased by 10%. Numbers are given in the paragraph above.

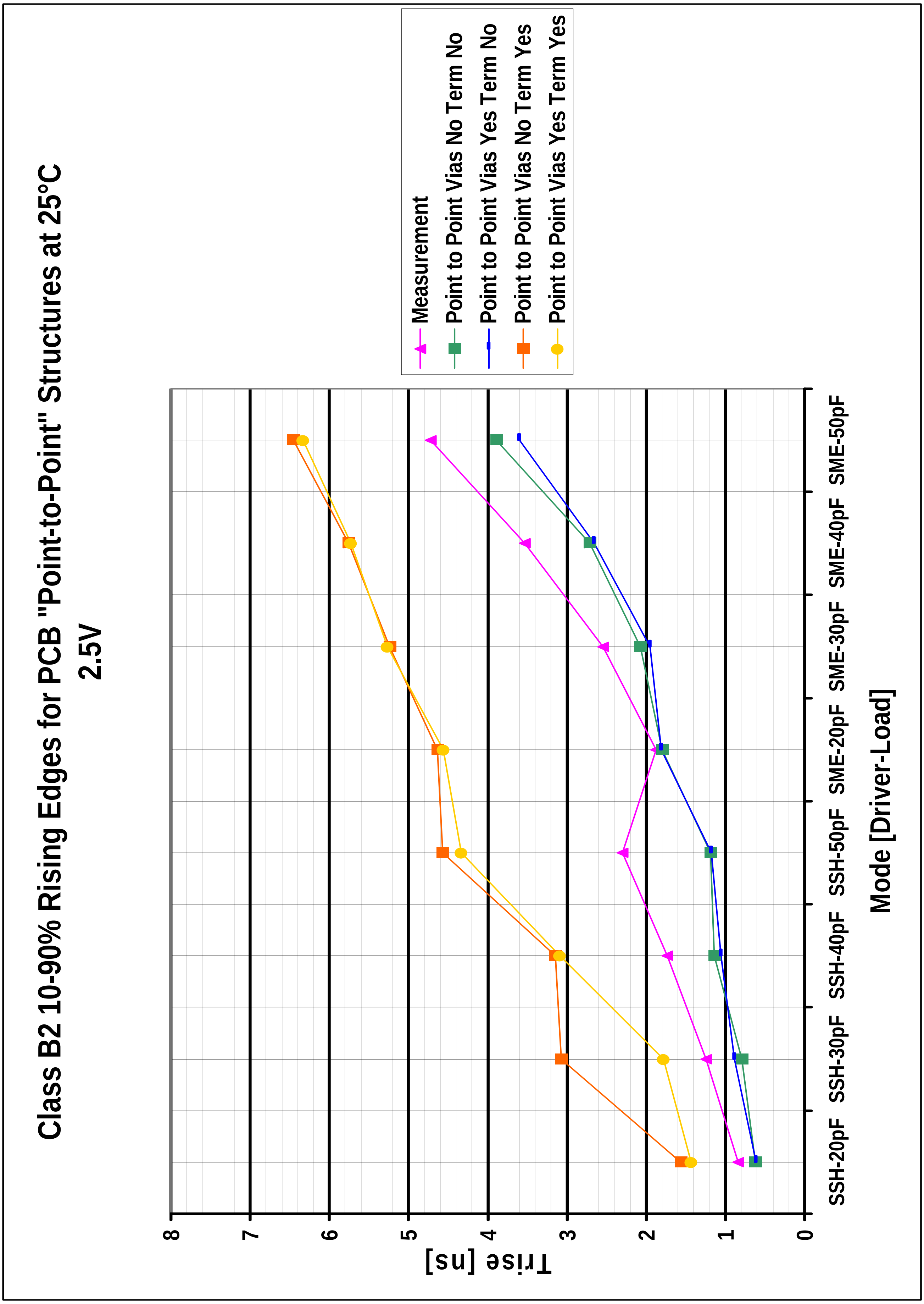


Figure 50: Class B2 rise times for "Point-to-Point" layout at 25°C

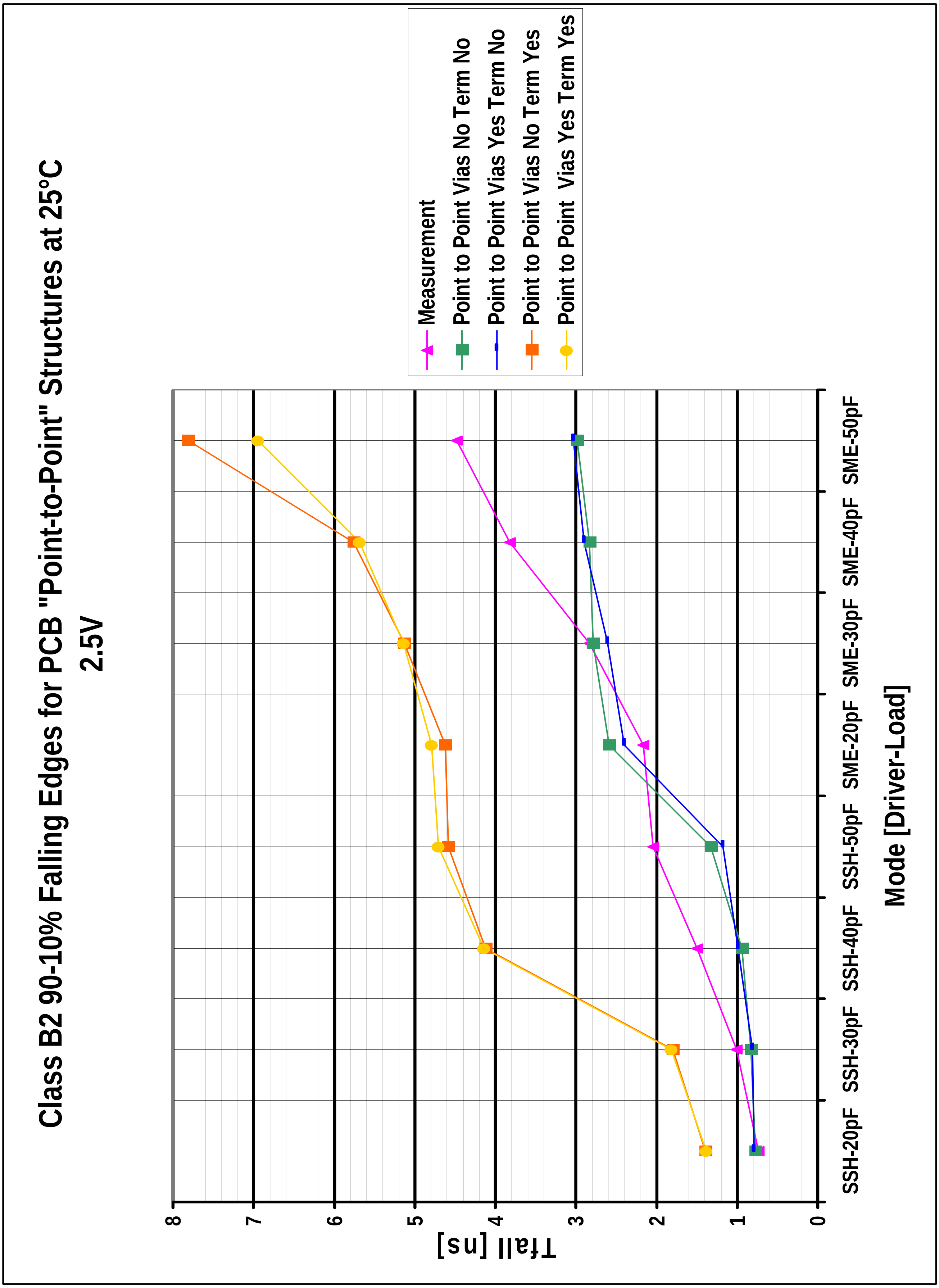


Figure 51: Class B2 fall times for "Point-to-Point" layout at 25°C

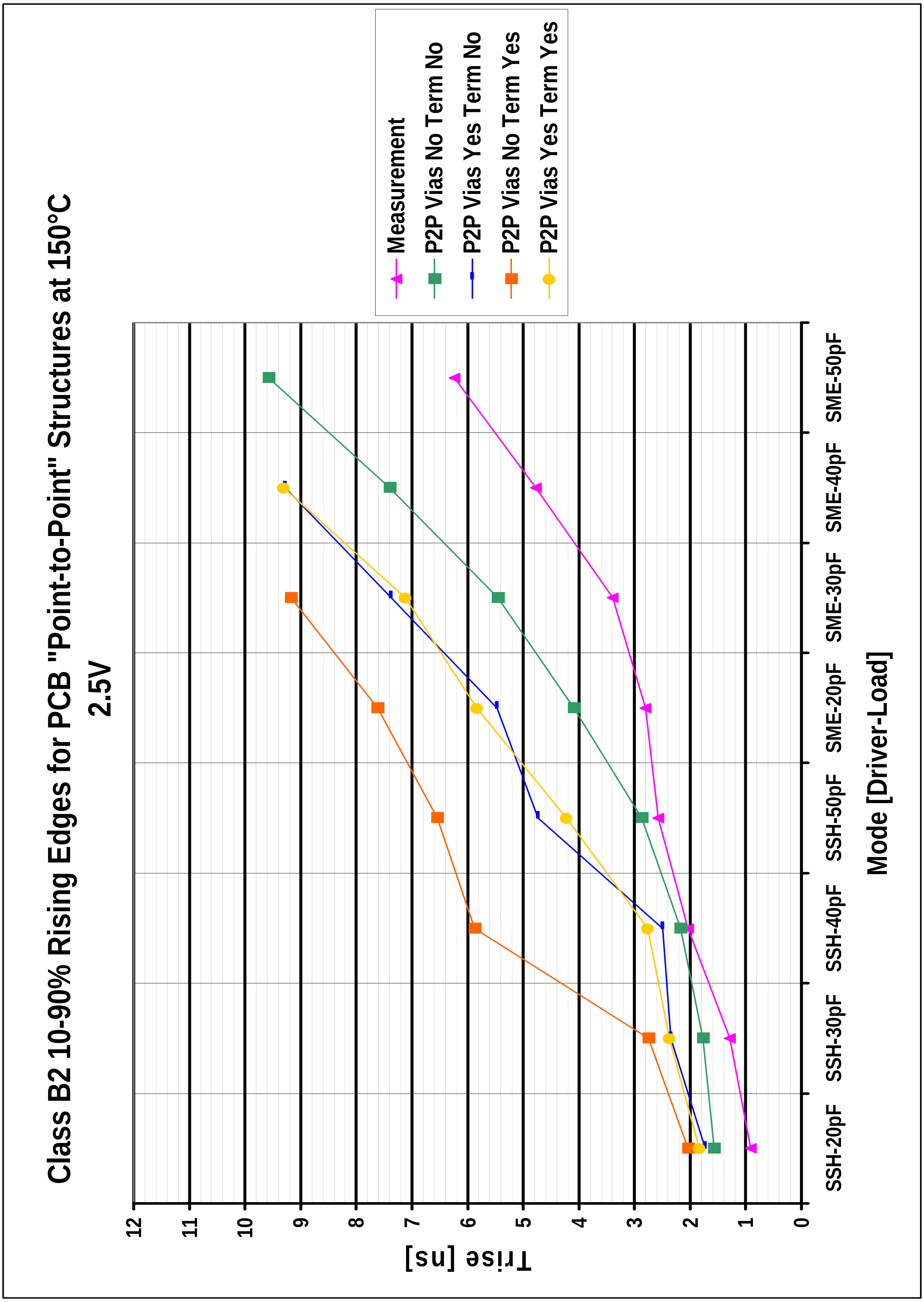


Figure 52: Class B2 rise times for “Point-to-Point” layout at 150°C

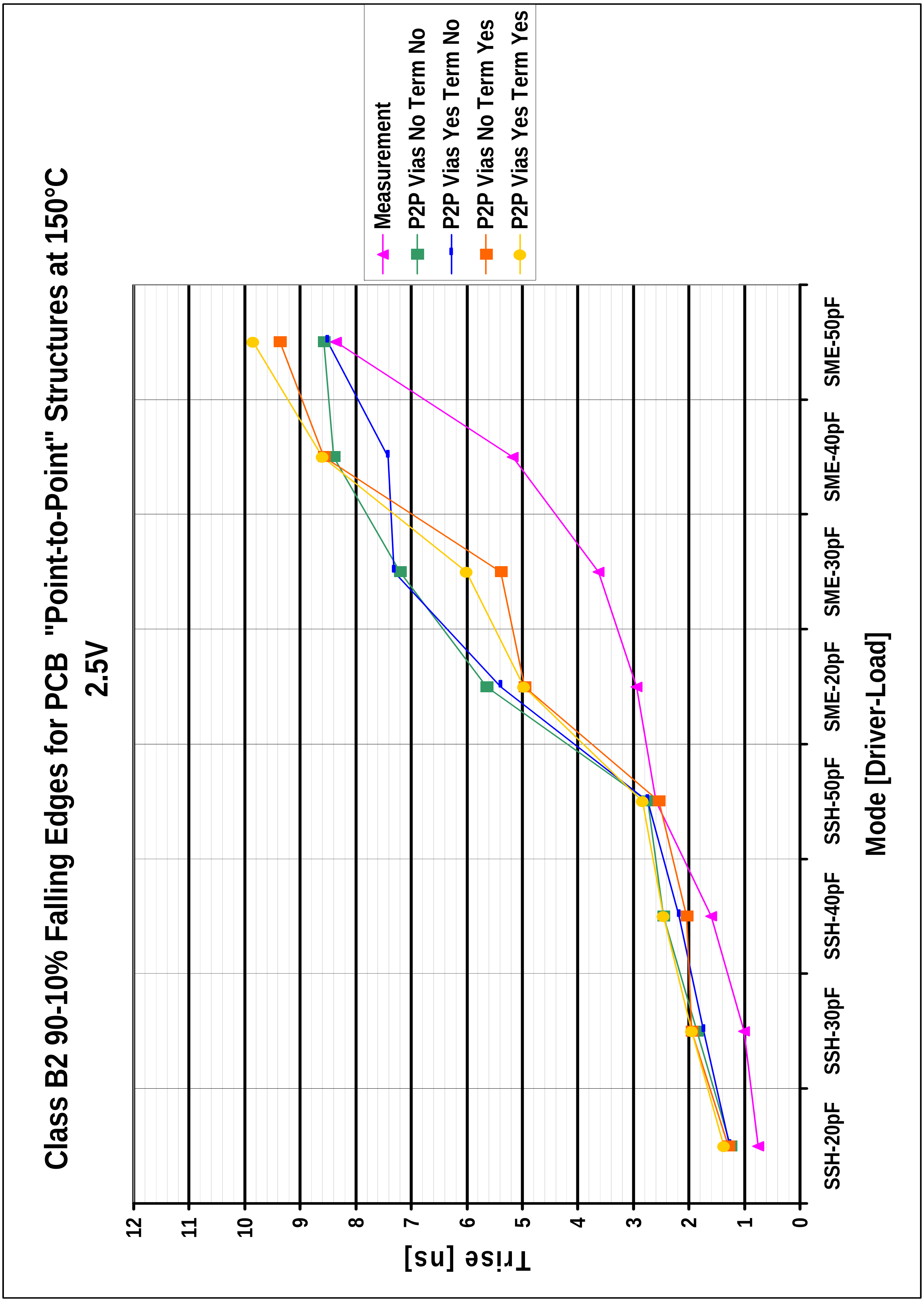


Figure 53: Class B2 fall times for "Point-to-Point" layout at 150°C

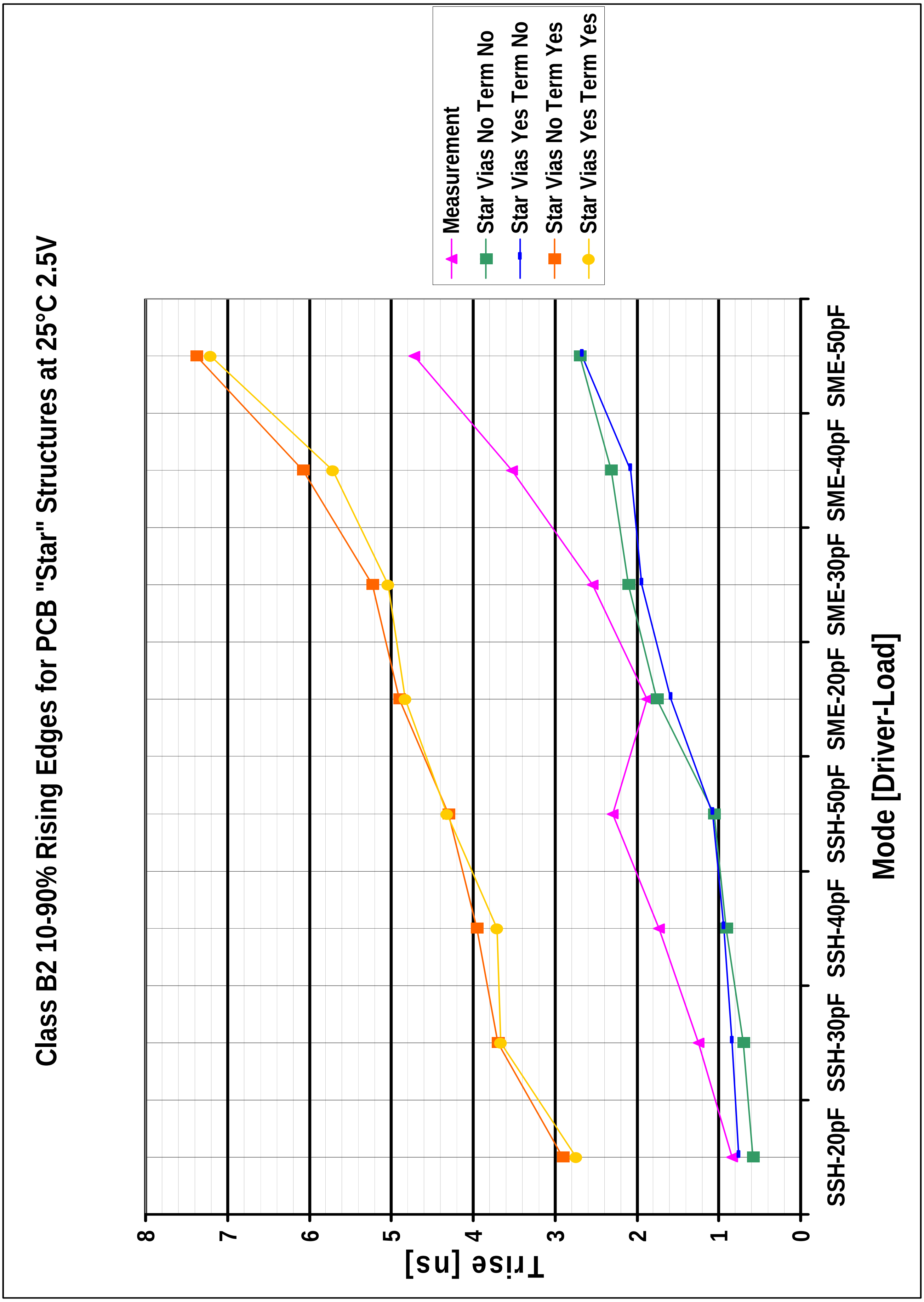


Figure 54: Class B2 rise times for "Star" layout at 25°C

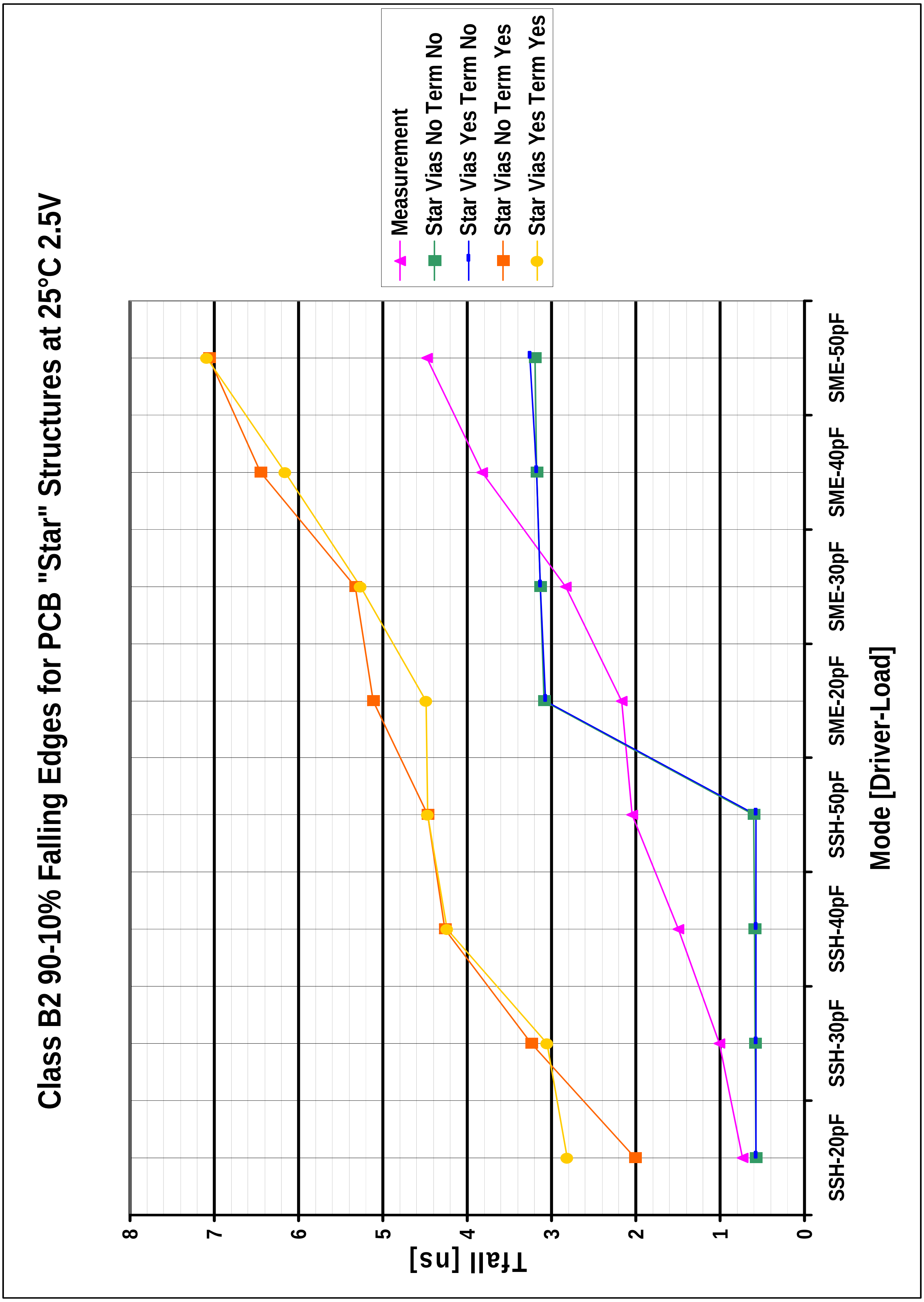


Figure 55: Class B2 fall times for “Star” layout at 25°C

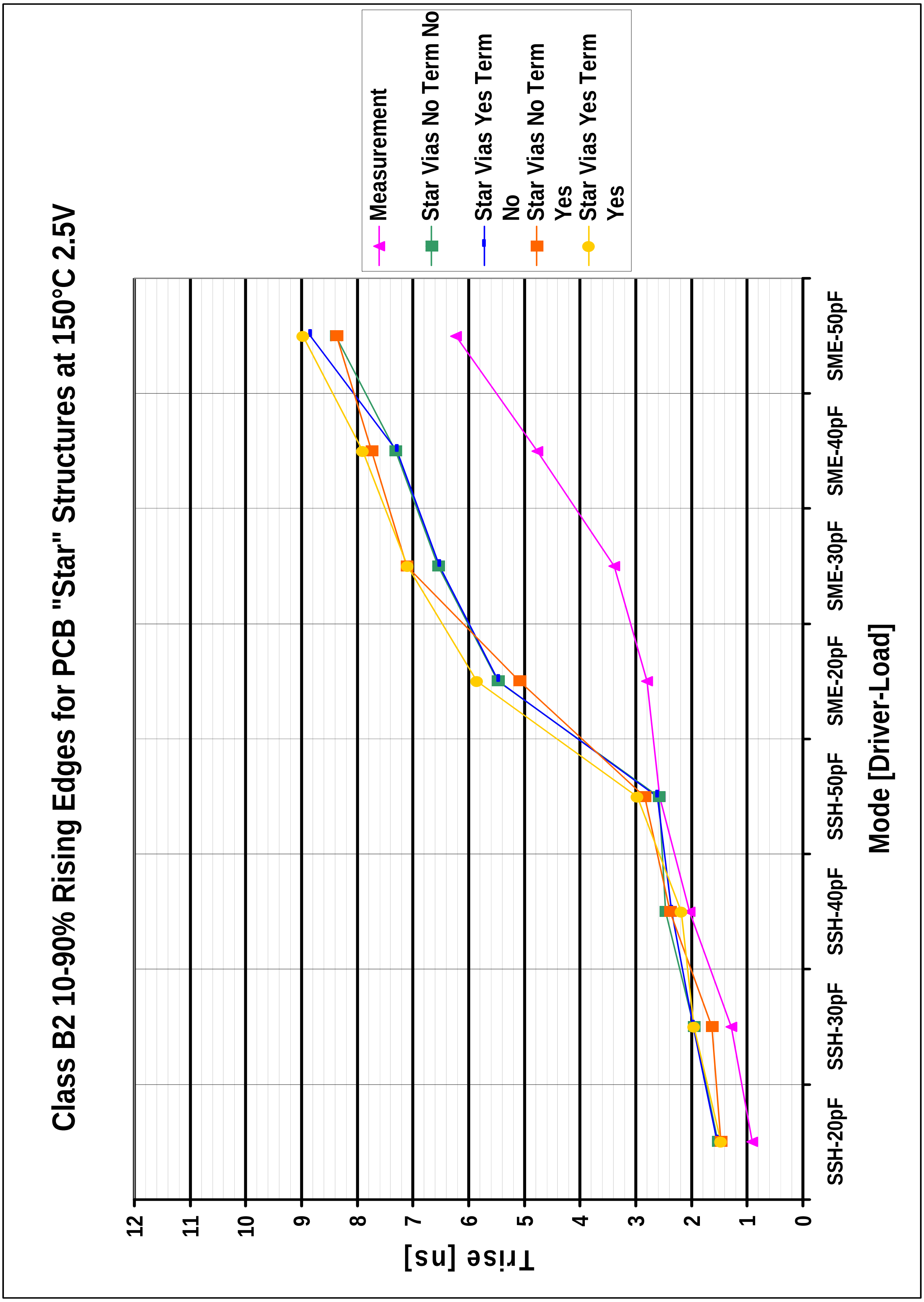


Figure 56: Class B2 rise times for “Star” layout at 150°C

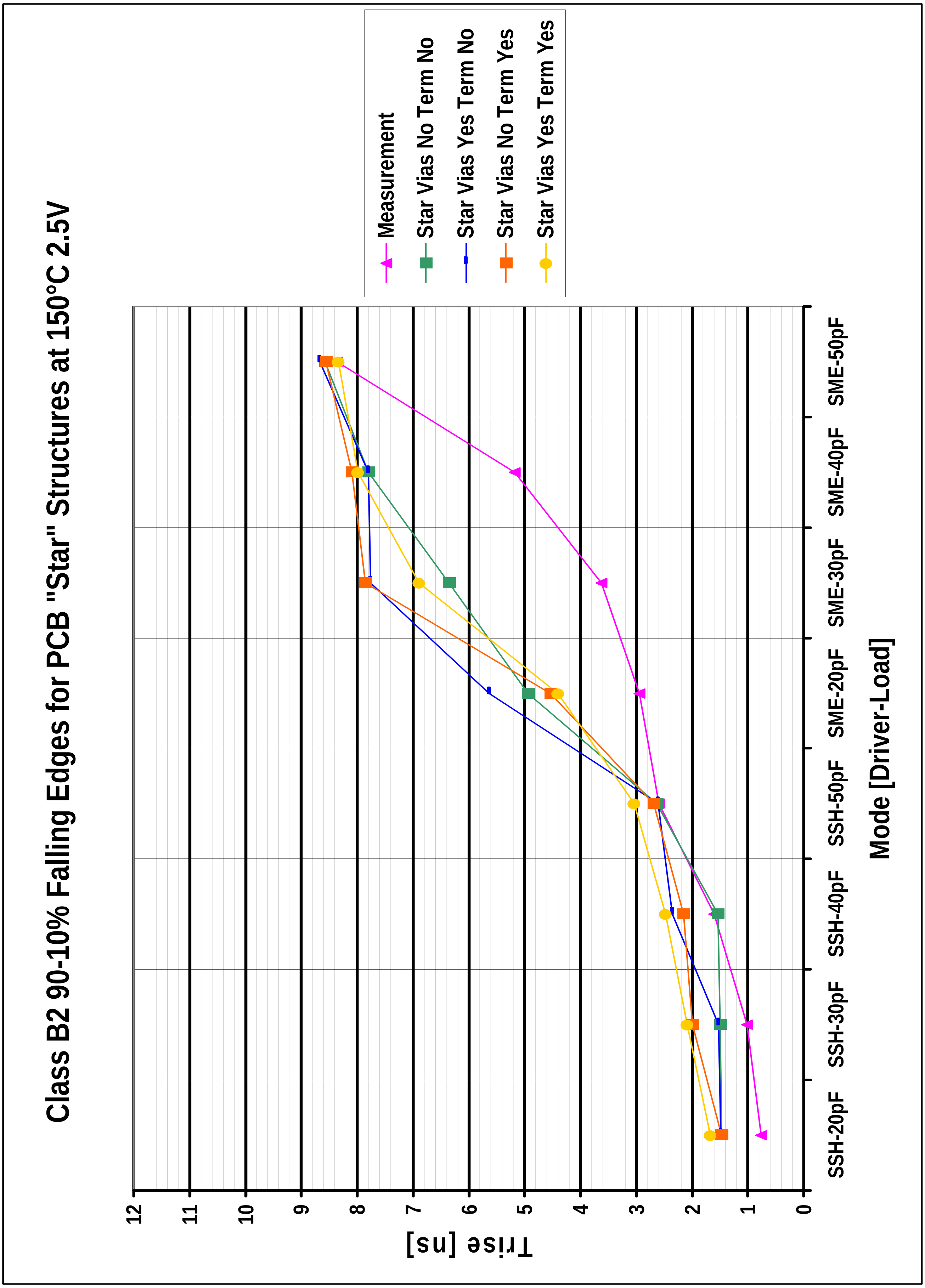


Figure 57: Class B2 fall times for “Star” layout at 150°C

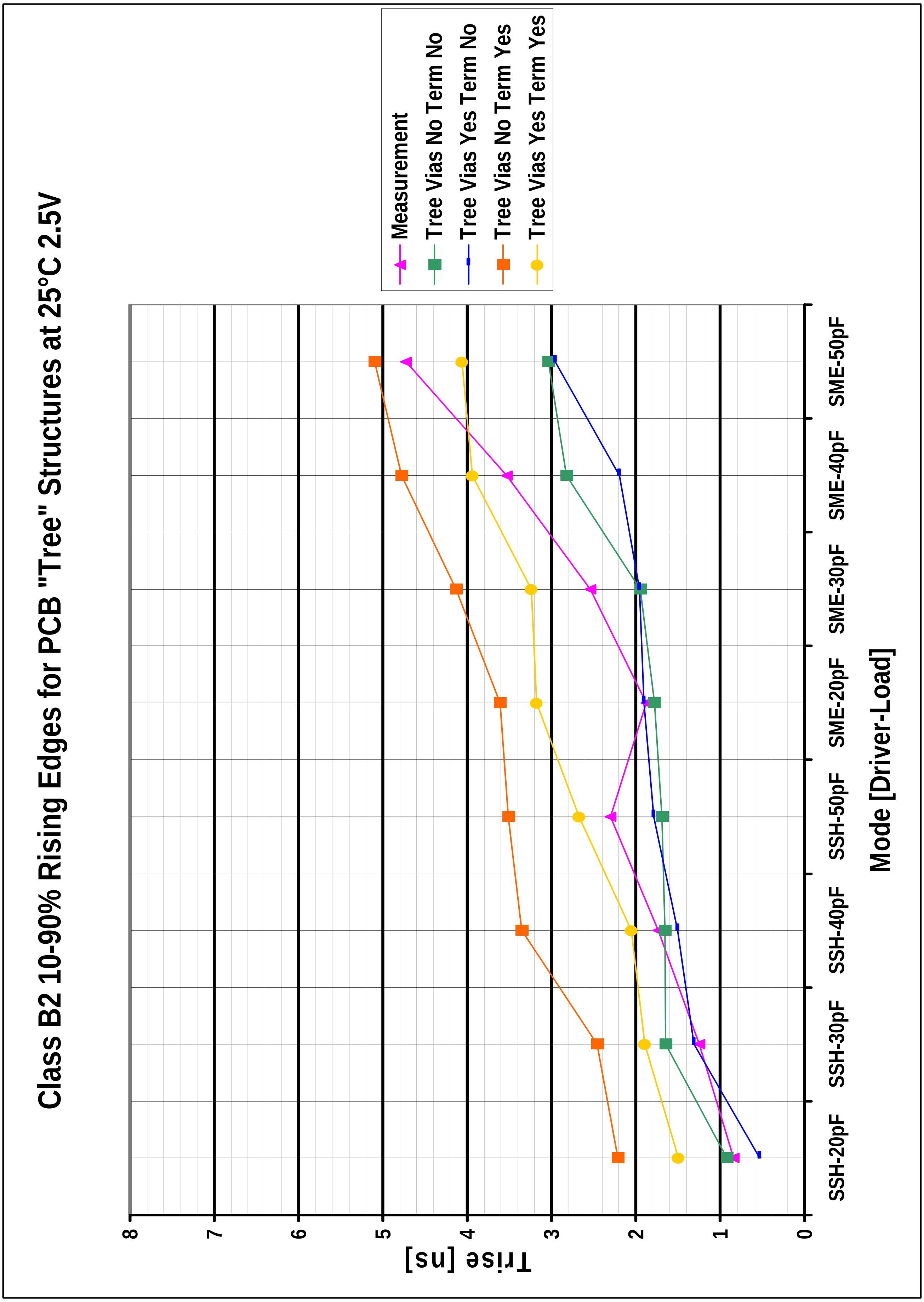


Figure 58: Class B2 rise times for “Tree” layout at 25°C

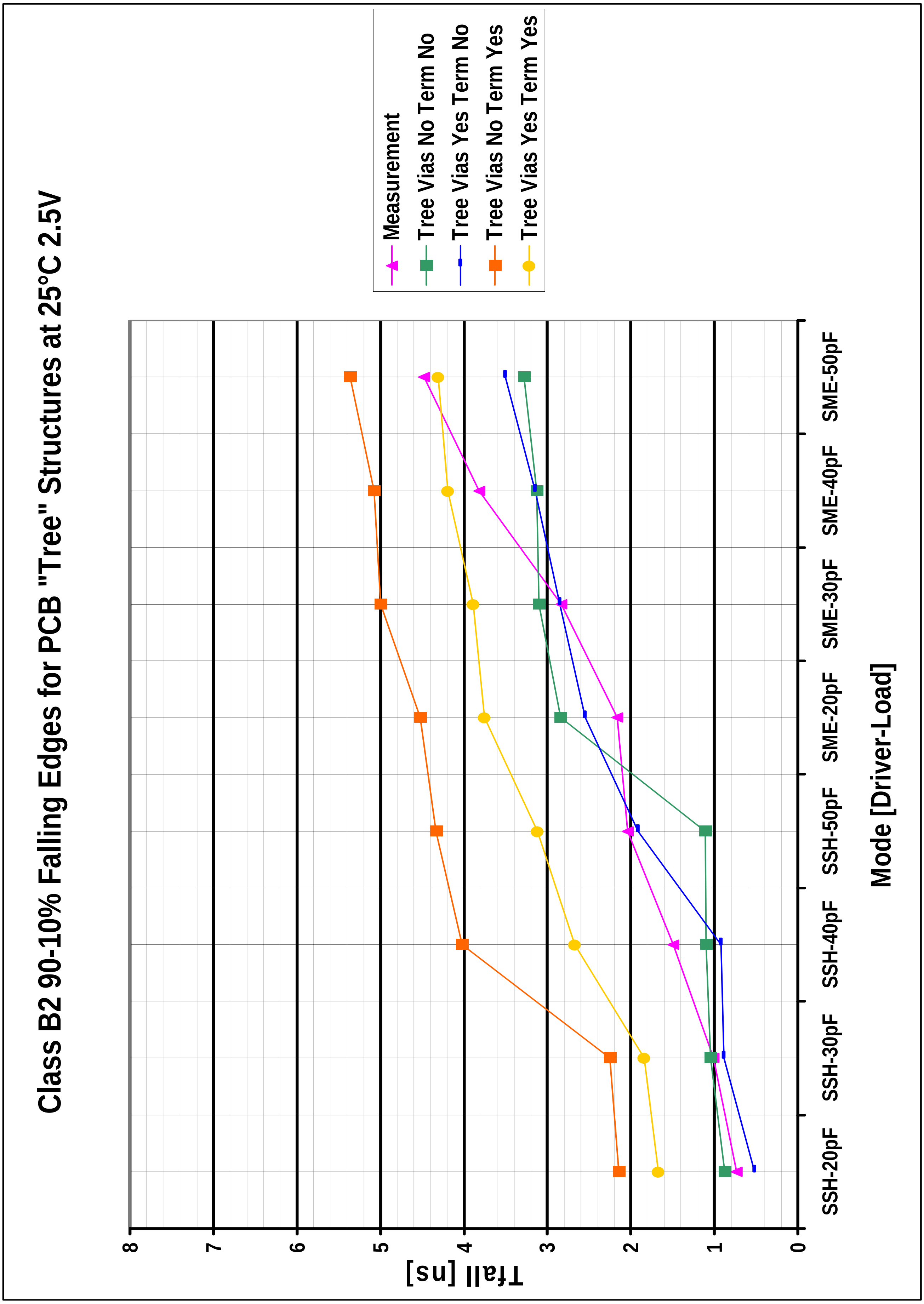


Figure 59: Class B2 fall times for "Tree" layout at 25°C

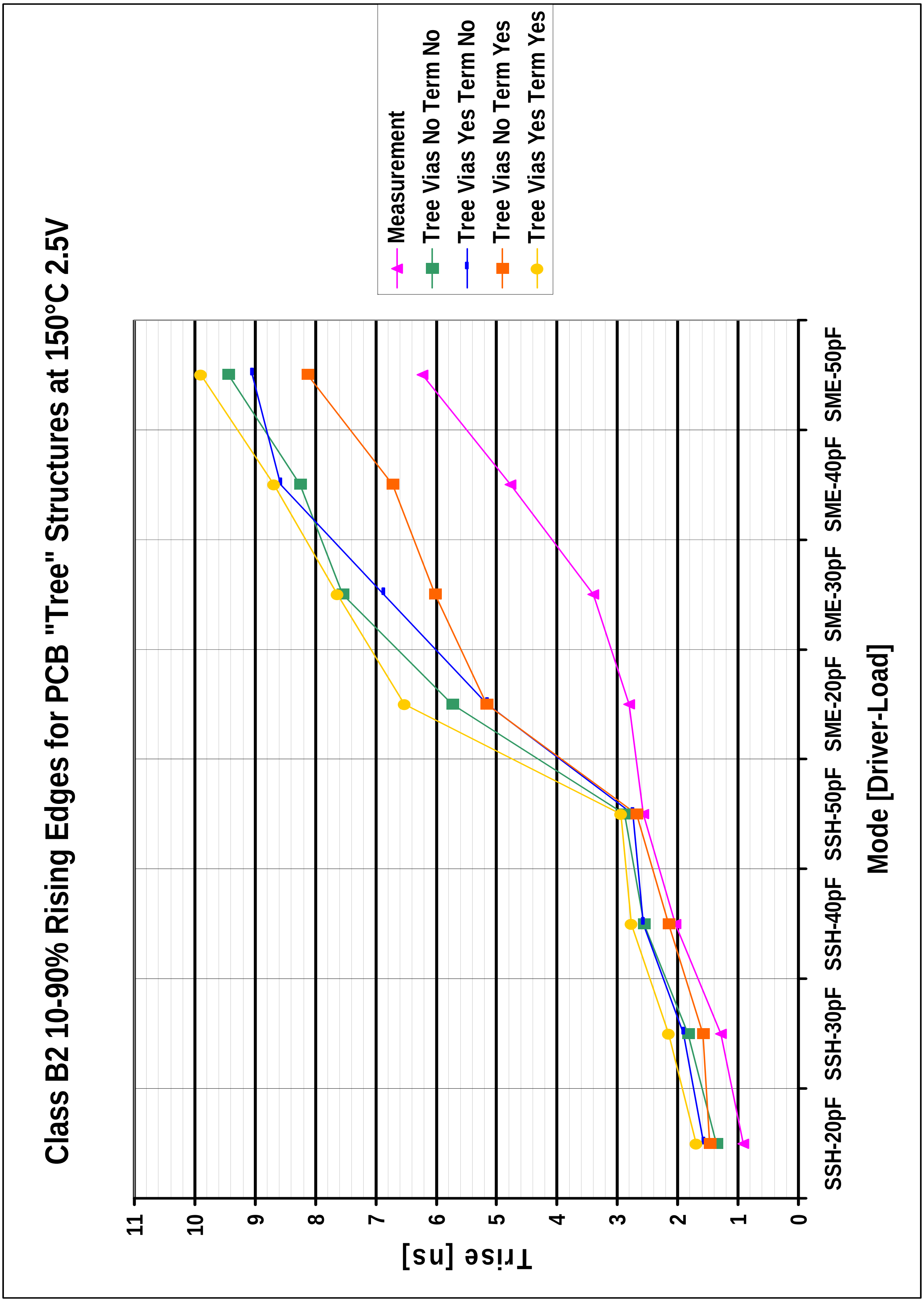


Figure 60: Class B2 rise times for “Tree” layout at 150°C

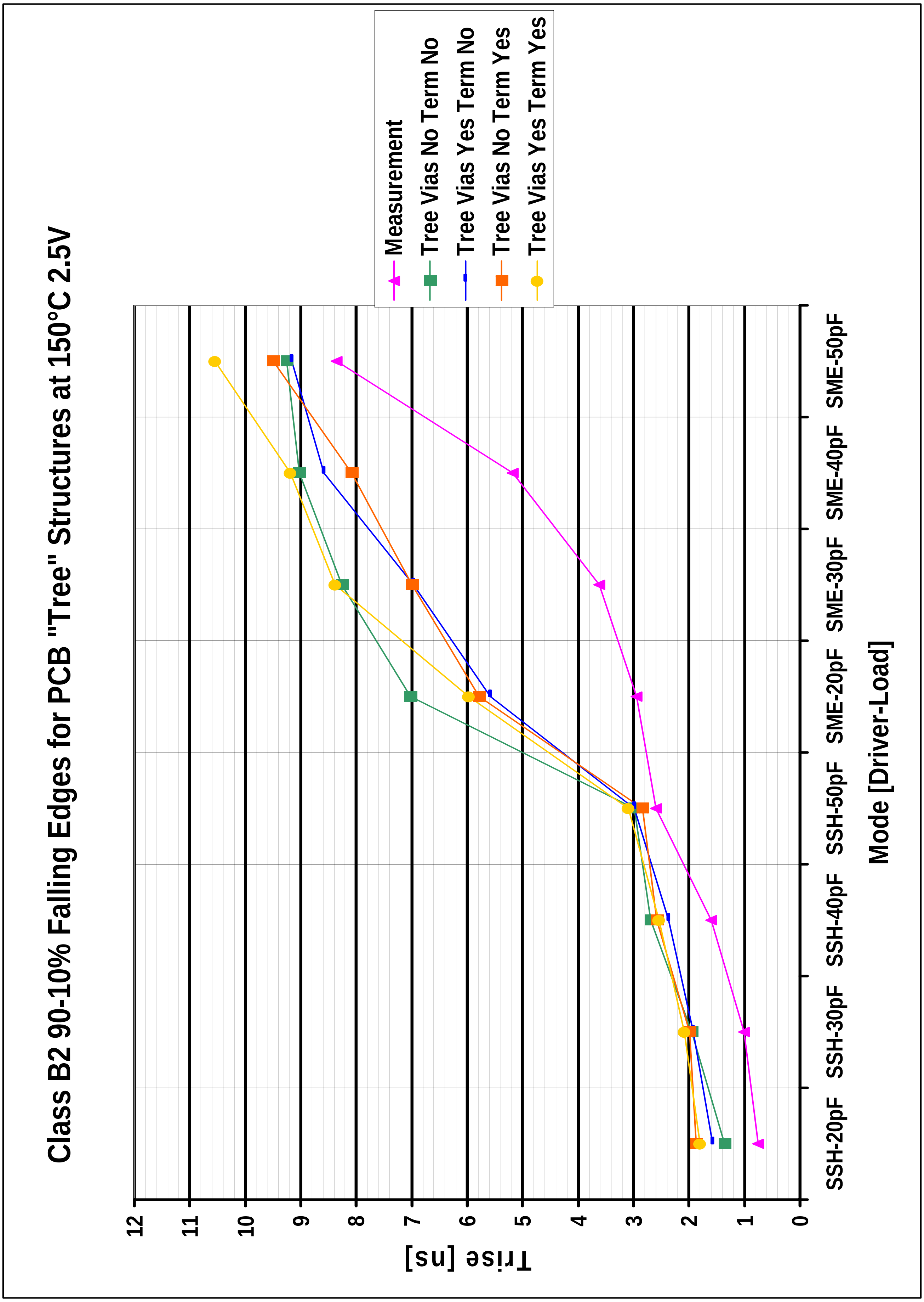


Figure 61: Class B2 fall times for "Tree" layout at 150°C

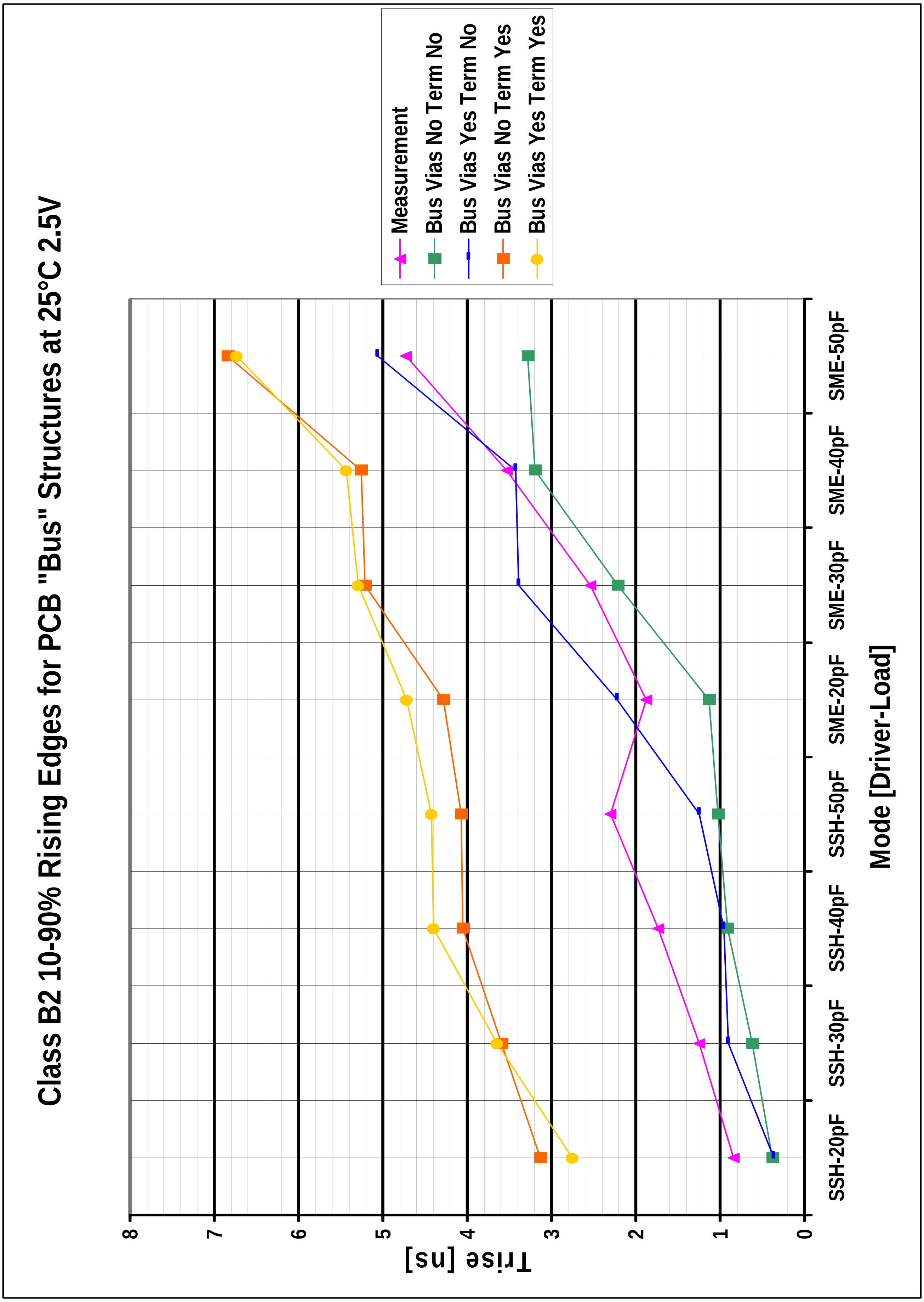


Figure 62: Class B2 rise times for "Bus" layout at 25°C

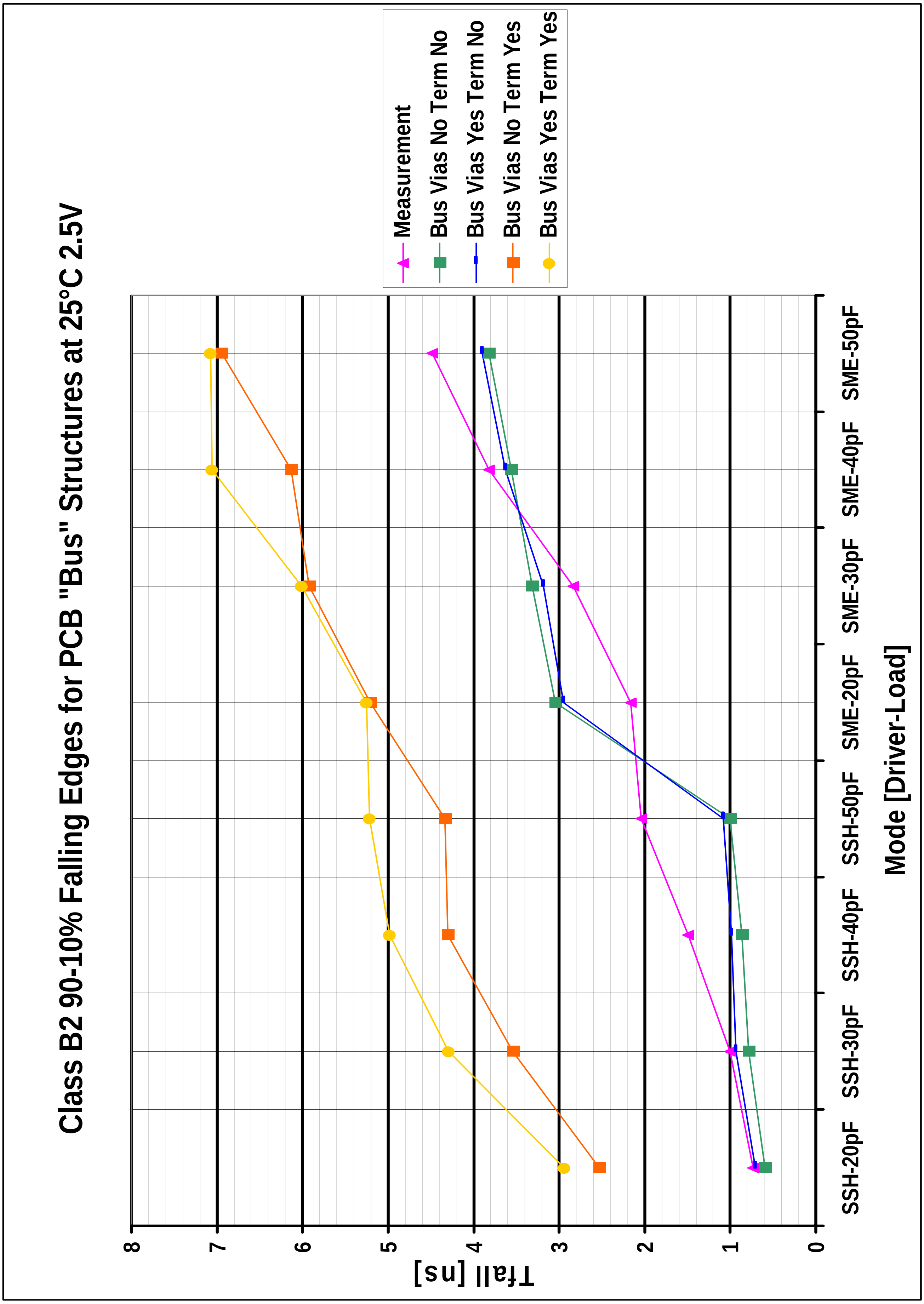


Figure 63: Class B2 fall times for "Bus" layout at 25°C

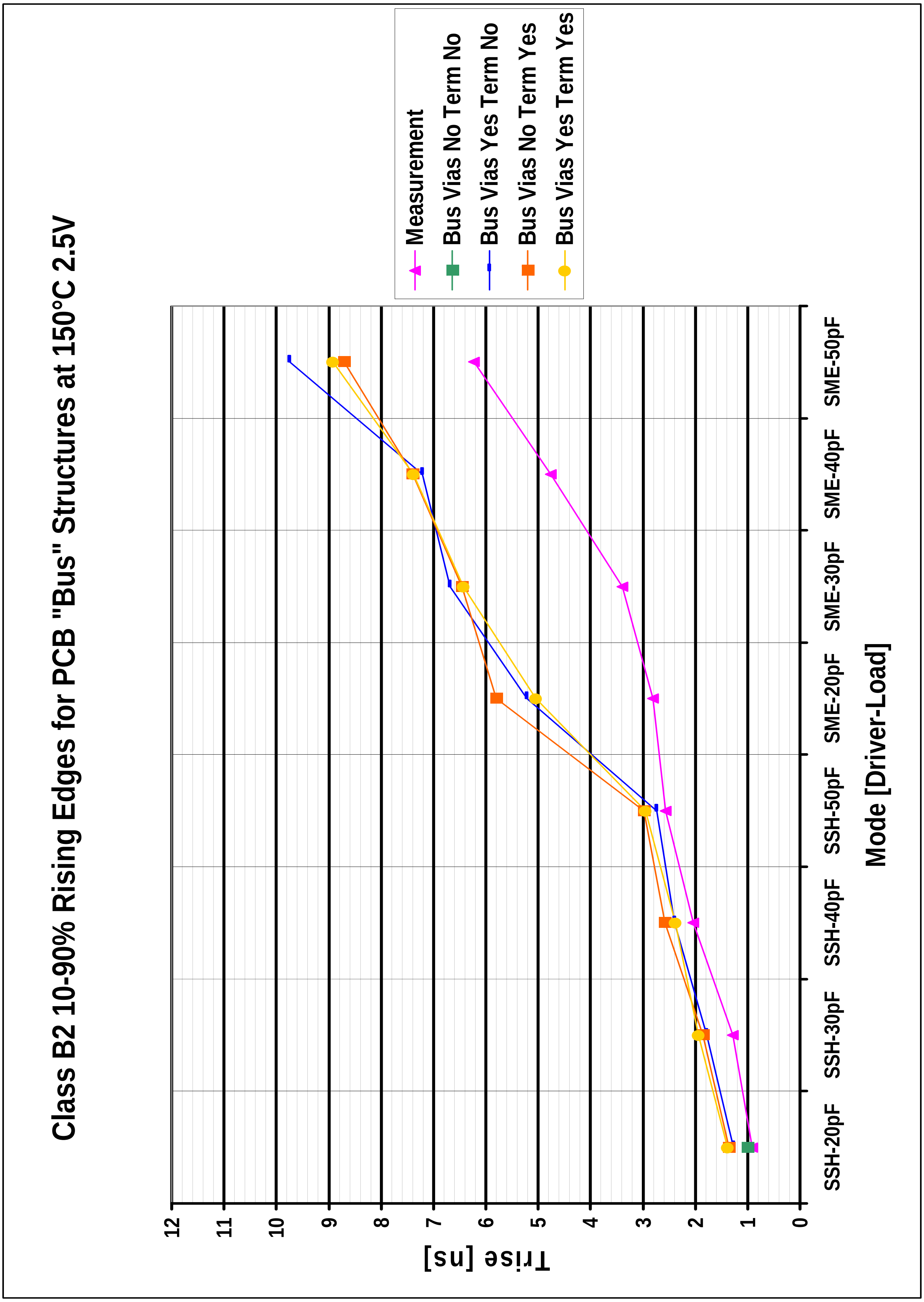


Figure 64: Class B2 rise times for "Bus" layout at 150°C

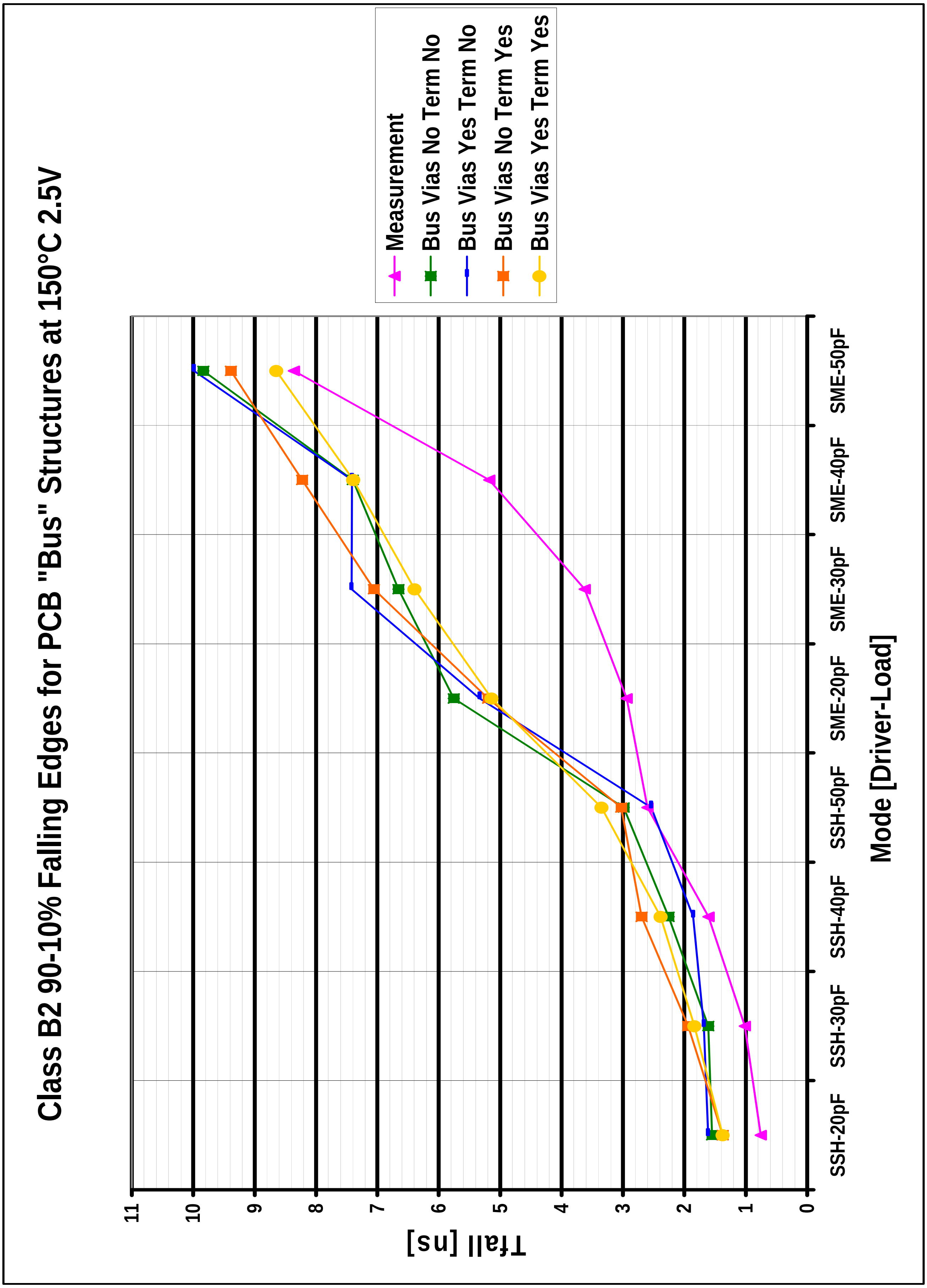


Figure 65: Class B2 fall times for “Bus” layout at 150°C

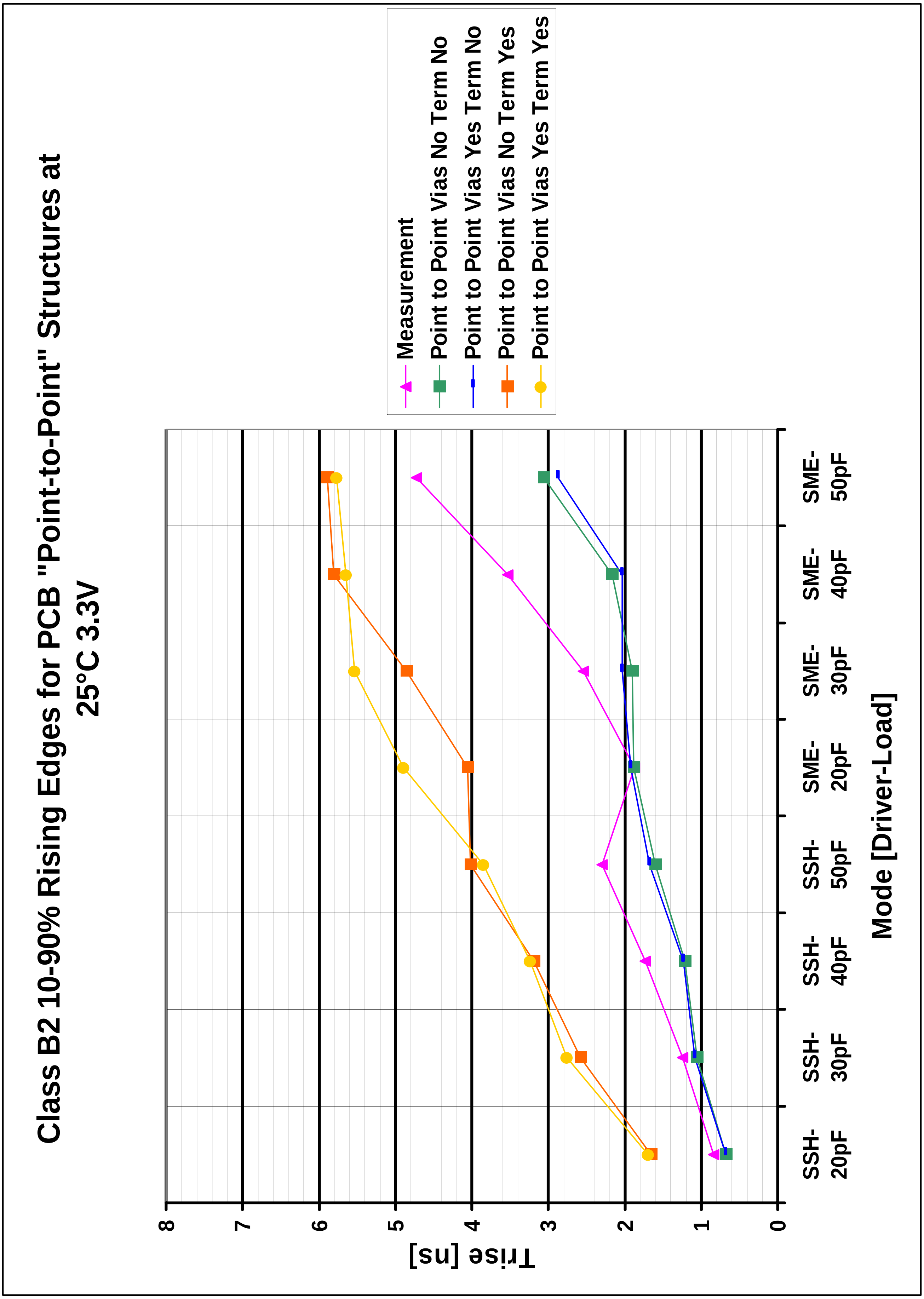


Figure 66: Class B2 rise times for "Point-to-Point" layout at 25°C

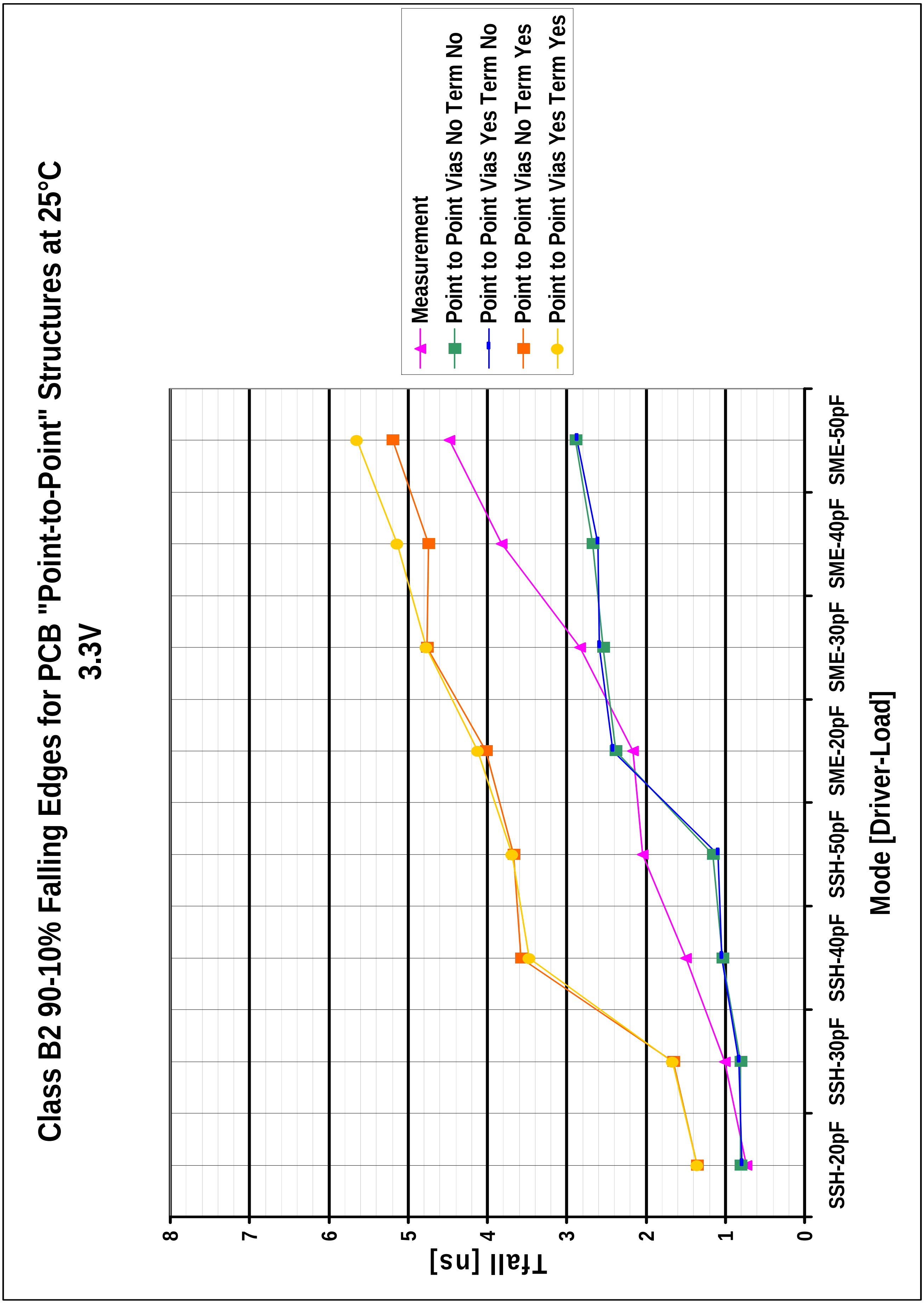


Figure 67: Class B2 fall times for “Point-to-Point” layout at 25°C

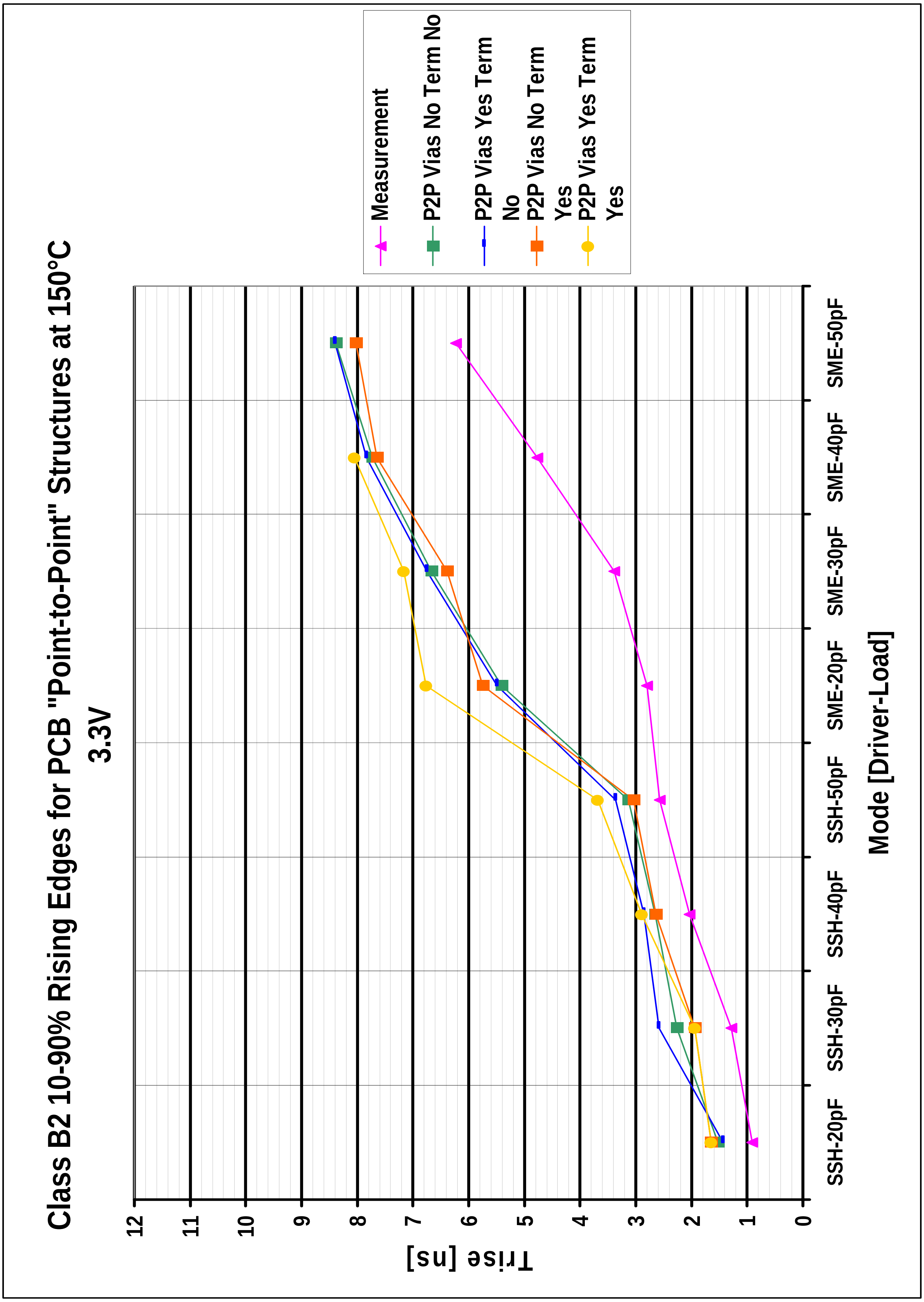


Figure 68: Class B2 rise times for “Point-to-Point” layout at 150°C

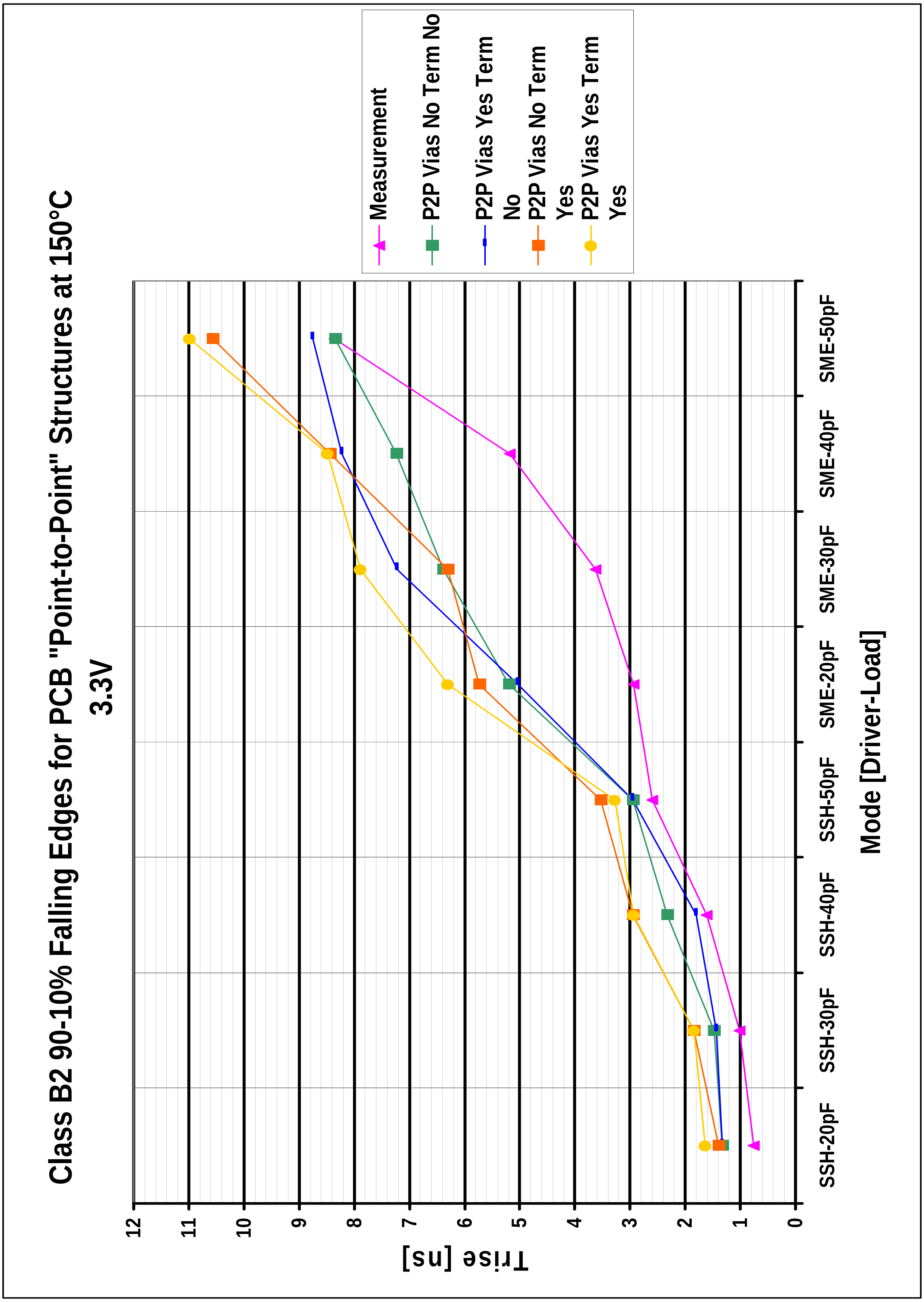


Figure 69: Class B2 fall times for “Point-to-Point” layout at 150°C

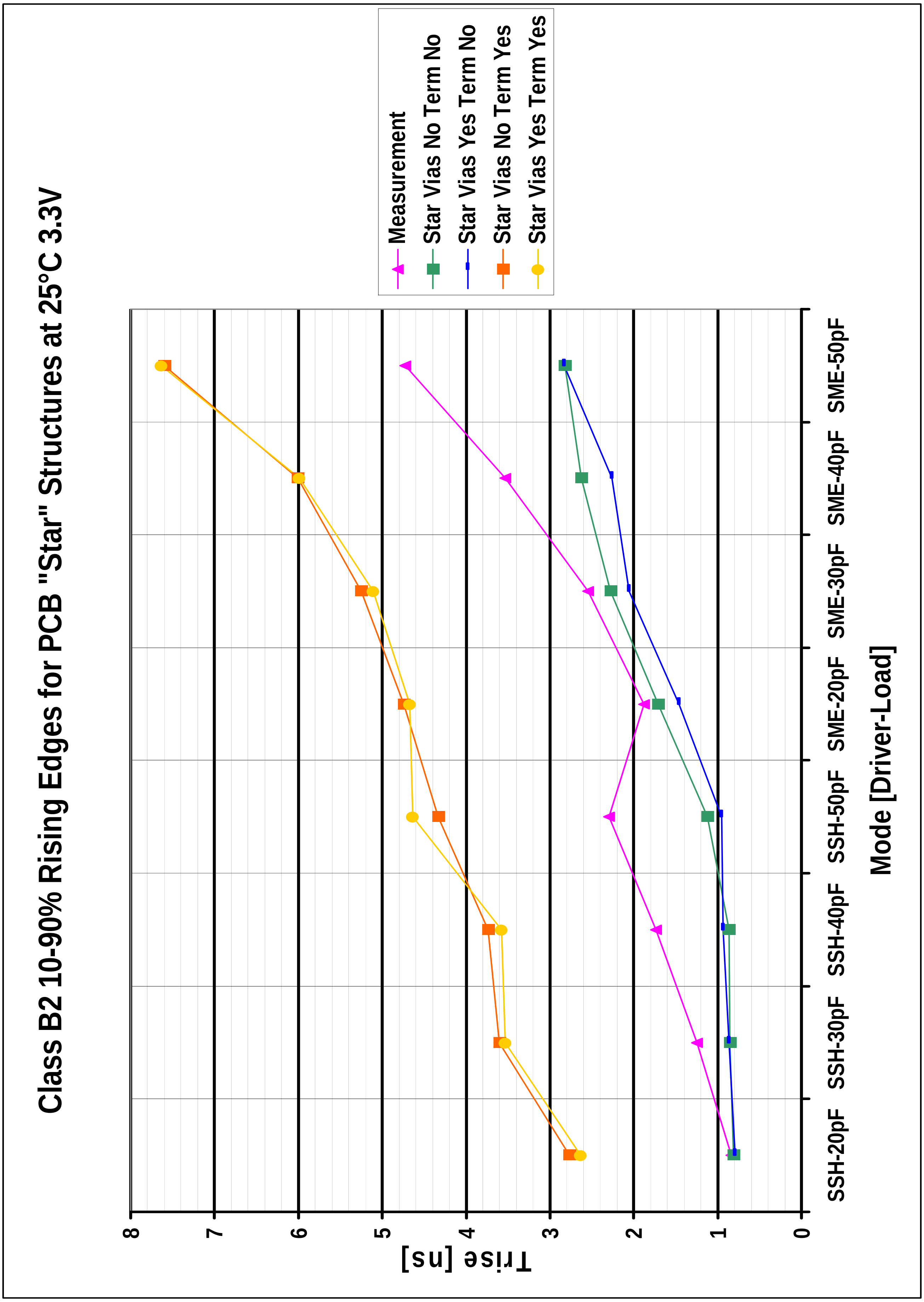


Figure 70: Class B2 rise times for “Star” layout at 25°C

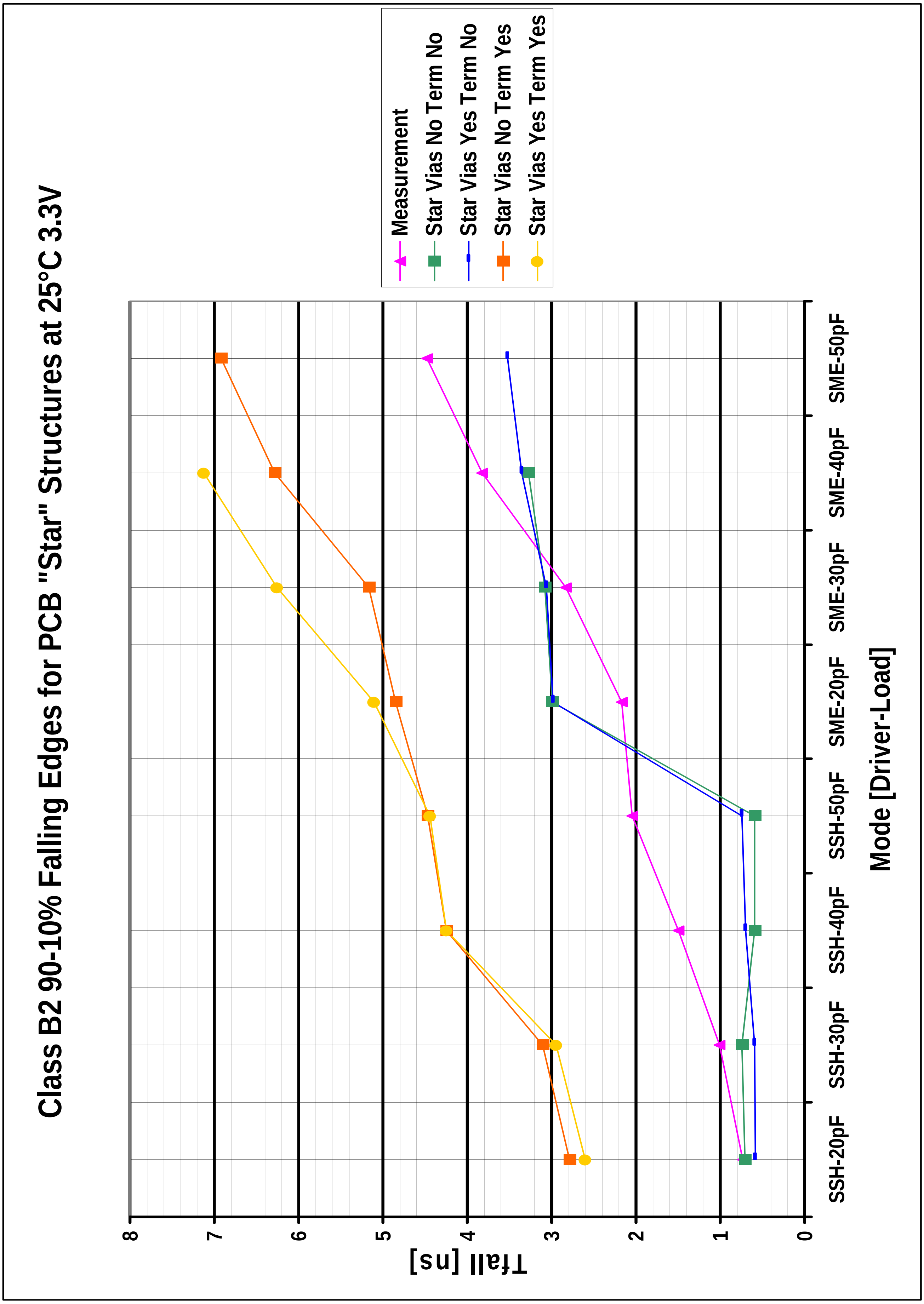


Figure 71: Class B2 fall times for “Star” layout at 25°C

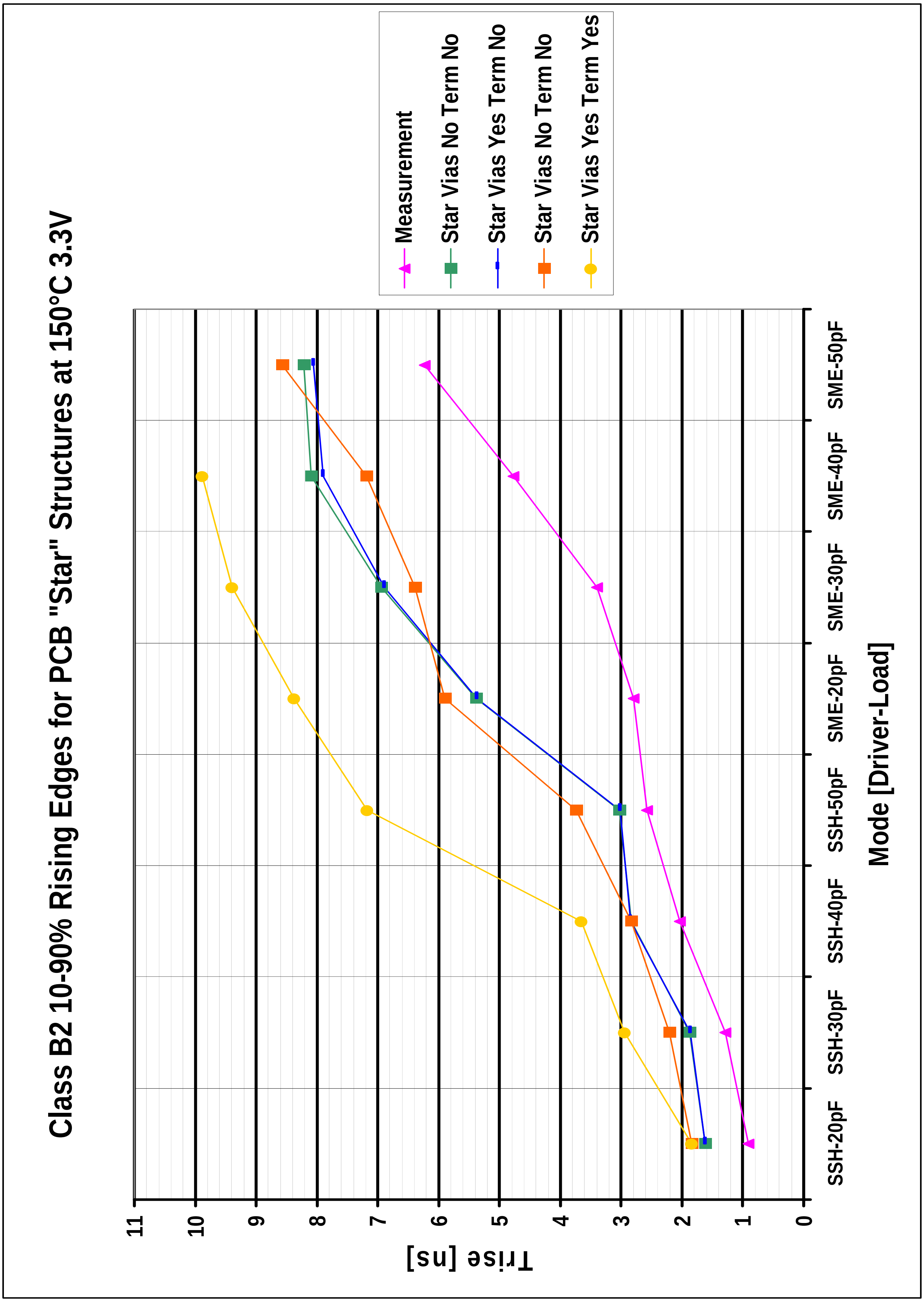


Figure 72: Class B2 rise times for “Star” layout at 150°C

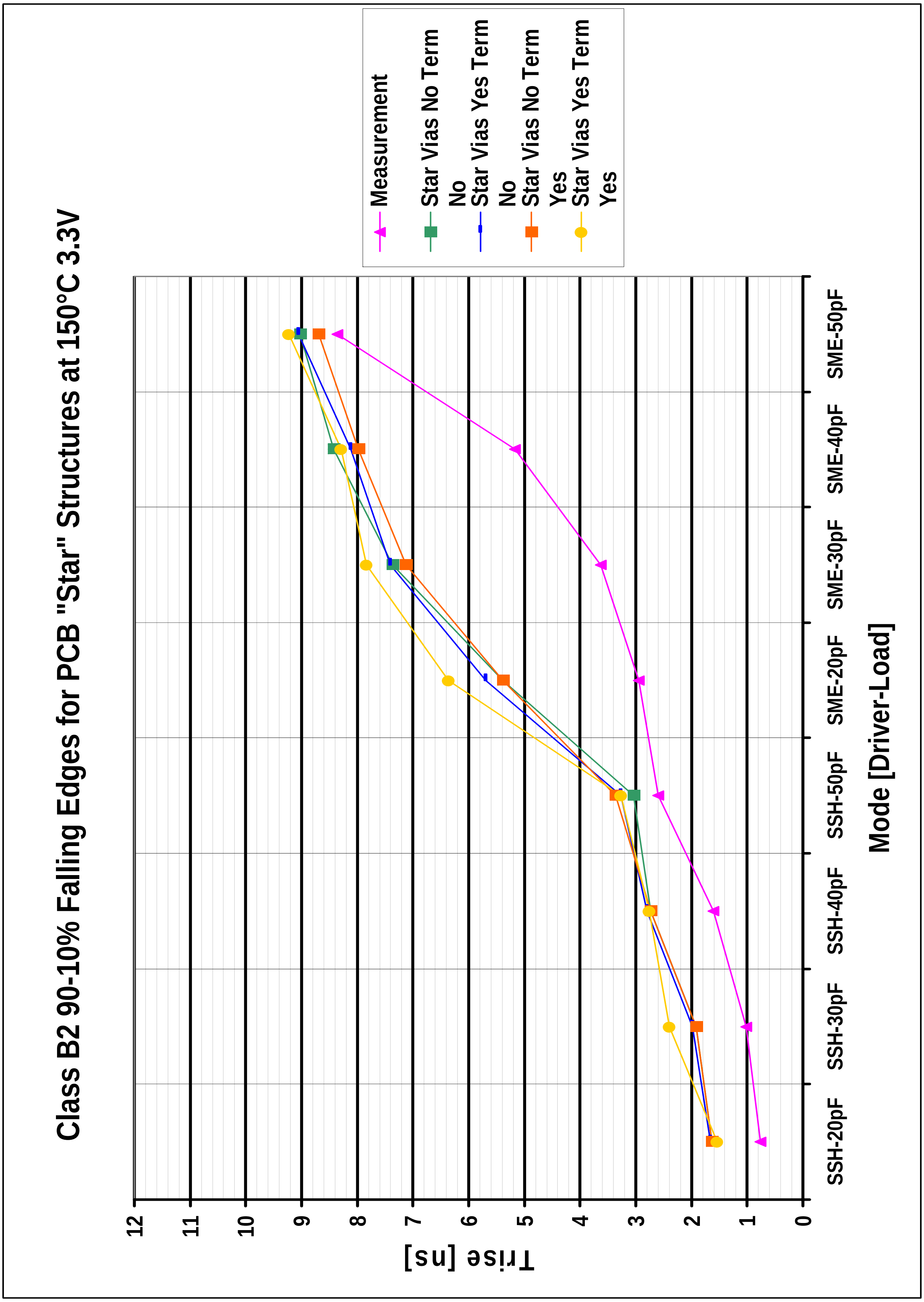


Figure 73: Class B2 fall times for "Star" layout at 150°C

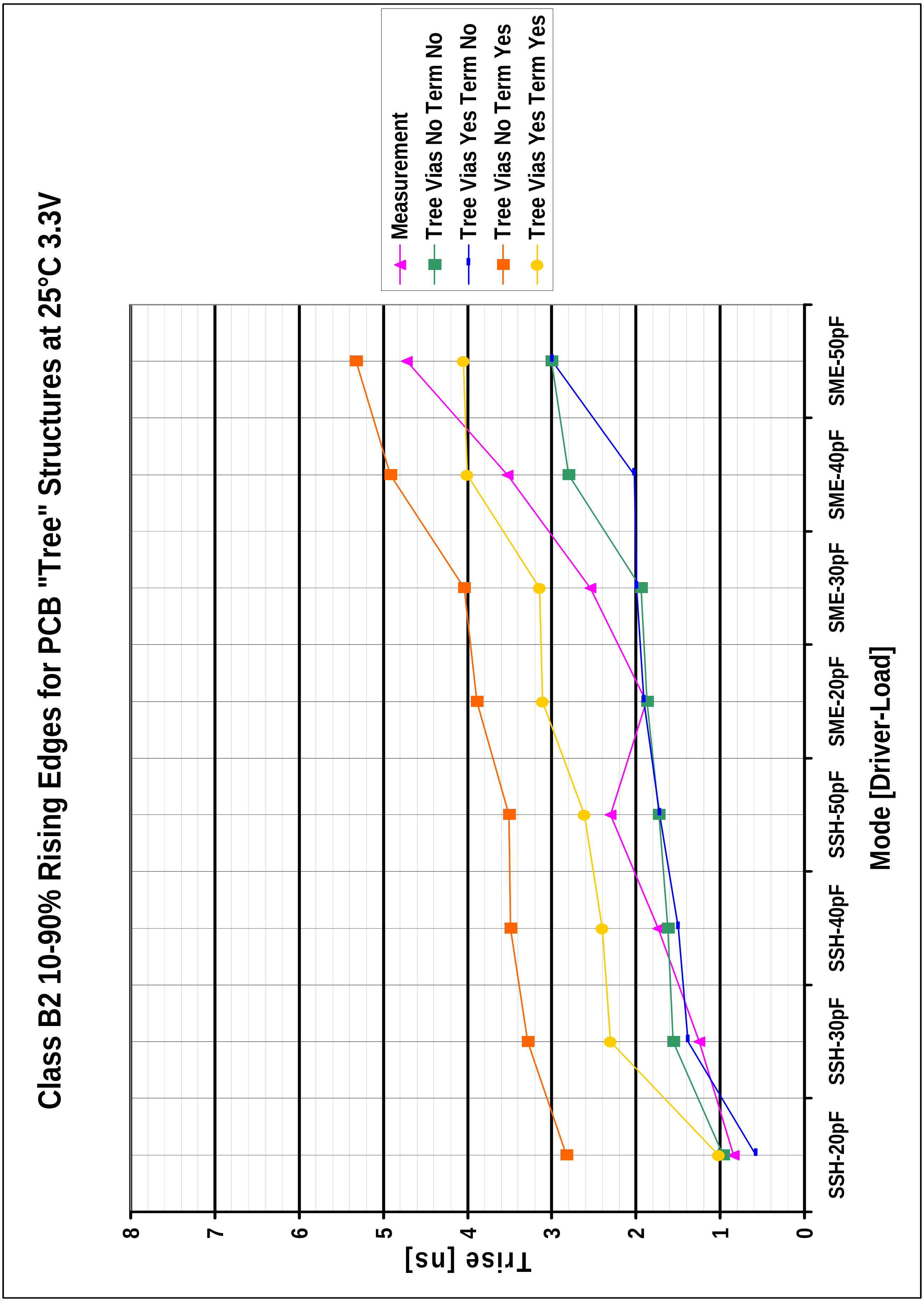


Figure 74: Class B2 rise times for "Tree" layout at 25°C

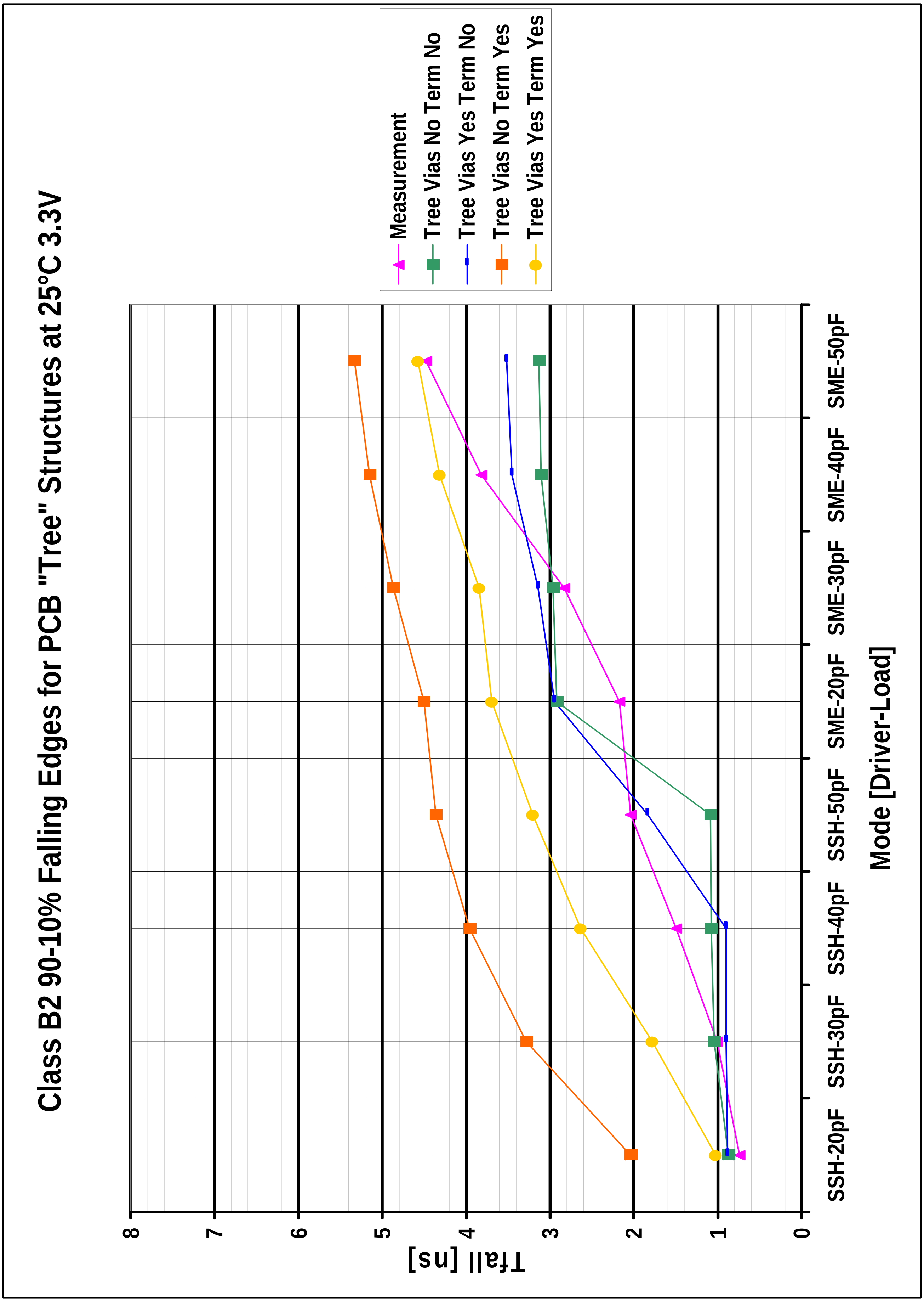


Figure 75: Class B2 rise times for “Tree” layout at 25°C

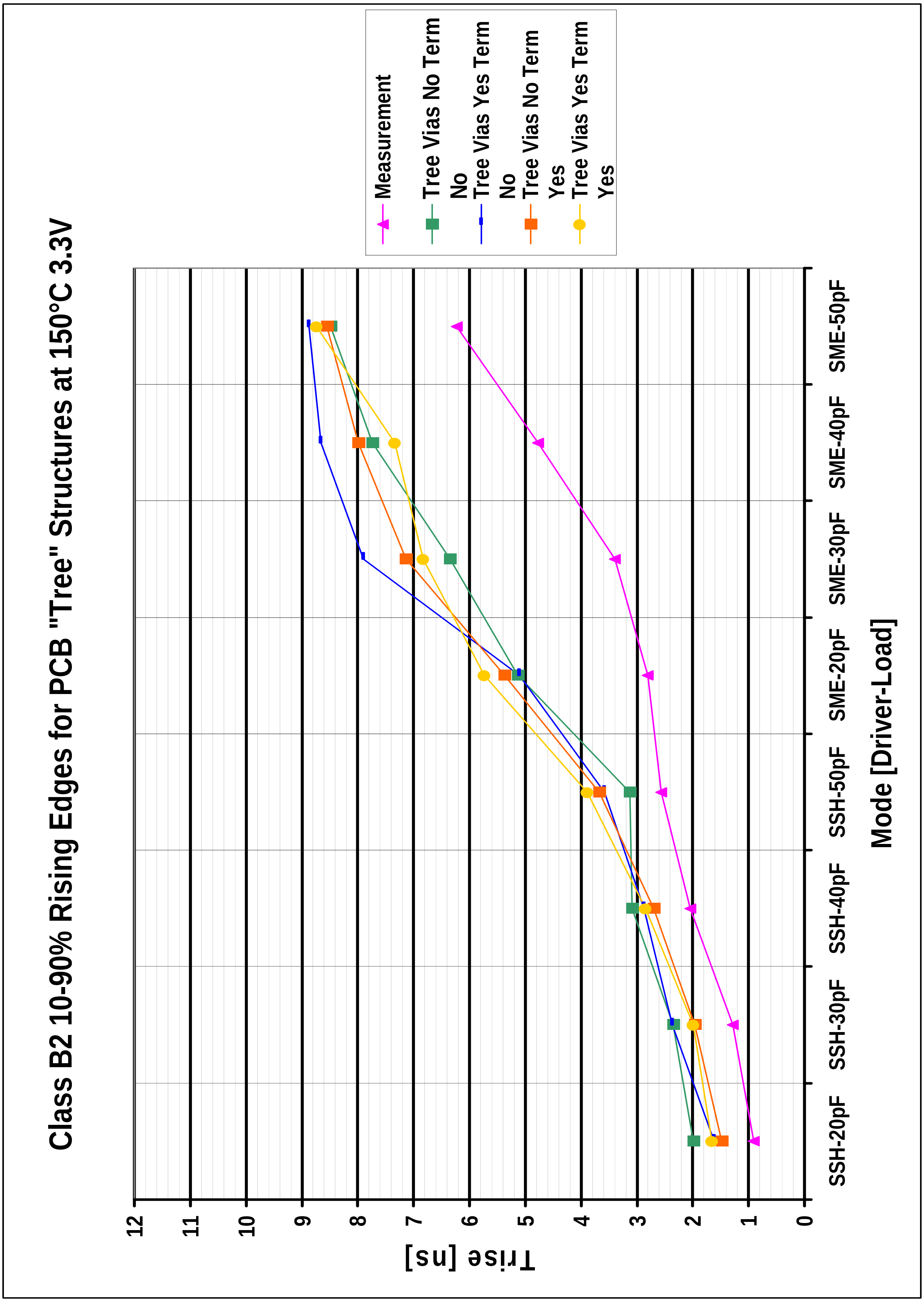


Figure 76: Class B2 rise times for “Tree” layout at 150°C

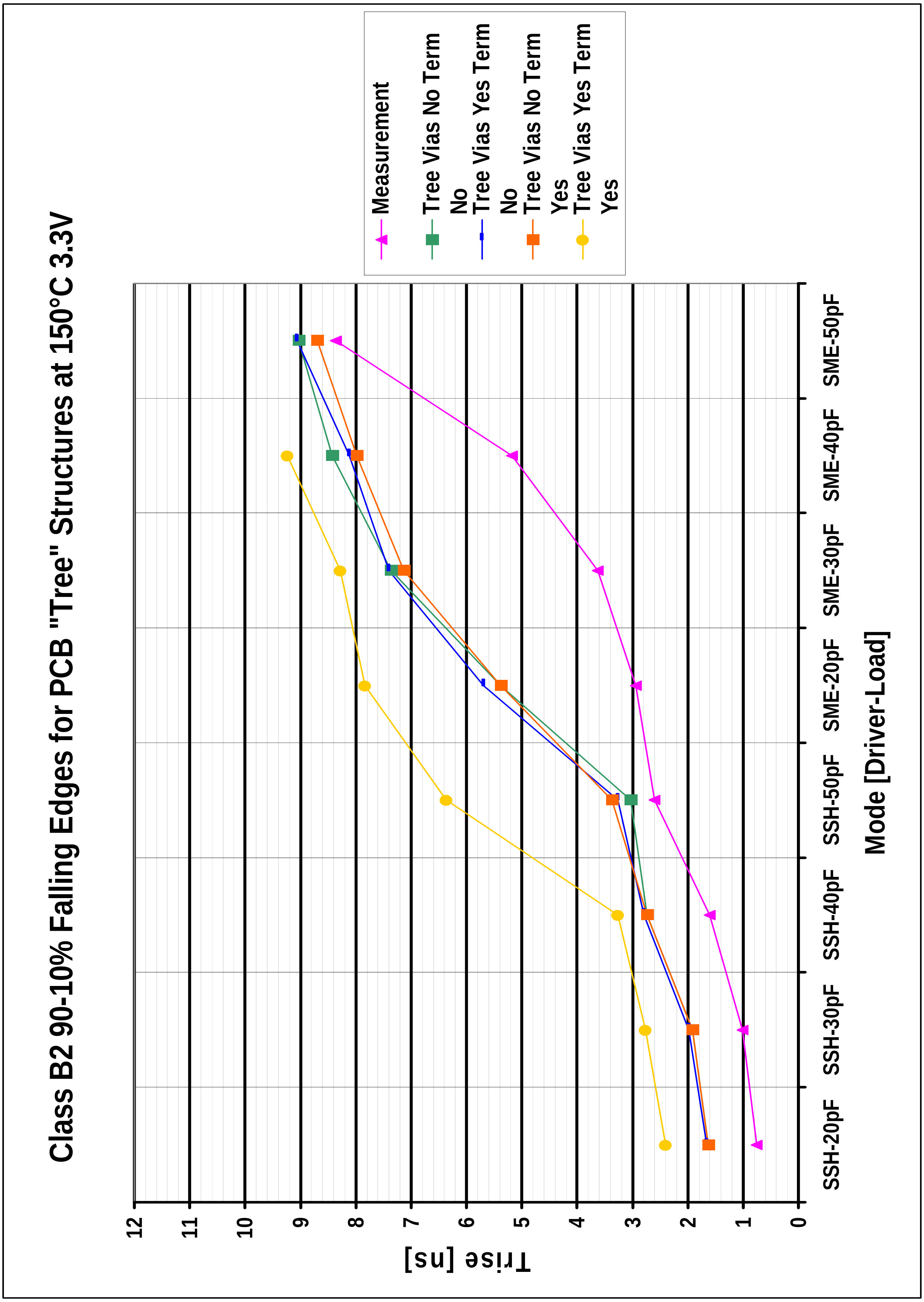


Figure 77: Class B2 fall times for "Tree" layout at 150°C

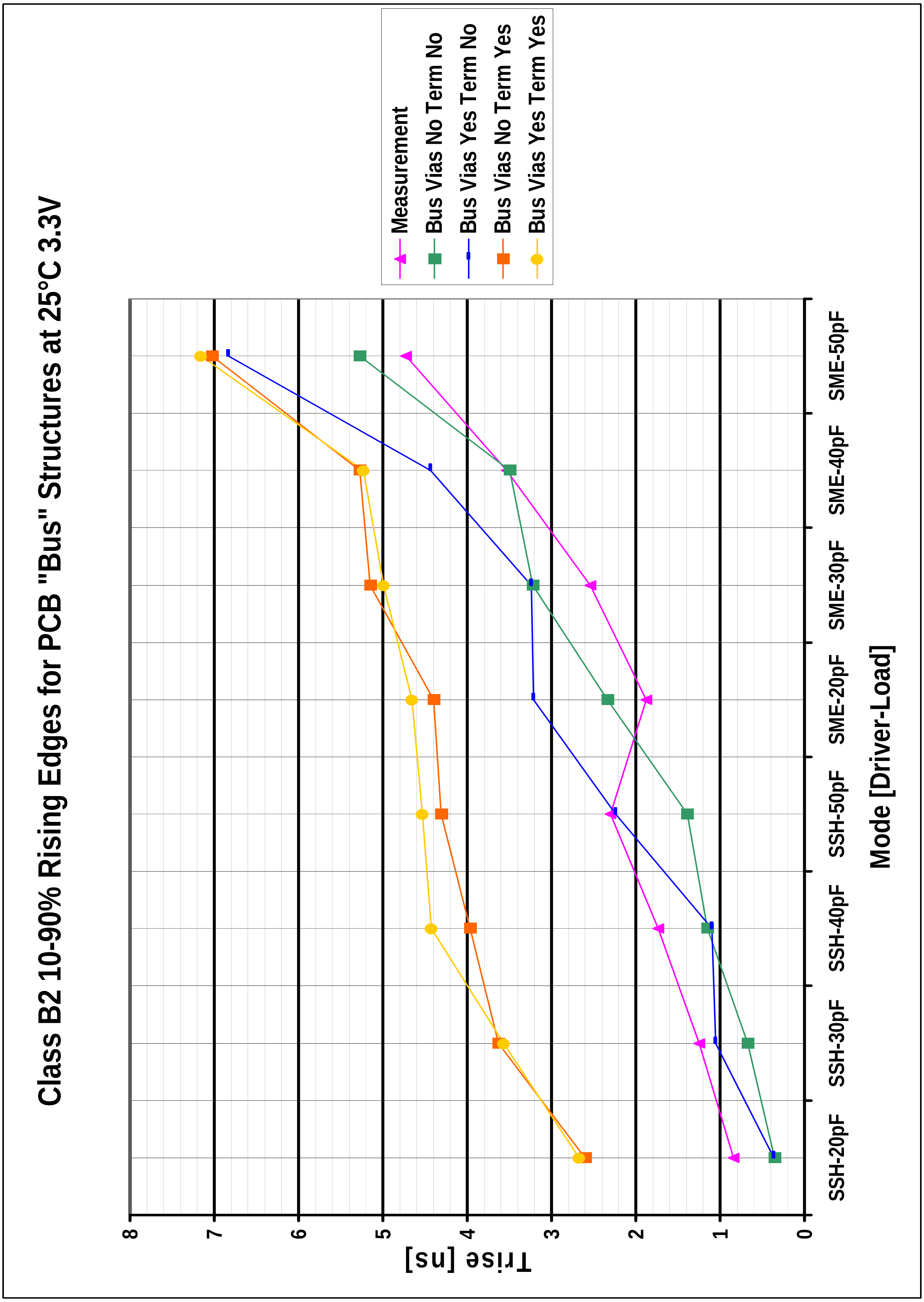


Figure 78: Class B2 rise times for "Bus" layout at 25°C

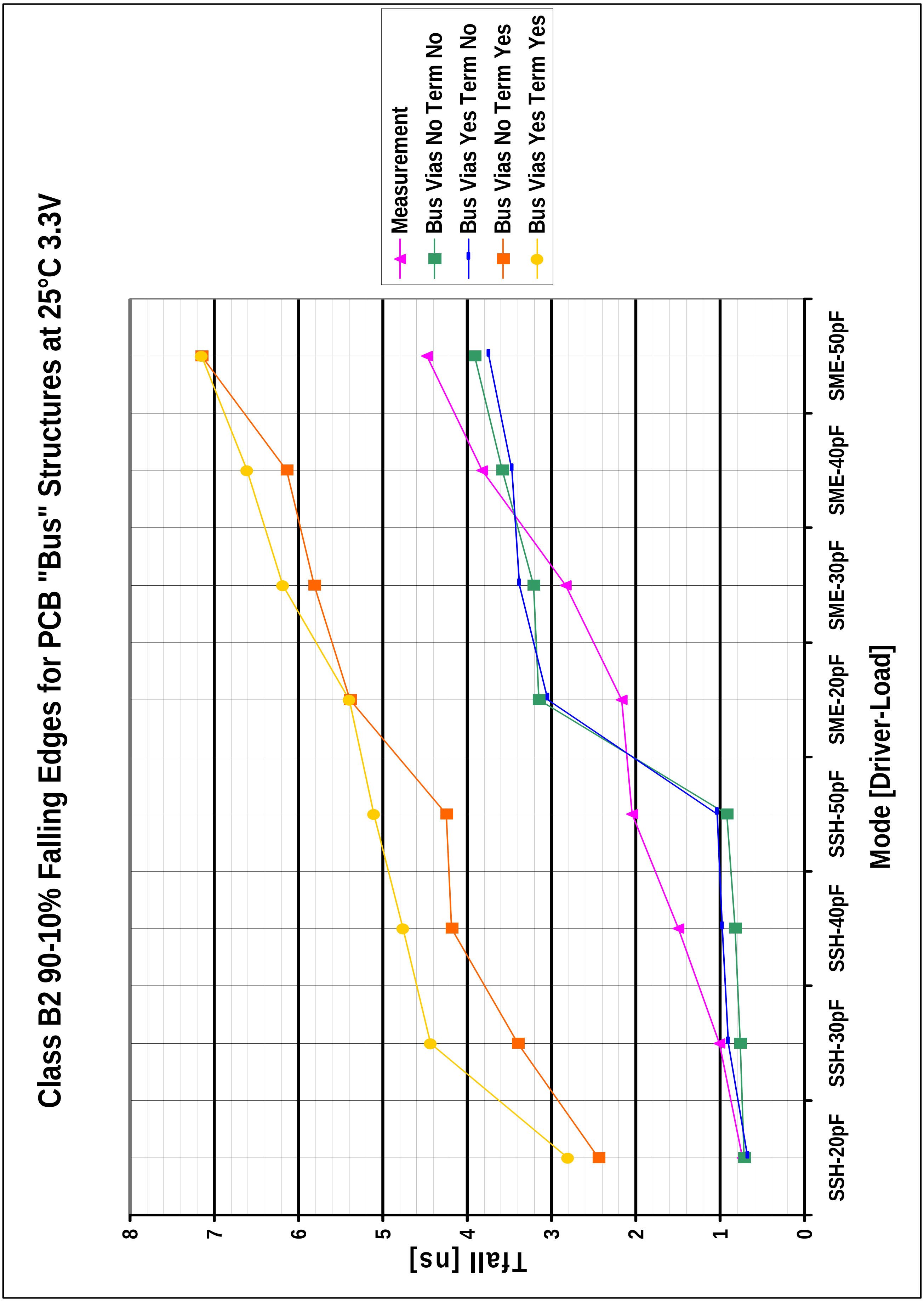


Figure 79: Class B2 fall times for "Tree" layout at 25°C

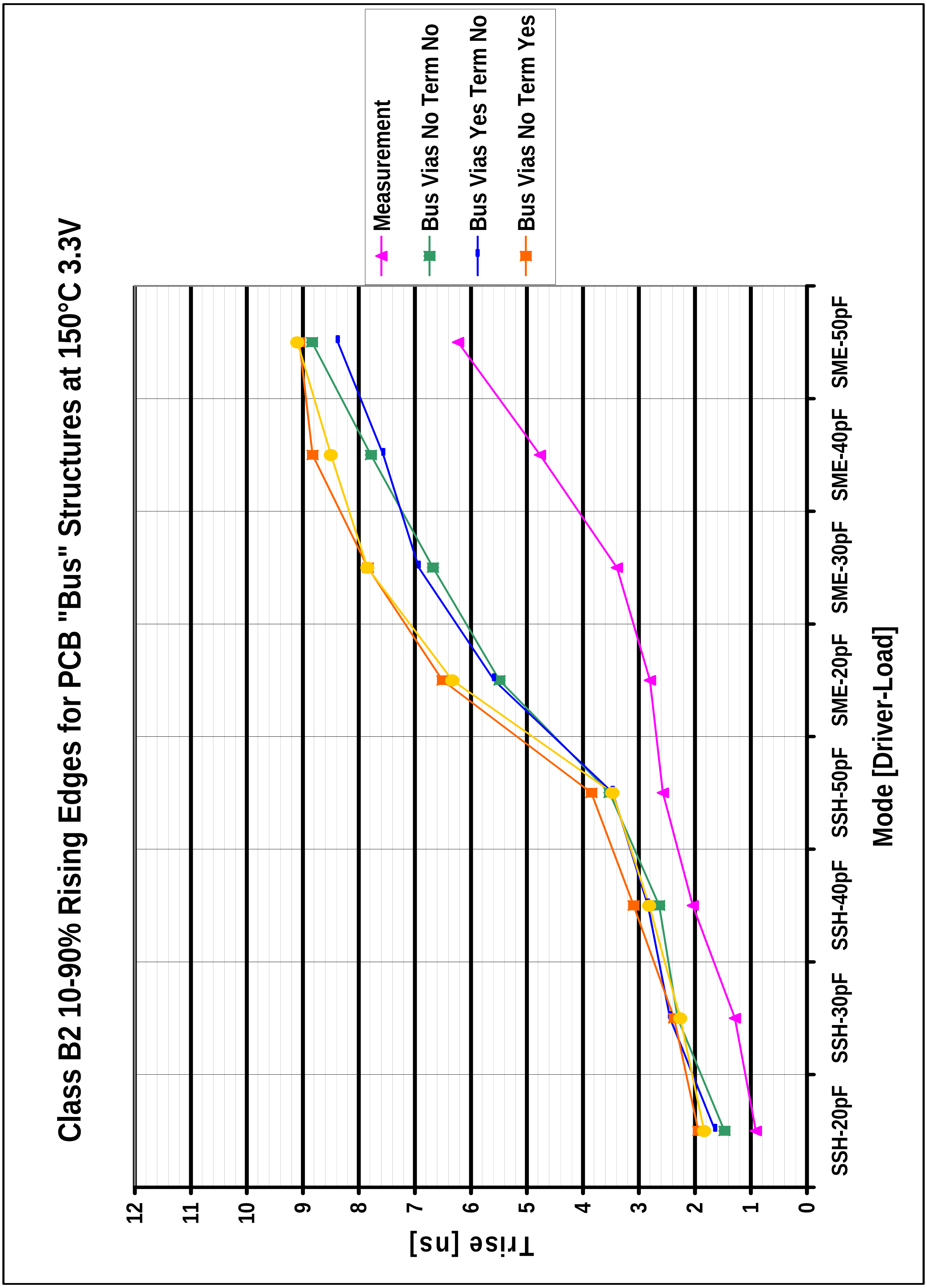


Figure 80: Class B2 rise times for “Bus” layout at 150°C

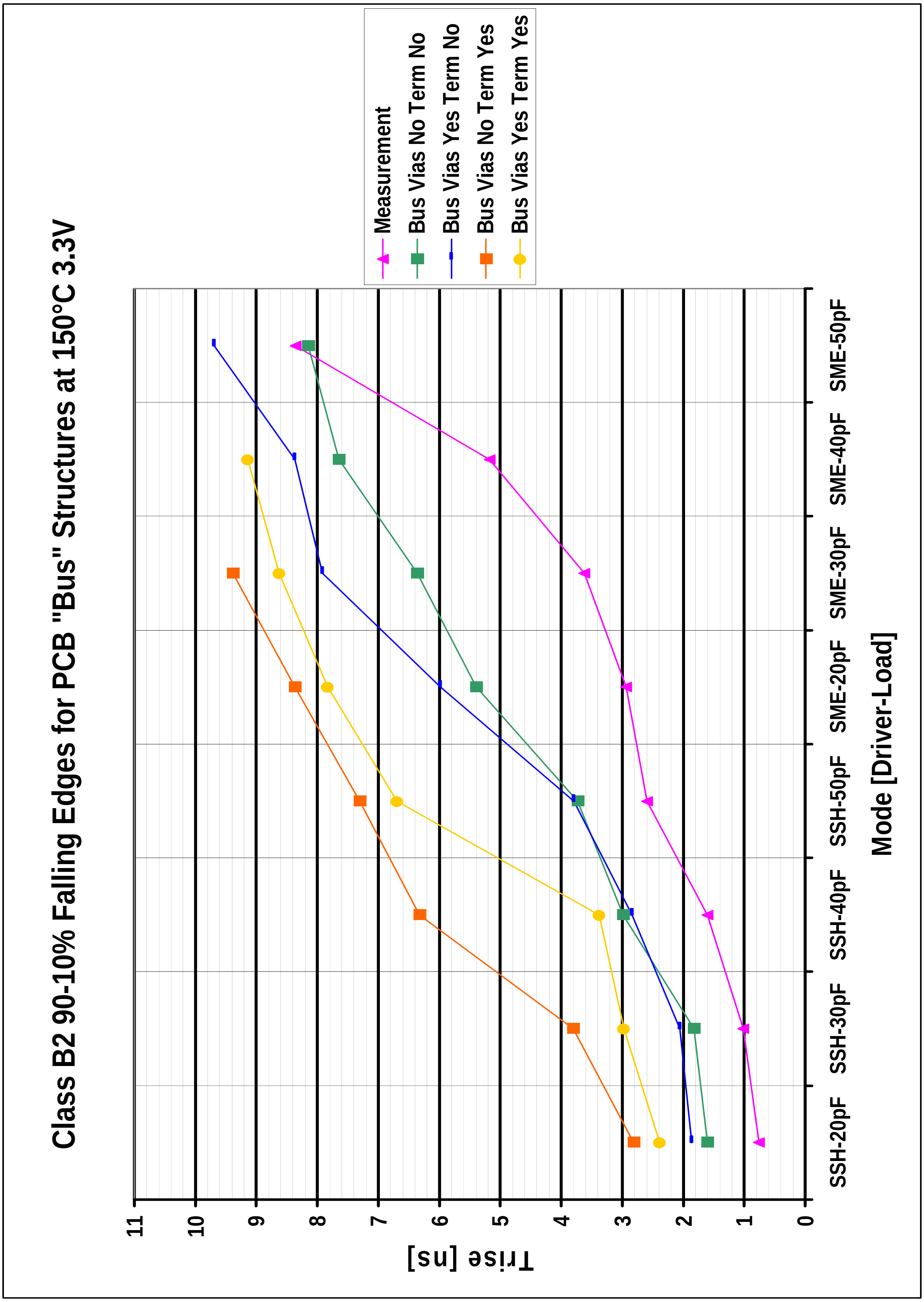


Figure 81: Class B2 rise times for “Bus” layout at 150°C

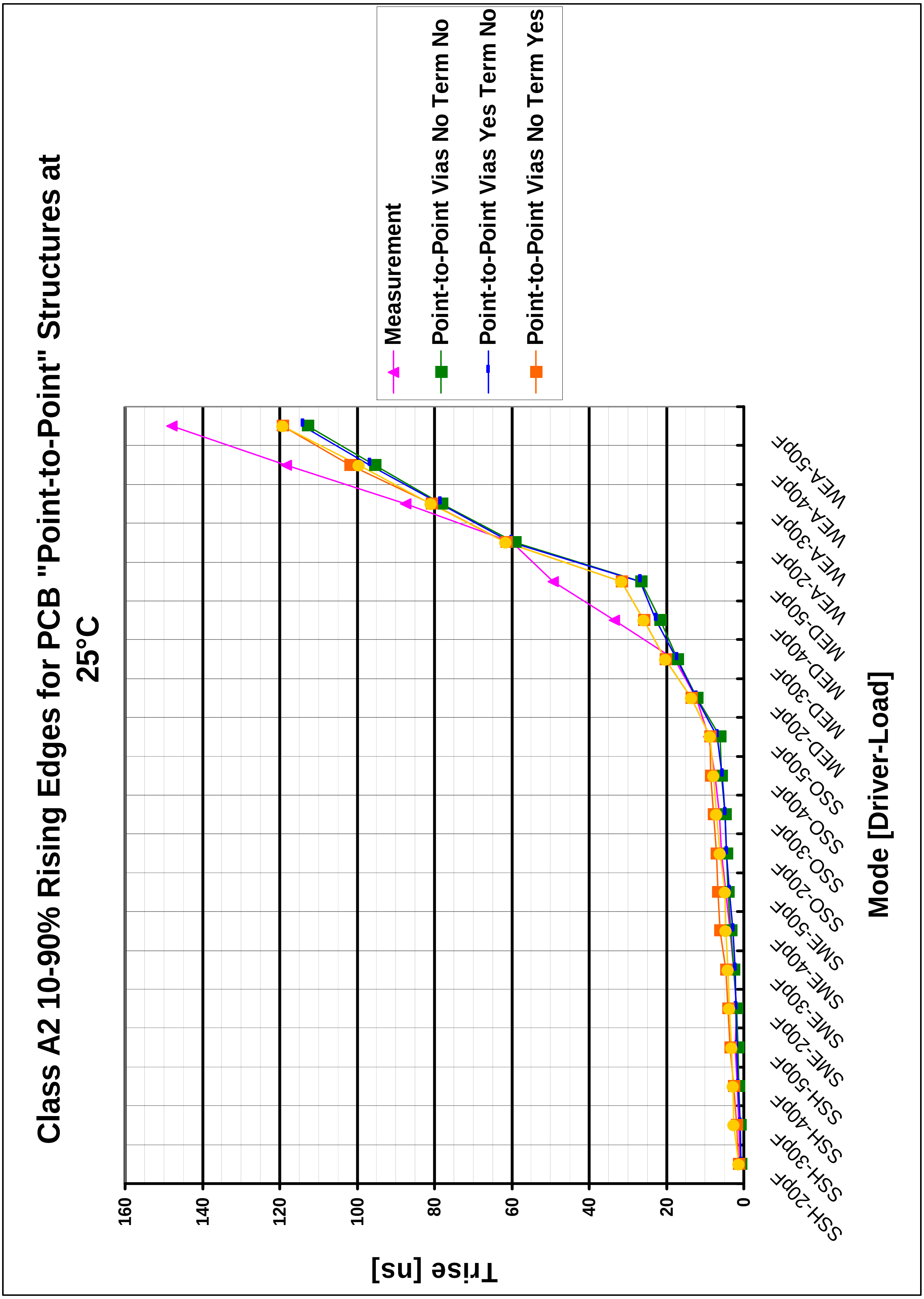


Figure 82: Class A2 rise times for “Point-to-Point” layout at 25°C

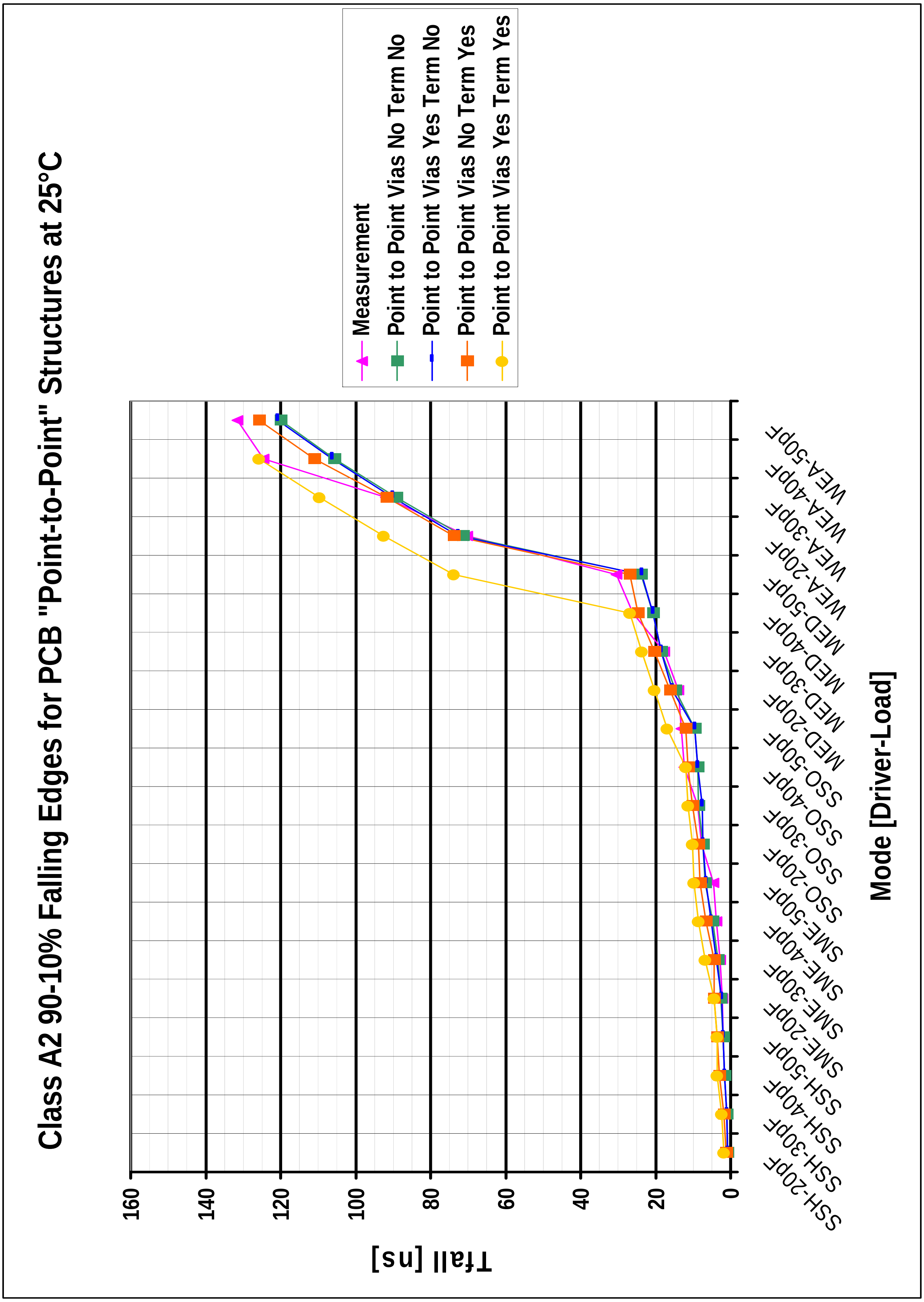


Figure 83: Class A2 fall times for "Point-to-Point" layout at 25°C

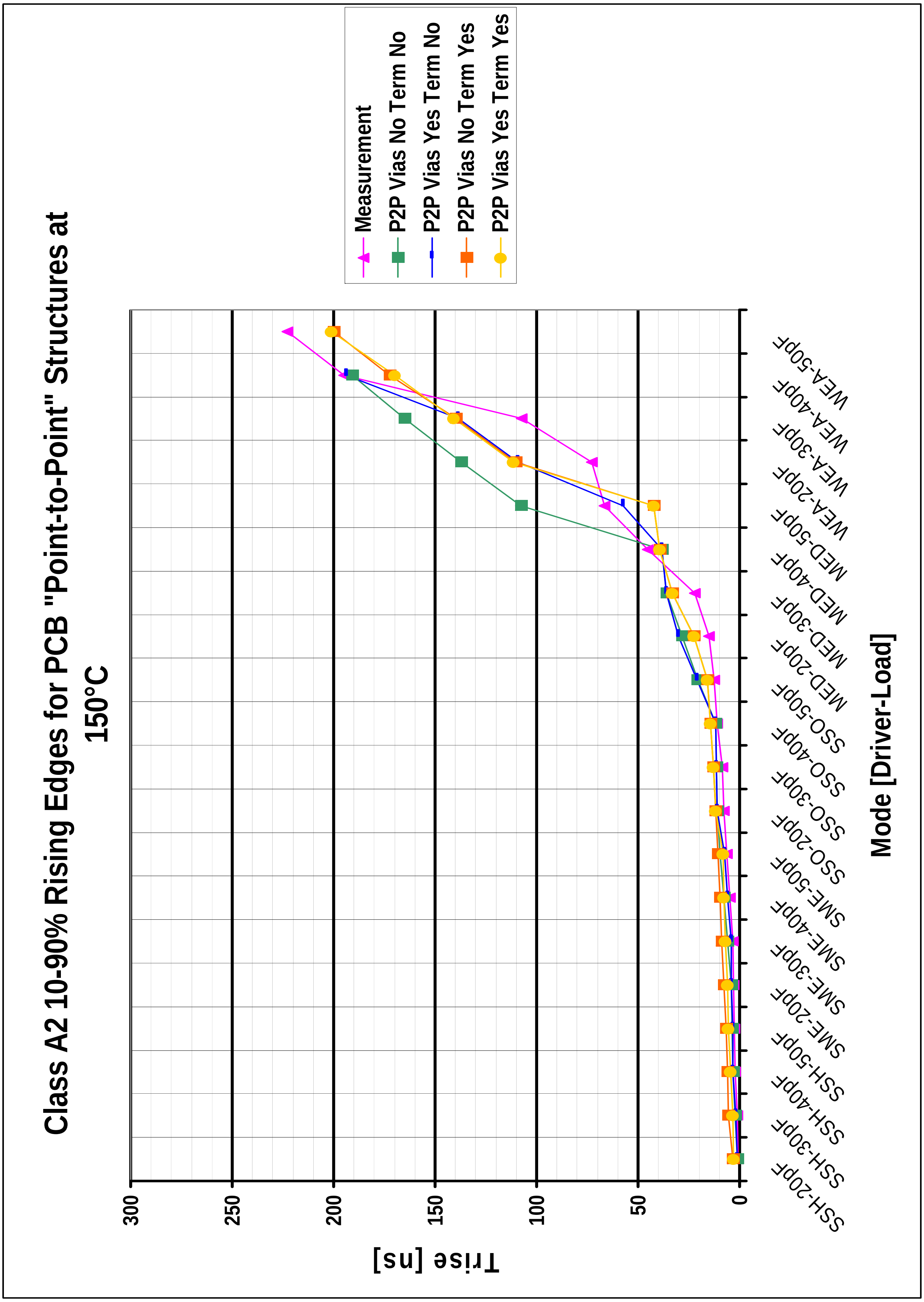


Figure 84: Class A2 rise times for "Point-to-Point" layout at 150°C

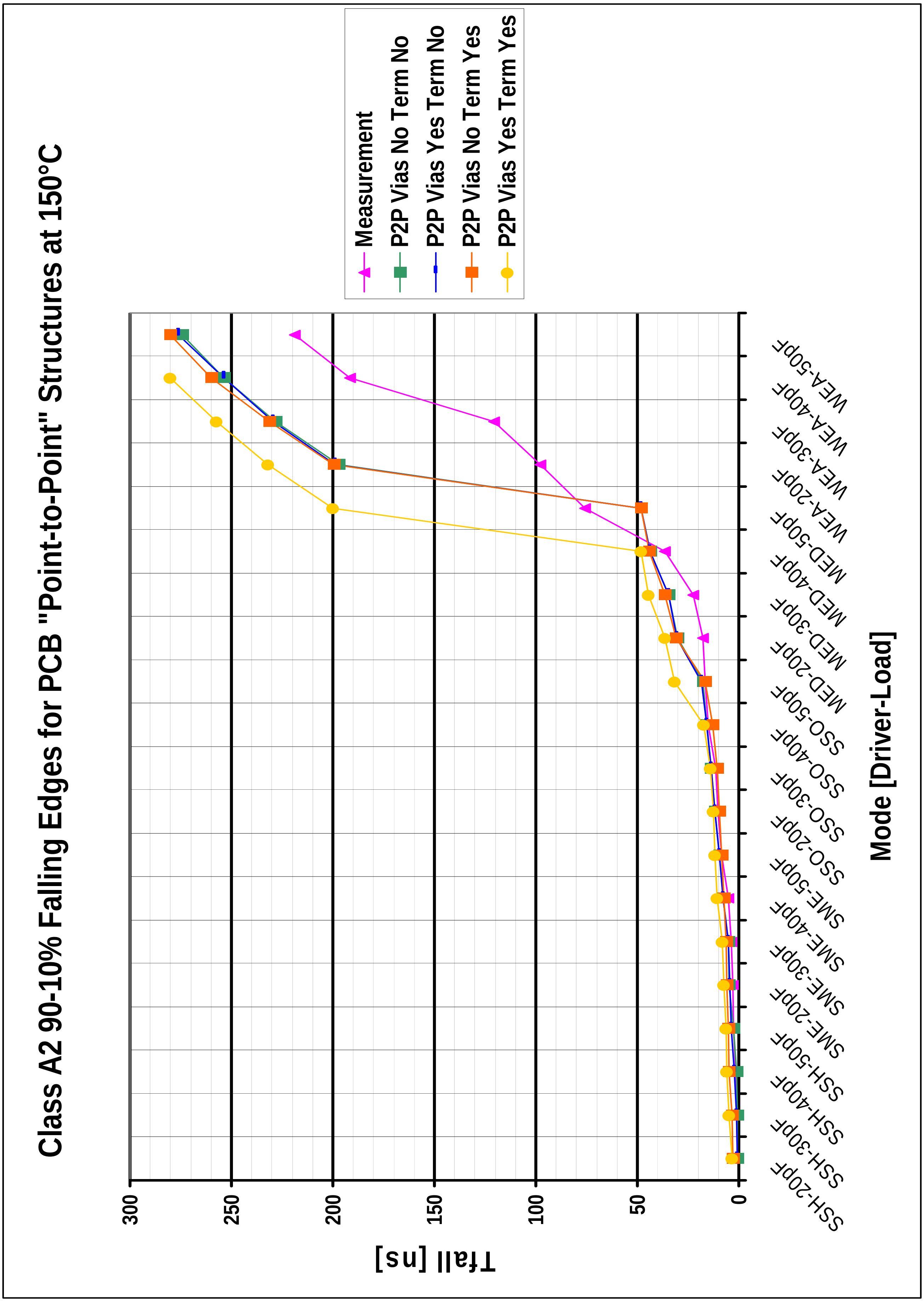


Figure 85: Class A2 fall times for “Point-to-Point” layout at 150°C

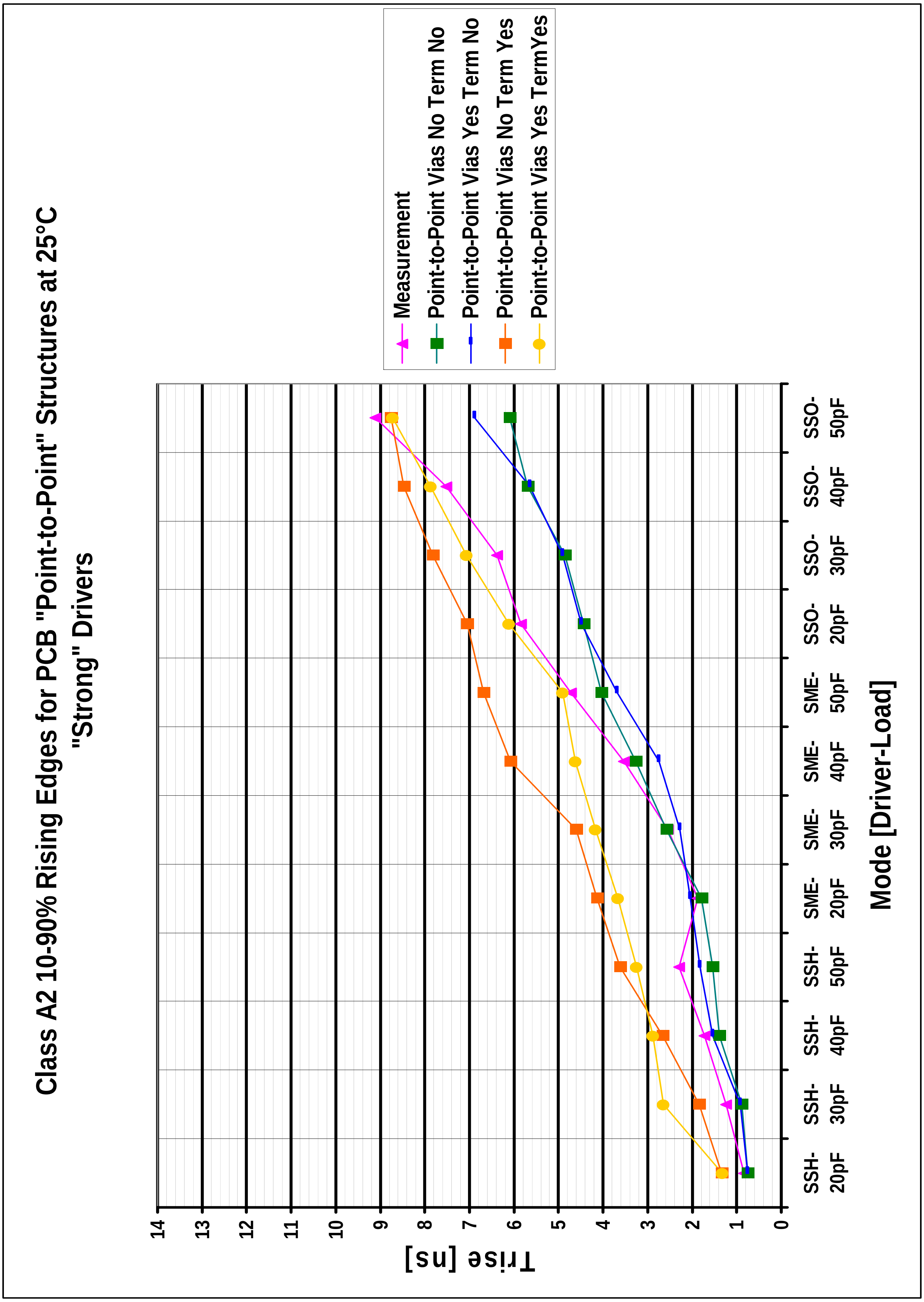


Figure 86: Zoomed rise times Class A2- Point-to-Point layout for strong driver settings at 25°C

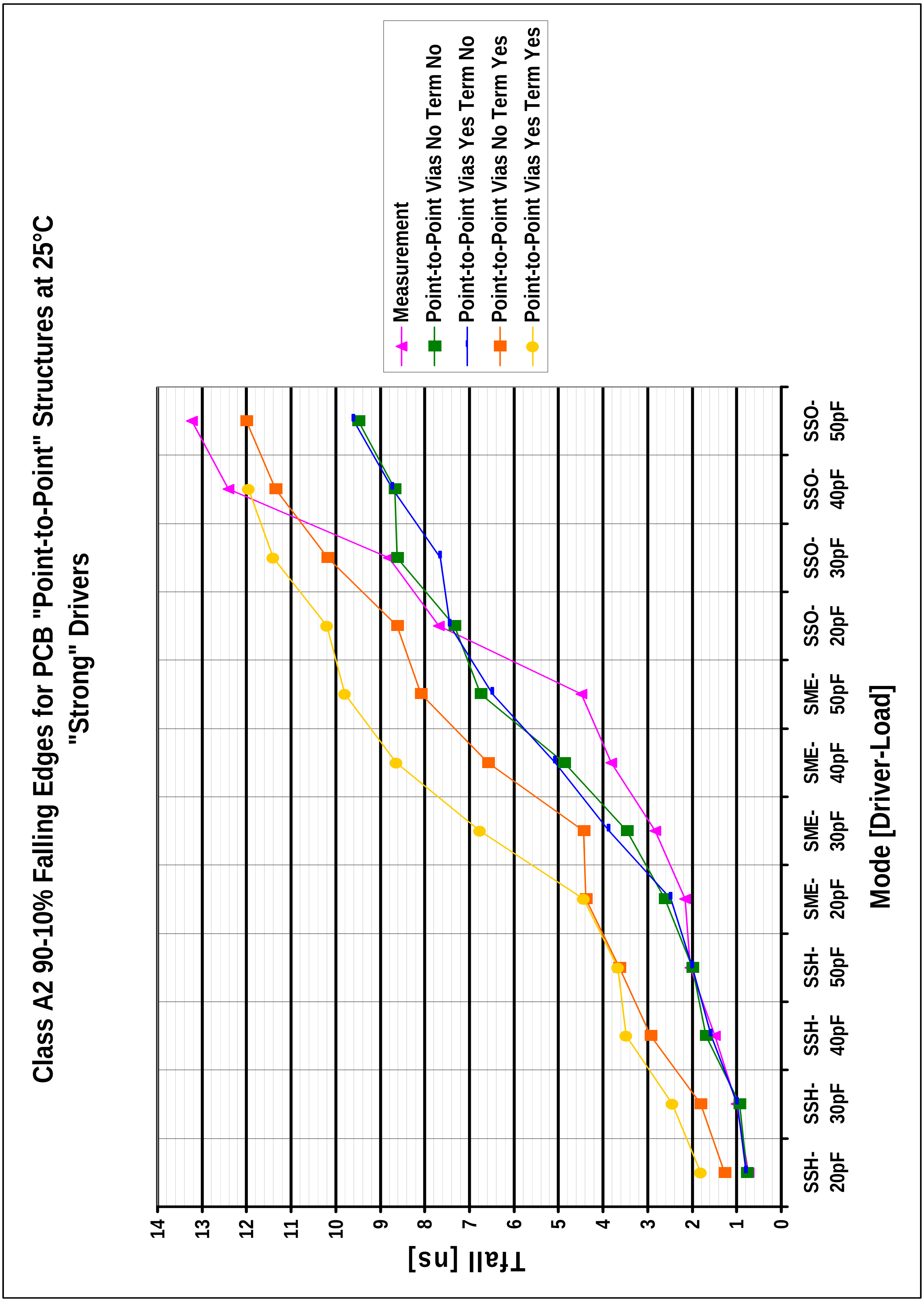


Figure 87: Zoomed fall times Class A2- Point-to-Point layout for strong driver settings at 25°C

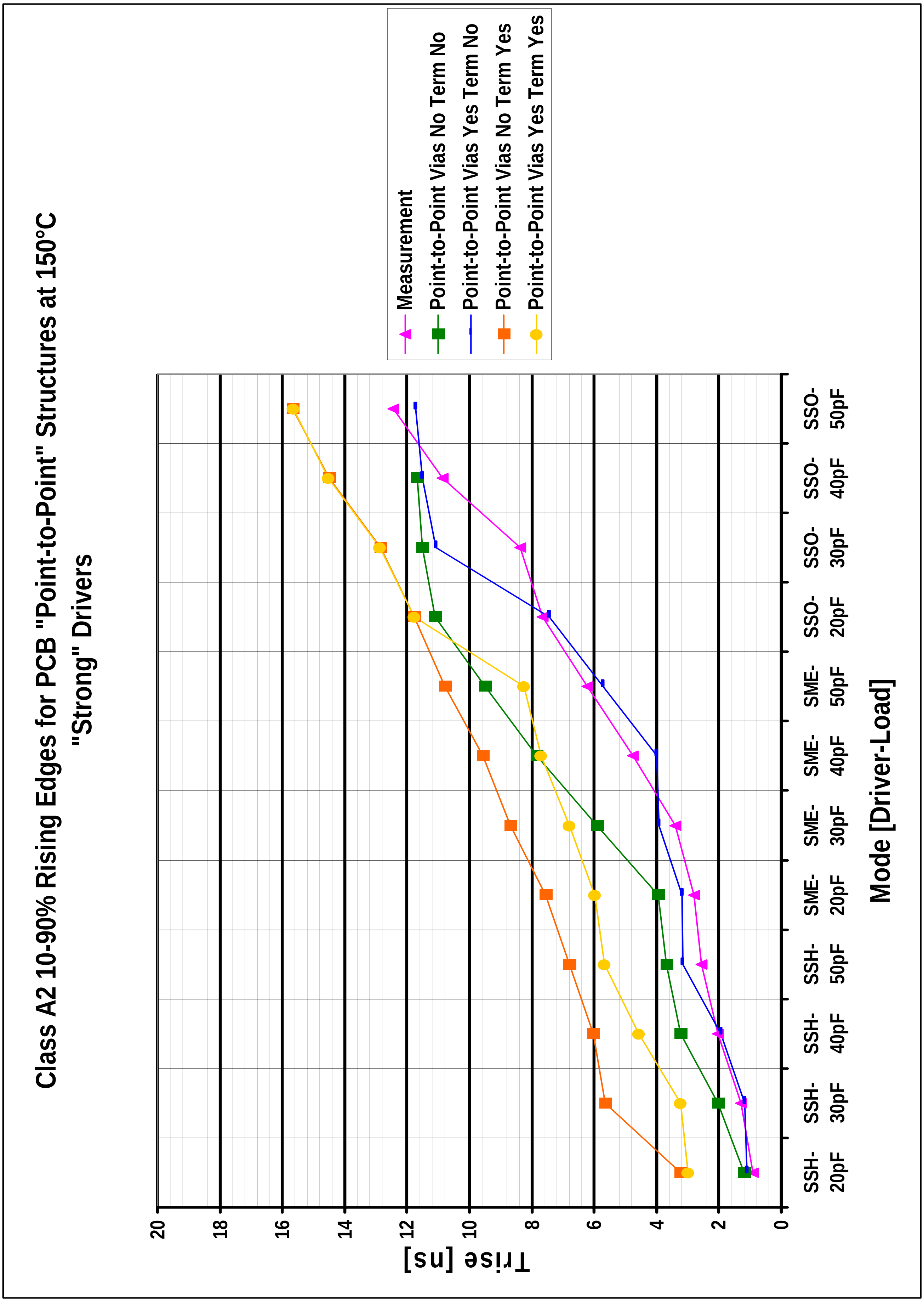


Figure 88: Zoomed rise times Class A2- P2P layout for strong driver settings at 150°C

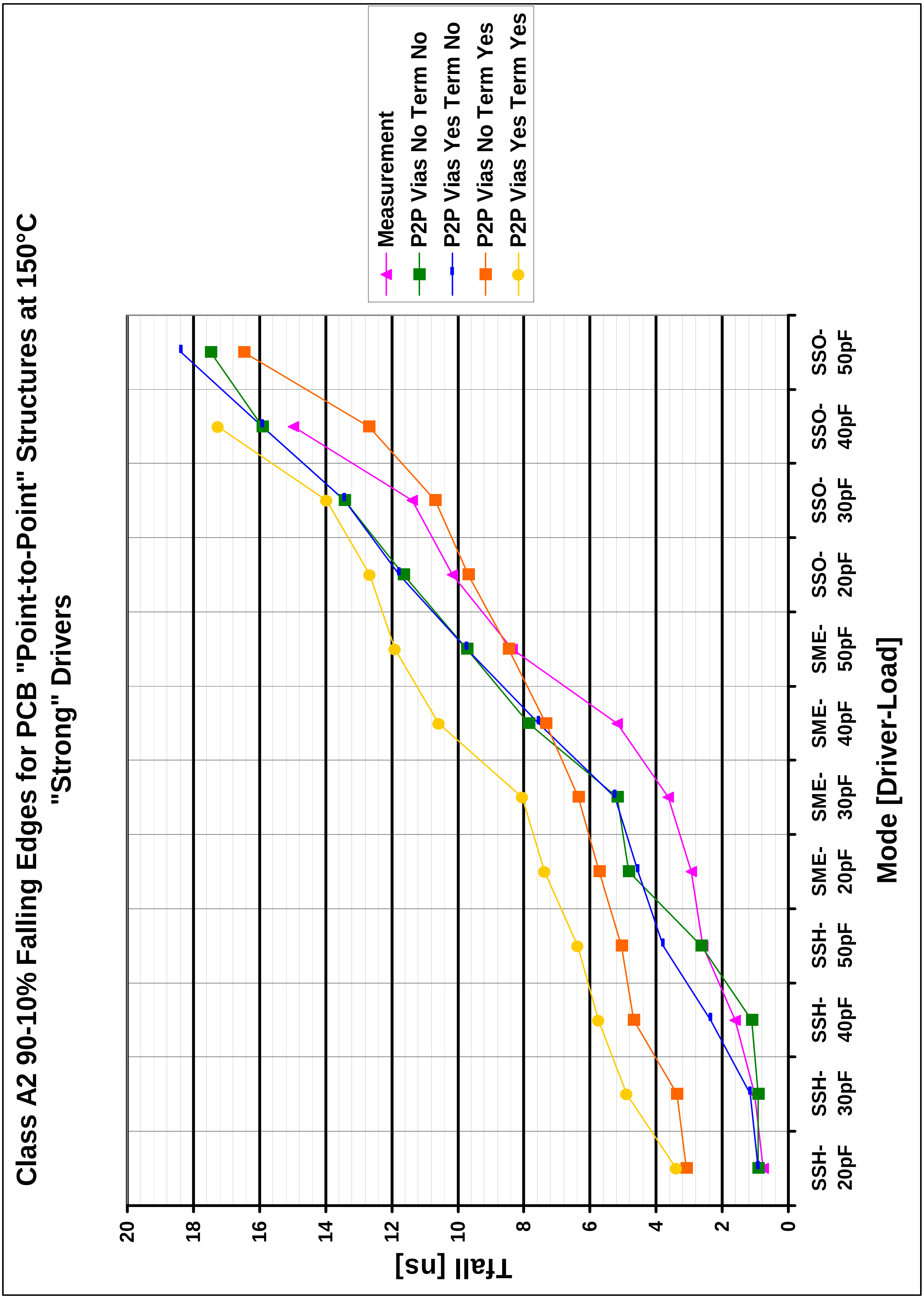


Figure 89: Zoomed fall times Class A2- P2P layout for strong driver settings at 150°C

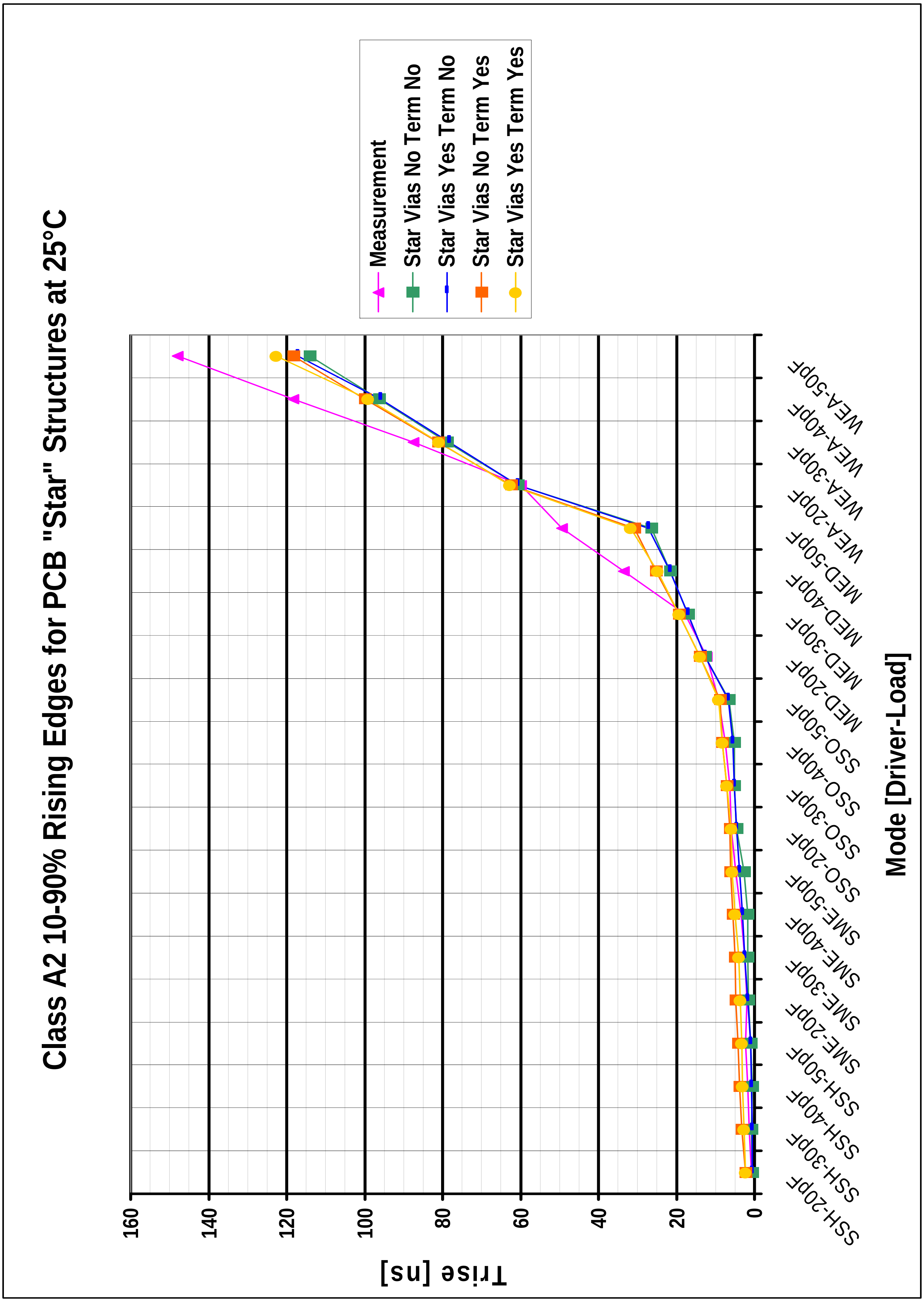


Figure 90: Class A2 rise times for "Star" layout at 25°C

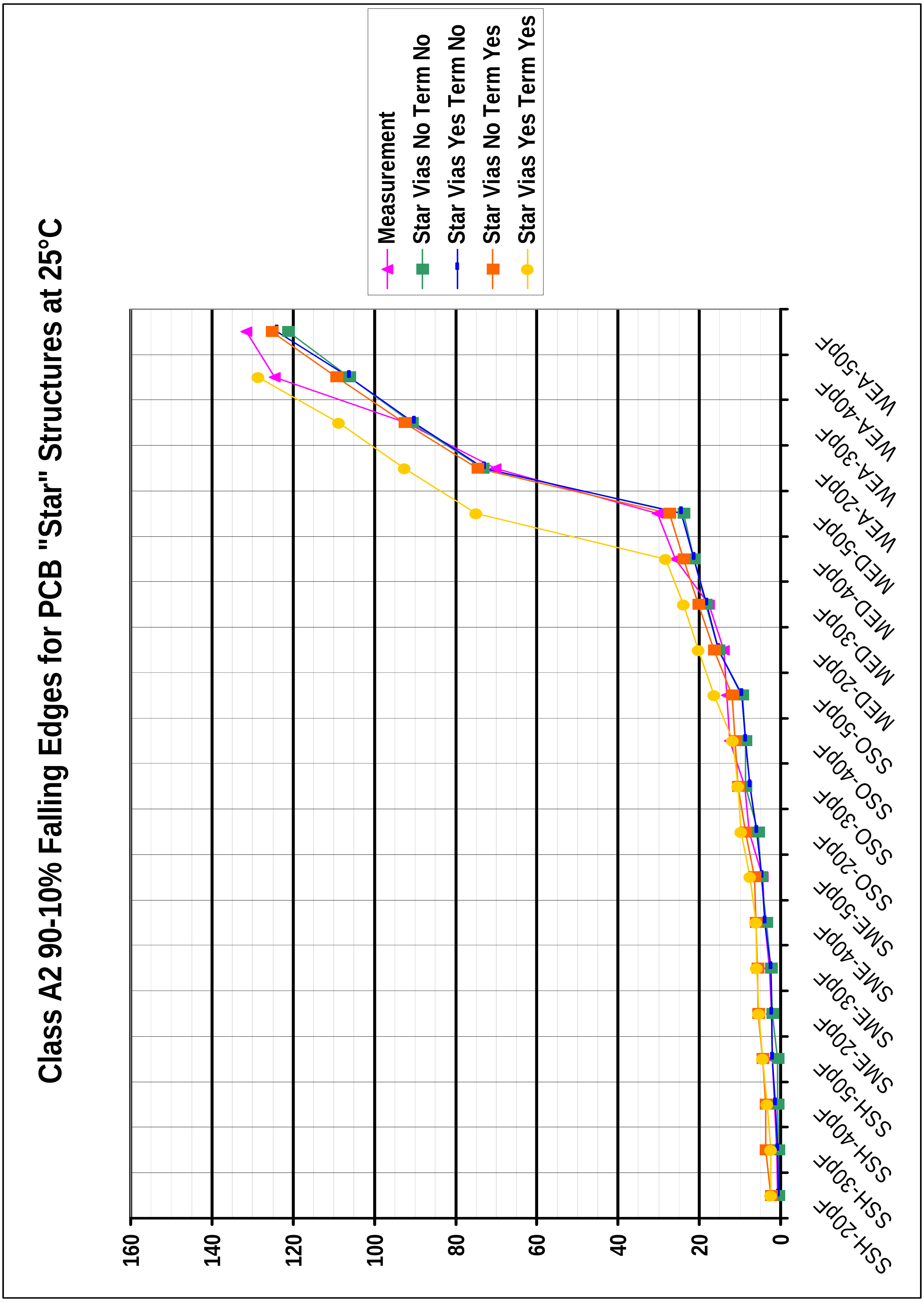


Figure 91: Class A2 fall times for “Star” layout at 25°C

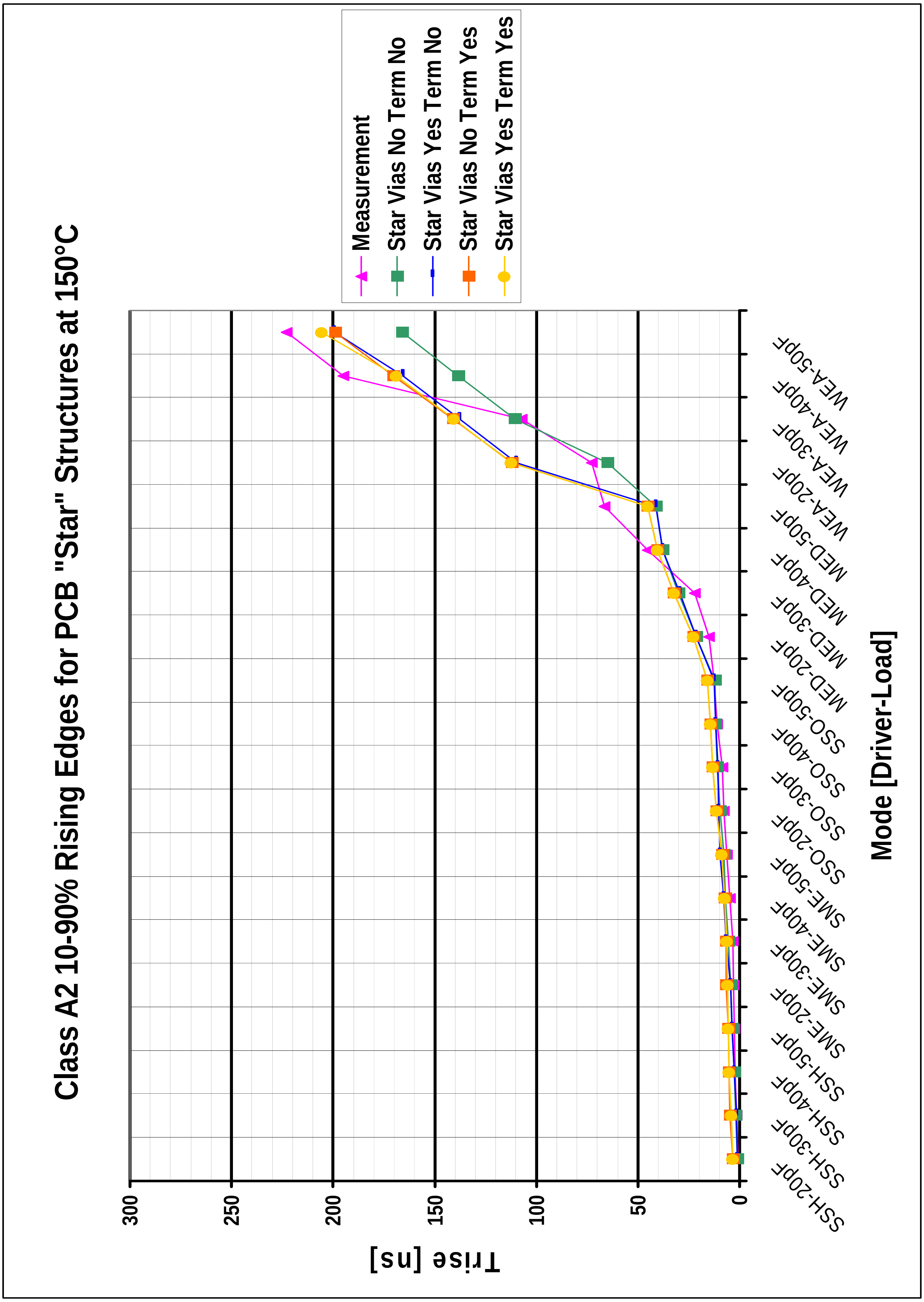


Figure 92: Class A2 rise times for “Star” layout at 150°C

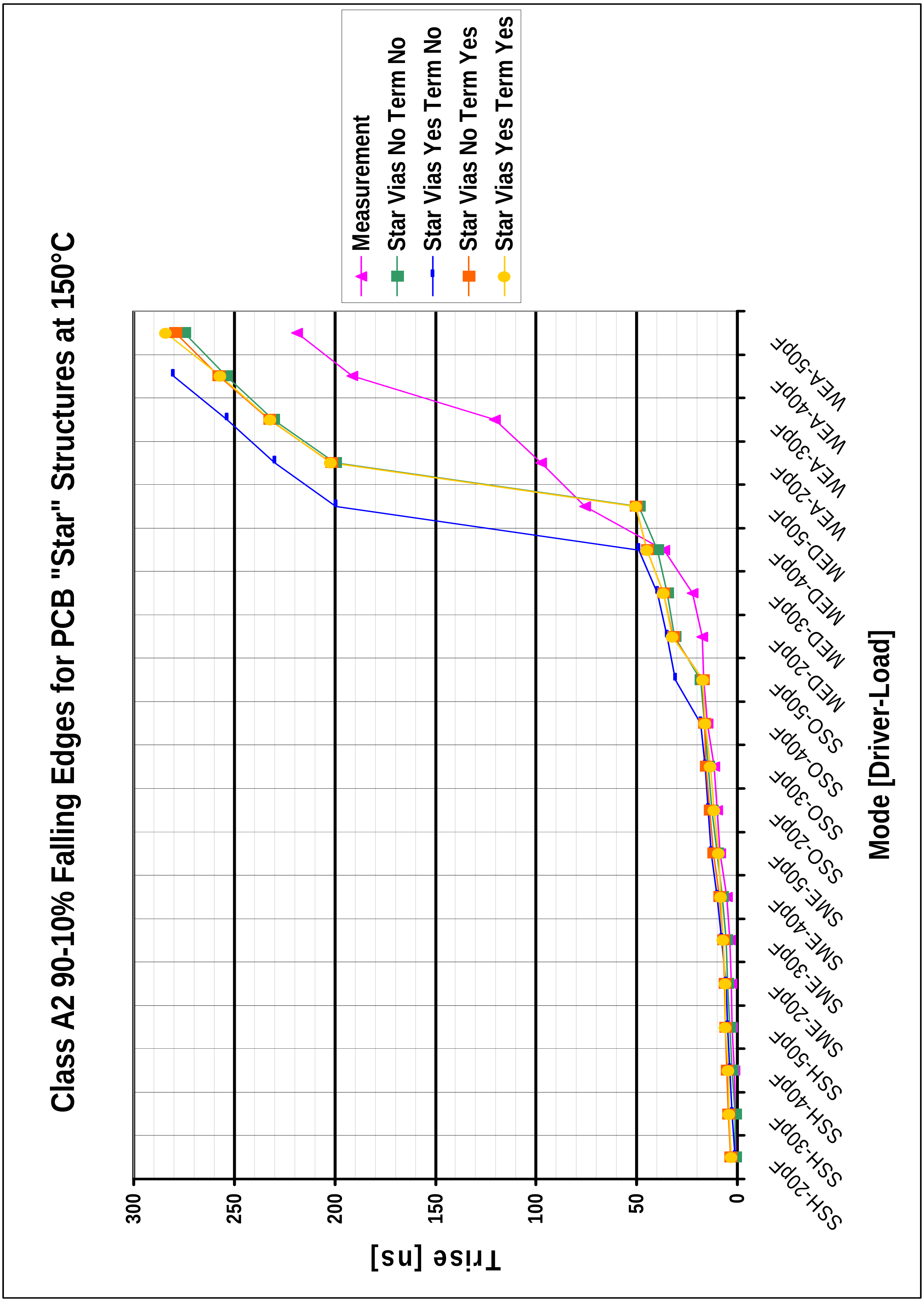


Figure 93: Class A2 fall times for "Star" layout at 150°C

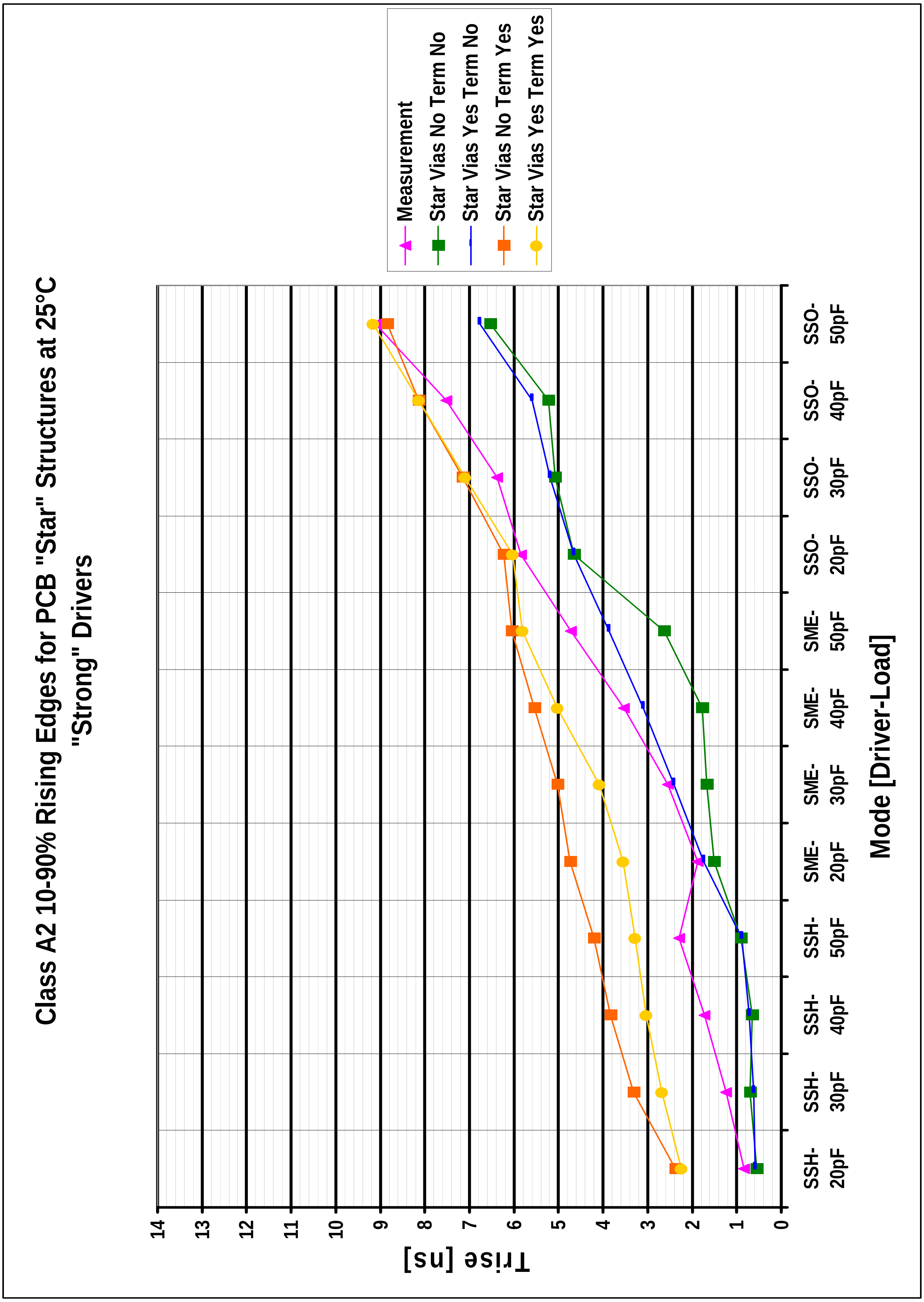


Figure 94: Zoomed rise times Class A2- Star layout for strong driver settings at 25°C

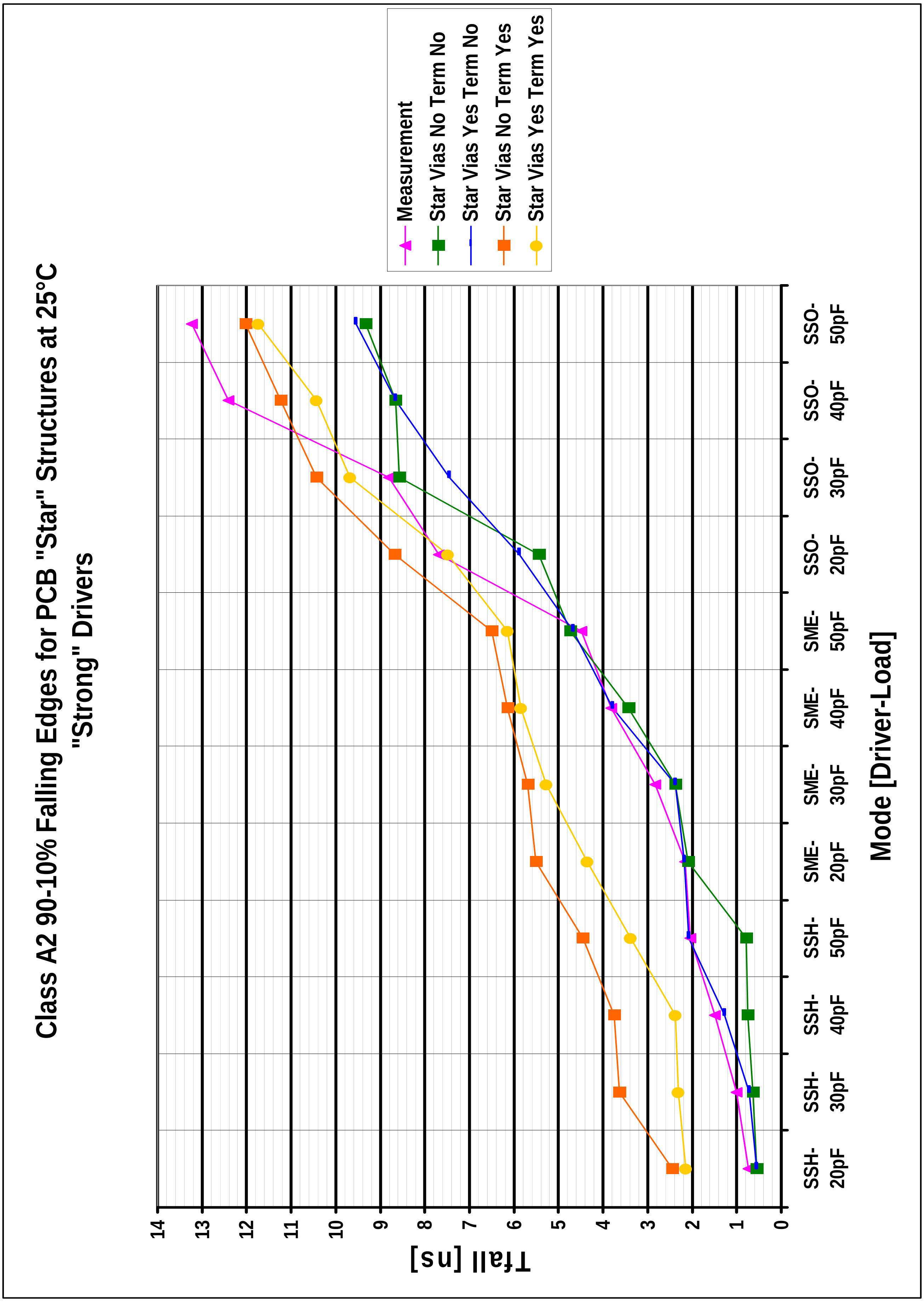


Figure 95: Zoomed fall times Class A2- Star layout for strong driver settings at 25°C

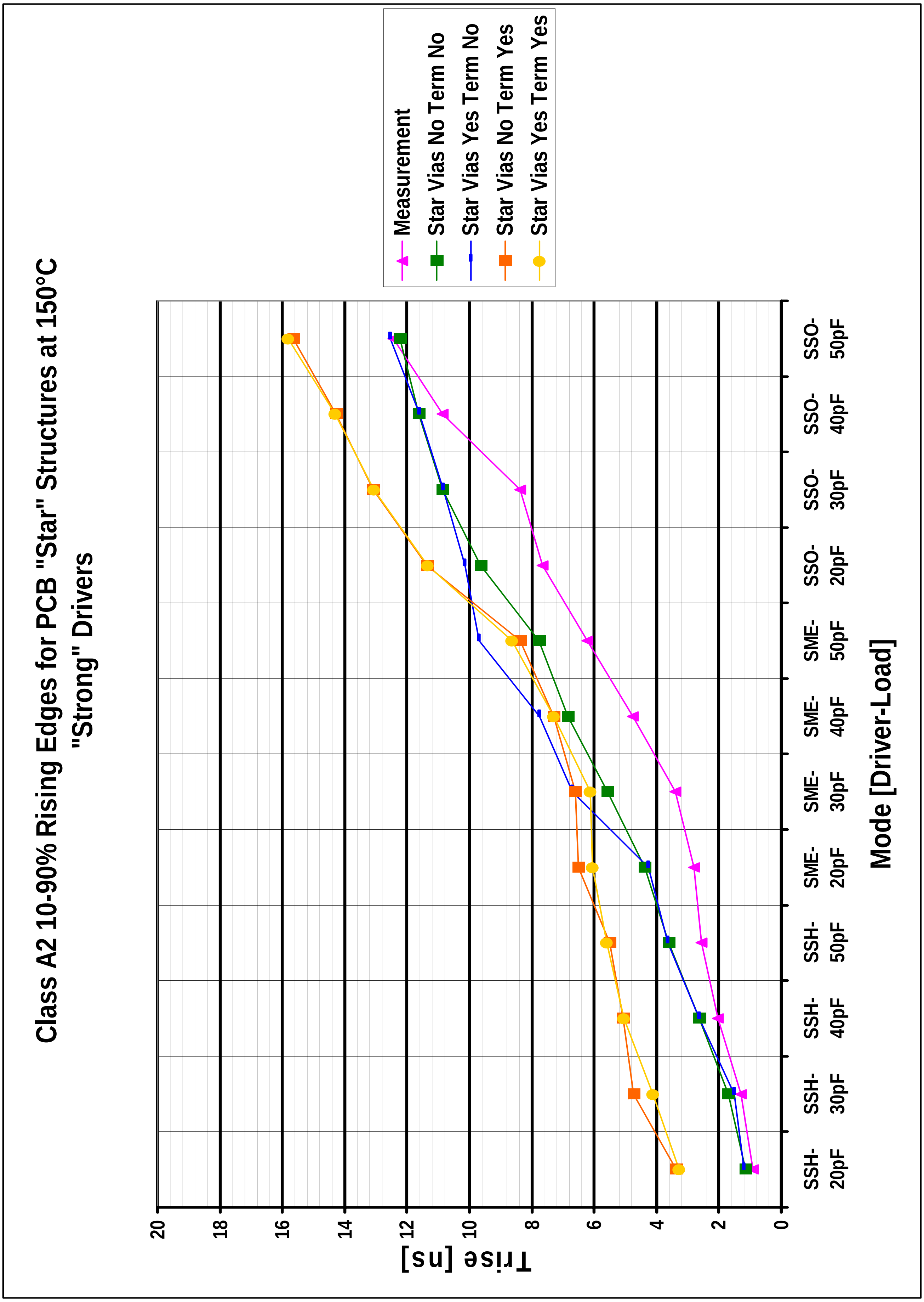


Figure 96: Zoomed rise times Class A2- Star layout for strong driver settings at 150°C

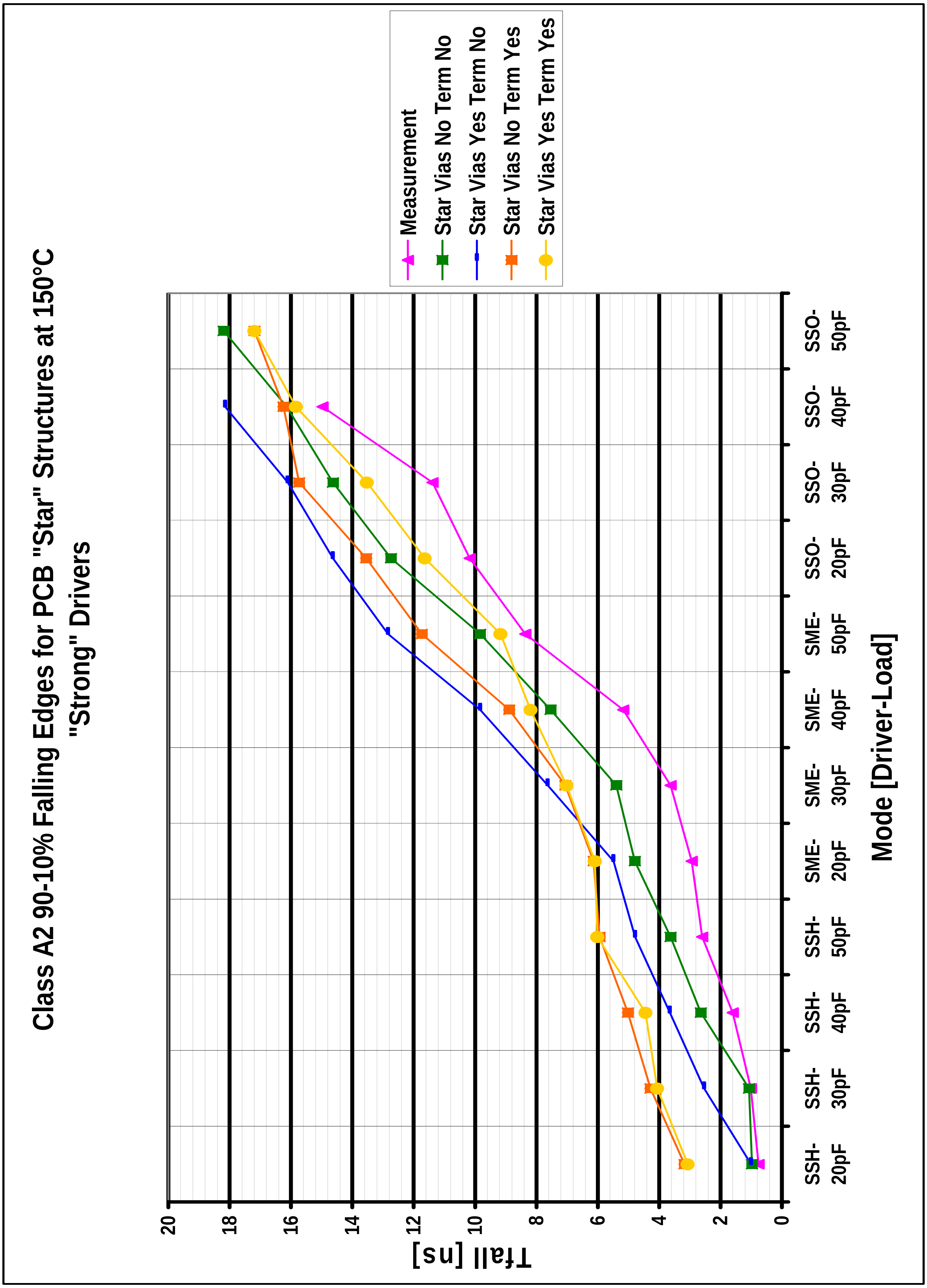


Figure 97: Zoomed fall times Class A2- Star layout for strong driver settings at 150°C

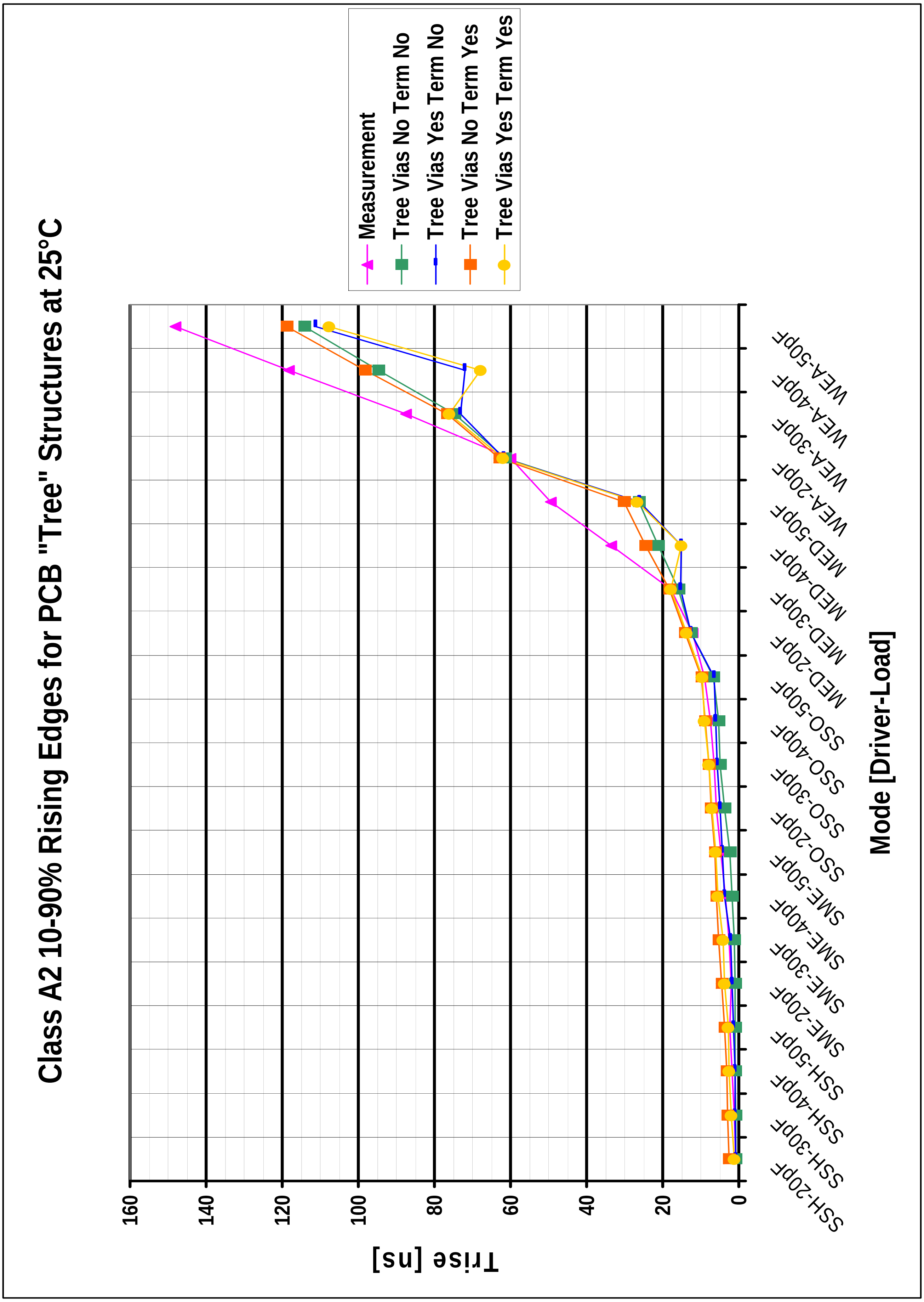


Figure 98: Class A2 rise times for “Tree” layout at 25°C

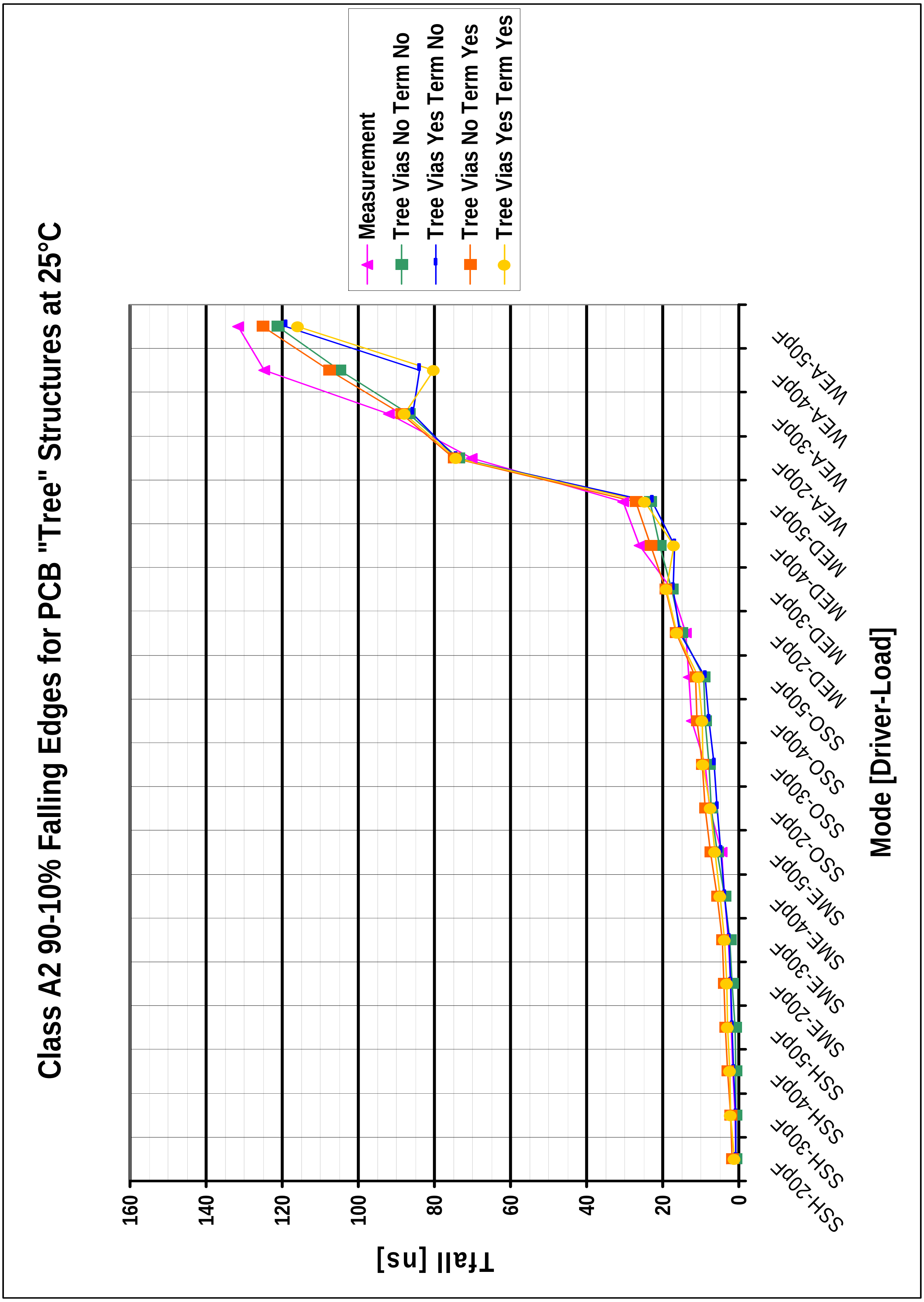


Figure 99: Class A2 fall times for “Tree” layout at 25°C

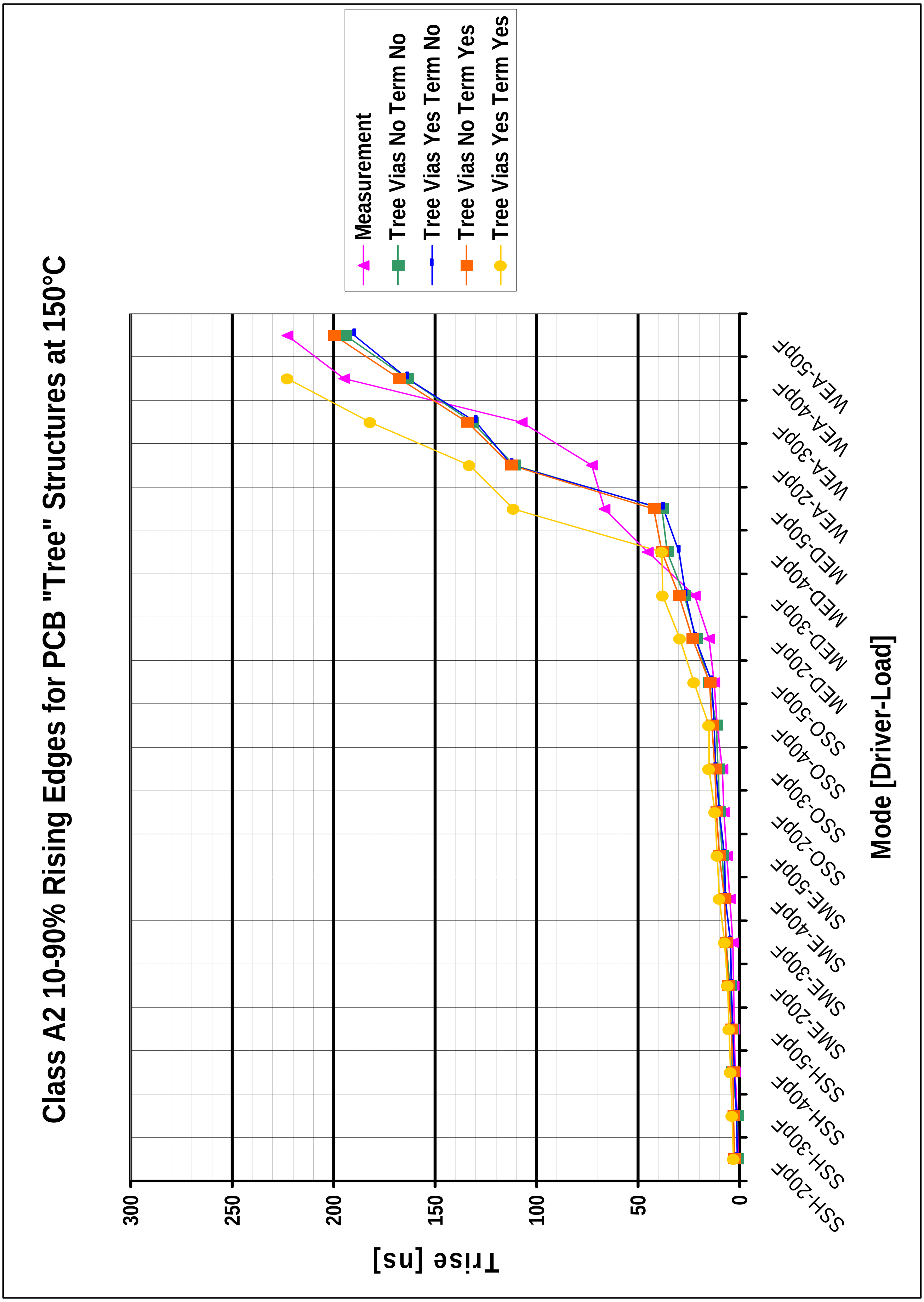


Figure 100: Class A2 rise times for “Tree” layout at 150°C

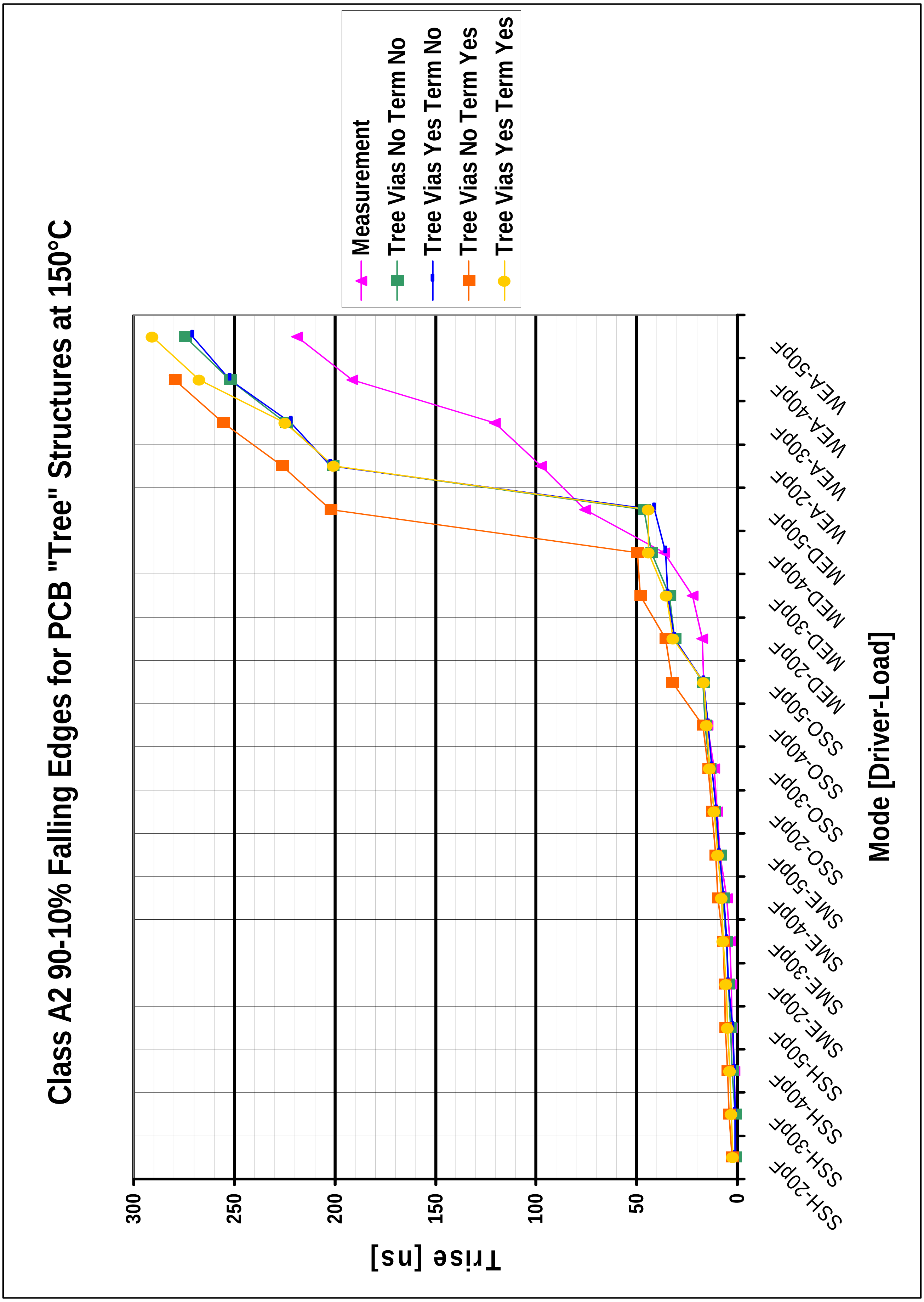


Figure 101: Class A2 fall times for "Tree" layout at 150°C

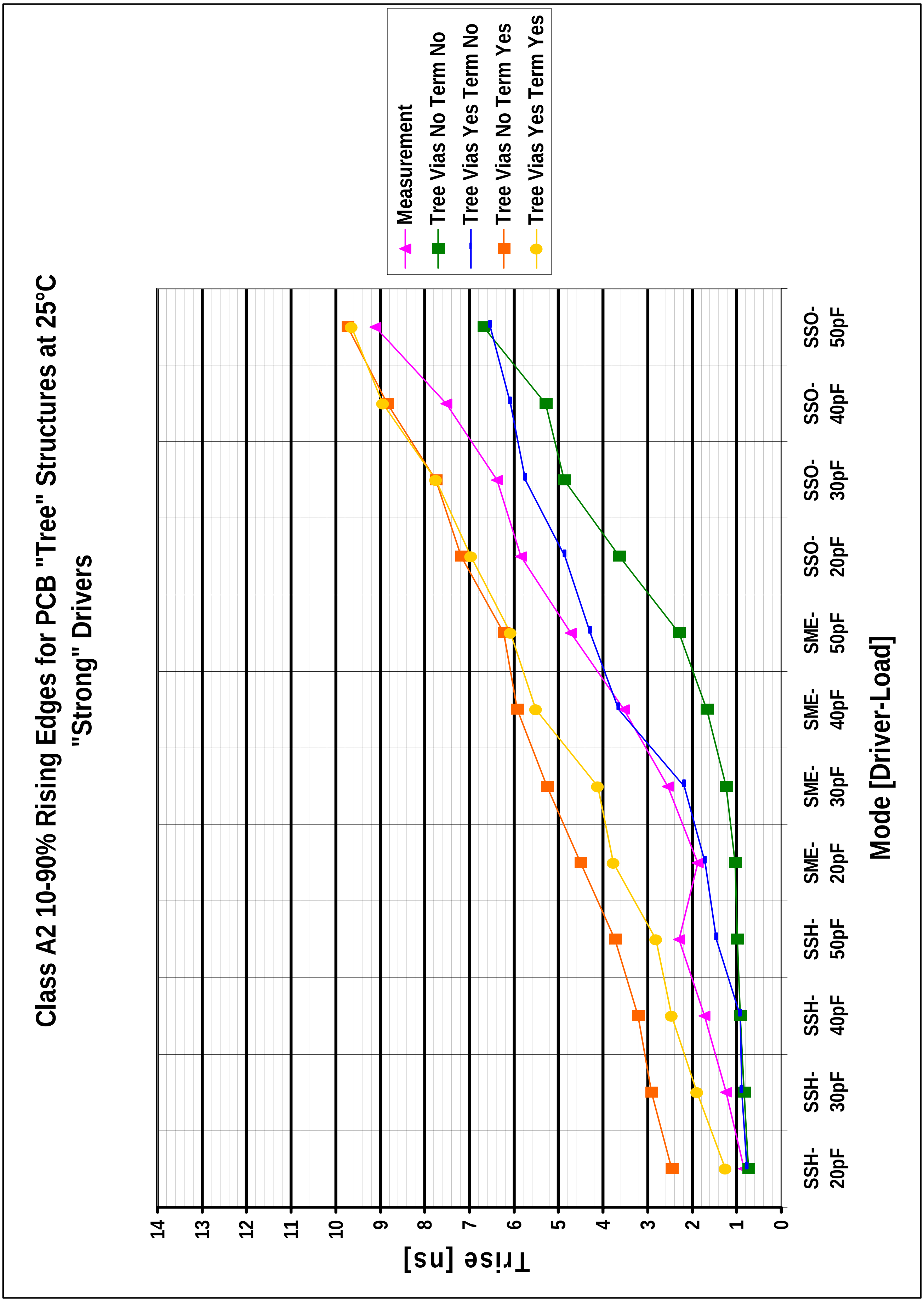


Figure 102: Zoomed rise times Class A2-Tree layout for Strong Driver Settings at 25°C

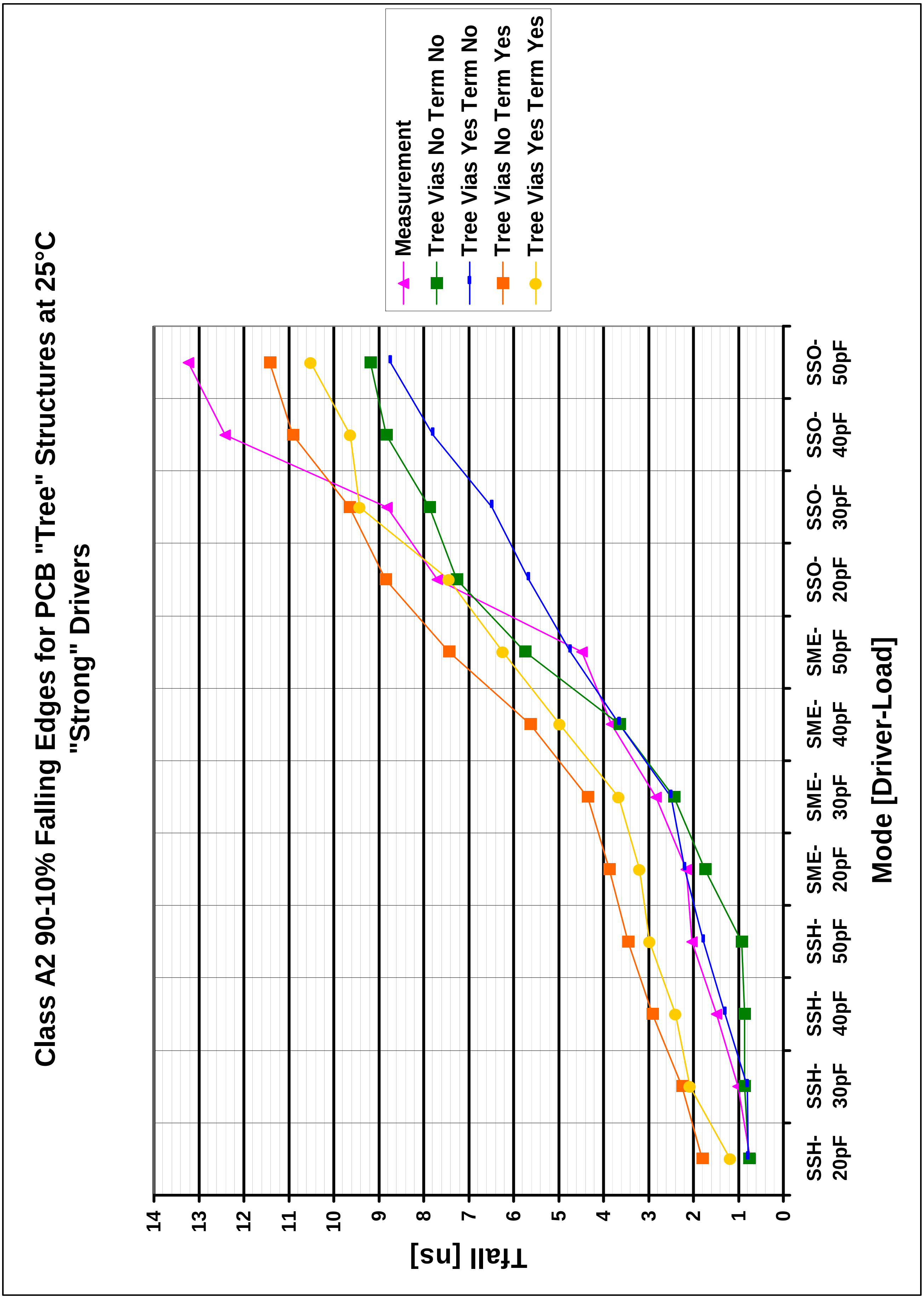


Figure 103: Zoomed fall times Class A2- Tree layout for strong driver settings at 25°C

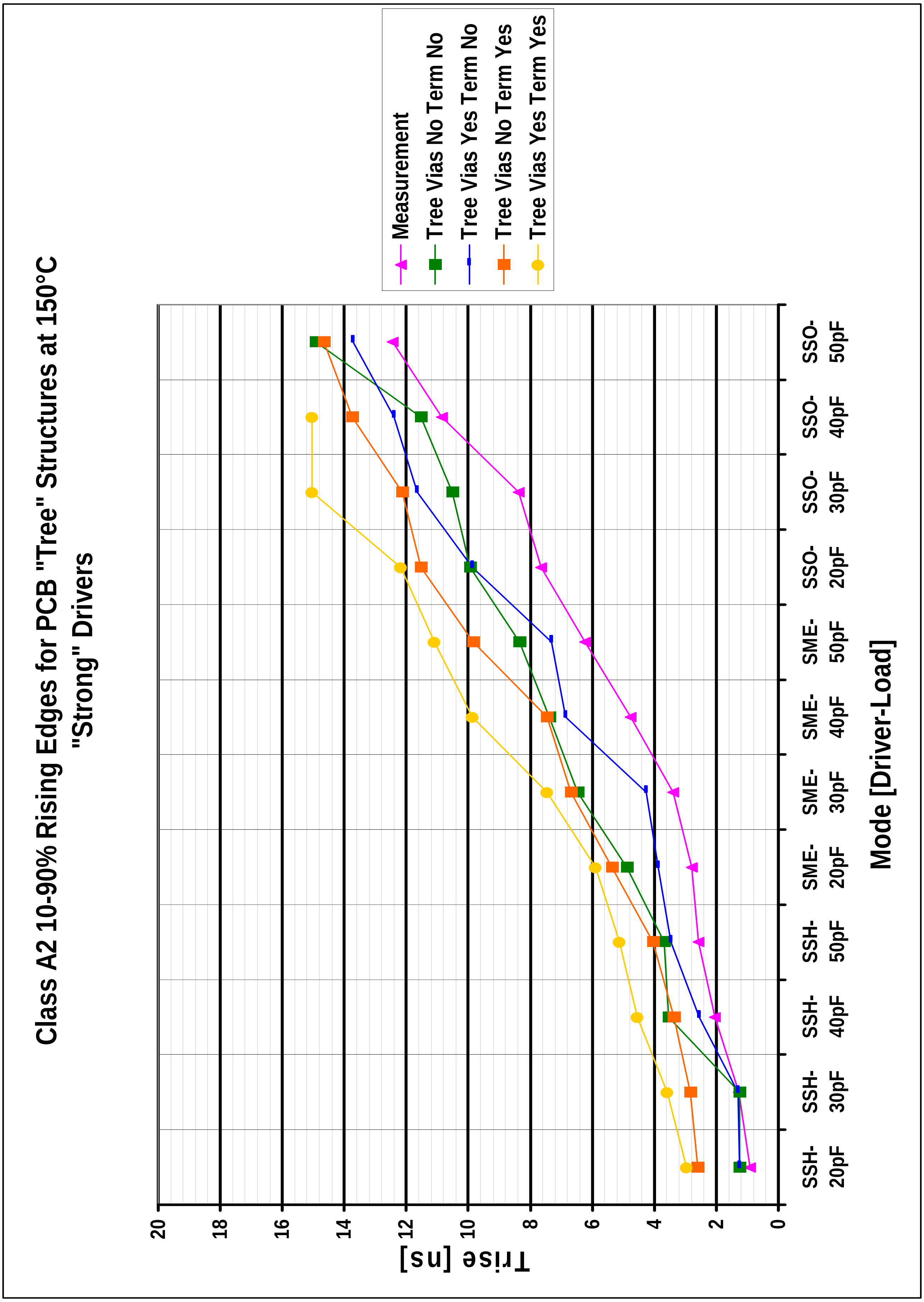


Figure 104: Zoomed rise times Class A2 Tree layout for strong driver settings at 150°C

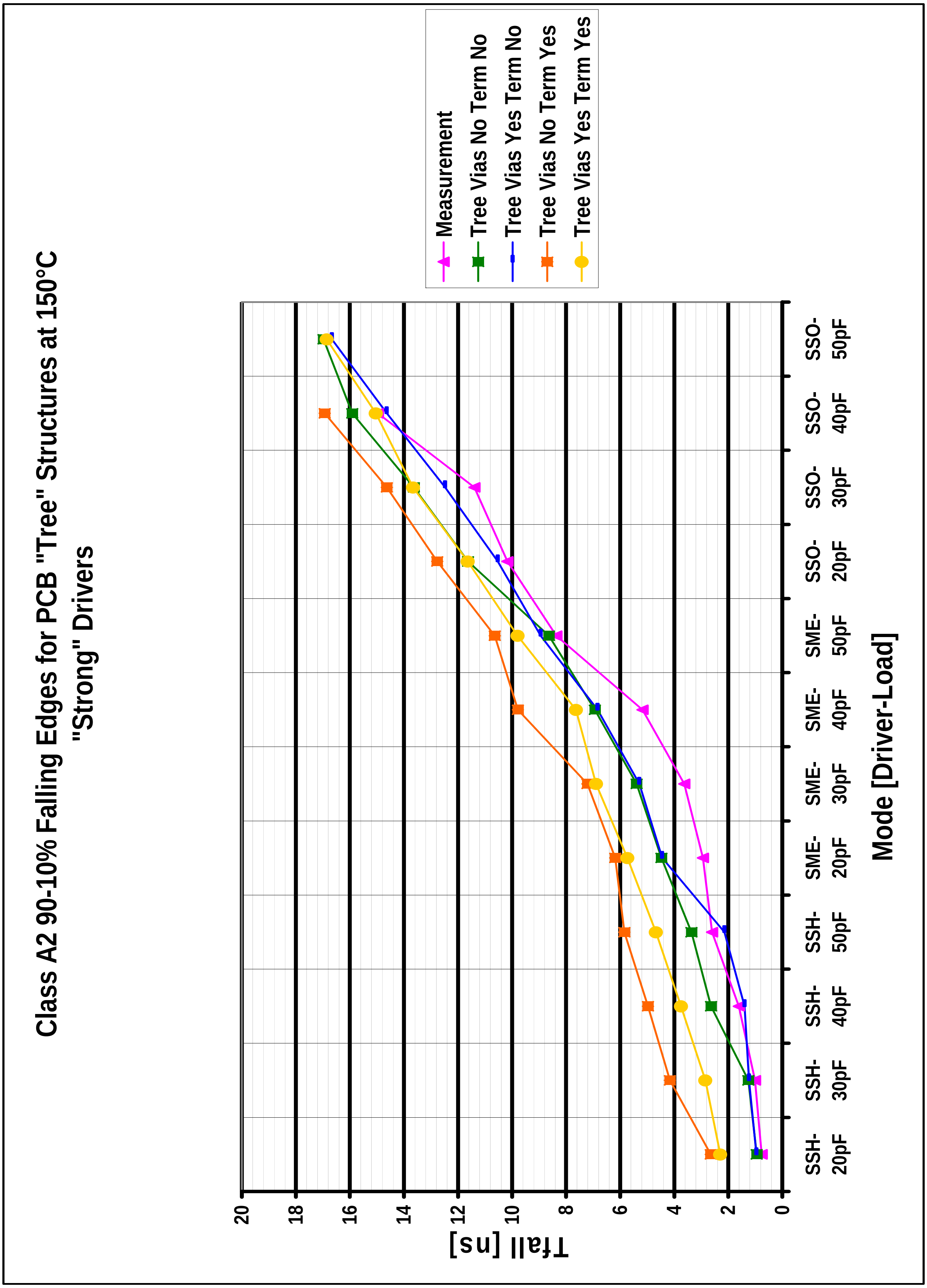


Figure 105: Zoomed fall times Class A2 Tree layout for strong driver settings at 150°C

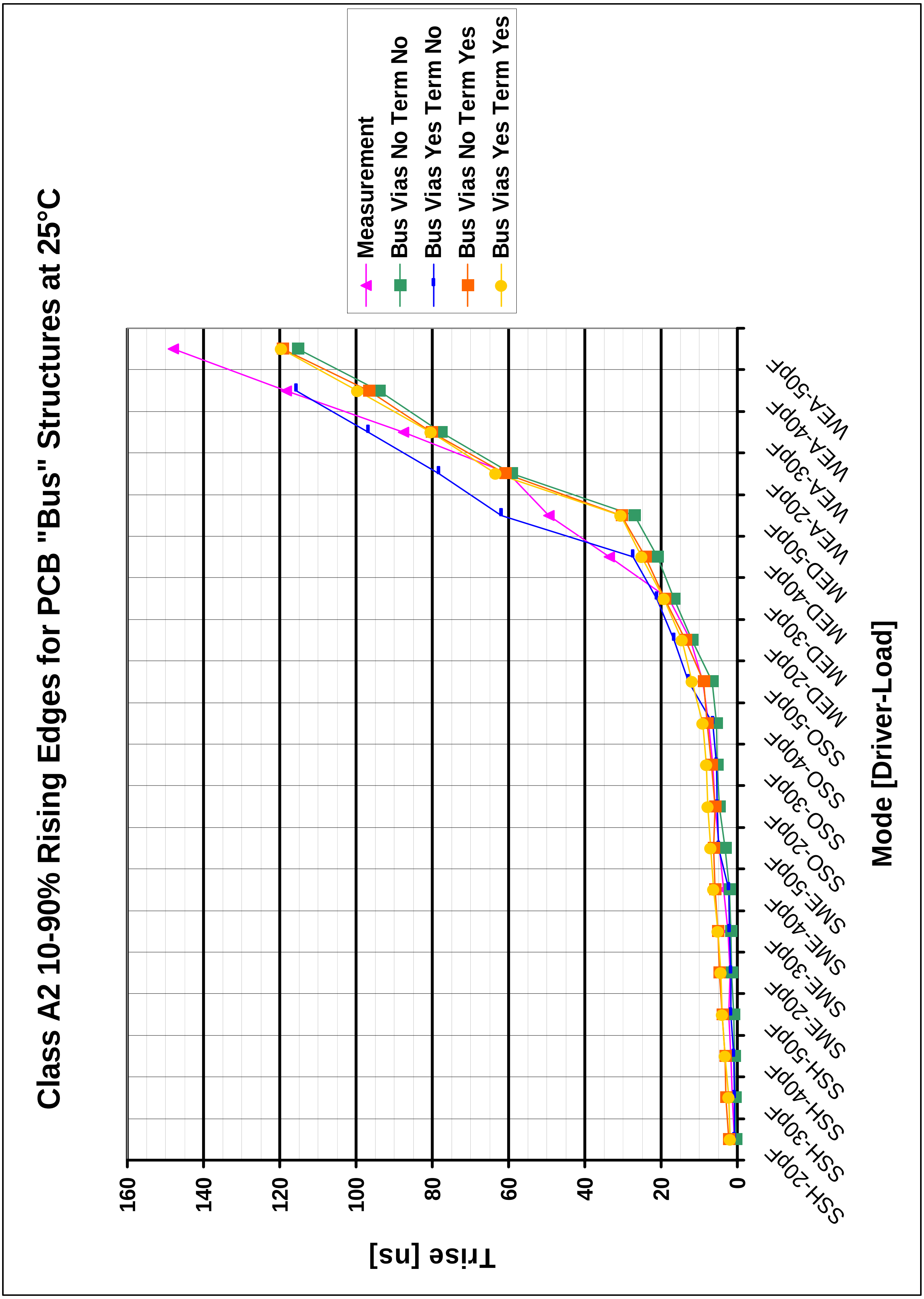


Figure 106: Class A2 rise times for "Bus" layout at 25°C

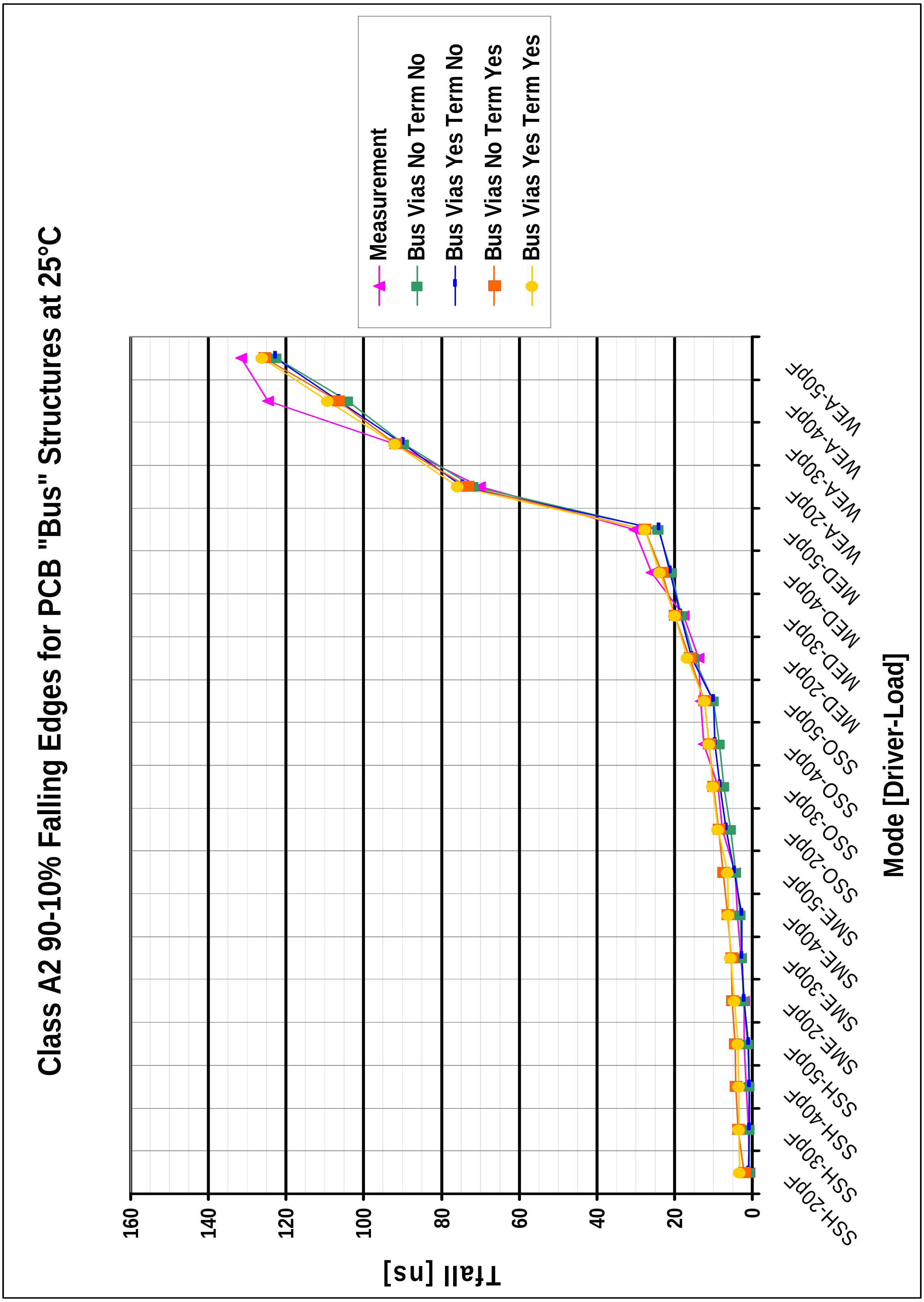


Figure 107: Class A2 fall times for “Bus” layout at 25°C

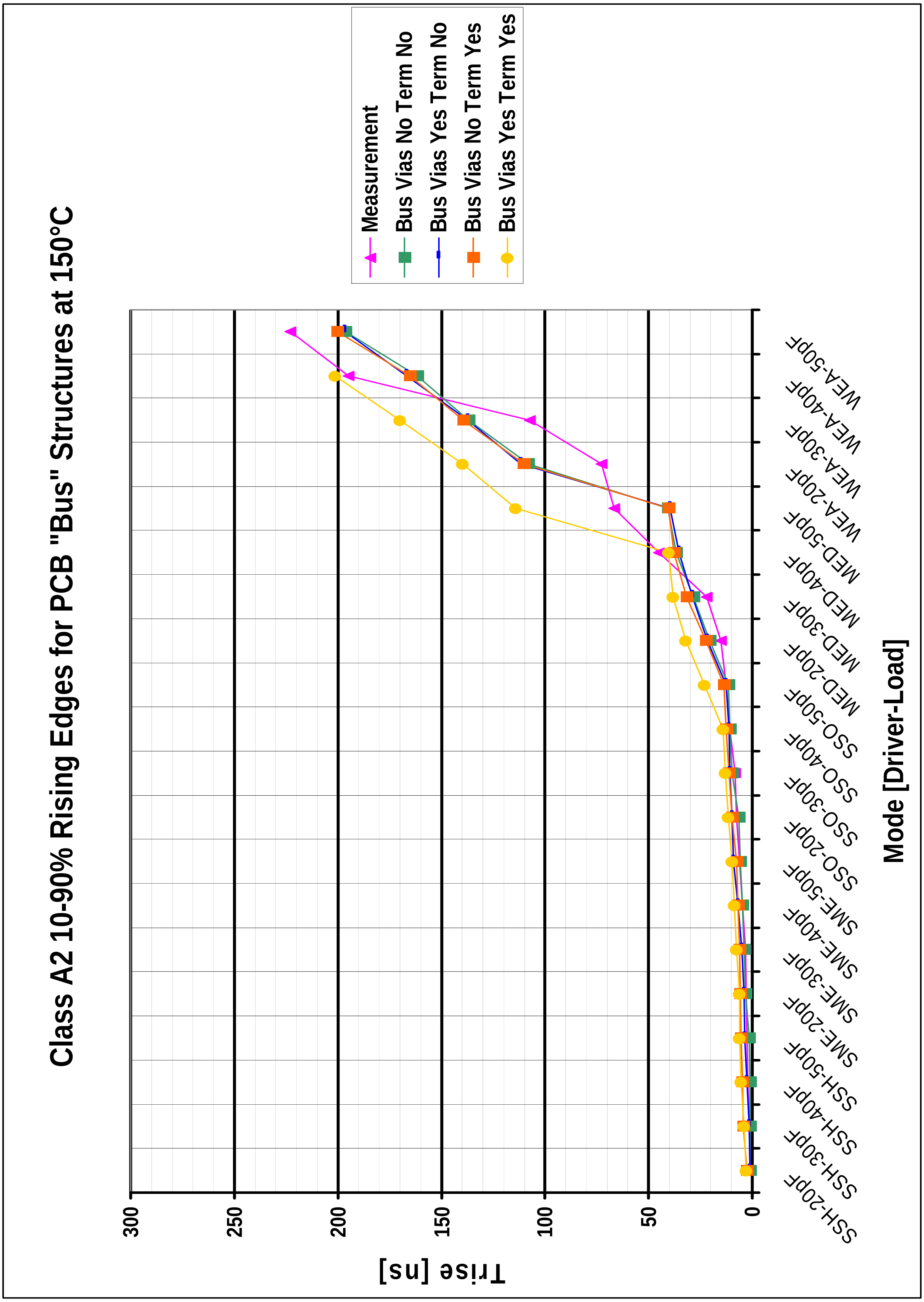


Figure 108: Class A2 rise times for “Bus” layout at 150°C

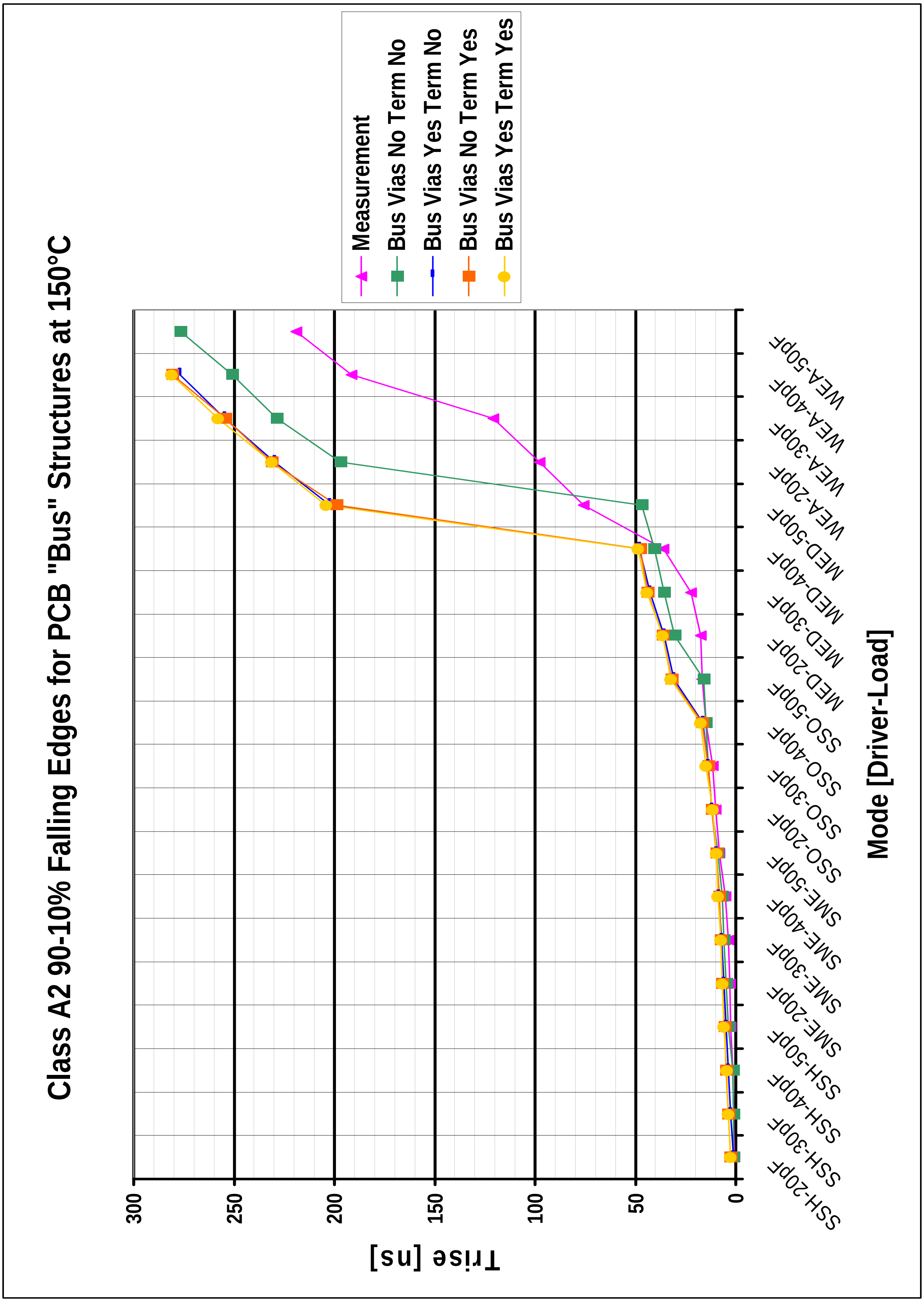


Figure 109: Class A2 fall times for "Bus" layout at 150°C

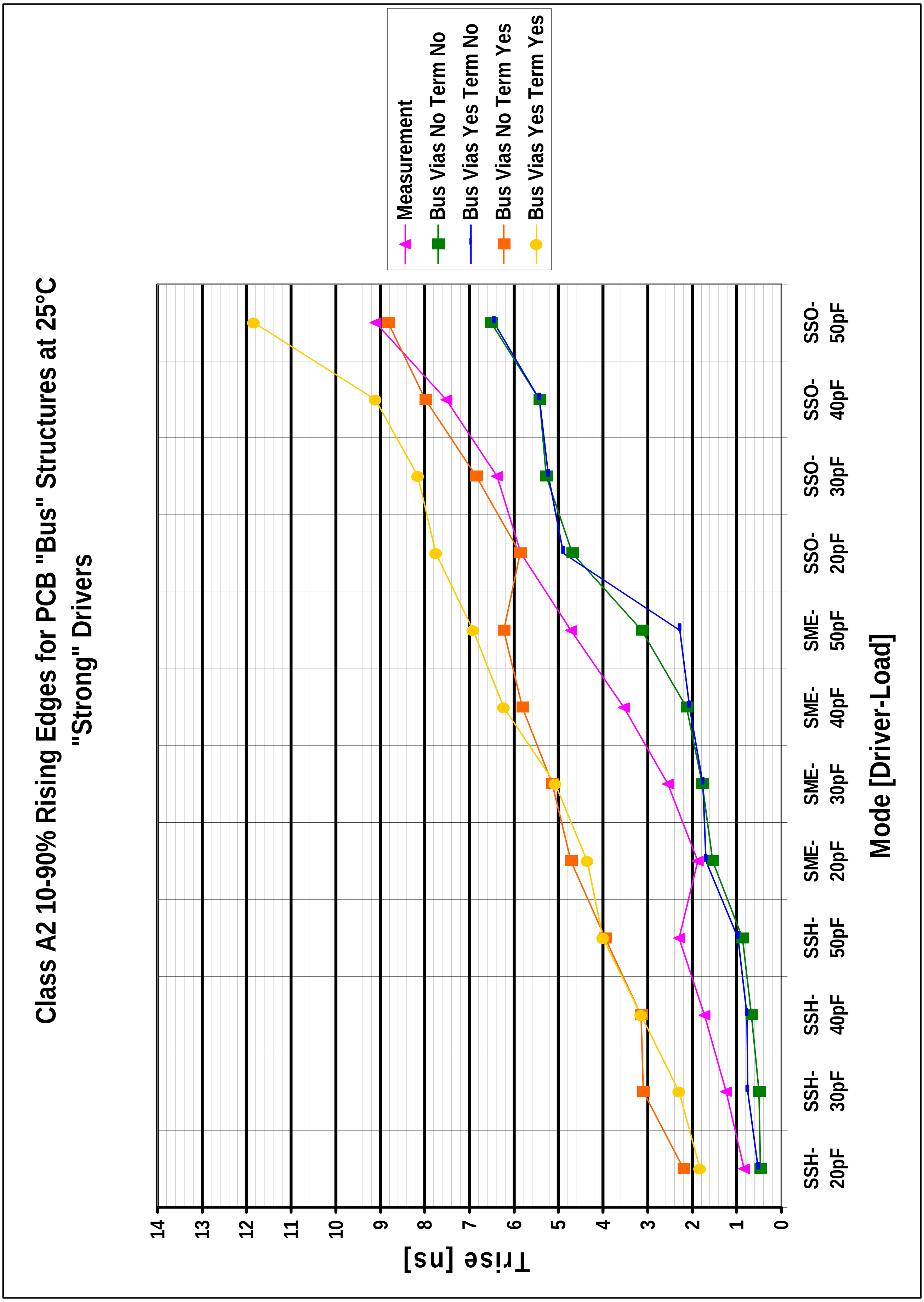


Figure 110: Zoomed rise times Class A2-Bus layout for strong driver settings at 25°C

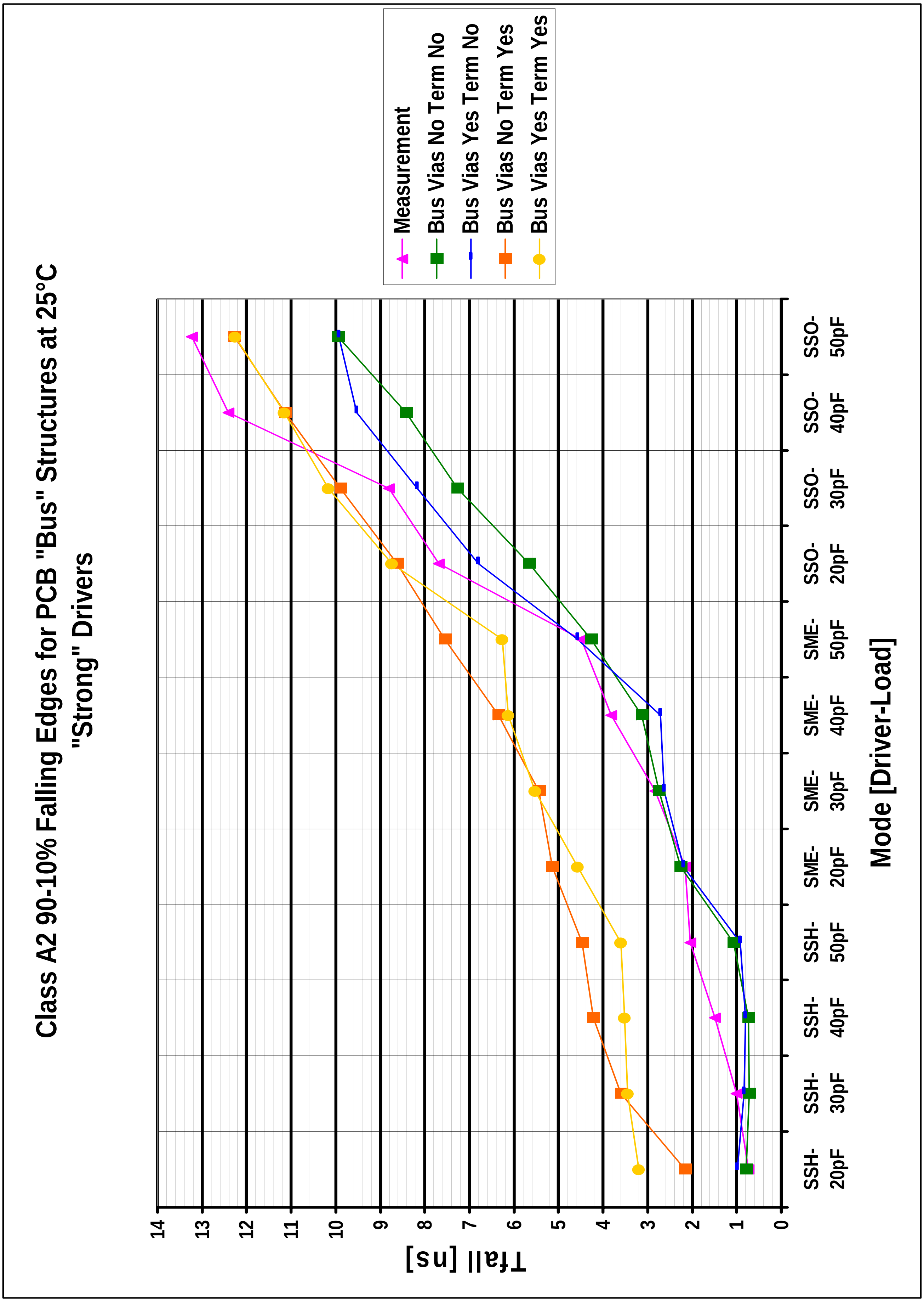


Figure 111: Zoomed fall times Class A2-Bus layout for strong driver settings at 25°C

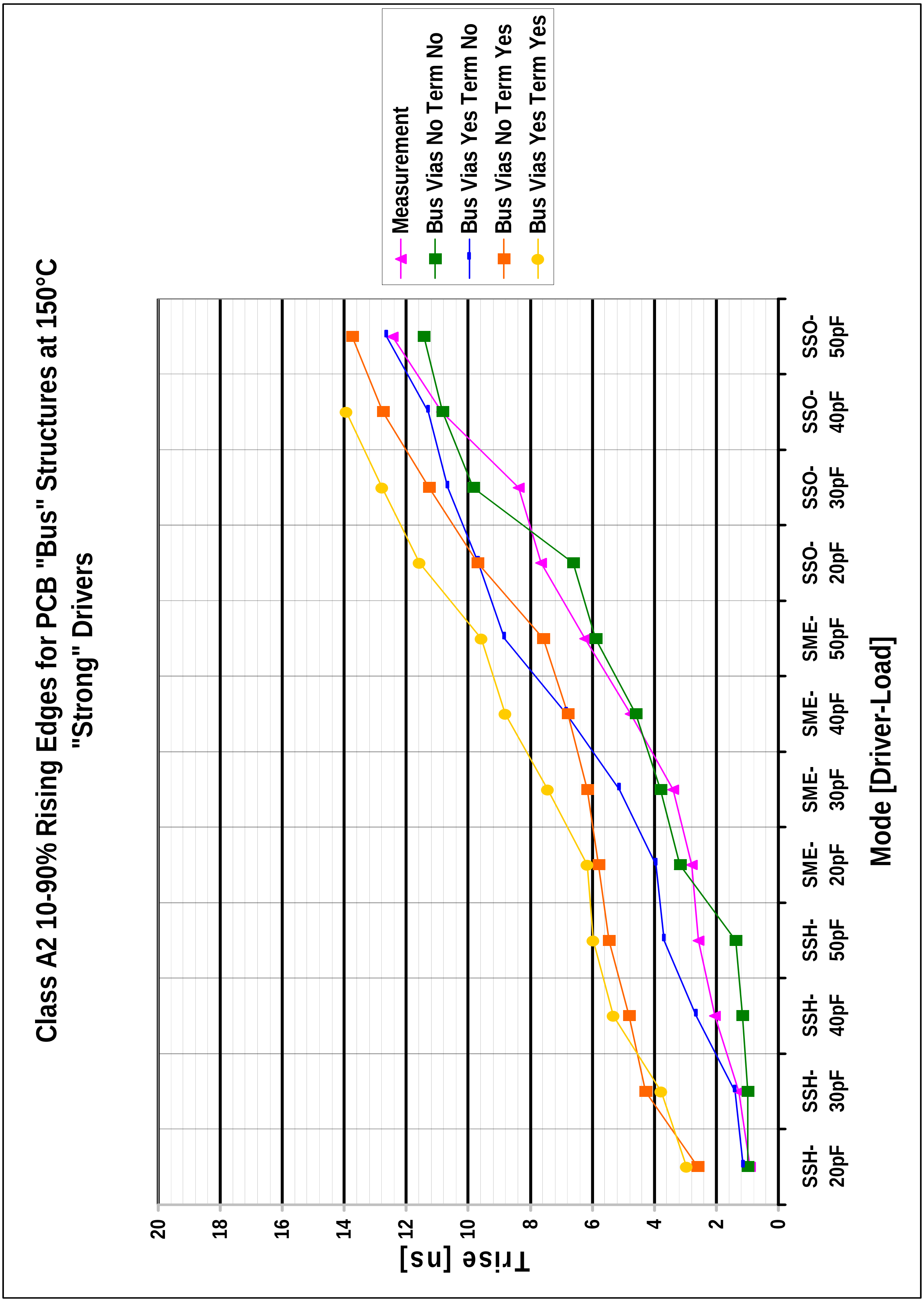


Figure 112: Zoomed rise times Class A2-Bus layout for strong driver settings at 150°C

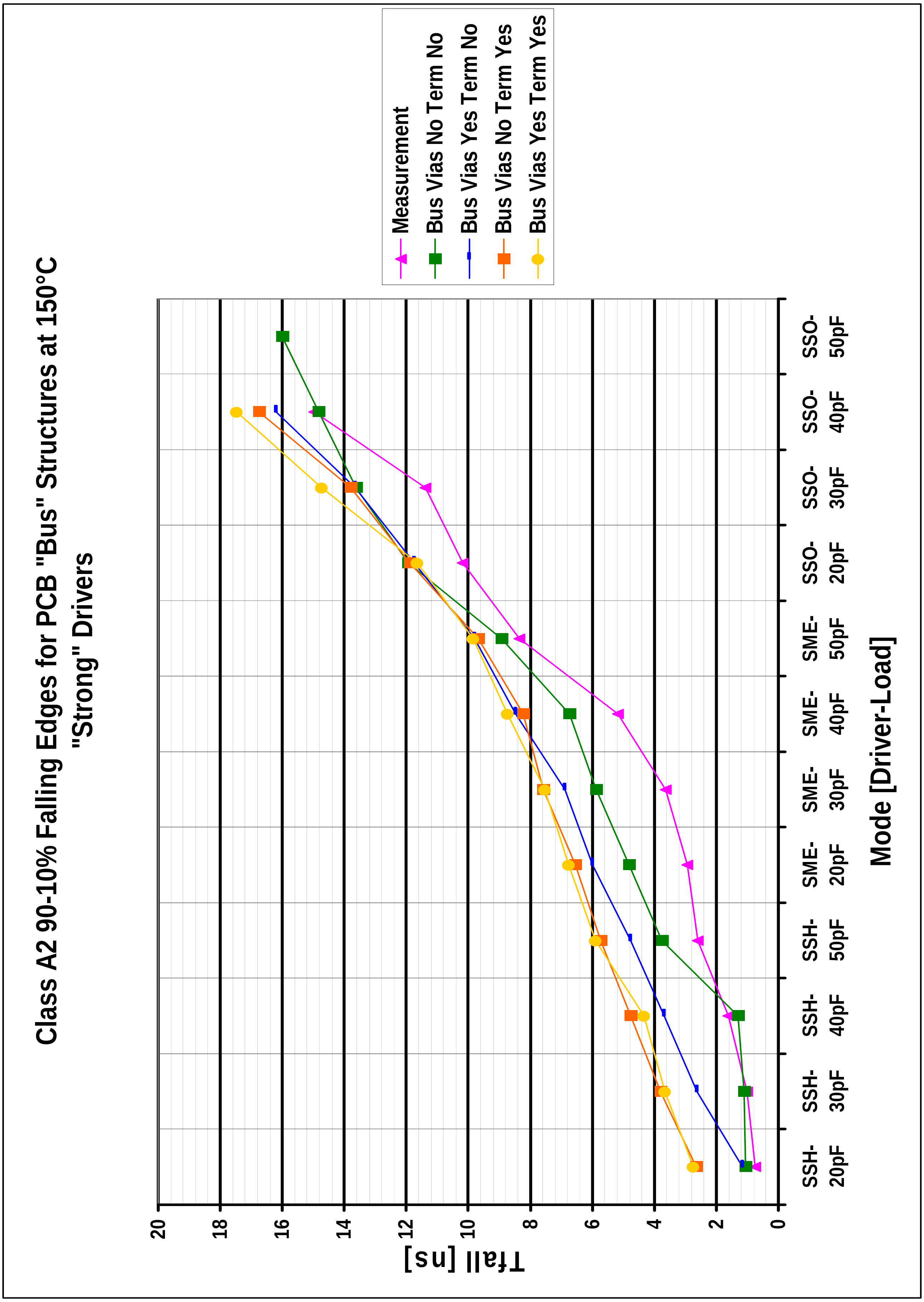


Figure 113: Zoomed fall times Class A2-Bus layout for strong driver settings at 150°C

4.1.2.2 Influence of layout structures on rise/fall times

Fig. 114-121 indicate that the different structures lead to quite similar timing results. Any considerations of layout structures are only suggested when assessing time-critical signals using strong driver modes, see figures 116-117 and 120-121.

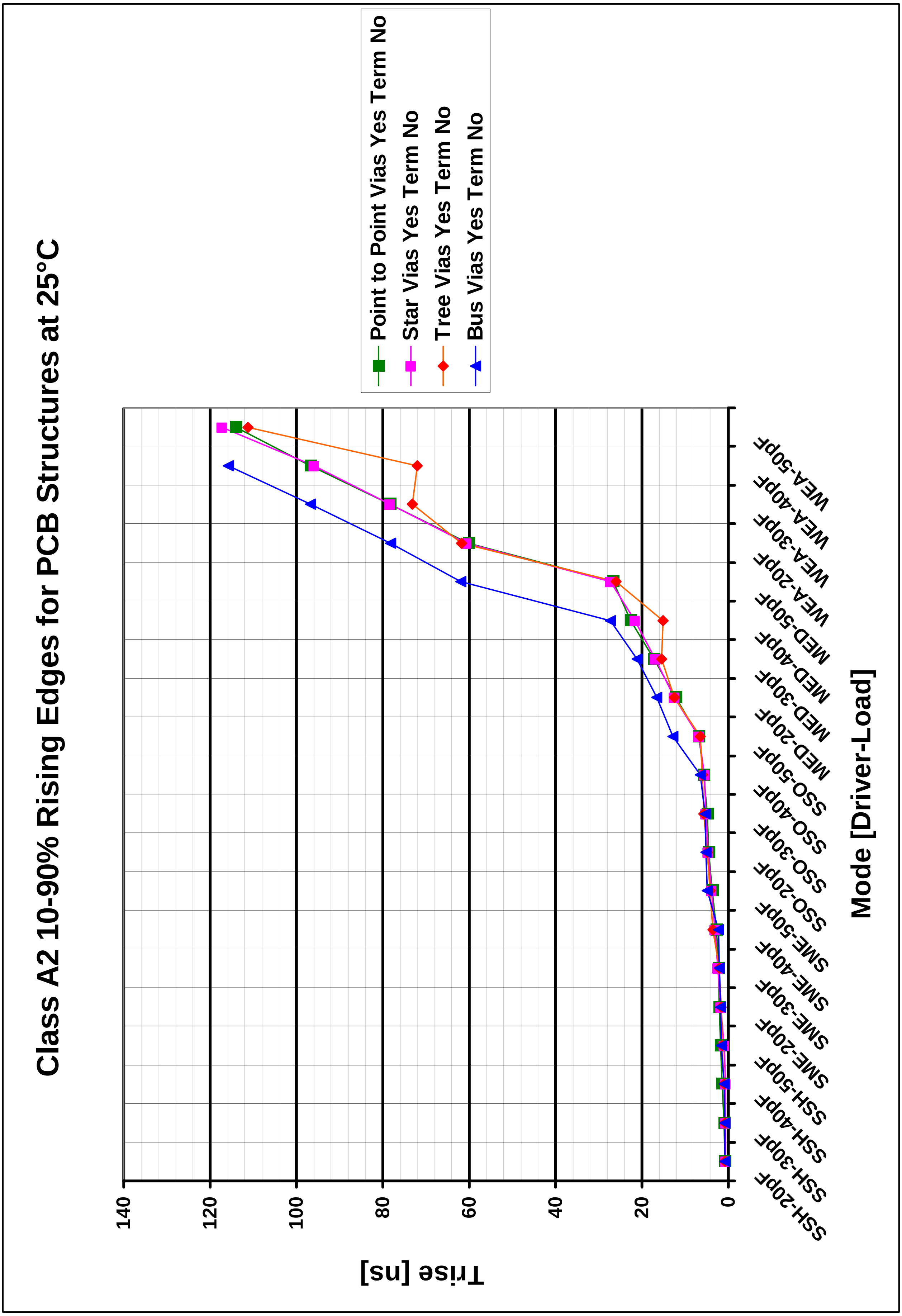


Figure 114: Class A2 rise times for all PCB structures at 25°C

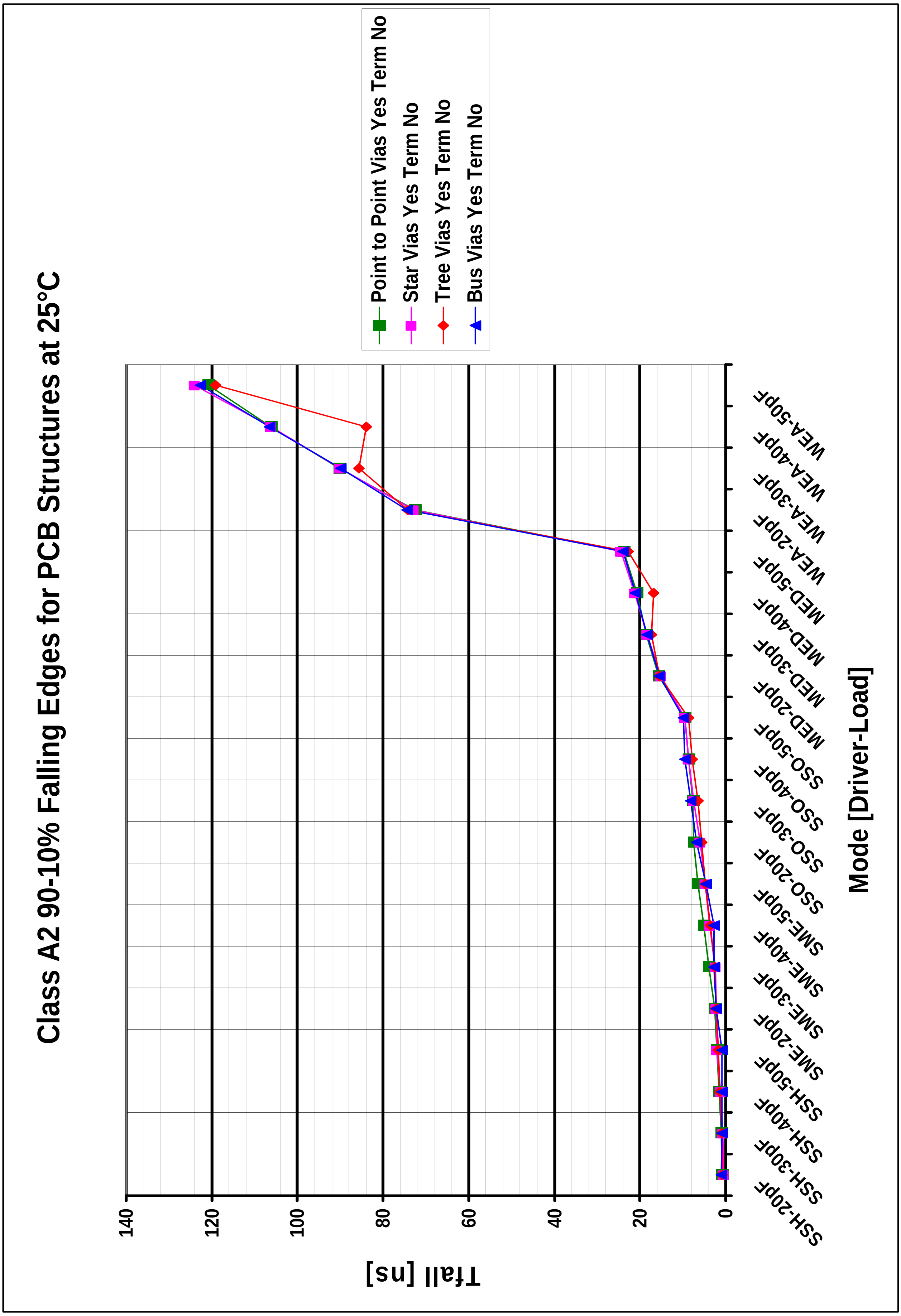


Figure 115: Class A2 fall times for all PCB structures at 25°C

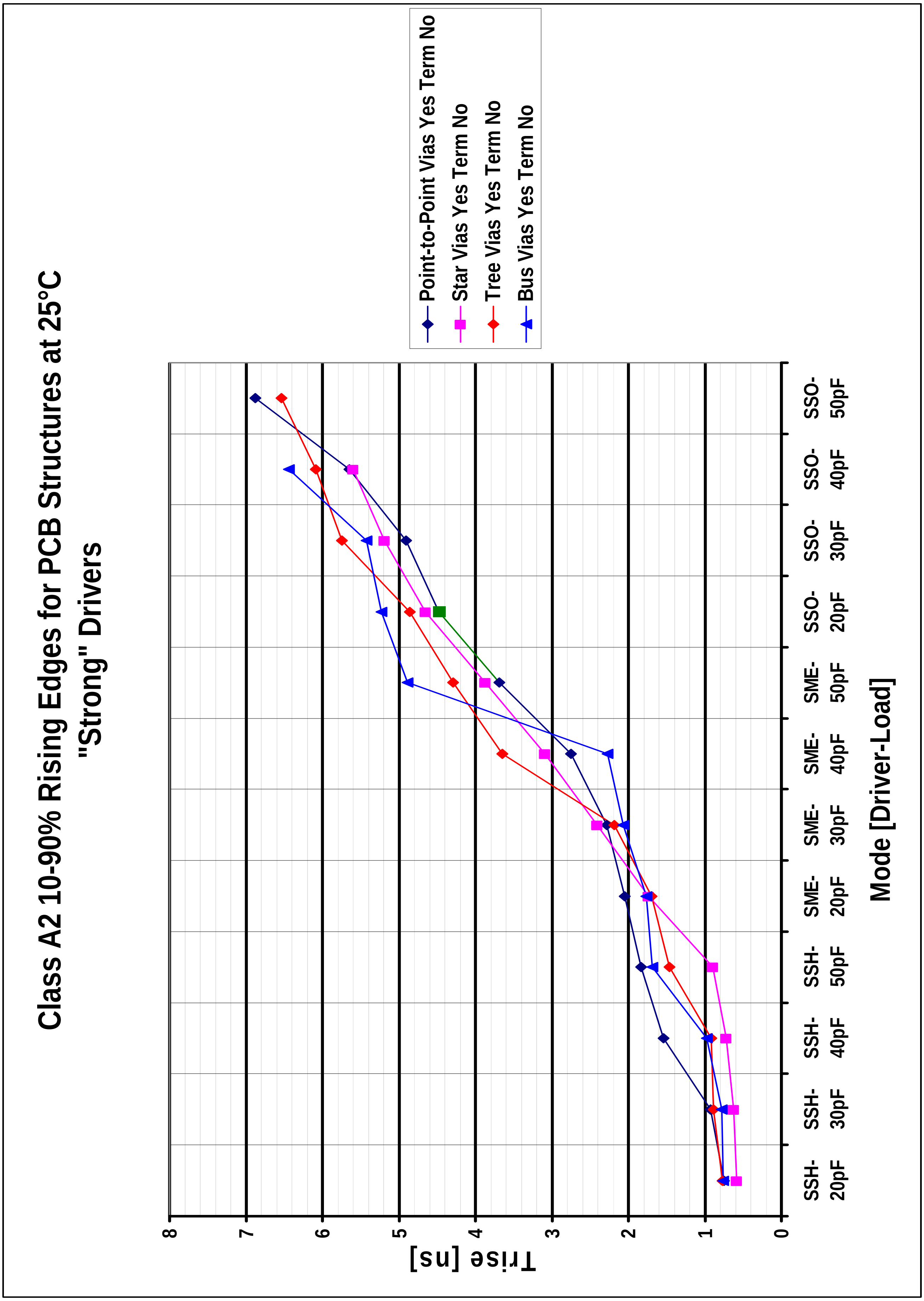


Figure 116: Zoomed rise times Class A2- all PCB structures for strong driver settings at 25°C

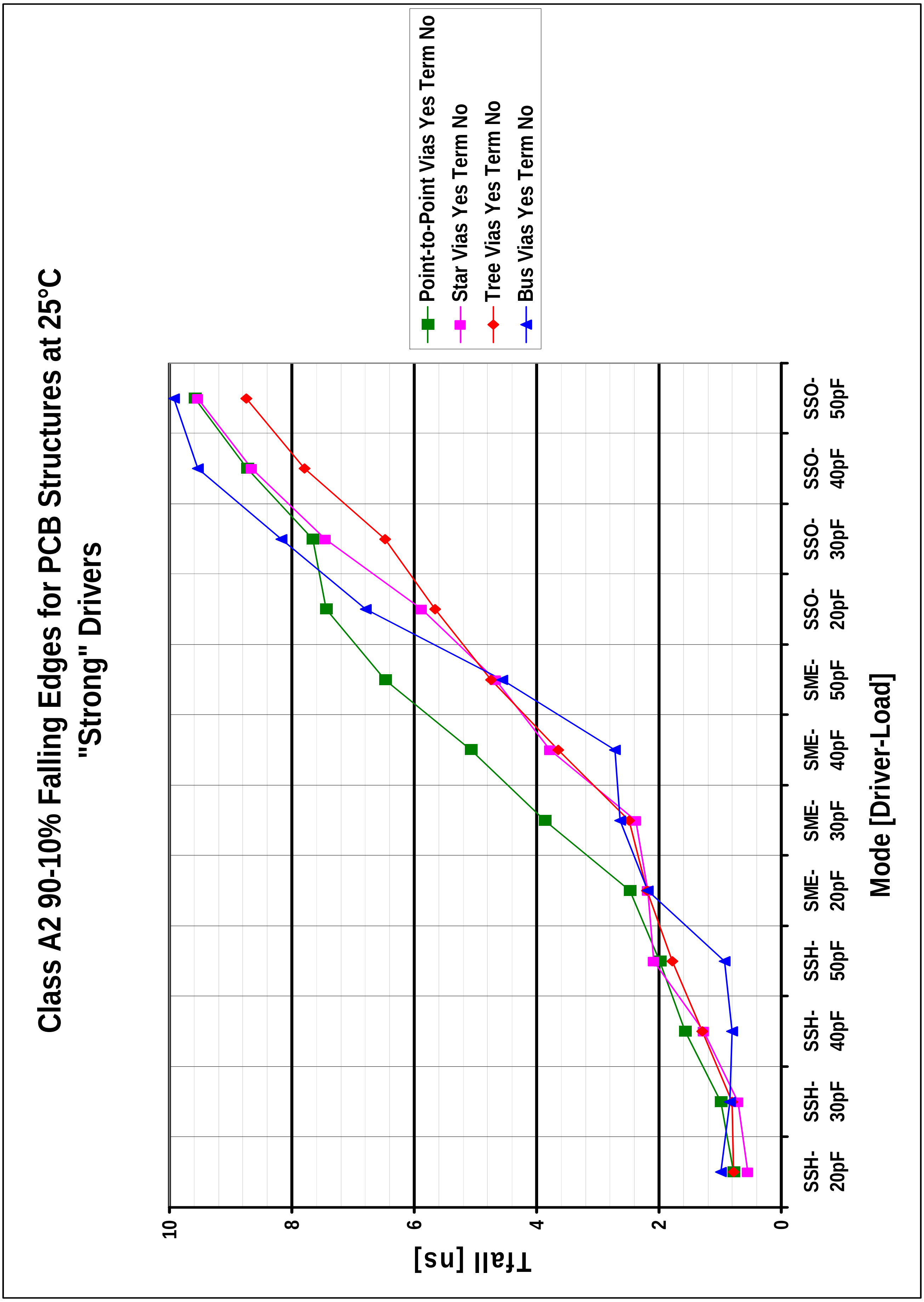


Figure 117: Zoomed fall times Class A2- all PCB structures for strong driver settings at 25°C

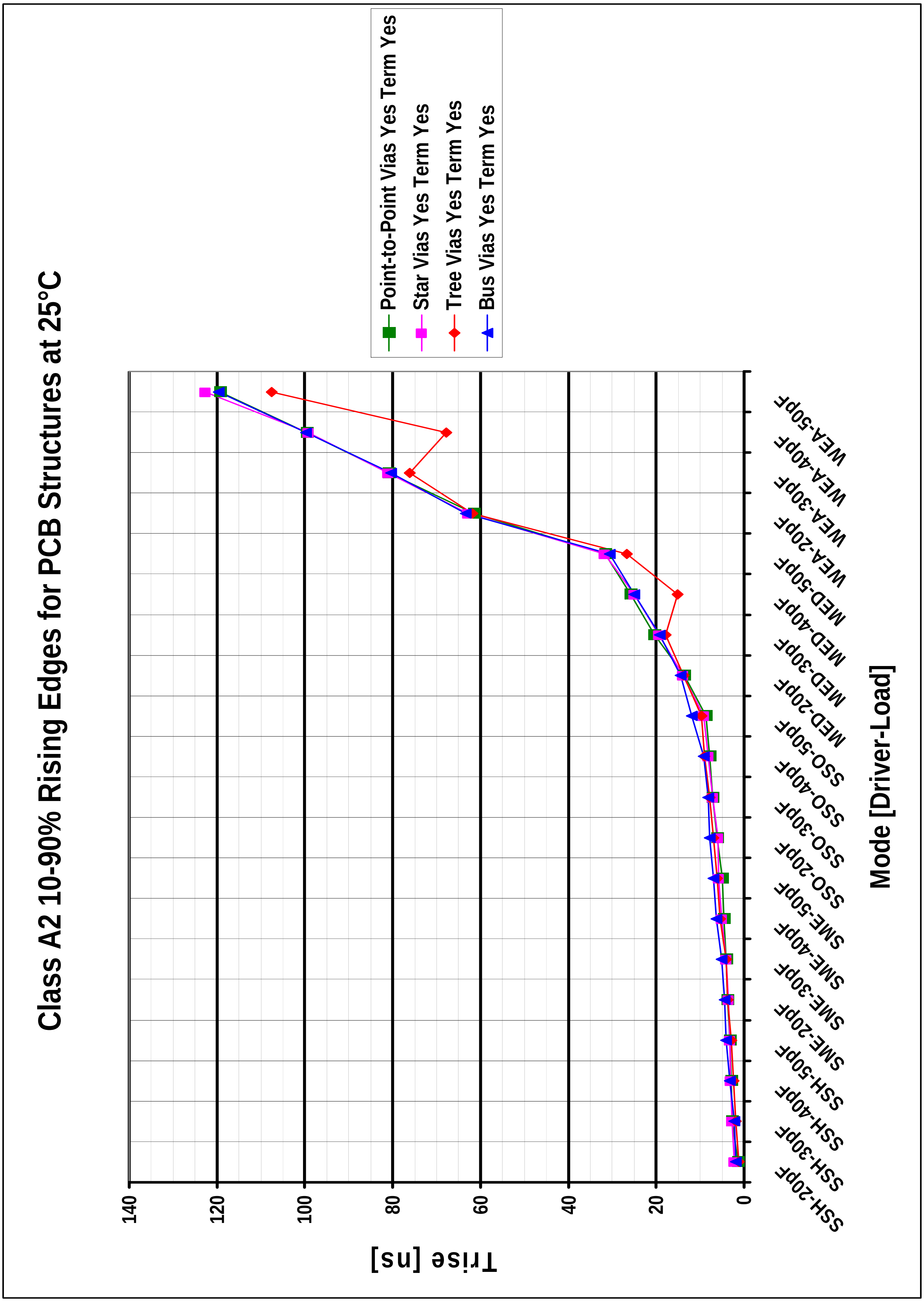


Figure 118: Class A2 rise times for all PCB structures at 25°C

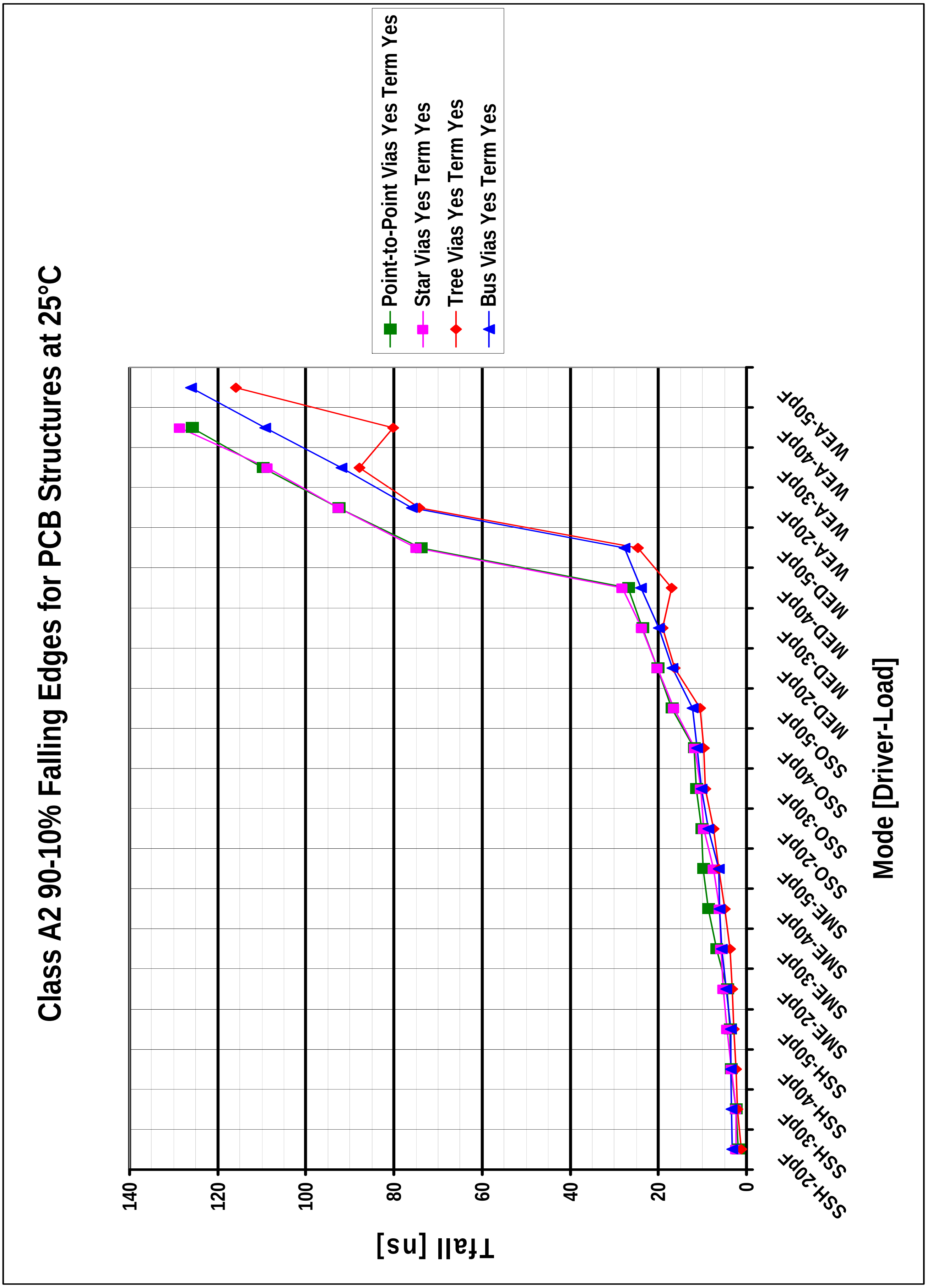


Figure 119: Class A2 fall times for all PCB structures at 25°C

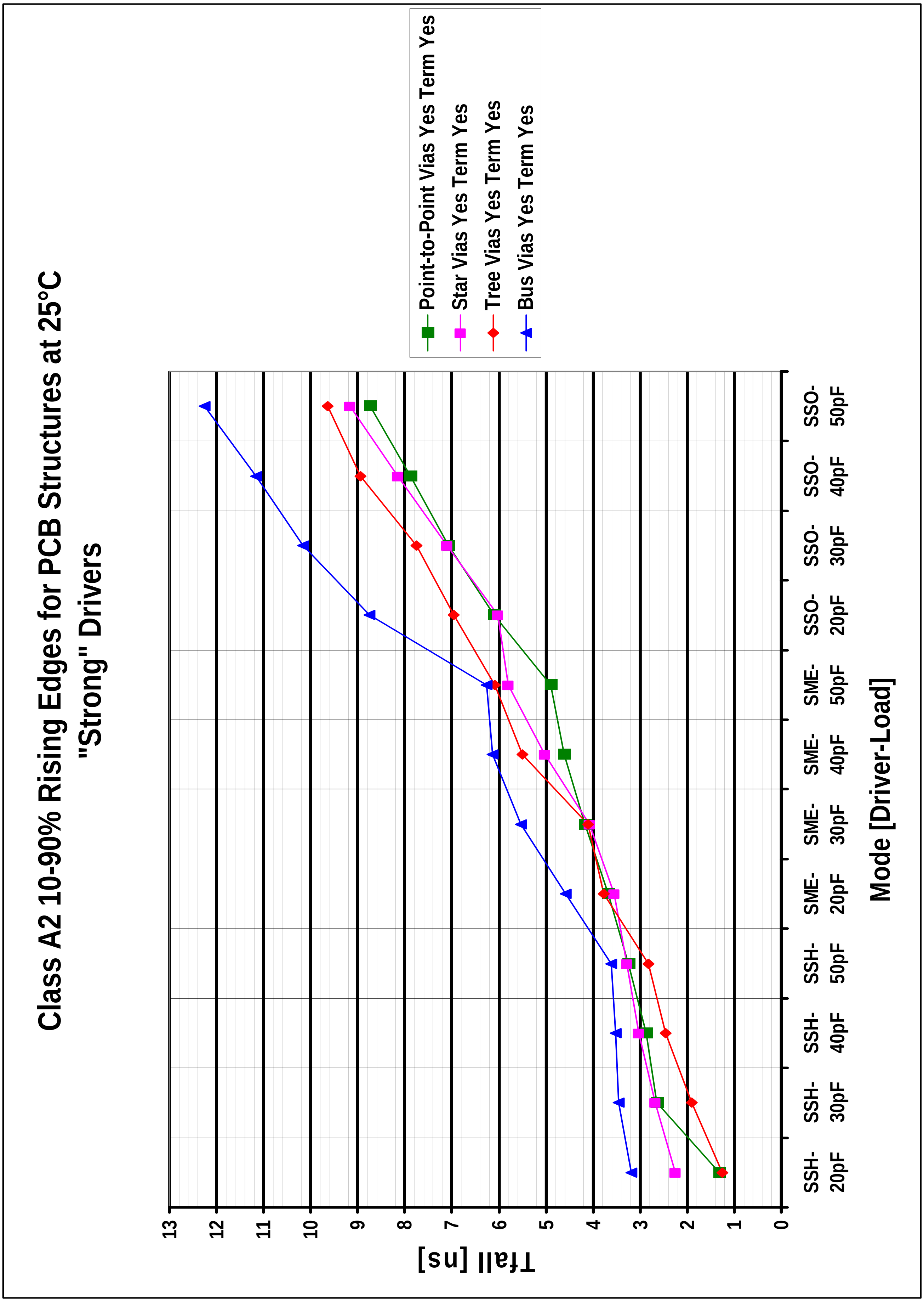


Figure 120: Zoomed rise times Class A2- all PCB structures for strong driver settings at 25°C

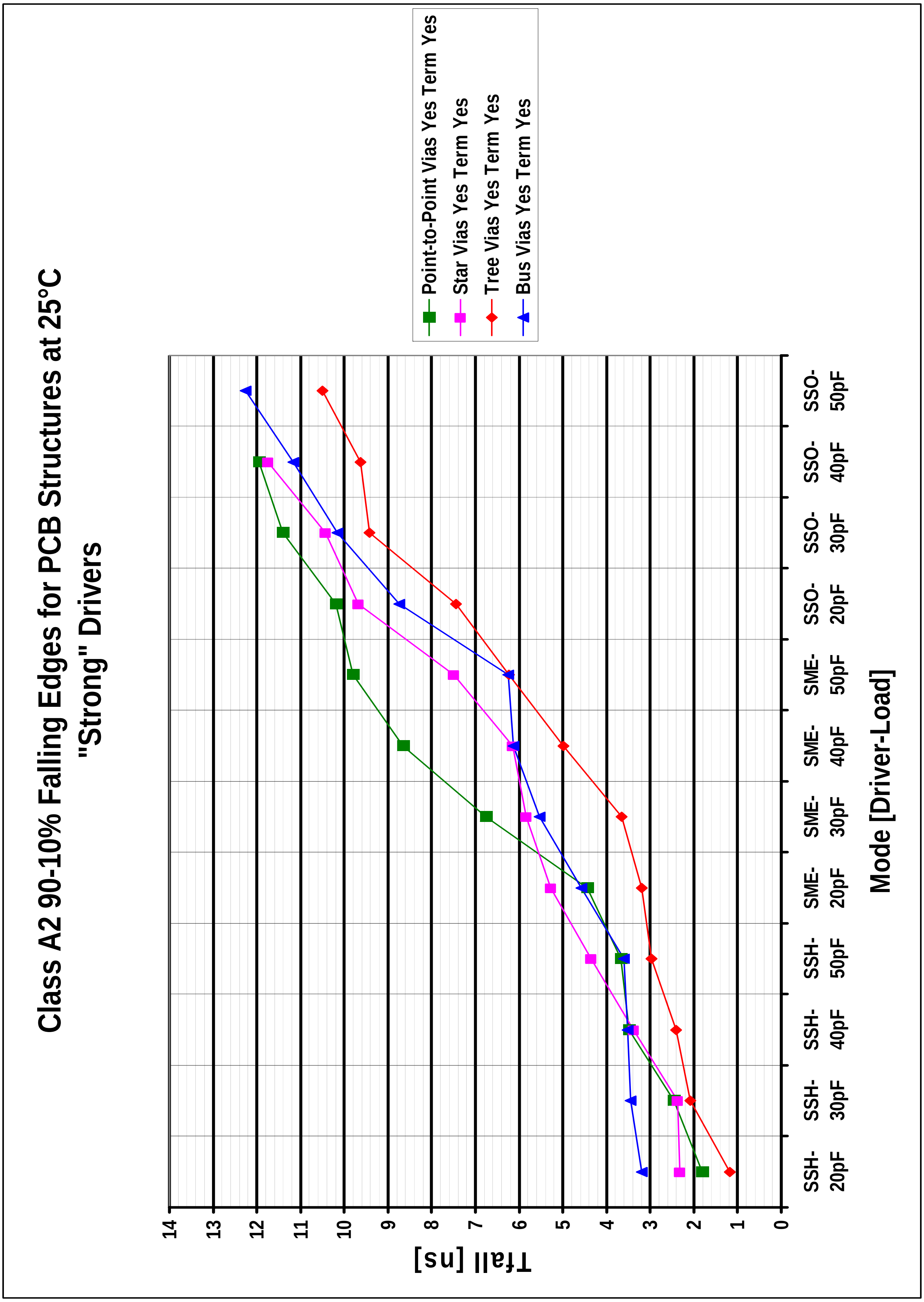


Figure 121: Zoomed fall times Class A2- all PCB structures for strong driver settings at 25°C

4.1.3 Rise/fall waveforms

The following waveforms result from Speed2000™ timing simulations of the PCB structures described in chapter 4.1.1. Since the waveforms of the different structures are very similar, only "point-to-point" and "bus" structures are presented here with loads of 20pF and 40pF. However, the influence of via contacts and termination resistors is visible from the waveforms.

Each of Fig. 123-158 contains 4 waveforms for a given pad type (Class A or Class B), a given ambient temperature (25°C or 150°C) and a given driver strength. Depending on these settings, certain clock frequencies can be driven or not. The waveforms show one of the frequencies: 80MHz, 40MHz, 20MHz, 10MHz or 1MHz – whatever is the highest frequency for a given setting which shows an acceptable signal integrity (i.e. high and low voltage levels are reached during switching).

Note the different high voltage levels for Class A and Class B pads: Since Class B pads are implemented for the EBU interface drivers, the Class B simulations use 2.5V high level, whereas the Class A simulations use 3.3V high level.

The 4 configurations shown in one figure are distributed as follows:

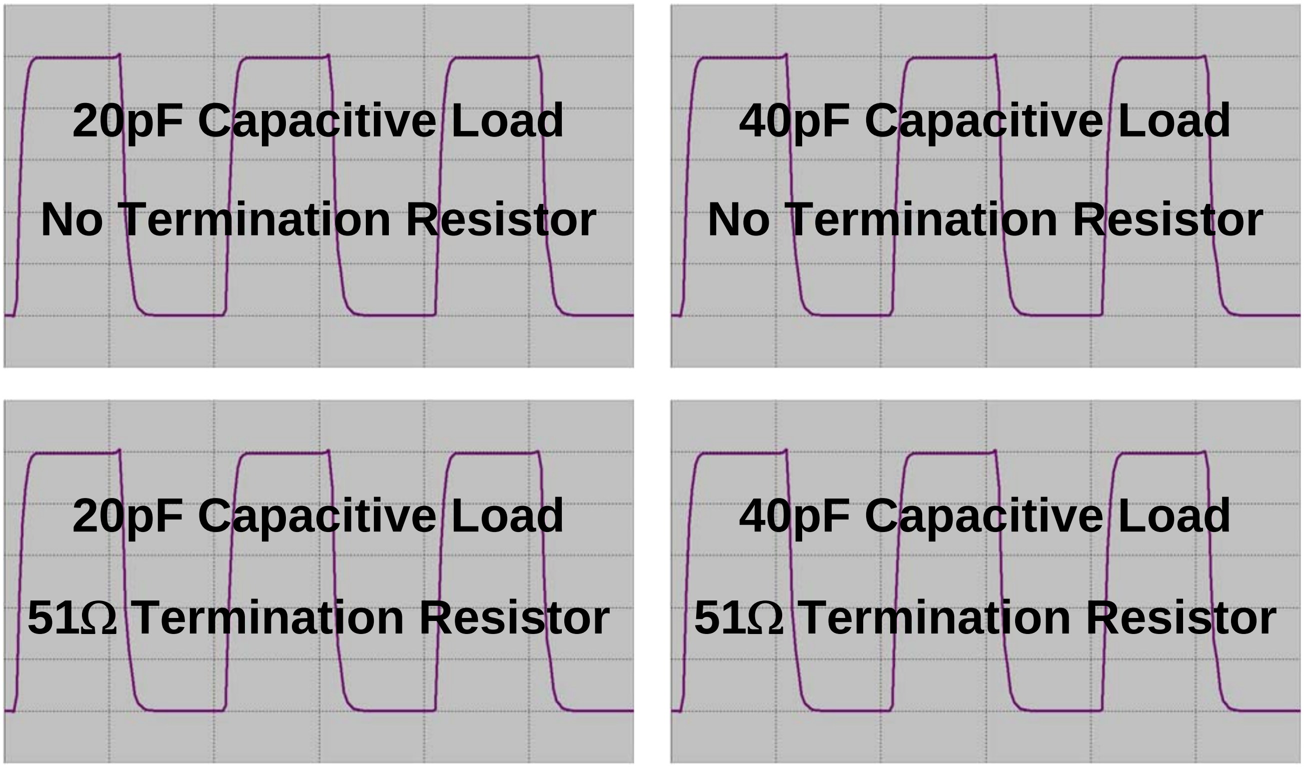


Figure 122: General grouping of waveform configurations

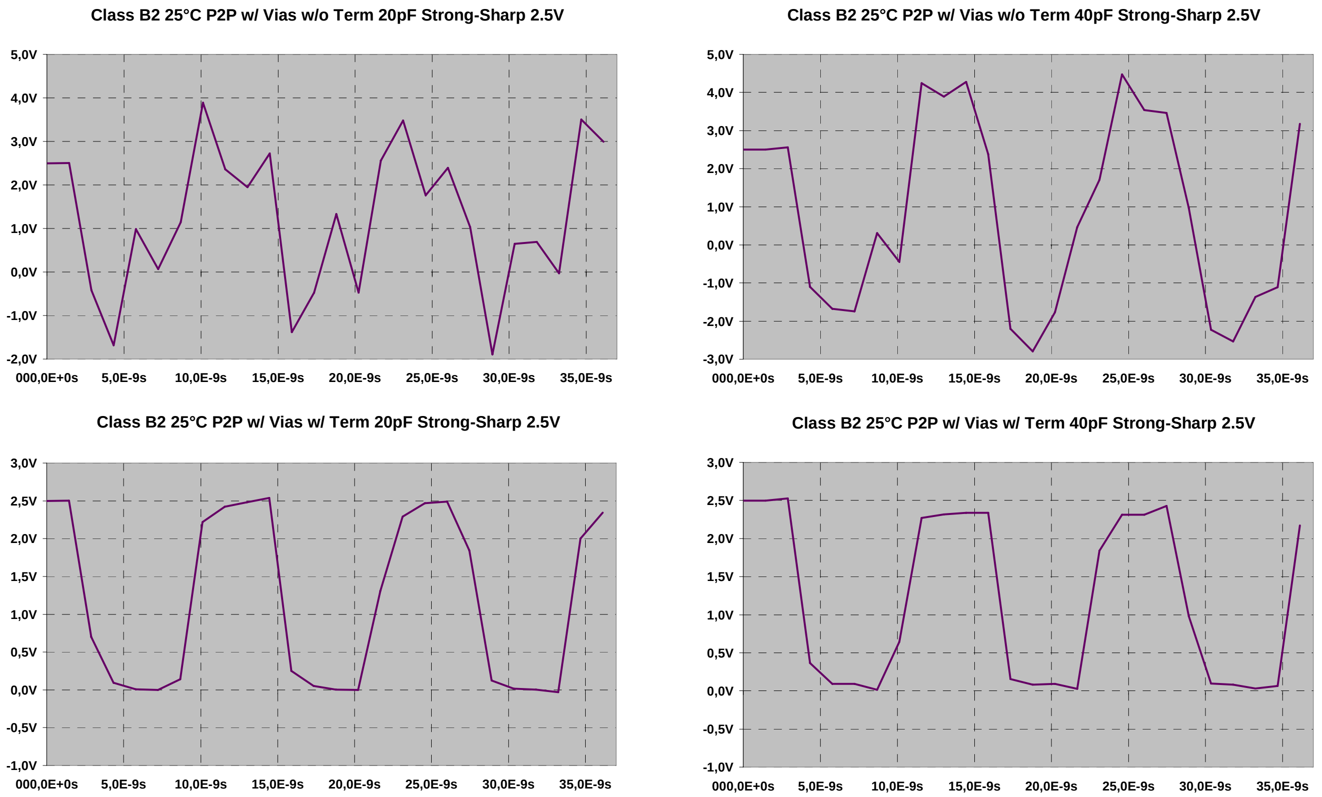


Figure 123: Waveforms Class B2 80 MHz “Strong-Sharp” /“Point-to-Point” at 25°C ambient temperature

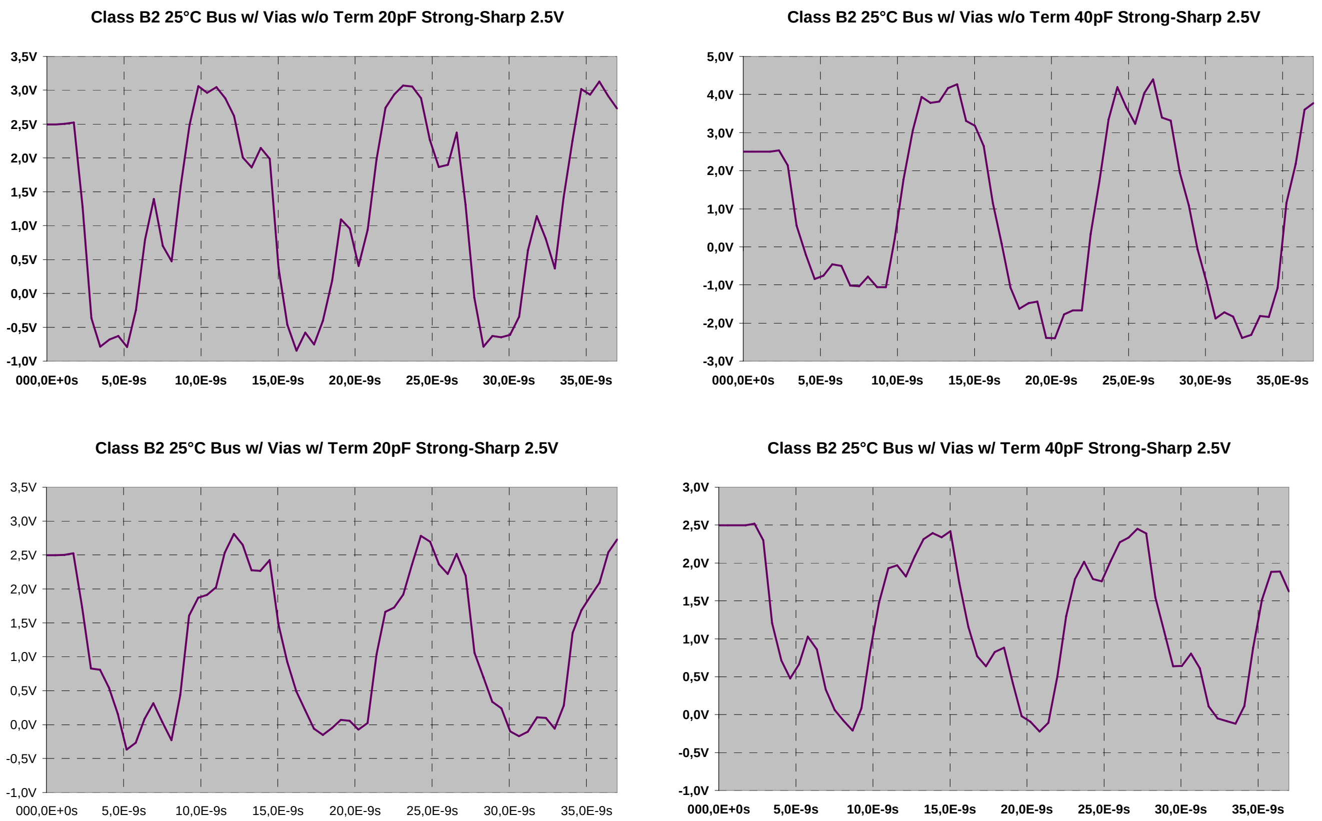


Figure 124: Waveforms Class B2 80 MHz “Strong-Sharp” /“Bus” at 25°C ambient temperature

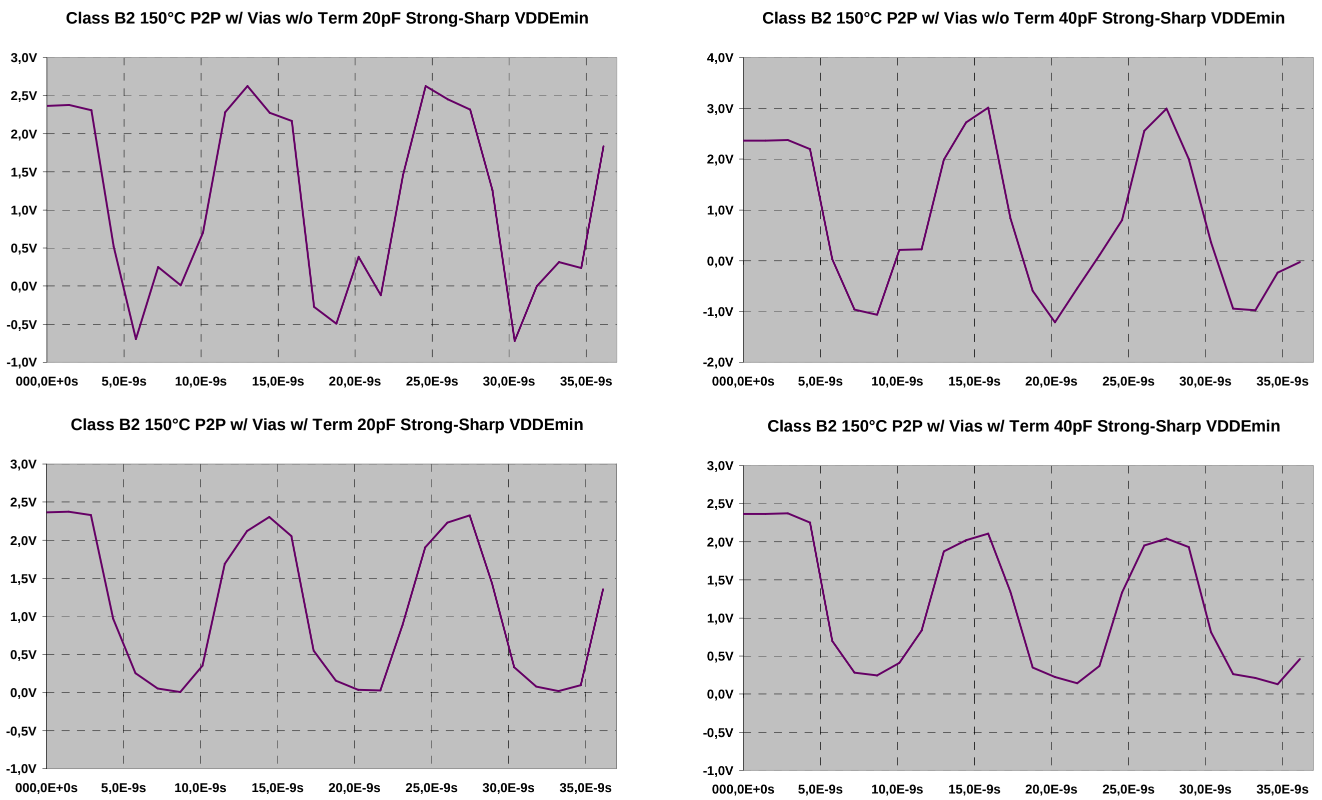


Figure 125:Waveforms Class B2 80 MHz “Strong-Sharp” /“Point-to-Point”at 150°C ambient temperature

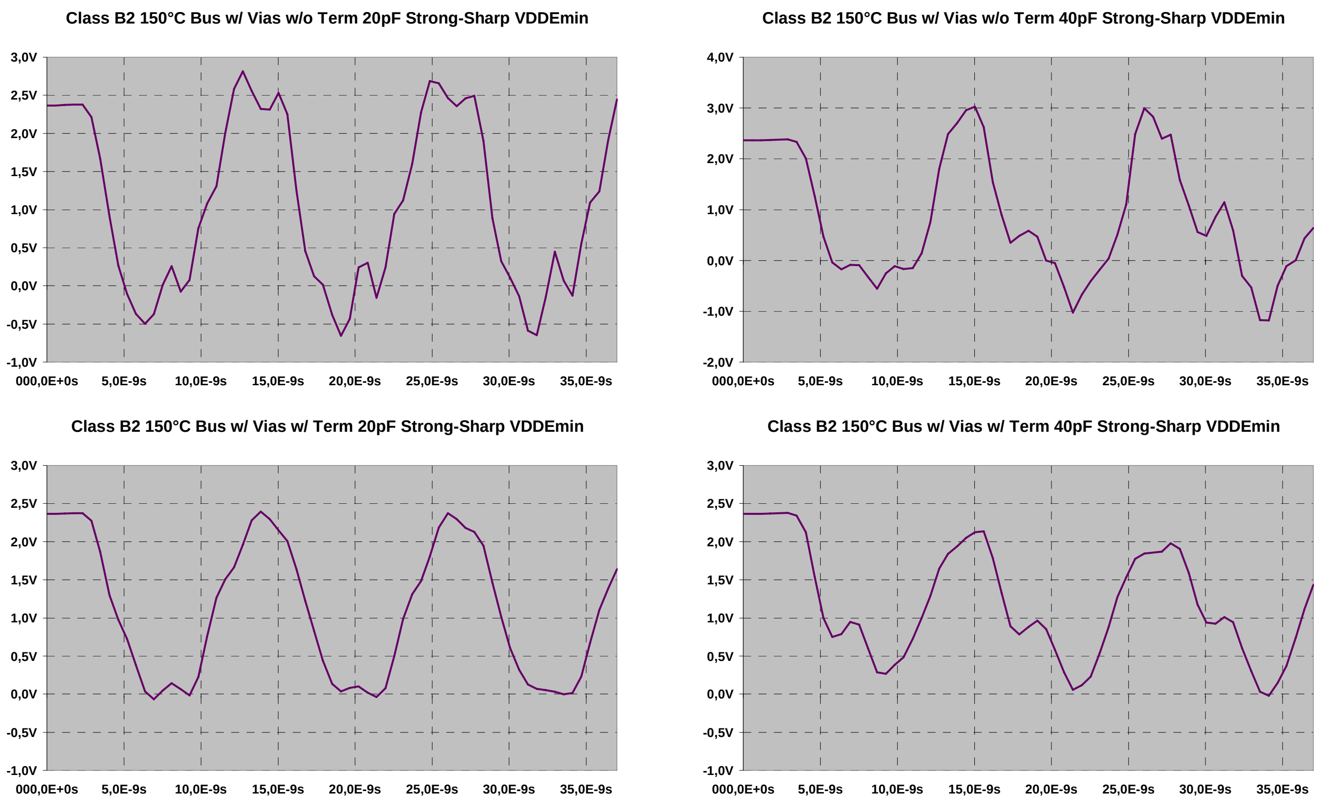


Figure 126: Waveforms Class B2 80 MHz “Strong-Sharp” /“Bus” at 150°C ambient temperature

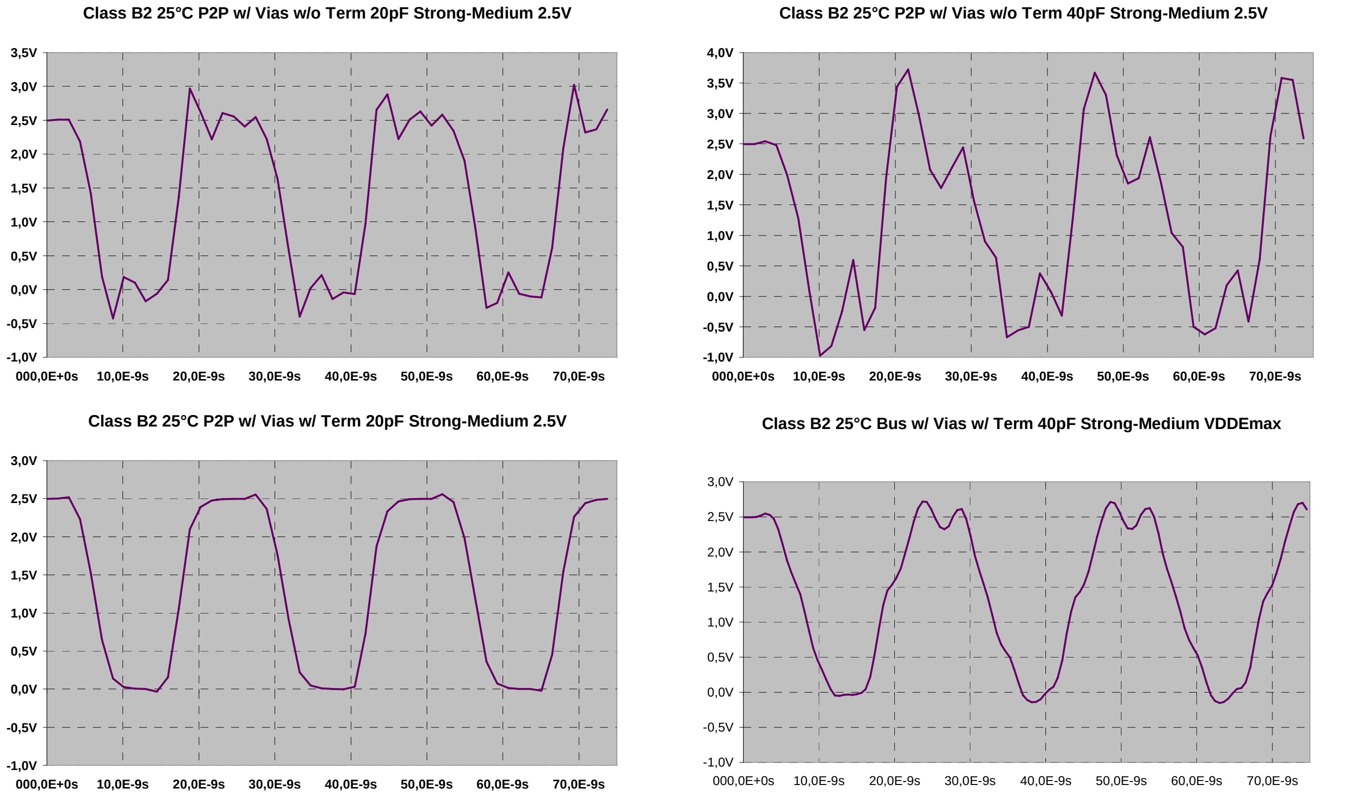


Figure 127: Waveforms Class B2 40 MHz “Strong-Med” / “Point-to-Point” at 25°C ambient temperature

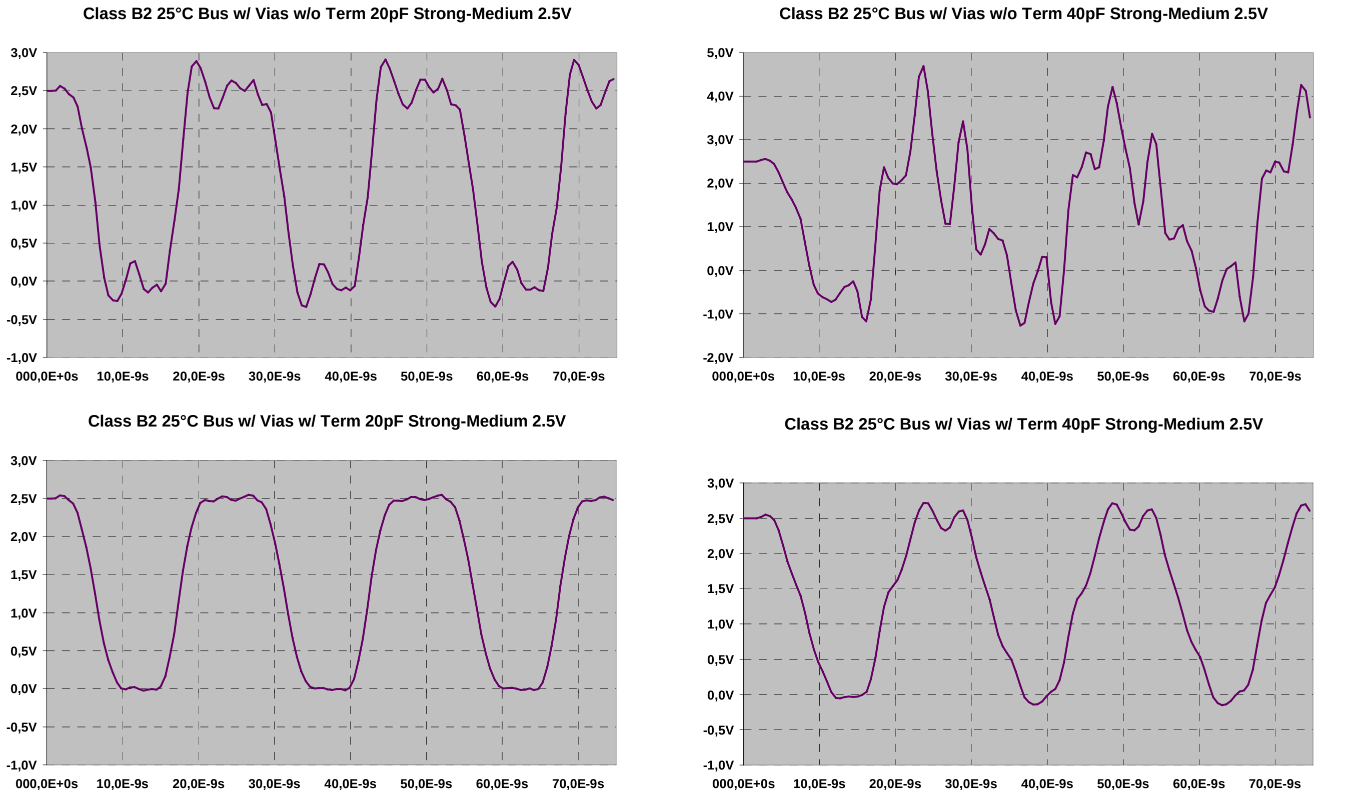


Figure 128: Waveforms Class B2 40 MHz “Strong-Med” / “Bus” at 25°C ambient temperature

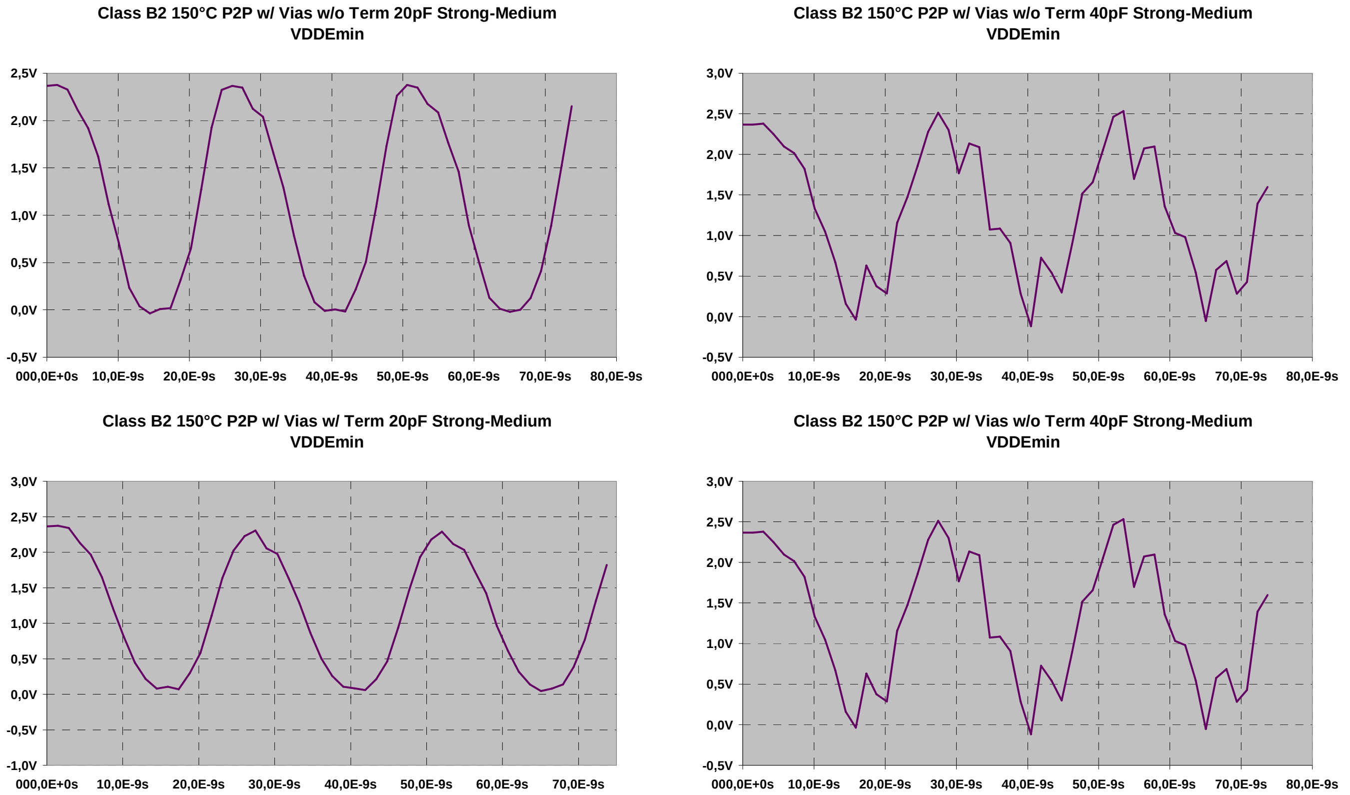


Figure 129: Waveforms Class B2 40 MHz "Strong-Med" / "Point-to-Point" at 150°C ambient temperature

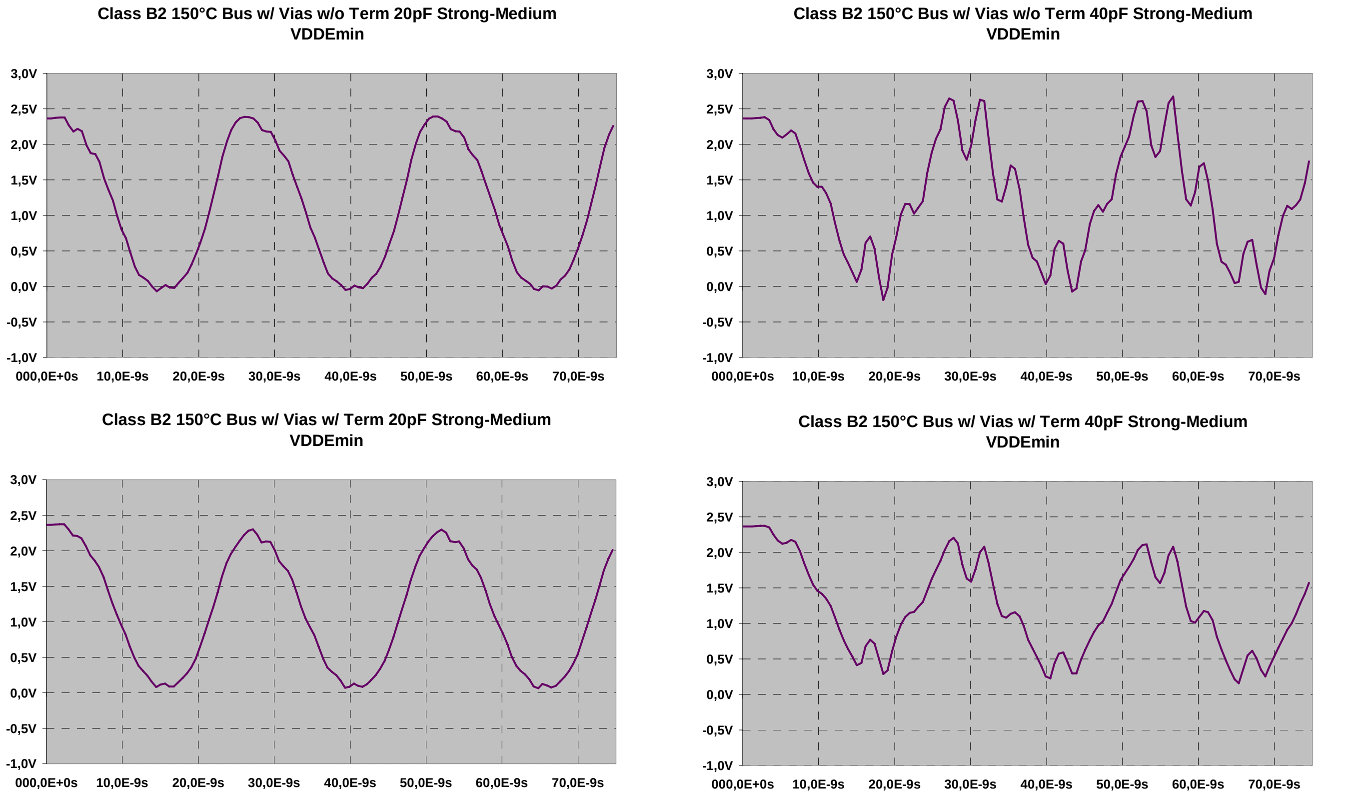


Figure 130: Waveforms Class B2 40 MHz "Strong-Med" / "Bus" at 150°C ambient temperature

Class B2 3.3V:-

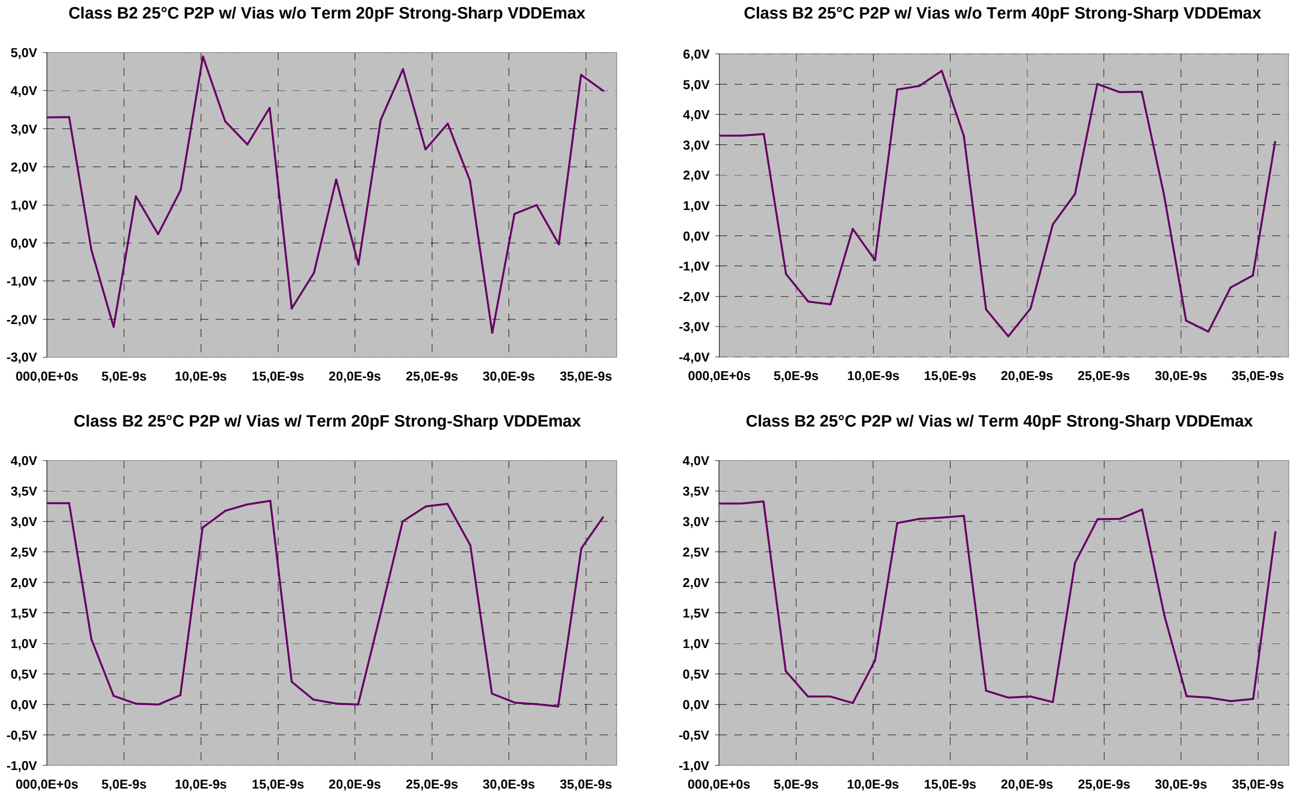


Figure 131: Waveforms Class B2 80 MHz “Strong-Sharp” / “P2P” at 25°C ambient temperature

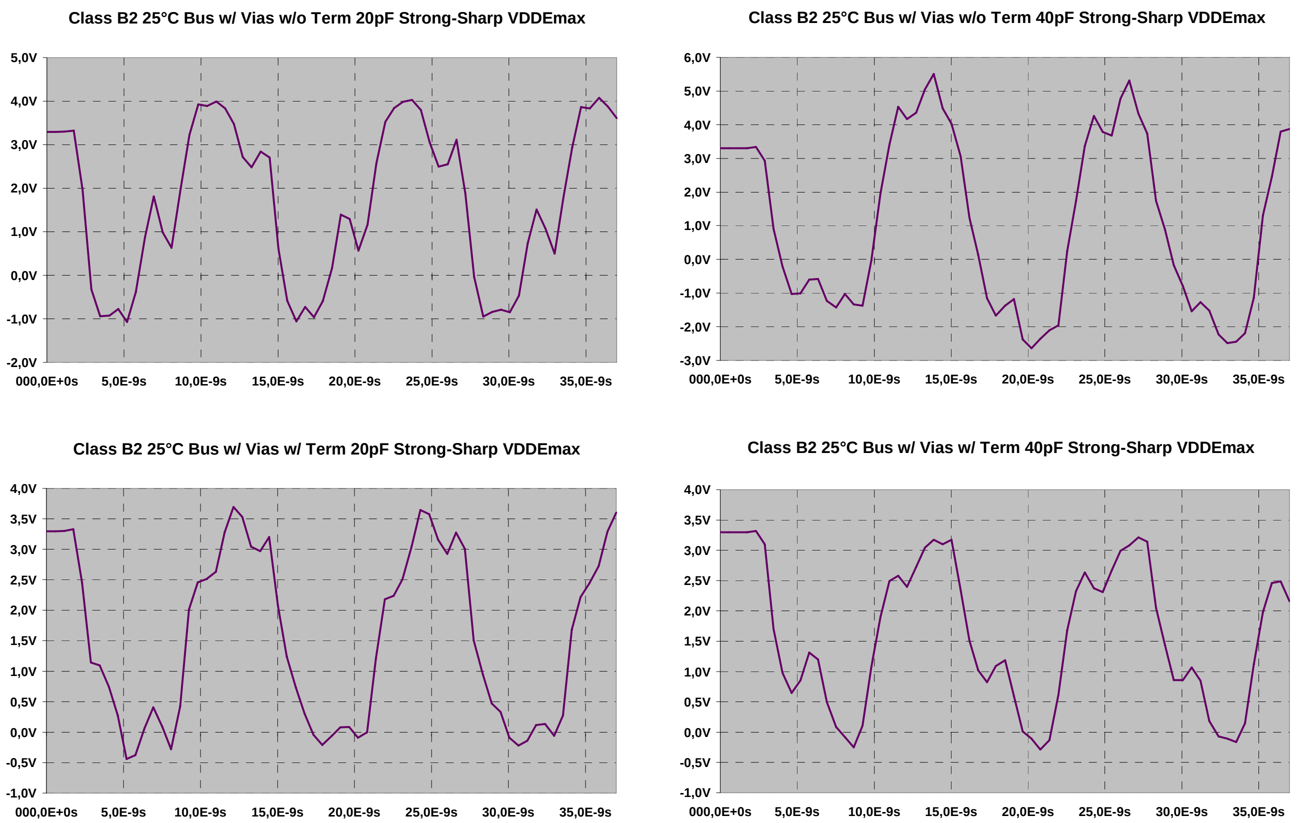


Figure 132: Waveforms Class B2 80 MHz “Strong-Sharp” / “Bus” at 25°C ambient temperature

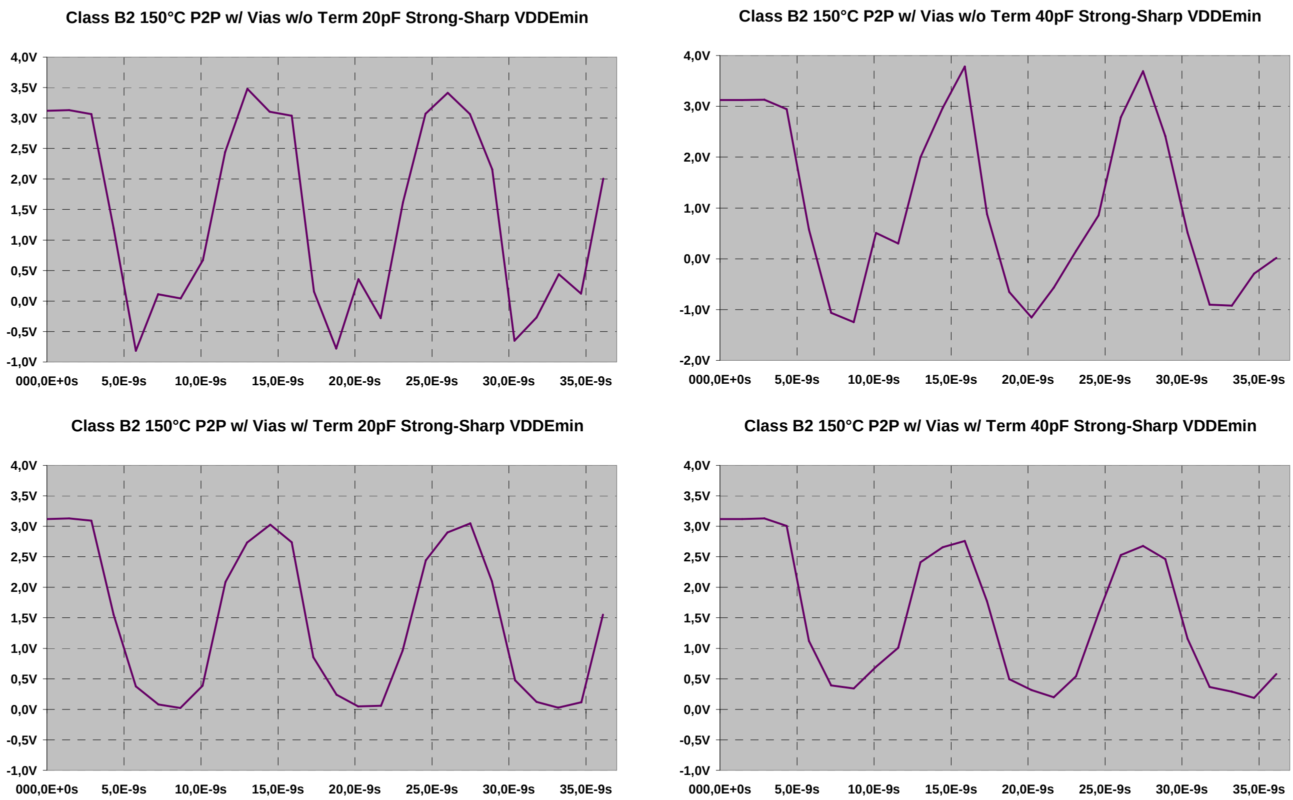


Figure 133: Waveforms Class B2 80 MHz "Strong-Sharp" / "P2P" at 150°C ambient temperature

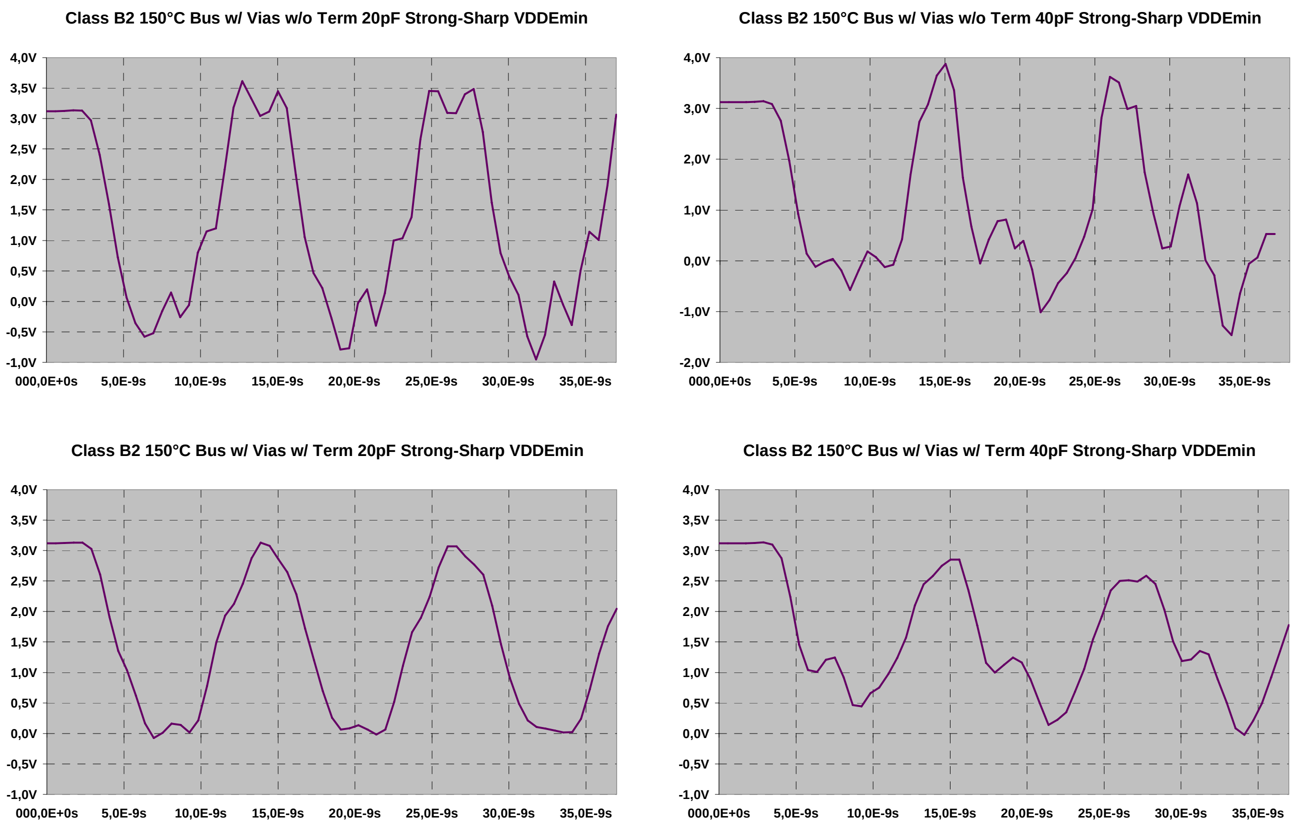


Figure 134: Waveforms Class B2 80 MHz "Strong-Sharp" / "Bus" at 150°C ambient temperature

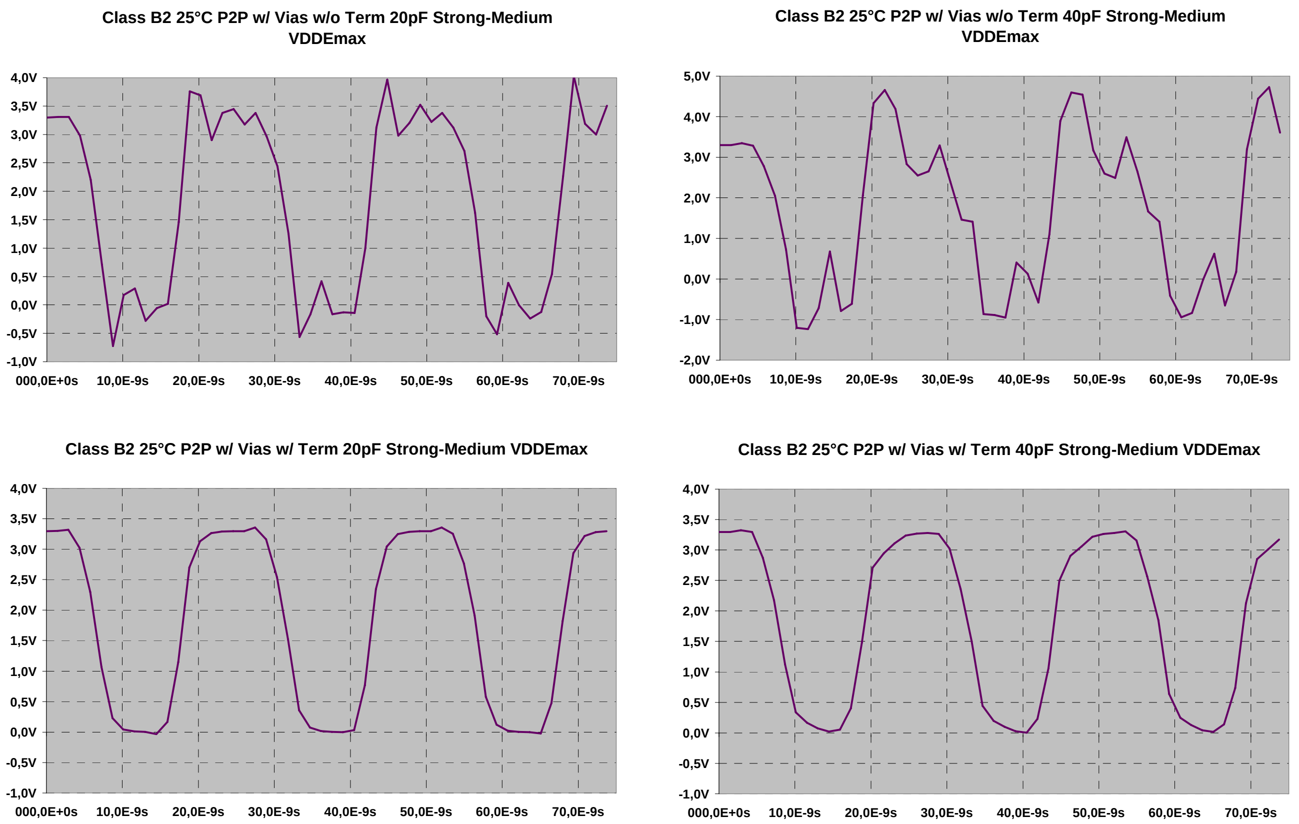


Figure 135: Waveforms Class B2 40 MHz “Strong-Medium” / “P2P” at 25°C ambient temperature

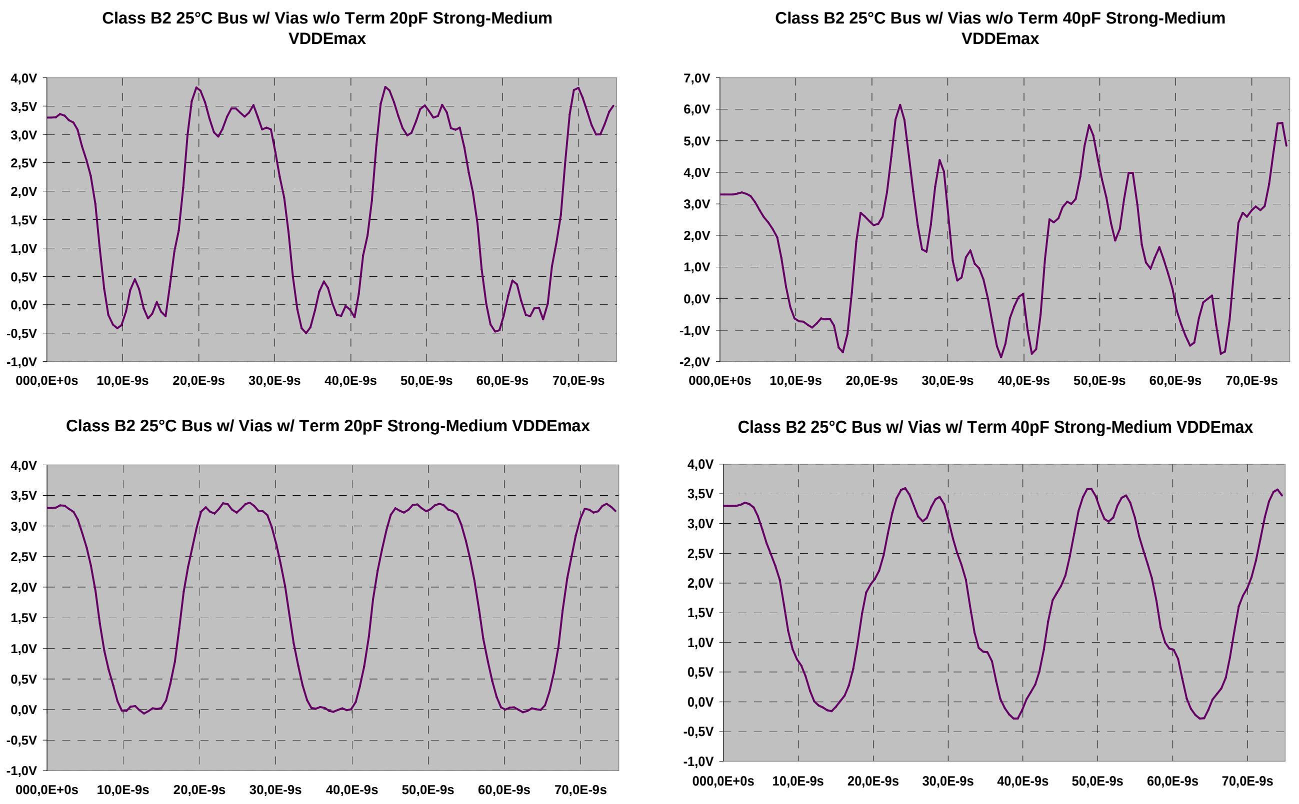


Figure 136: Waveforms Class B2 40 MHz “Strong-Medium” / “Bus” at 25°C ambient temperature

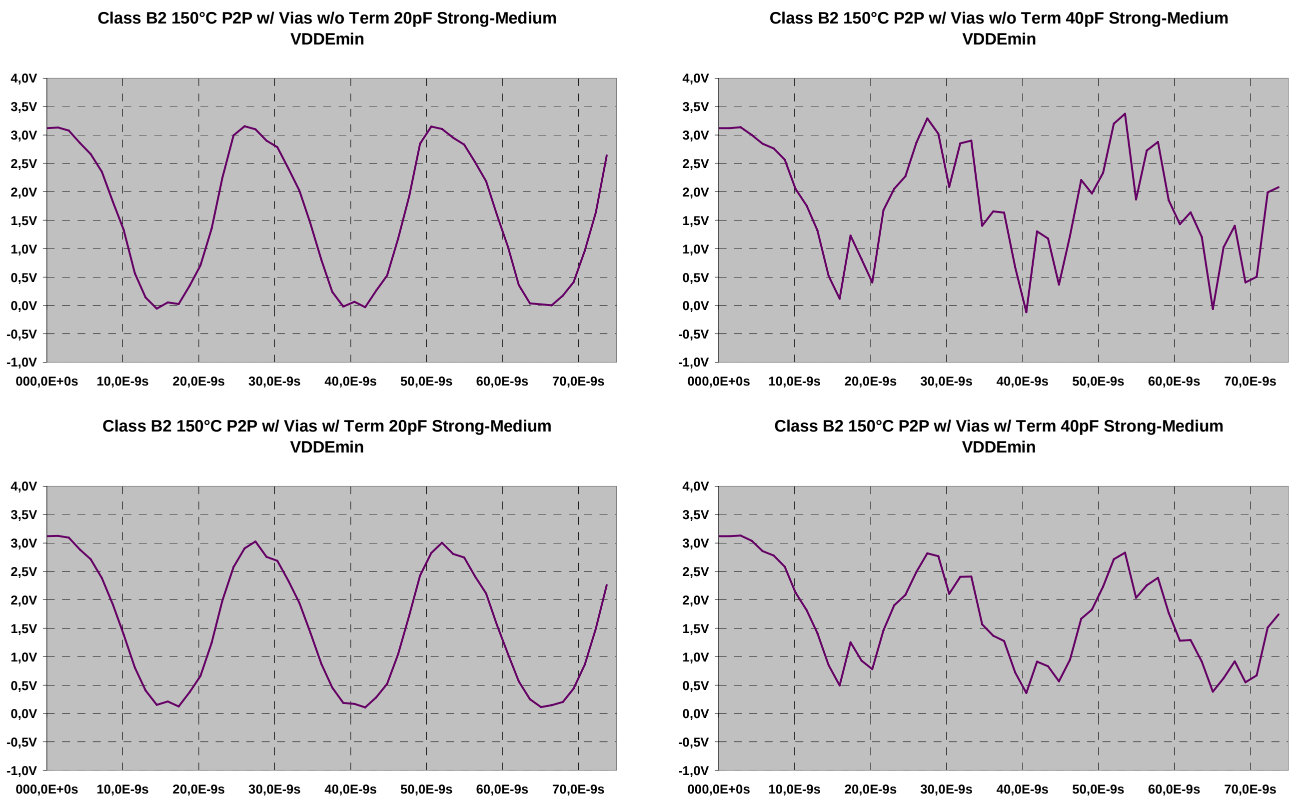


Figure 137: Waveforms Class B2 40 MHz "Strong-Medium" / "P2P" at 150°C ambient temperature

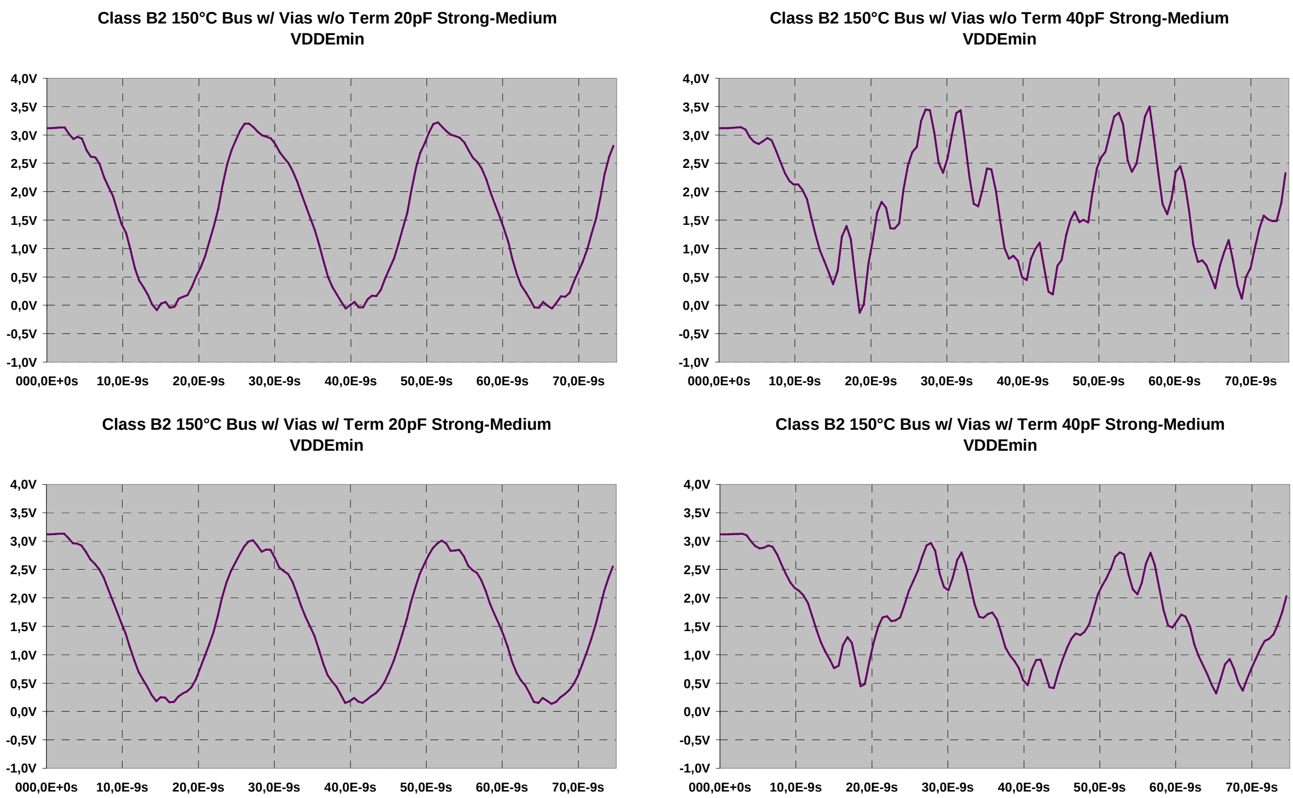


Figure 138: Waveforms Class B2 40 MHz "Strong-Medium" / "Bus" at 150°C ambient temperature

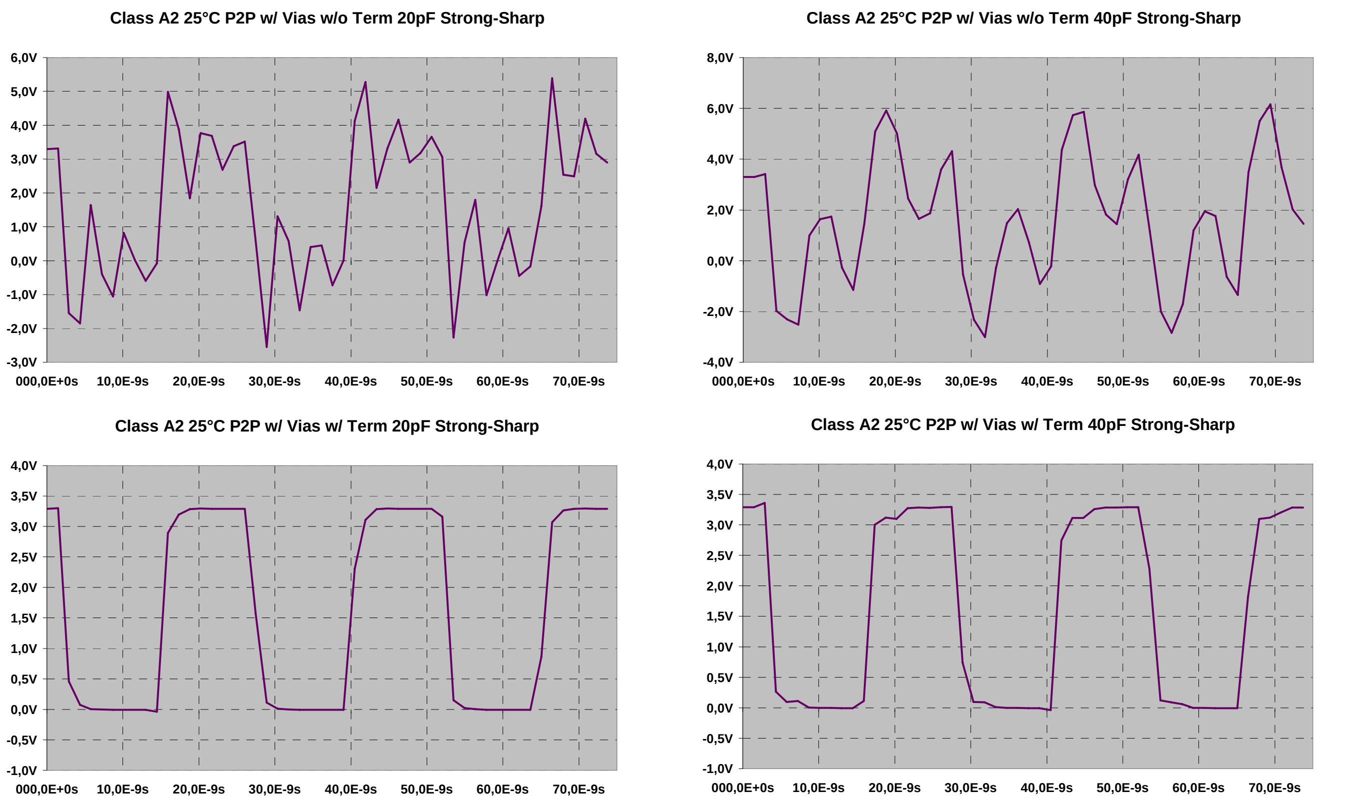


Figure 139: Waveforms Class A2 40 MHz “Strong-Sharp” / “Point-to-Point” at 25°C ambient temper.

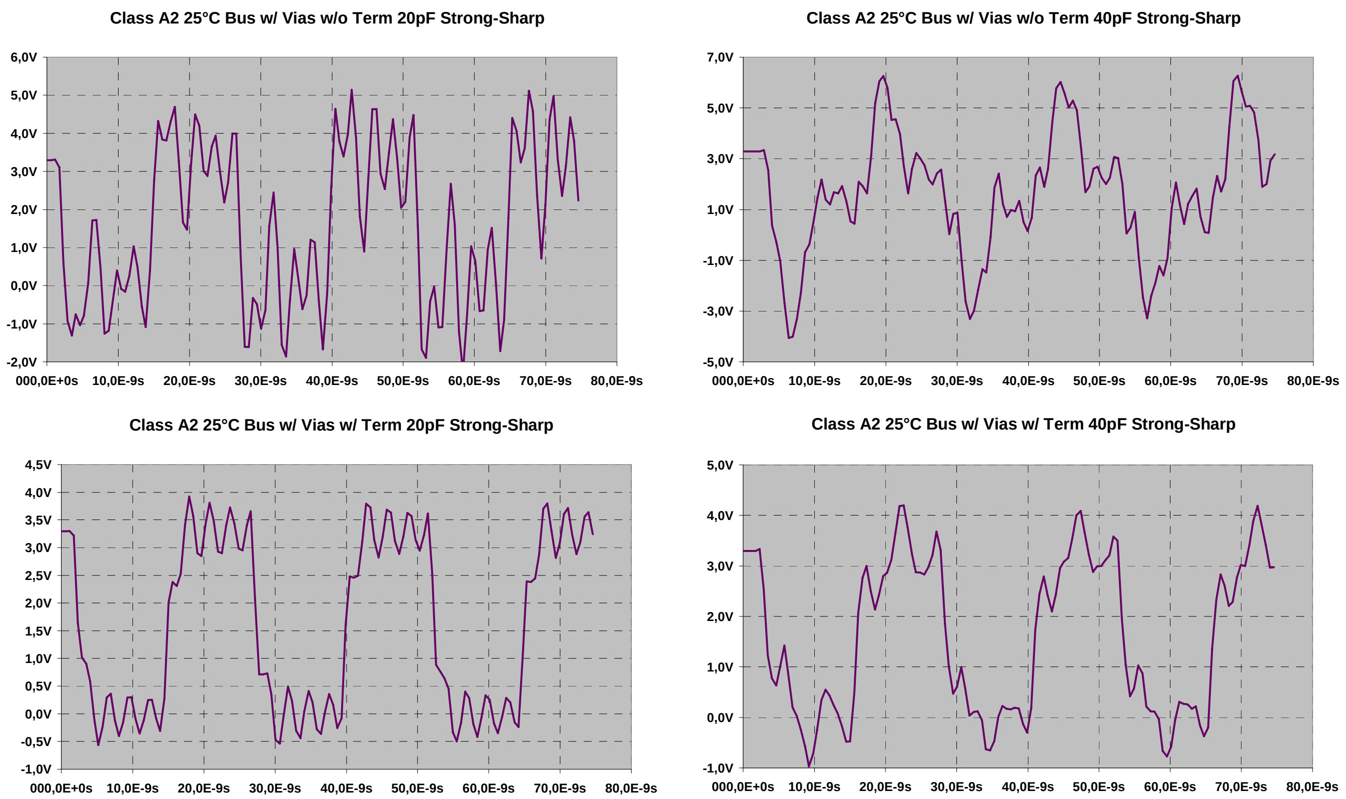


Figure 140: Waveforms Class A2 40 MHz “Strong-Sharp” / “Bus” at 25°C ambient temperature

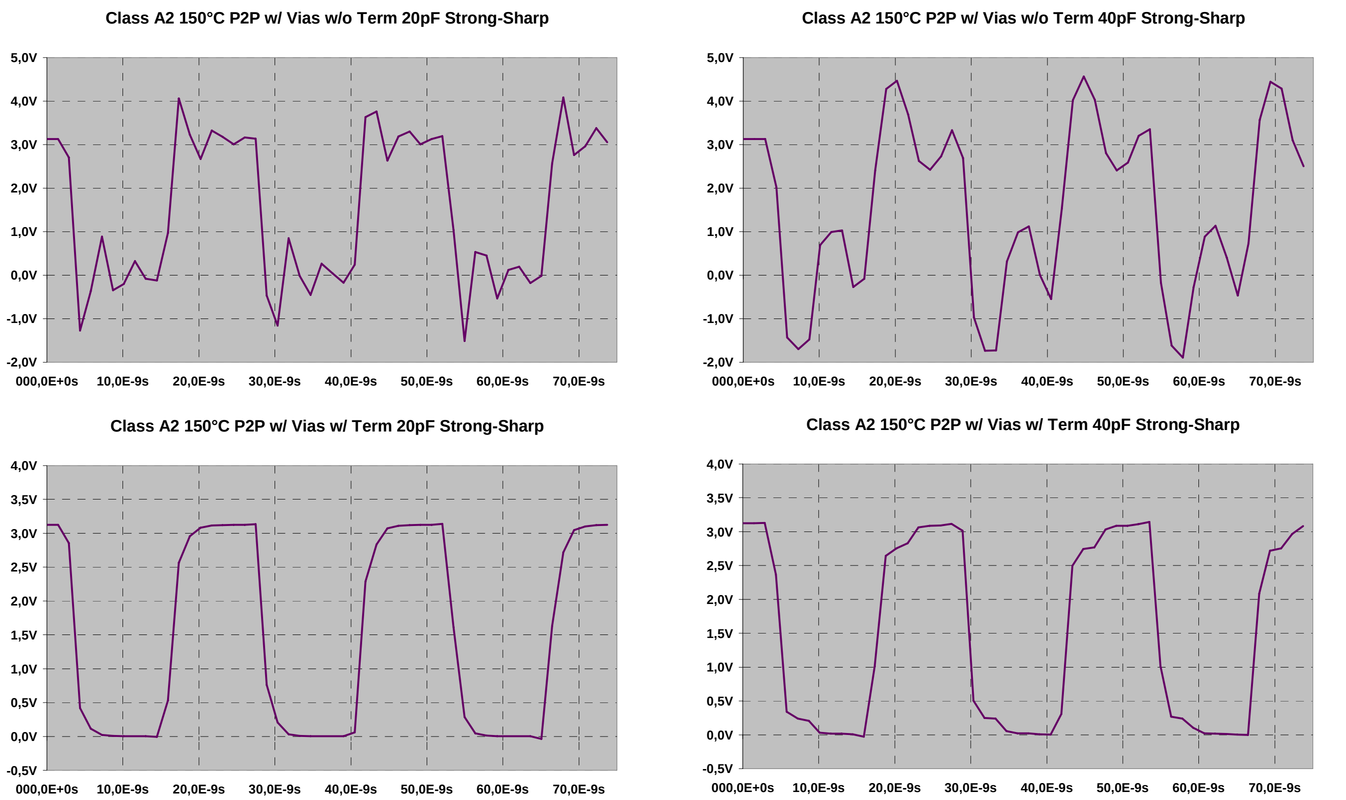


Figure 141: Waveforms Class A2 40 MHz "Strong-Sharp"/ "Point-to-Point" at 150°C ambient temper.

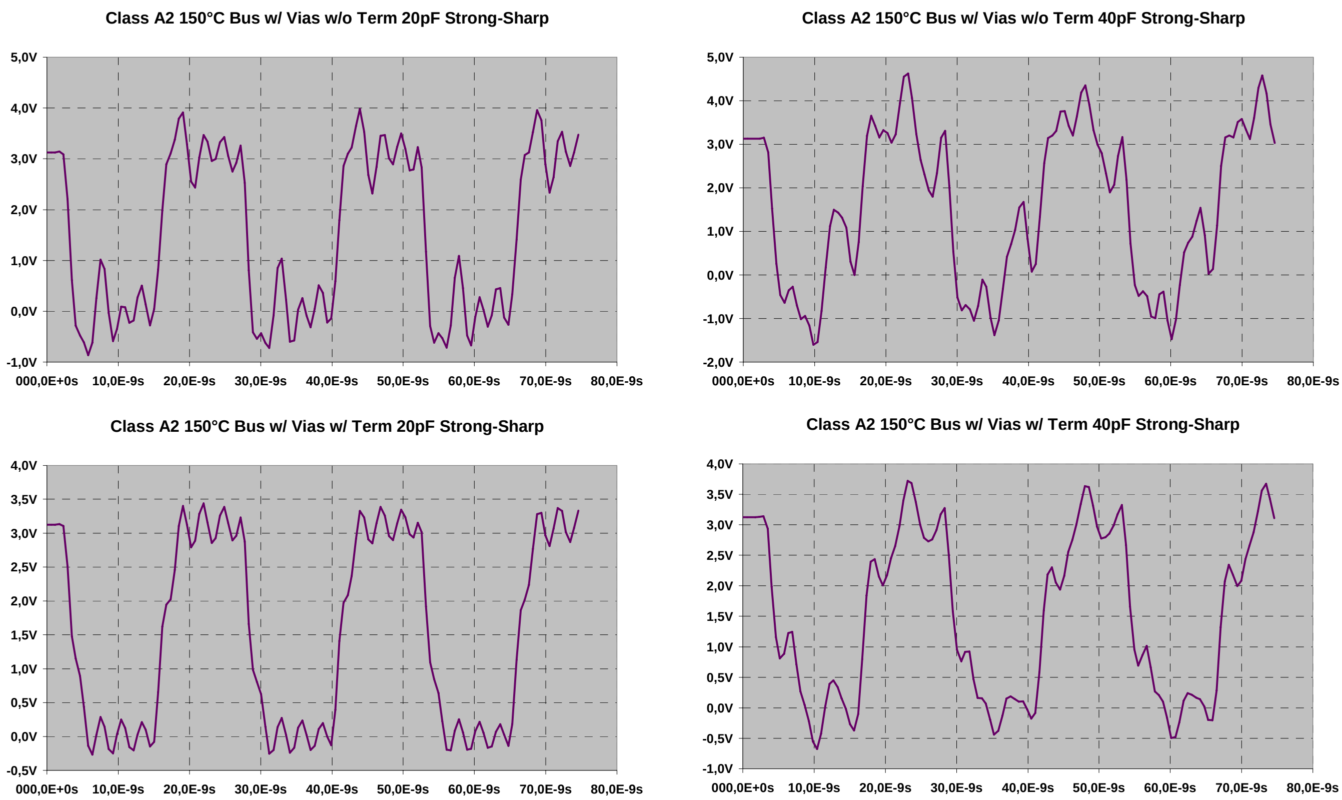


Figure 142: Waveforms Class A2 40 MHz "Strong-Sharp"/ "Bus" at 150°C ambient temper.

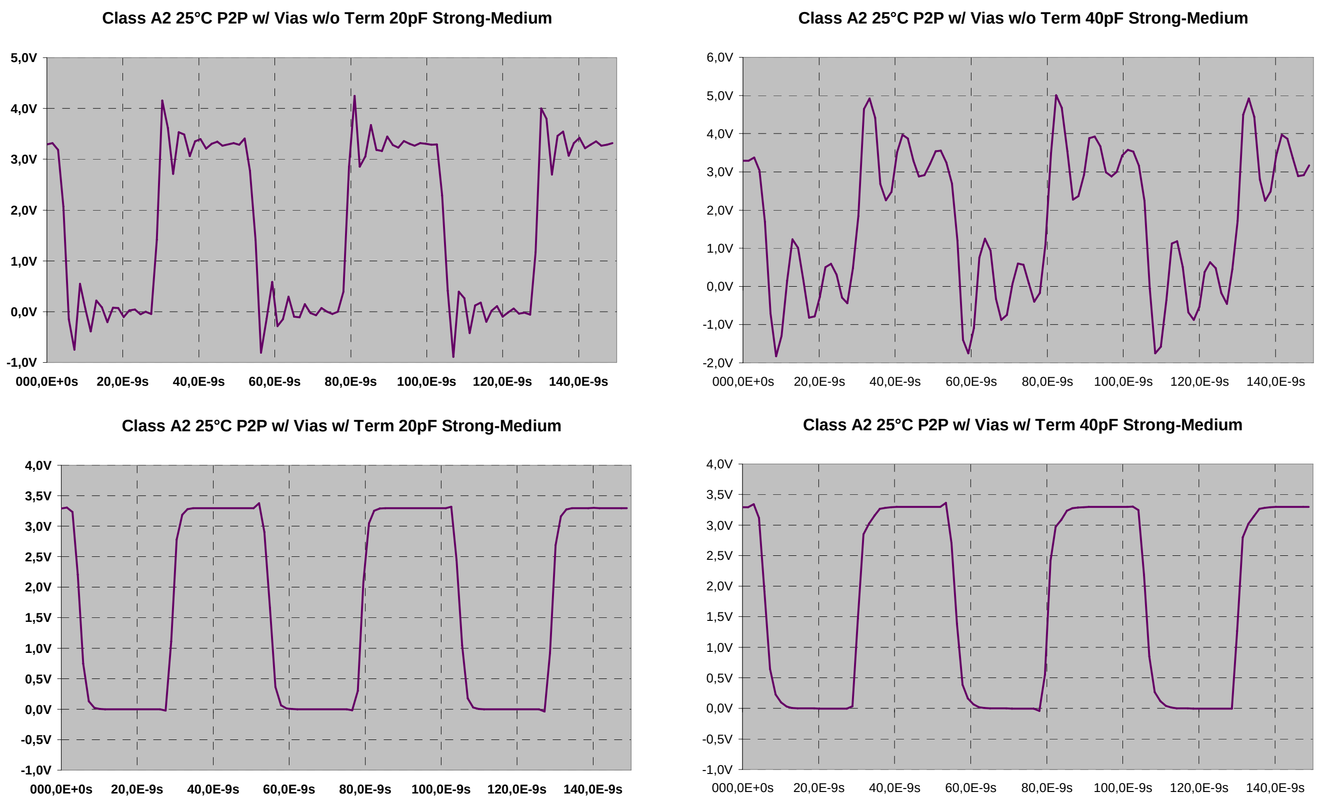


Figure 143: Waveforms Class A2 20 MHz "Strong-Medium" / "Point-to-Point" at 25°C ambient temper.

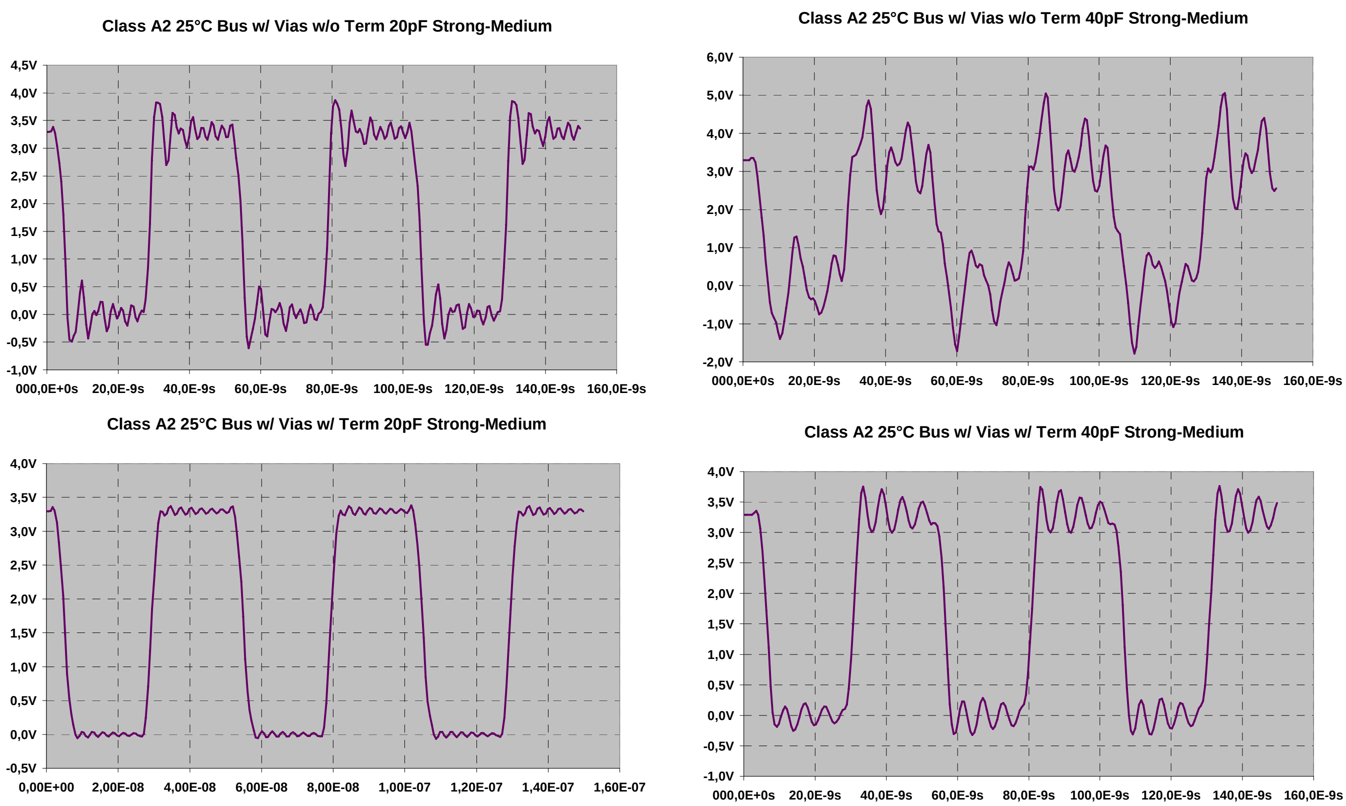


Figure 144: Waveforms Class A2 20 MHz "Strong-Medium" / "Bus" at 25°C ambient temper.

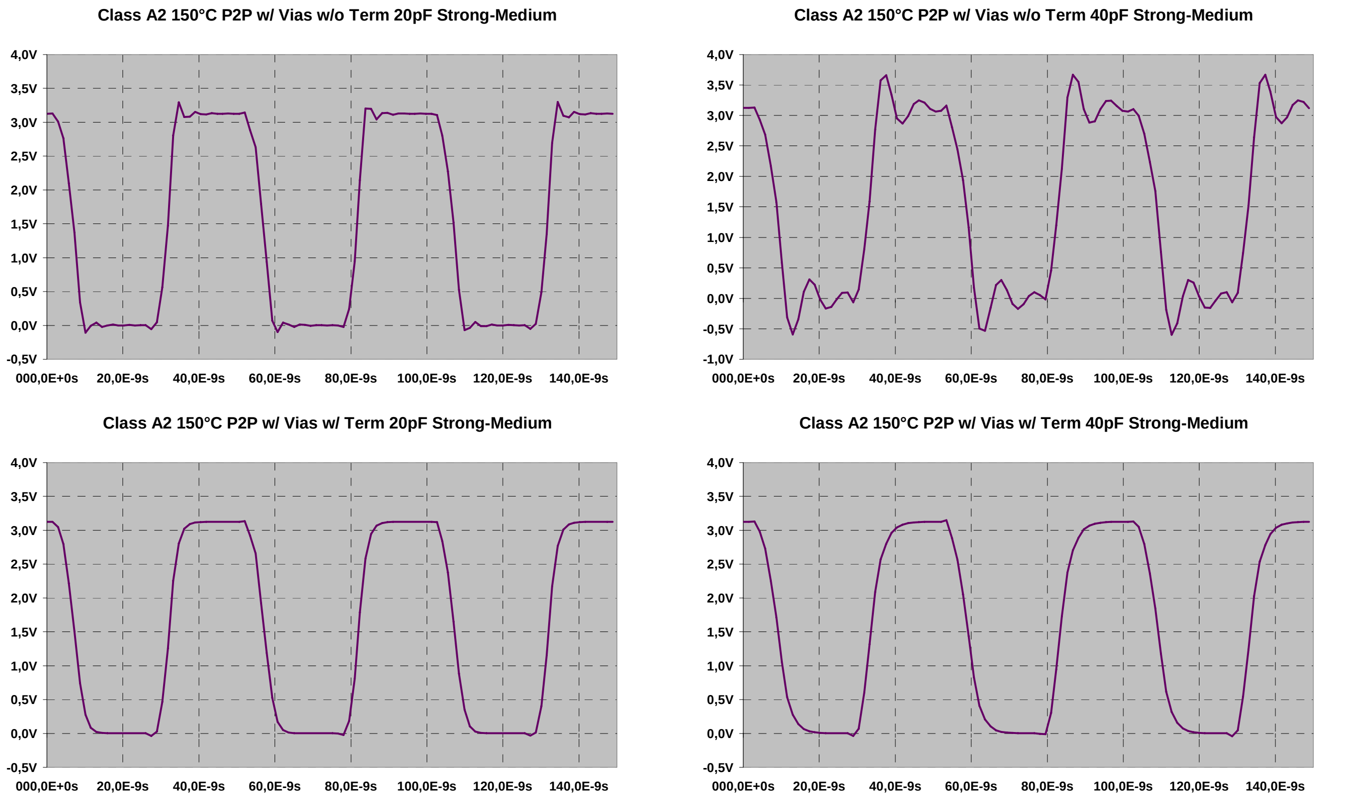


Figure 145: Waveforms Class A2 20 MHz “Strong-Medium” / “Point-to-Point” at 150°C ambient temper.

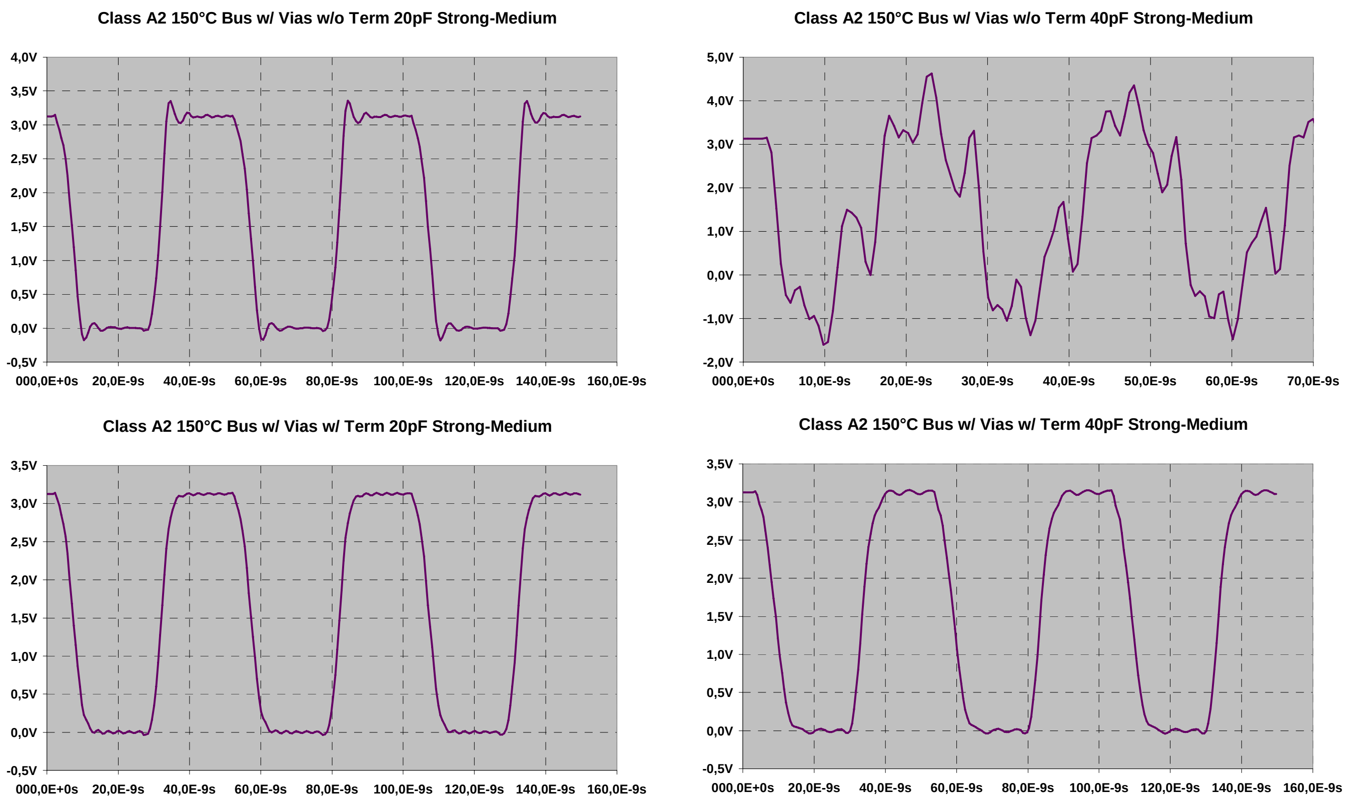


Figure 146: Waveforms Class A2 20 MHz “Strong-Medium” / “Bus” at 150°C ambient temper.

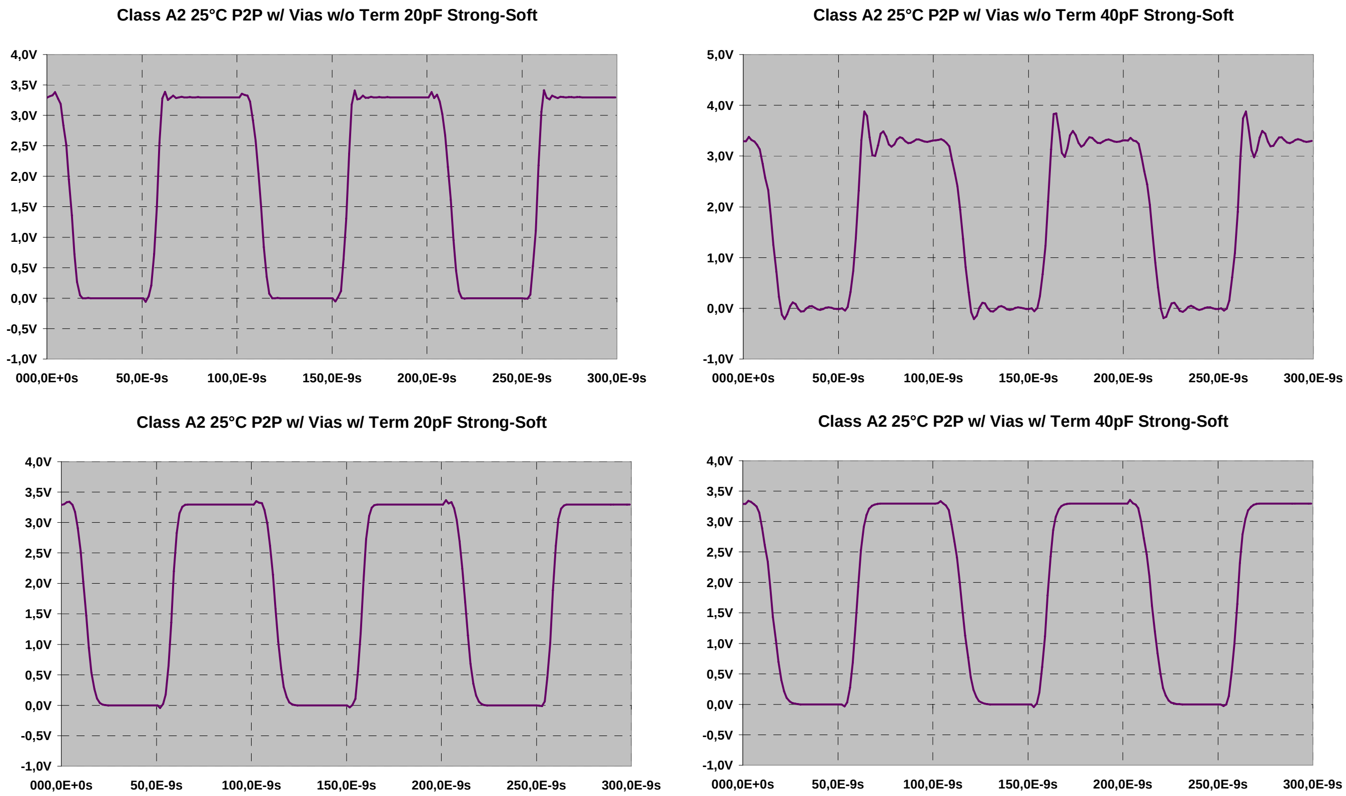


Figure 147: Waveforms Class A2 10 MHz “Strong-Soft” / “Point-to-Point” at 25°C ambient temper.

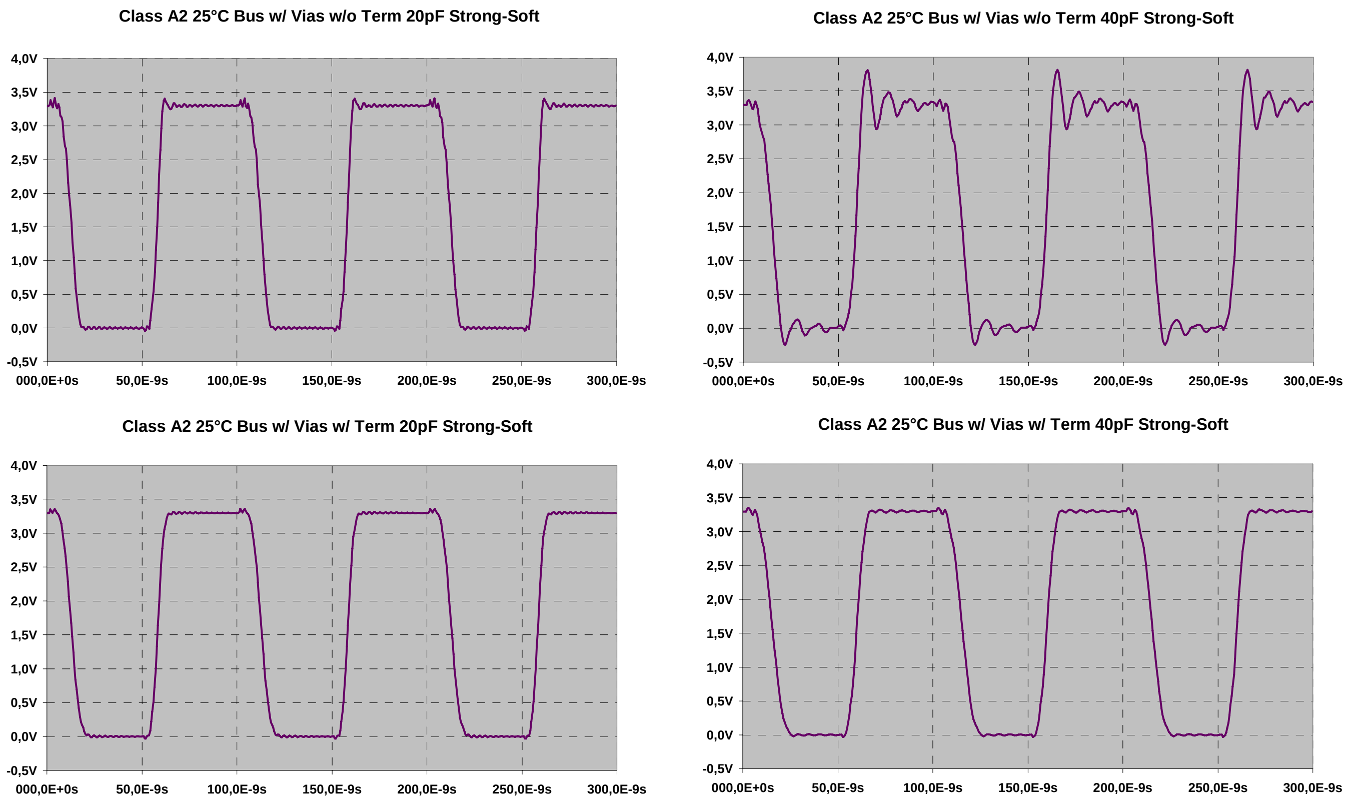


Figure 148: Waveforms Class A2 10 MHz “Strong-Soft” / “Bus” at 25°C ambient temper.

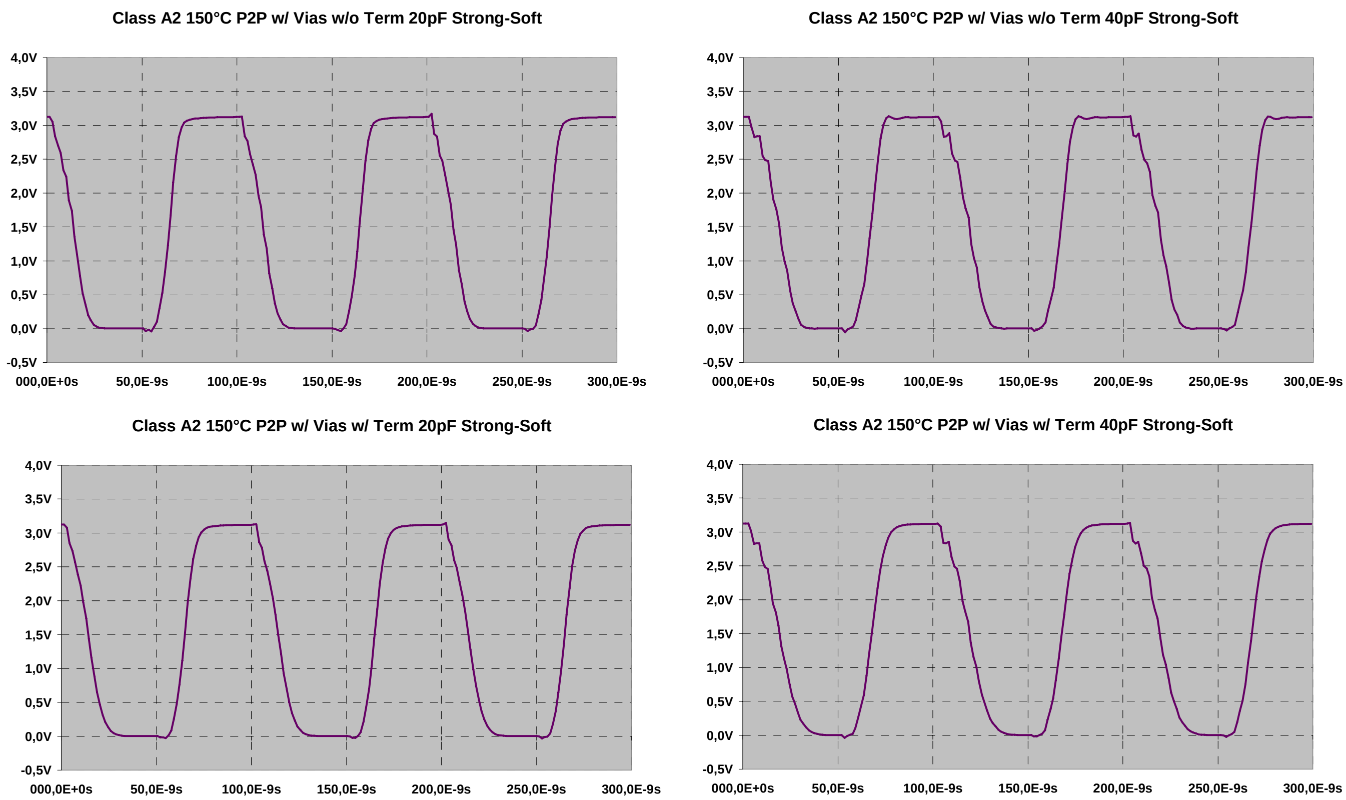


Figure 149: Waveforms Class A2 10 MHz “Strong-Soft” / “Point-to-Point” at 150°C ambient temper.

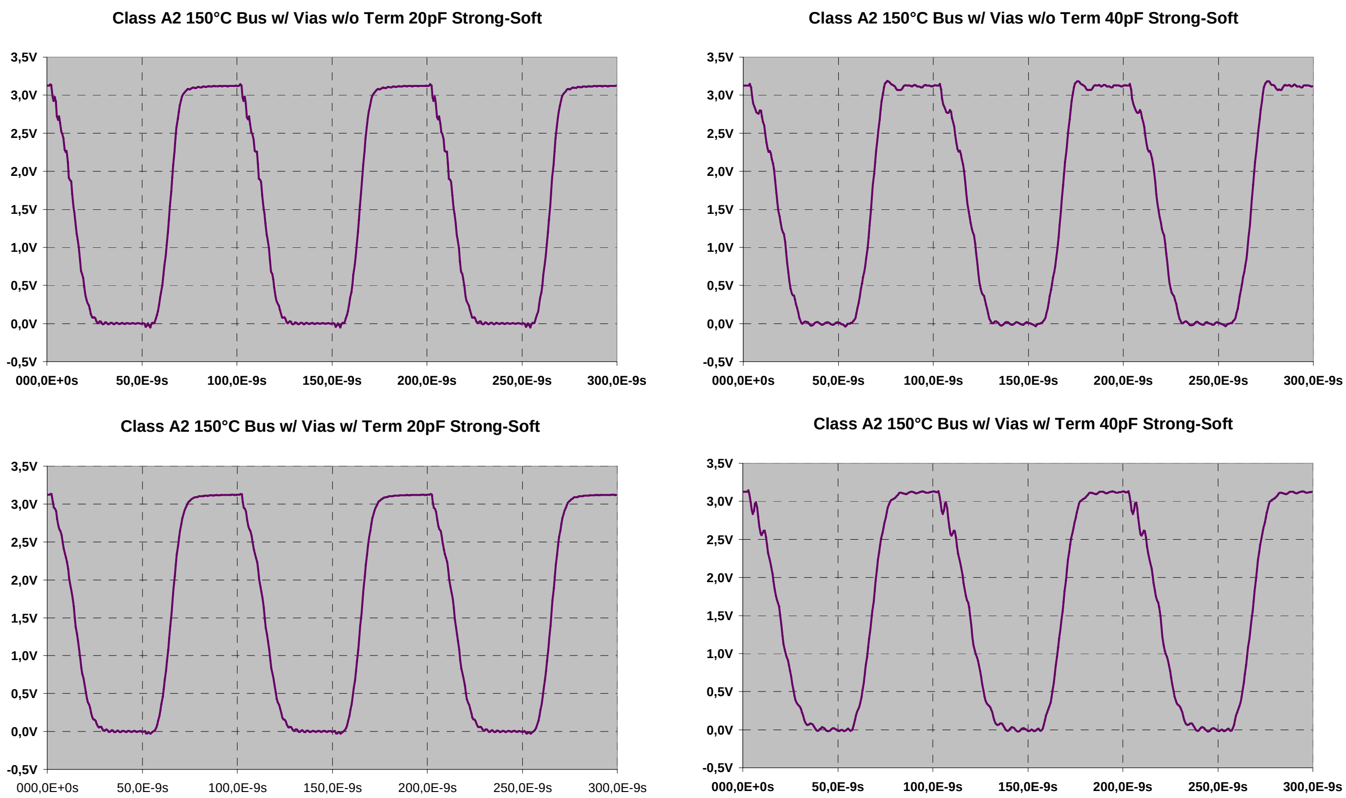


Figure 150: Waveforms Class A2 10 MHz “Strong-Soft” / “Bus” at 150°C ambient temper.

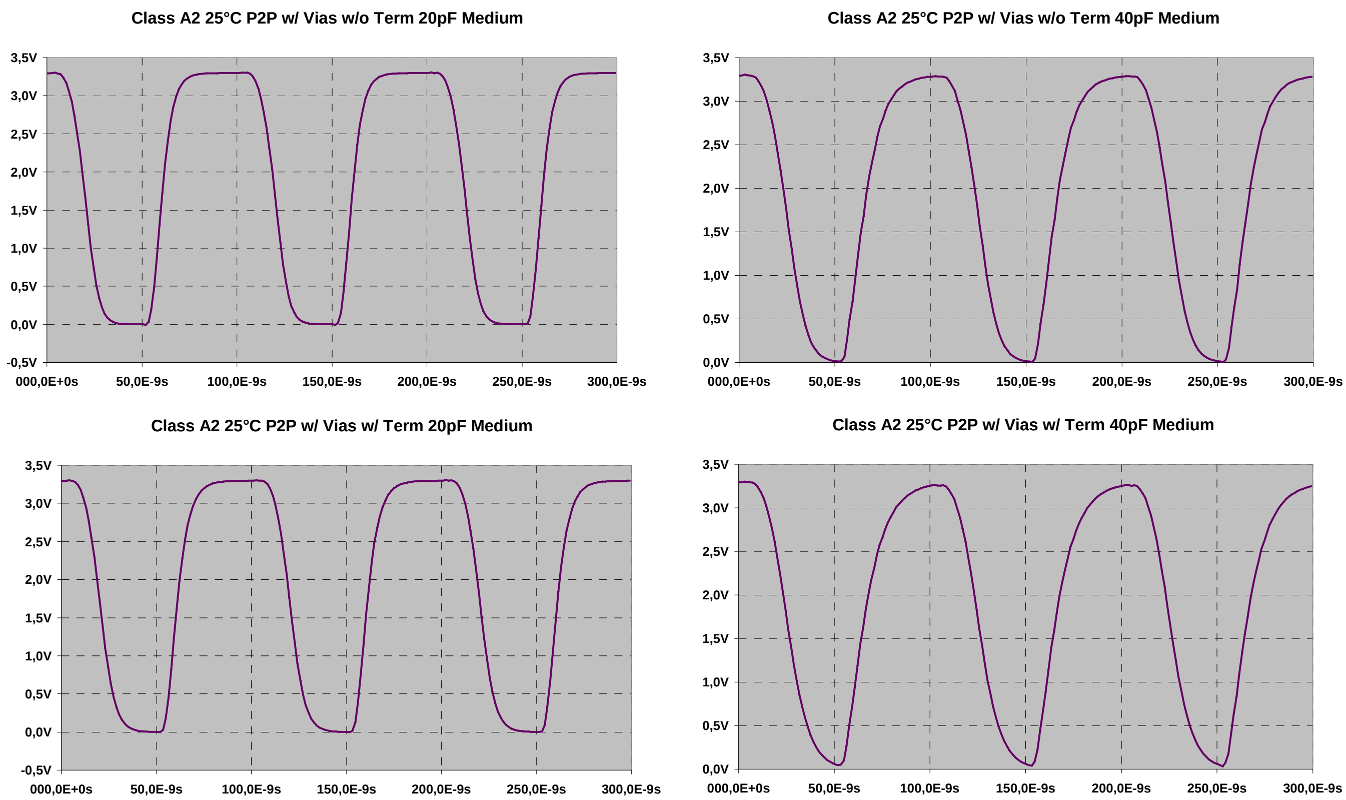


Figure 151: Waveforms Class A2 10 MHz “Medium” / “Point-to-Point” at 25°C ambient temper.

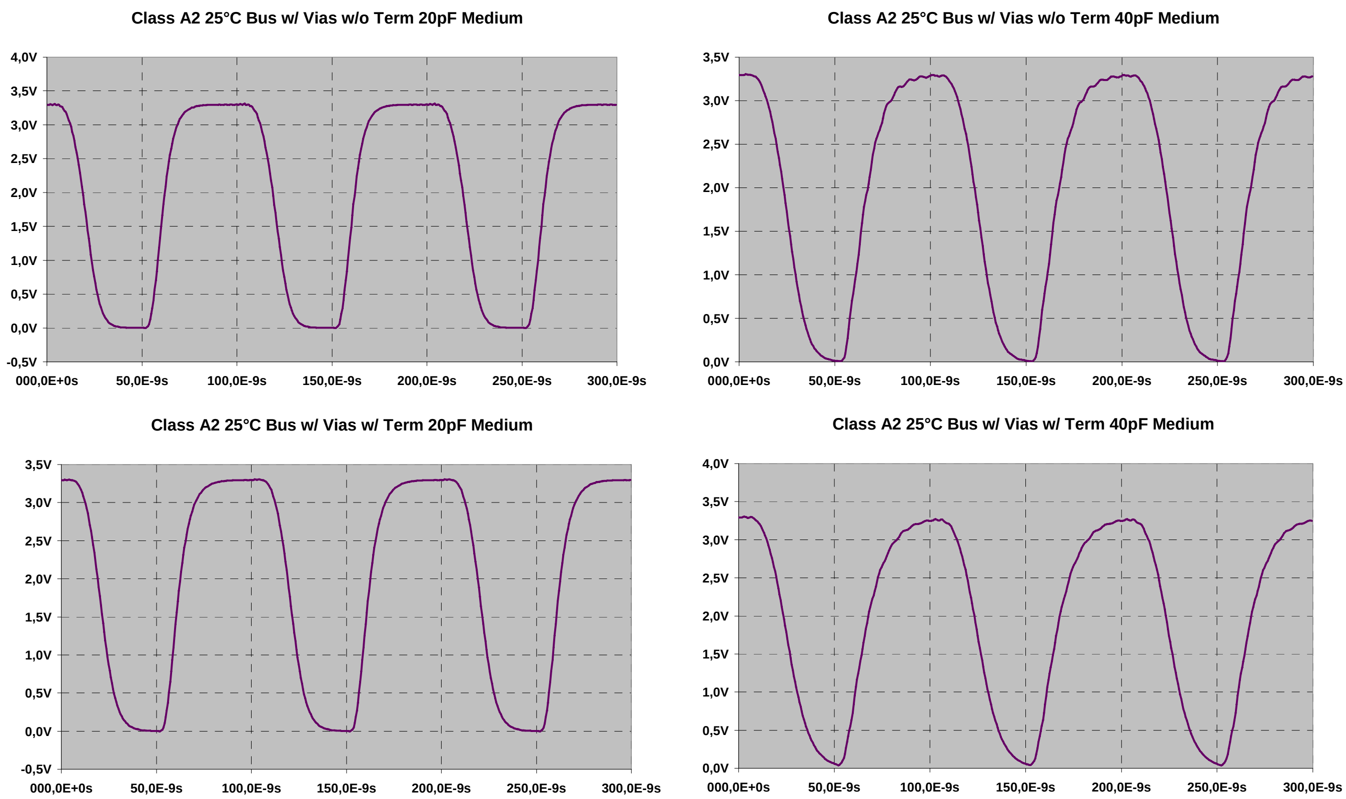


Figure 152: Waveforms Class A2 10 MHz “Medium” / “Bus” at 25°C ambient temper.

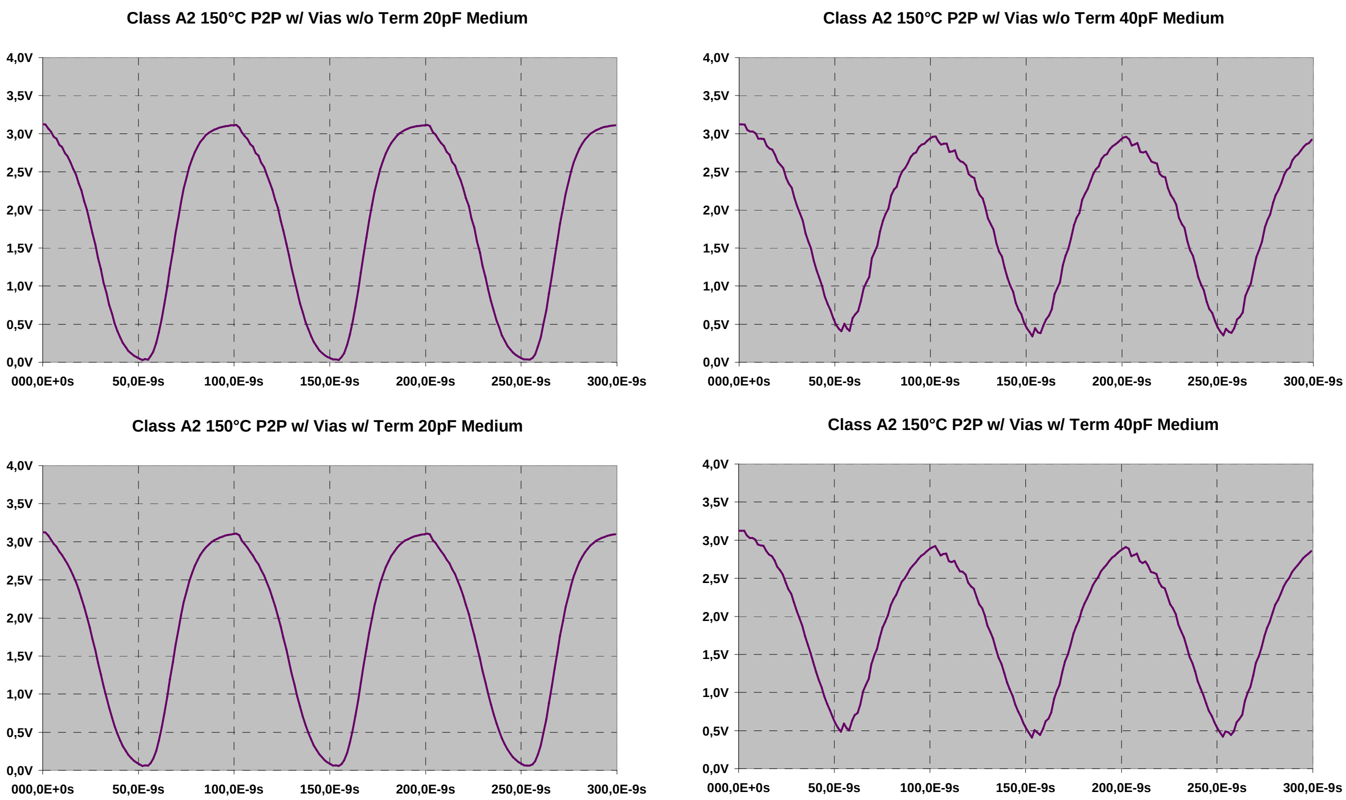


Figure 153: Waveforms Class A2 10 MHz “Medium” / “Point-to-Point” at 150°C ambient temper.

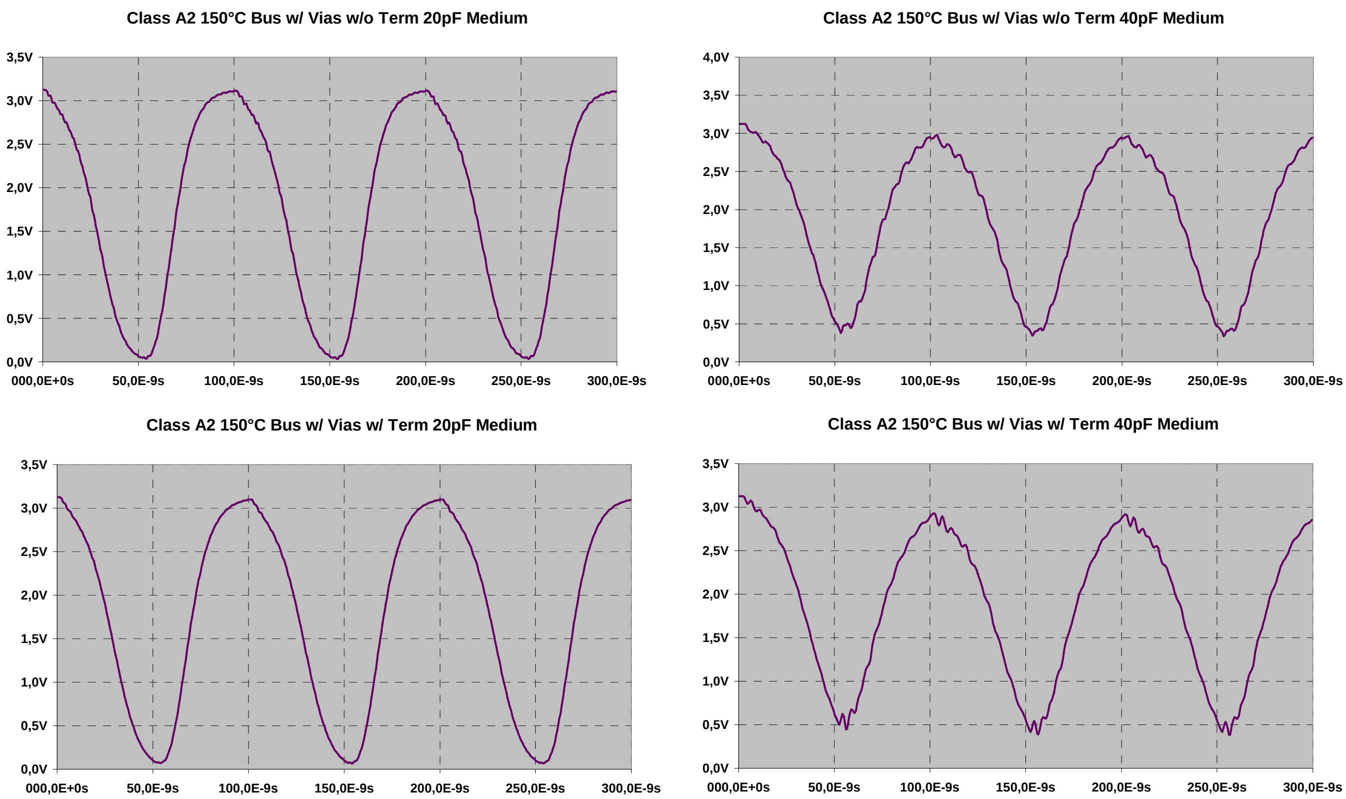


Figure 154: Waveforms Class A2 10 MHz “Medium” / “Bus” at 150°C ambient temper.

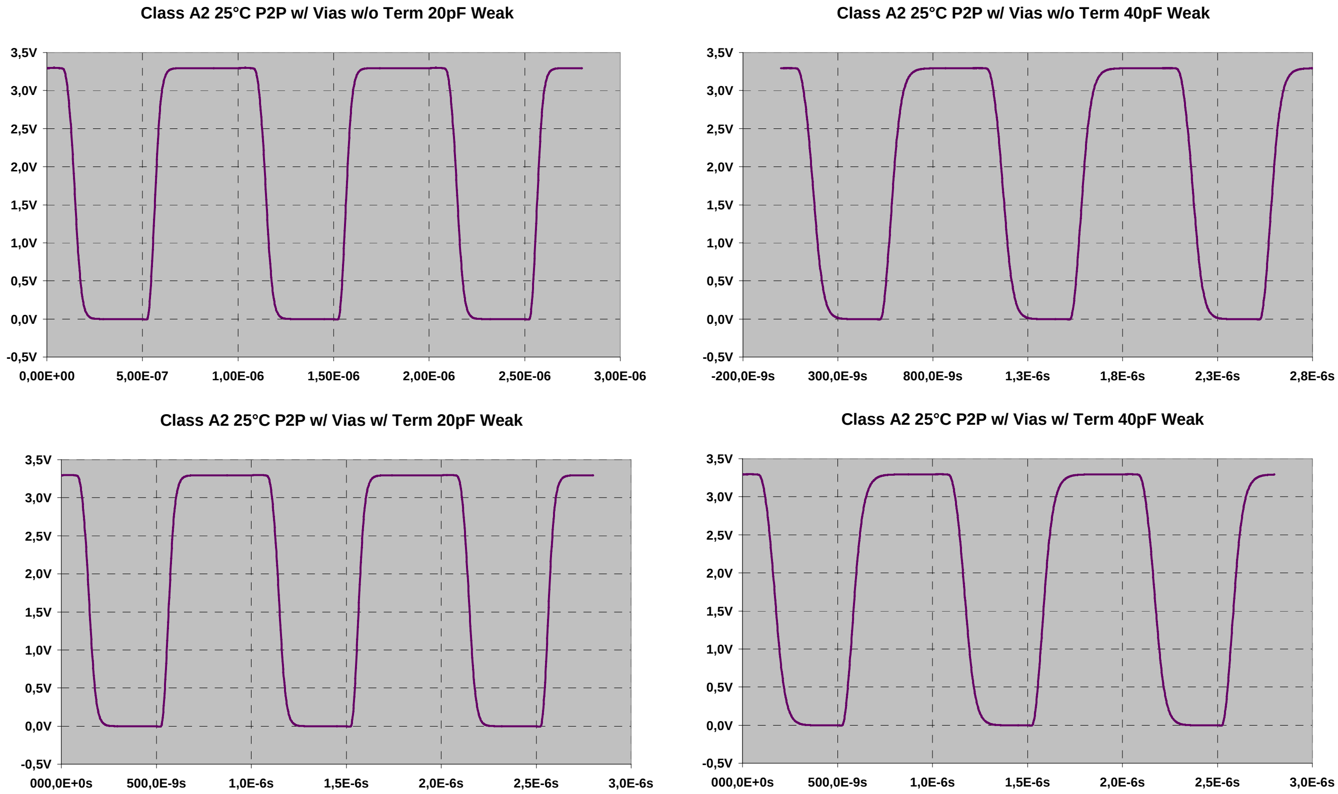


Figure 155: Waveforms Class A2 1 MHz “Weak” / “Point-to-Point” at 25°C ambient temper.

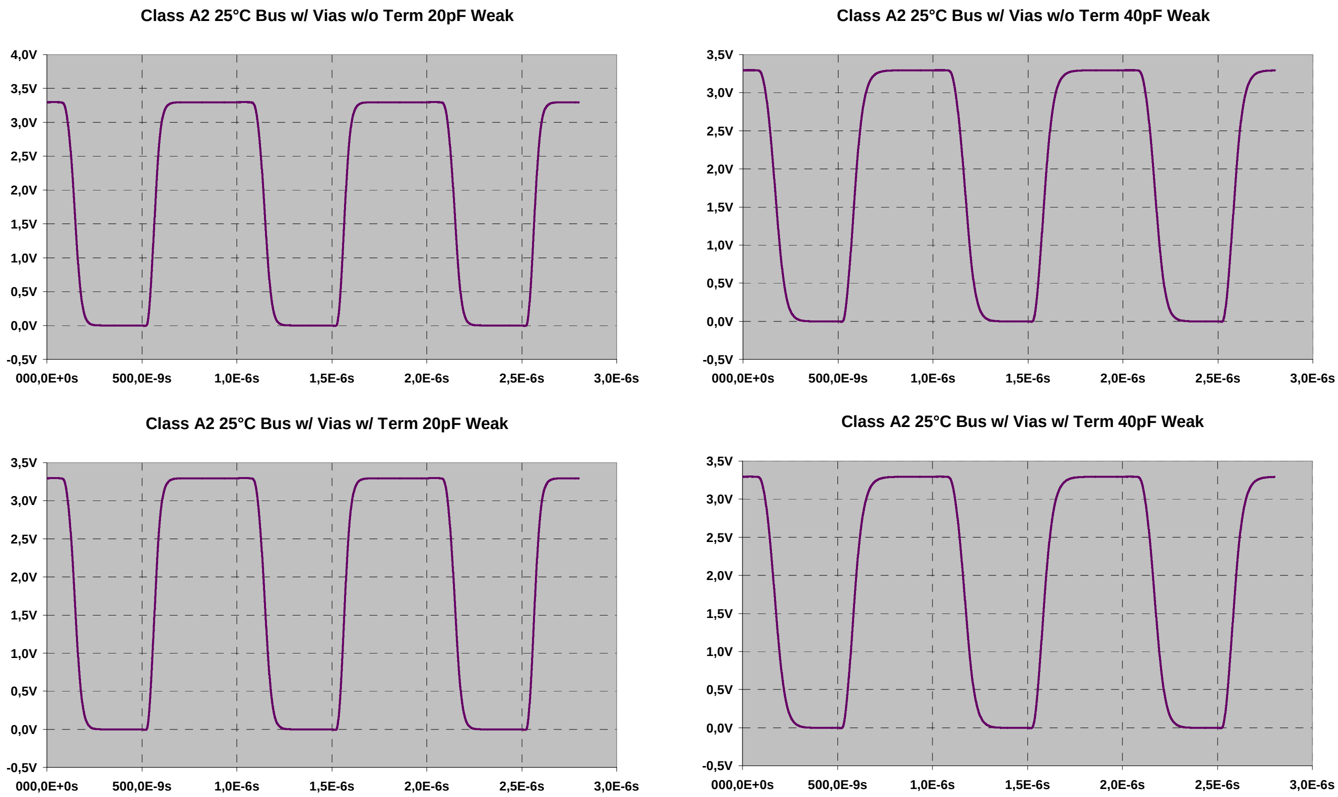


Figure 156: Waveforms Class A2 1 MHz “Weak” / “Bus” at 25°C ambient temper.

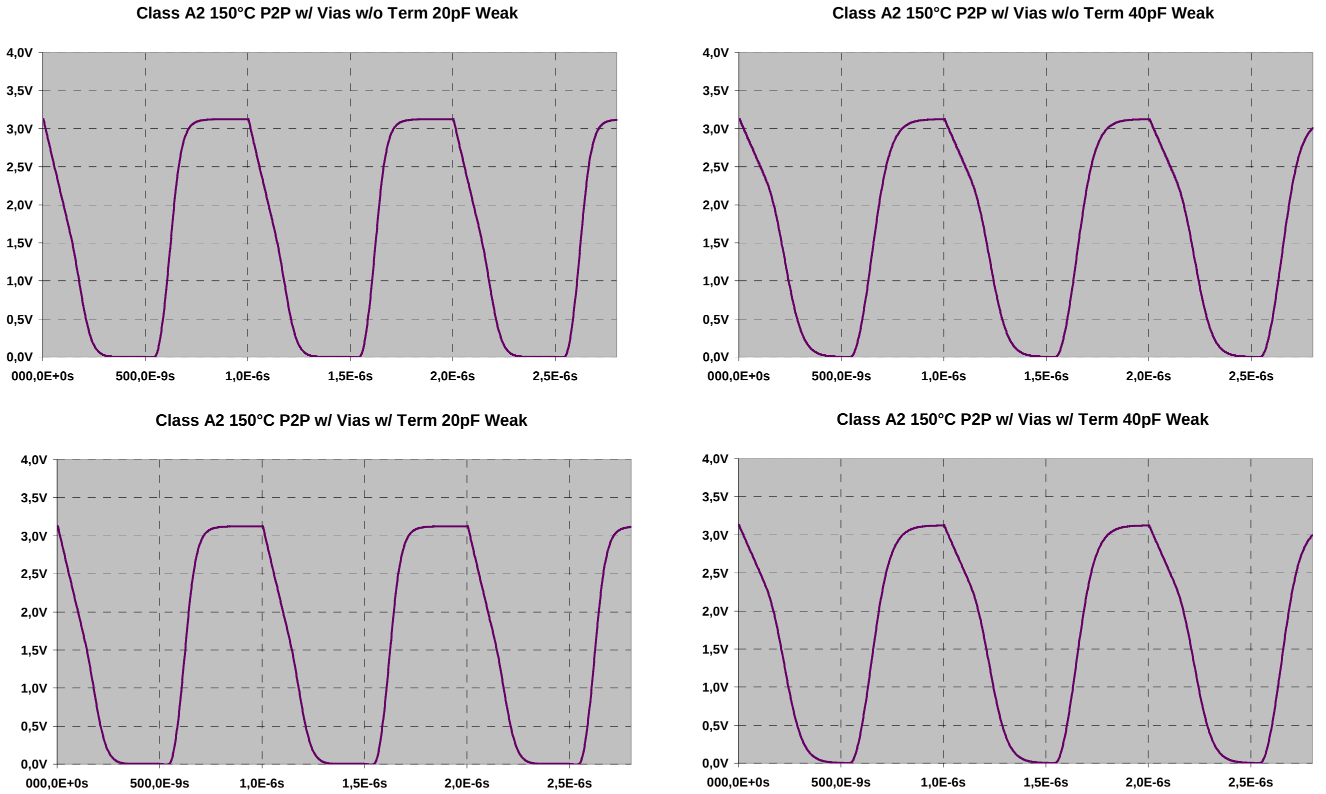


Figure 157: Waveforms Class A2 1 MHz “Weak” / “Point-to-Point” at 150°C ambient temper.

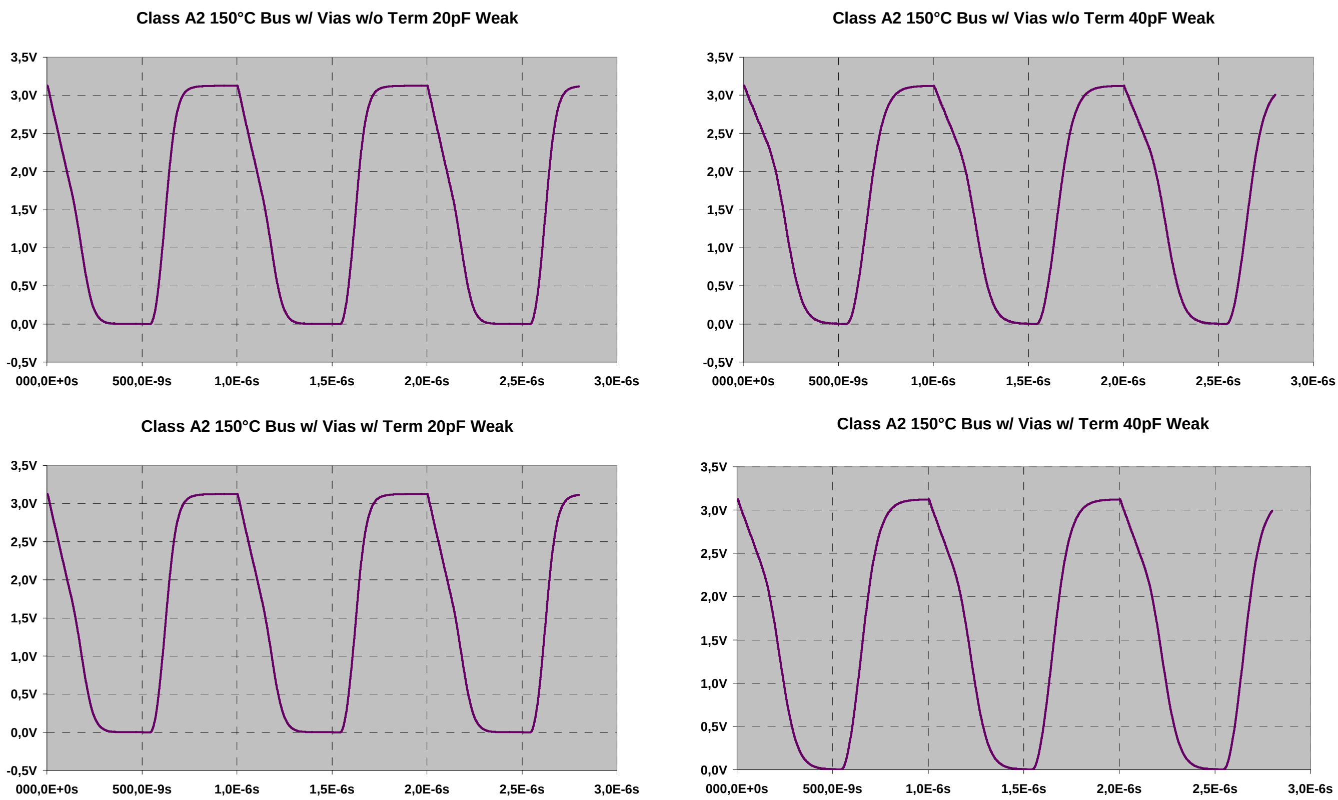


Figure 158: Waveforms Class A2 1 MHz “Weak” / “Bus” at 150°C ambient temper.

5 Measured Electromagnetic Emission

In addition to signal integrity, the scaling of pad drivers helps to reduce electromagnetic emission (EME) caused by switching output pins. This is because slower signal edges produce less high frequency contents in the emission spectra.

The following rule should be obeyed when selecting pad driver strength:

Use the weakest/slowest driver setting which provides the required signal timing at worst-case operating conditions.

Worst-case operating conditions are:

- maximum ambient temperature (e.g. +125°C)
- minimum pad supply voltage (e.g. 3.13V)
- realistic capacitive output load (consider trace length, trace structure, connected receiver input loads)

To illustrate the benefits of driver scaling for low EME, some sample measurement results are provided.

The measurements have been performed under two operating conditions:

Operating condition:
Port 2 toggling at low data rate with capacitive loads of 0pF, 10pF, 22pF, 33pF, 47pF.
Core running in idle loop.
Conducted emission measured at pad supply (VDDP) and core supply (VDDC) according to chapter 5.1.1.
Radiated emission measured in mini-TEM cell according to chapter 5.1.2.

Please note that all emission peaks visible between 900 MHz and 1000 MHz result from cellular phone activity and should be ignored when assessing the IC-related emission.

5.1 Description of test equipment

5.1.1 Conducted emission test configuration

Conducted emission is measured using the standardized 150Ω network, see Fig. 91. This network is used for both port and power supply emission measurements. For reference purpose, only the emission measured at the supply domains VDDP (3.3V pad supply) and VDDC (1.5V core supply) are documented. Emission reduction can be observed in a similar way on passive (i.e. non-switching) pad pins.

150Ω networks are provided for conducted emission measurements according IEC 61967 part 4 and BISS emission test specification.

For the measurements the probing points shown in Fig. 159 connected to VDD1 (is VDDC) and VDD2 (is VDDP) are used. No testing was performed at passive I/Os.

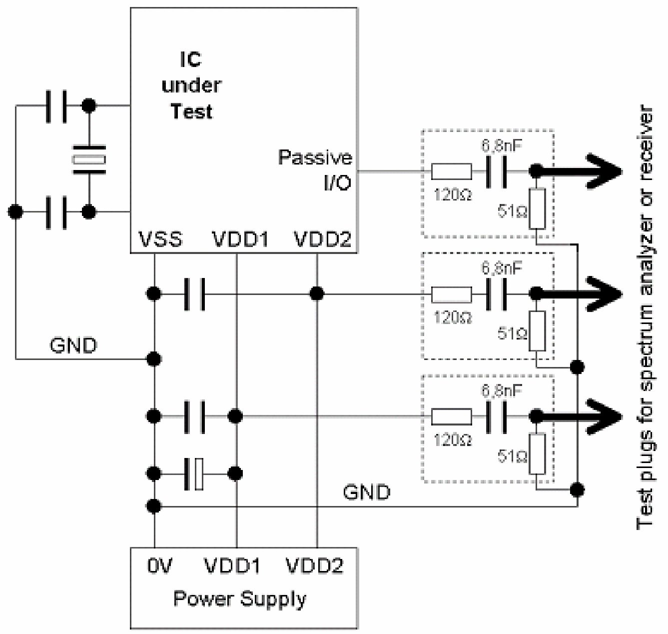


Figure 159: Conducted emission probing points

5.1.2 Radiated emission test configuration

Radiated emission is measured using the standard Mini TEM Cell according IEC 61967 part 2 and BISS emission test specification. The frequency range is from 150kHz to 1000MHz.

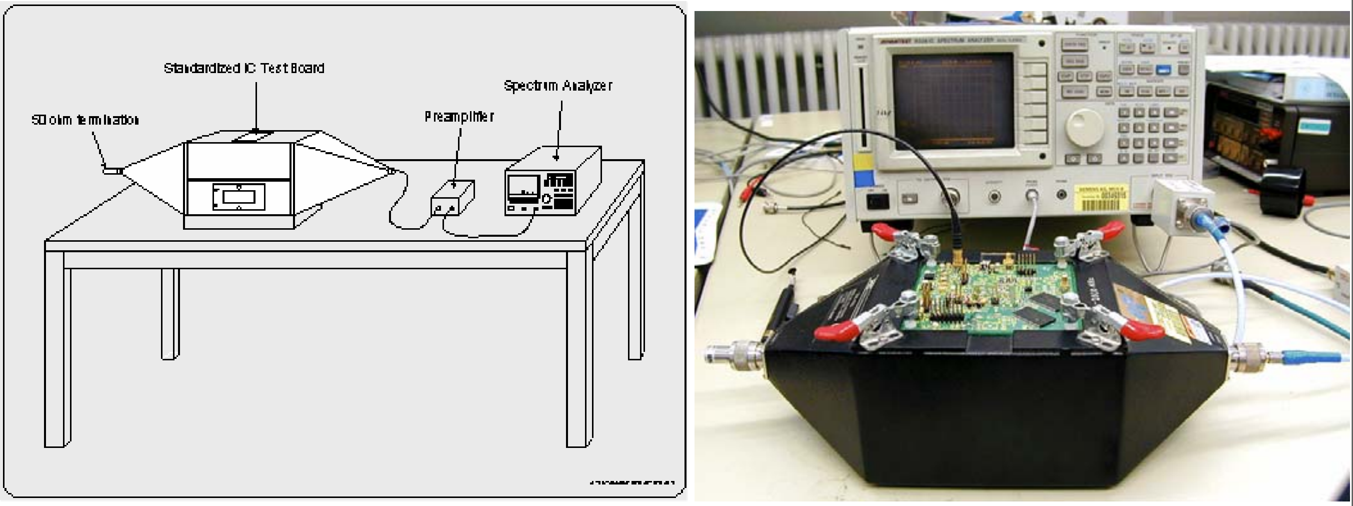


Figure 160: Radiated emission test setup

5.1.3 Instruments and software for emission data recognition

Spectrum analyzer:	Rohde&Schwarz FSP7 (9kHz ... 7GHz)
	Start frequency: 150kHz
	Stop frequency: 1001MHz
	Frequency step: 1.0MHz
	Span: 1.3MHz
	Attenuation: none
	Detector type: Max. peak
	RBW: 10kHz
	VBW: 3kHz
Measurement time:	For all measurements, the emission measurement time (10ms) at one frequency is longer than the test software loop duration.
Pre-Amplifier:	none
Data generation software:	National Instruments LabView: Measure Spectrum_VDE150Ohm_1.vi
	Infineon proprietary software for ASCII to Excel data conversion: DAT2XLS.exe, using vector addition of 0° and 90° oriented test board in case of radiated emission test.
Environment:	temperature 23°C ±5°C
Supply:	nominal voltage ±5%

For all measurements the noise floor is at least 6dB below the limit.

5.2 Emission measurement results

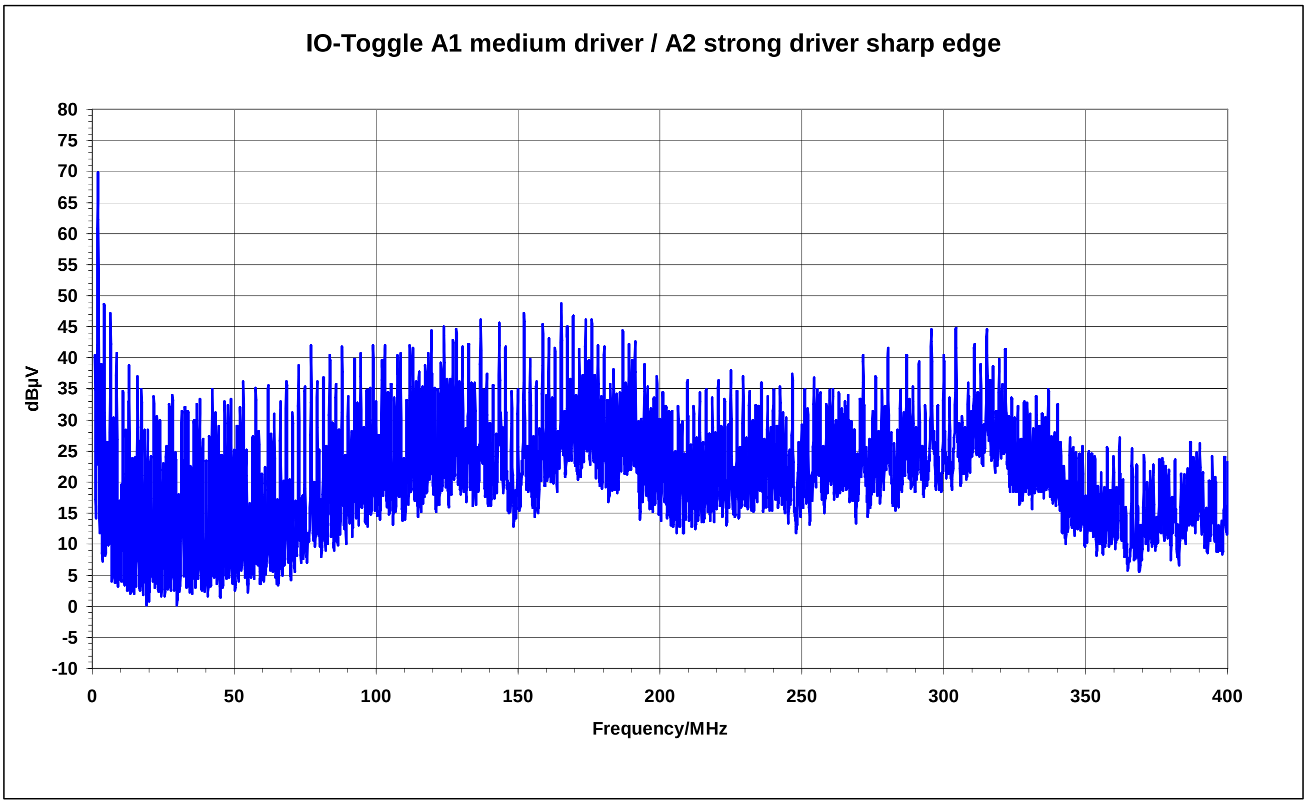


Figure 161: Class A1 “Medium” driver, Class A2 “Strong-Sharp” driver- conducted emission on VDDP

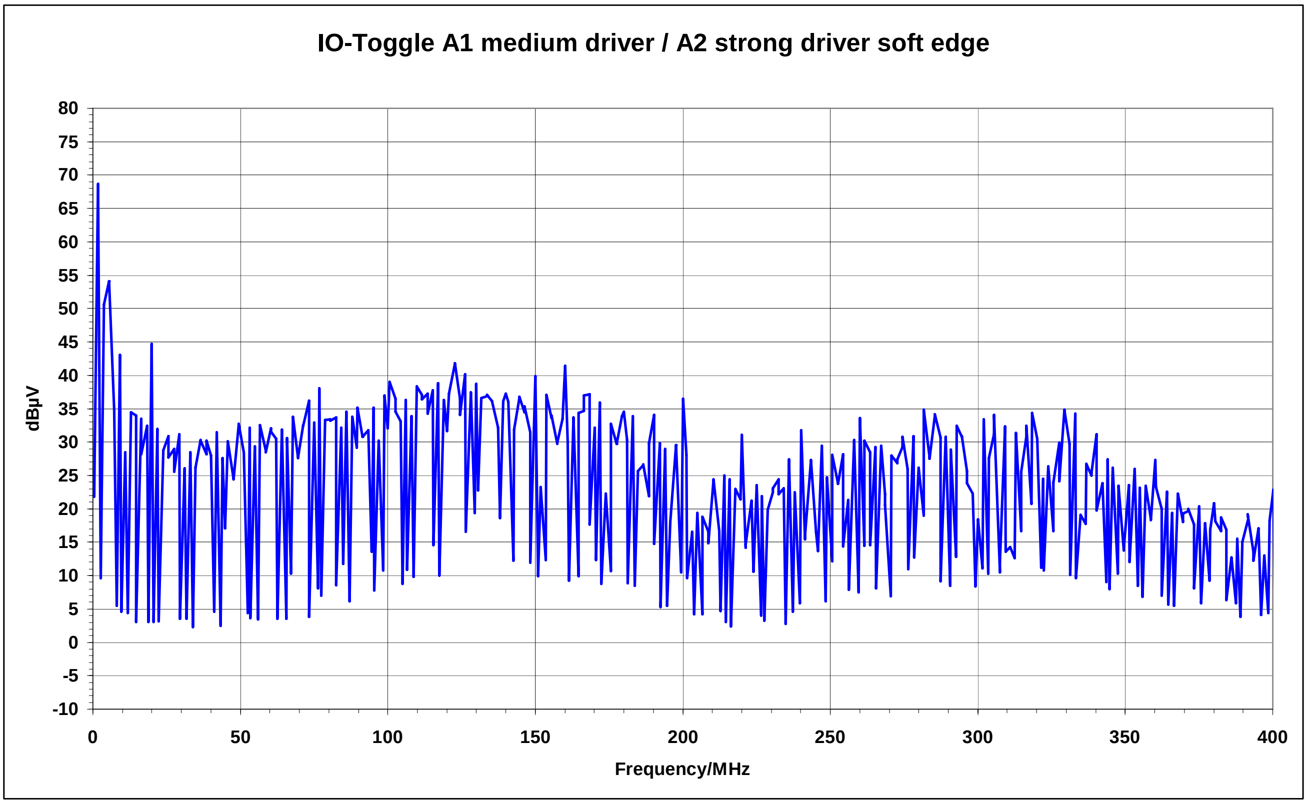


Figure 162: Class A1 “Medium” driver, Class A2 “Strong-Soft” driver- conducted emission on VDDP

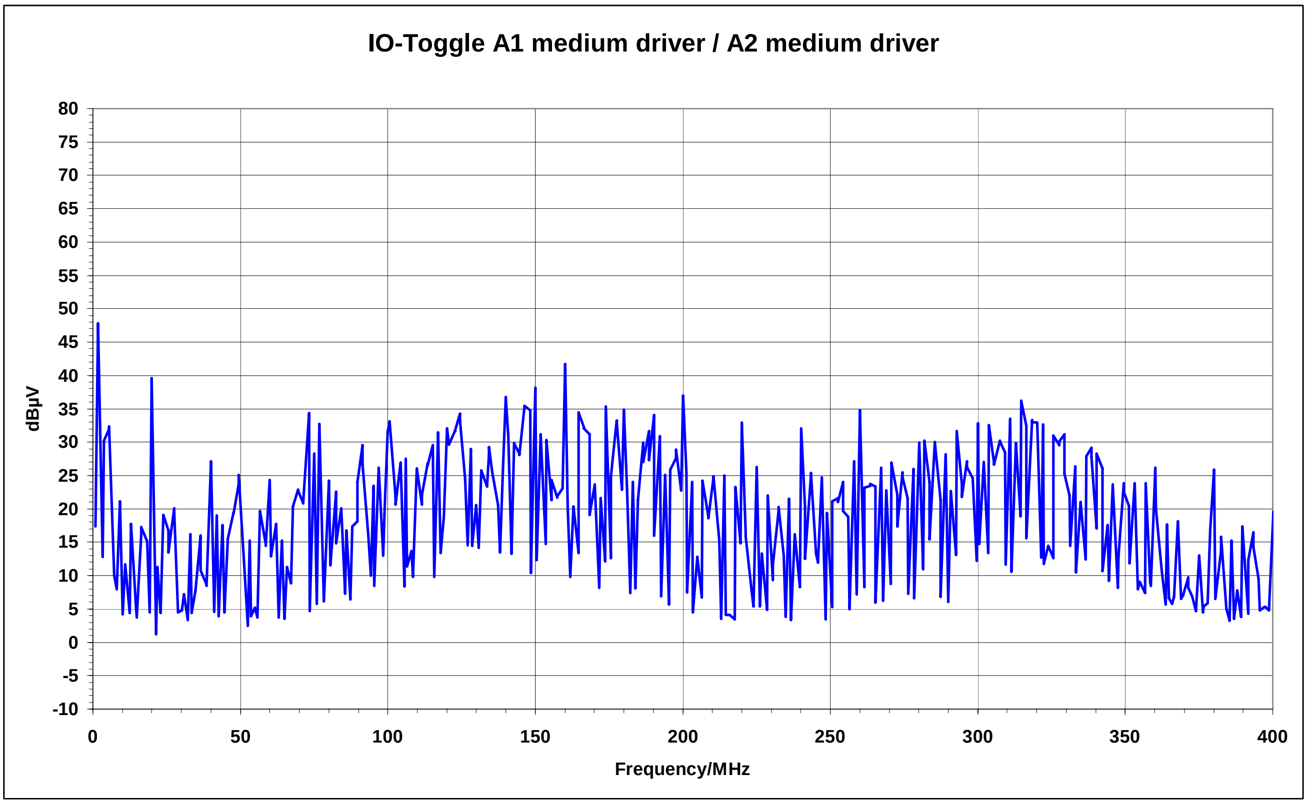


Figure 163: Class A1 "Medium" driver, Class A2 "Medium" driver- conducted emission on VDDP

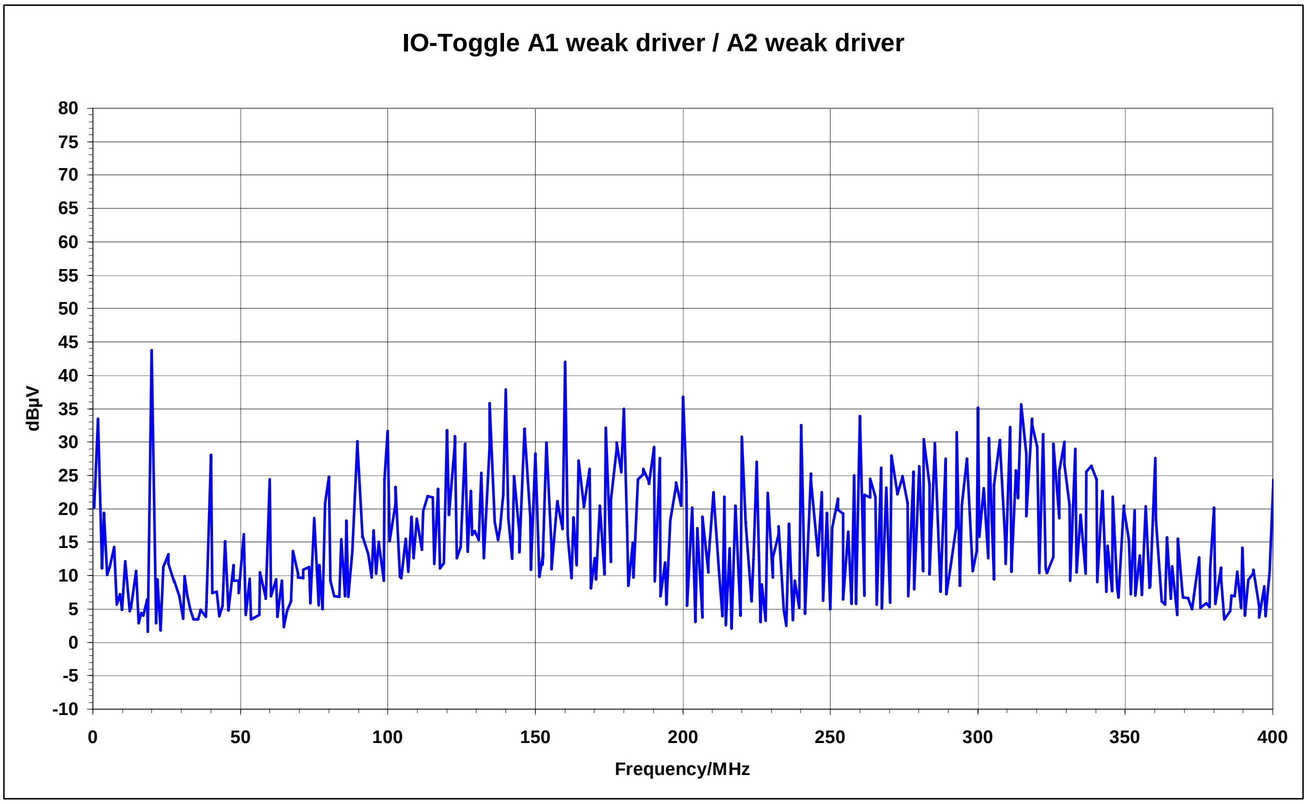


Figure 164: Class A1 "Medium" driver, Class A2 "Weak" driver- conducted emission on VDDP

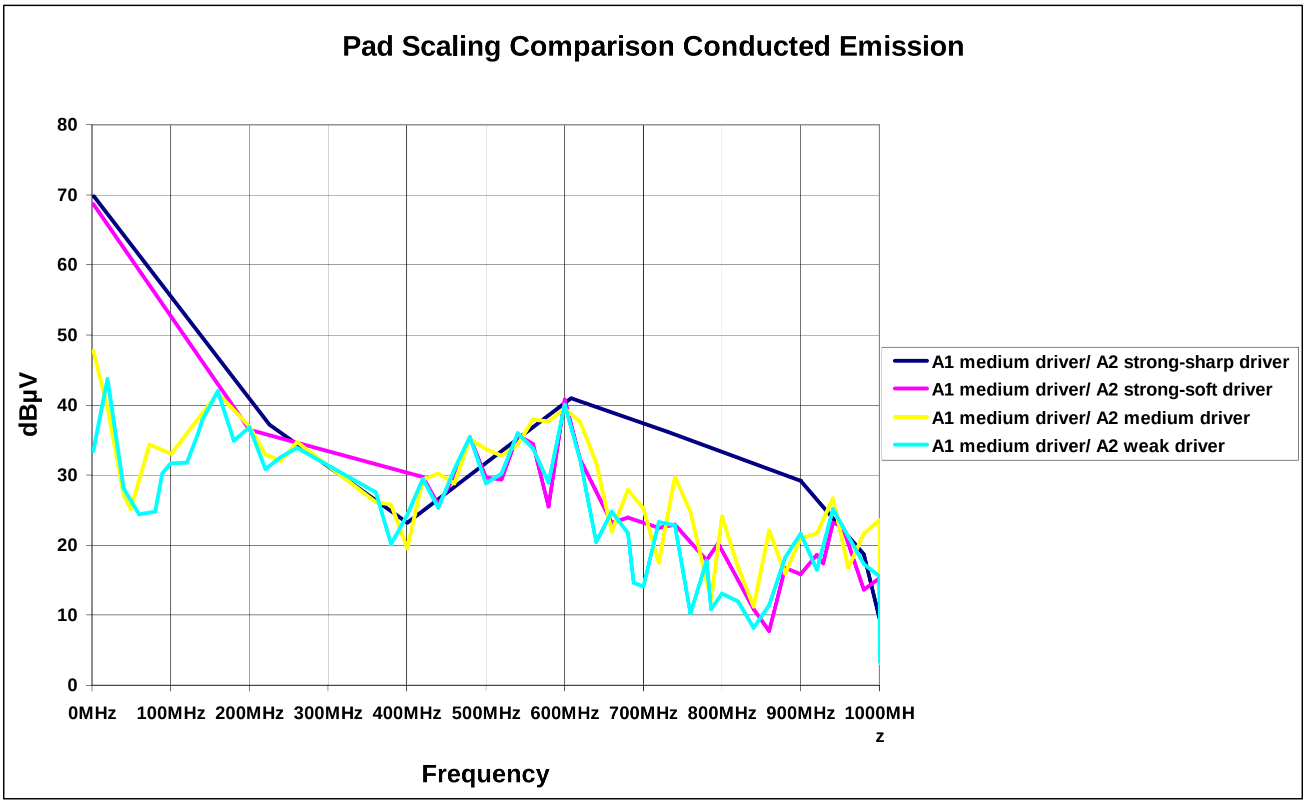


Figure 165: Pad scalingcomparison-conducted emission

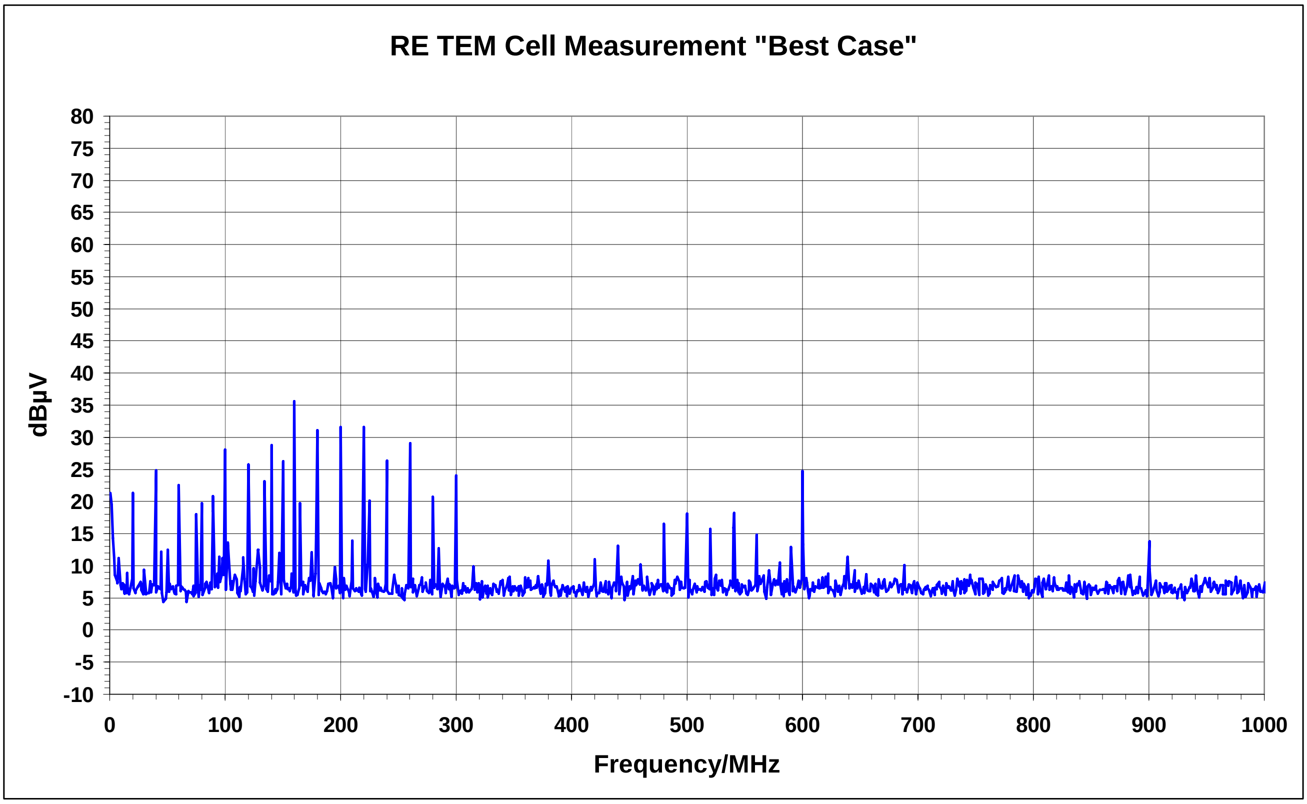


Figure 166: Class A2 “Best Case” at 0pF load – radiated emission

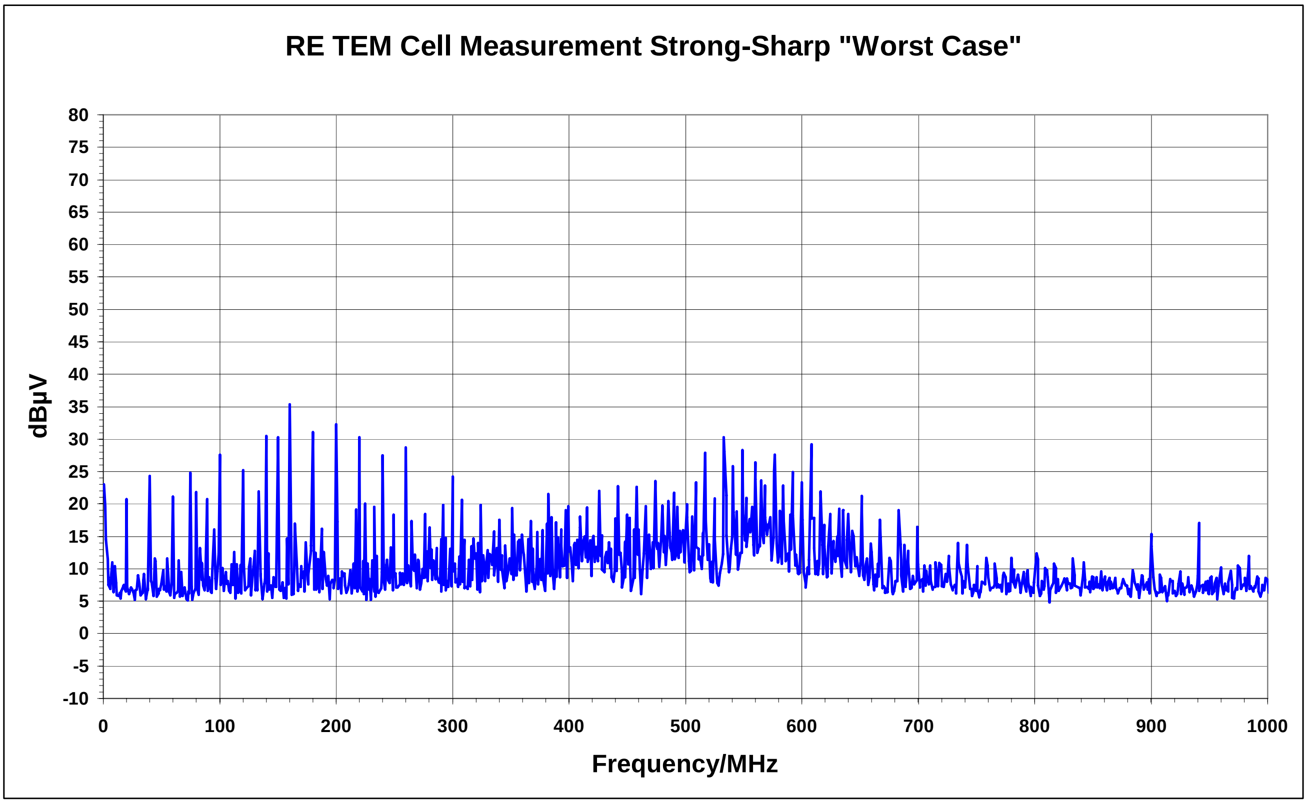


Figure 167: Class A2 "Strong-Sharp" driver at 0pF load – radiated emission

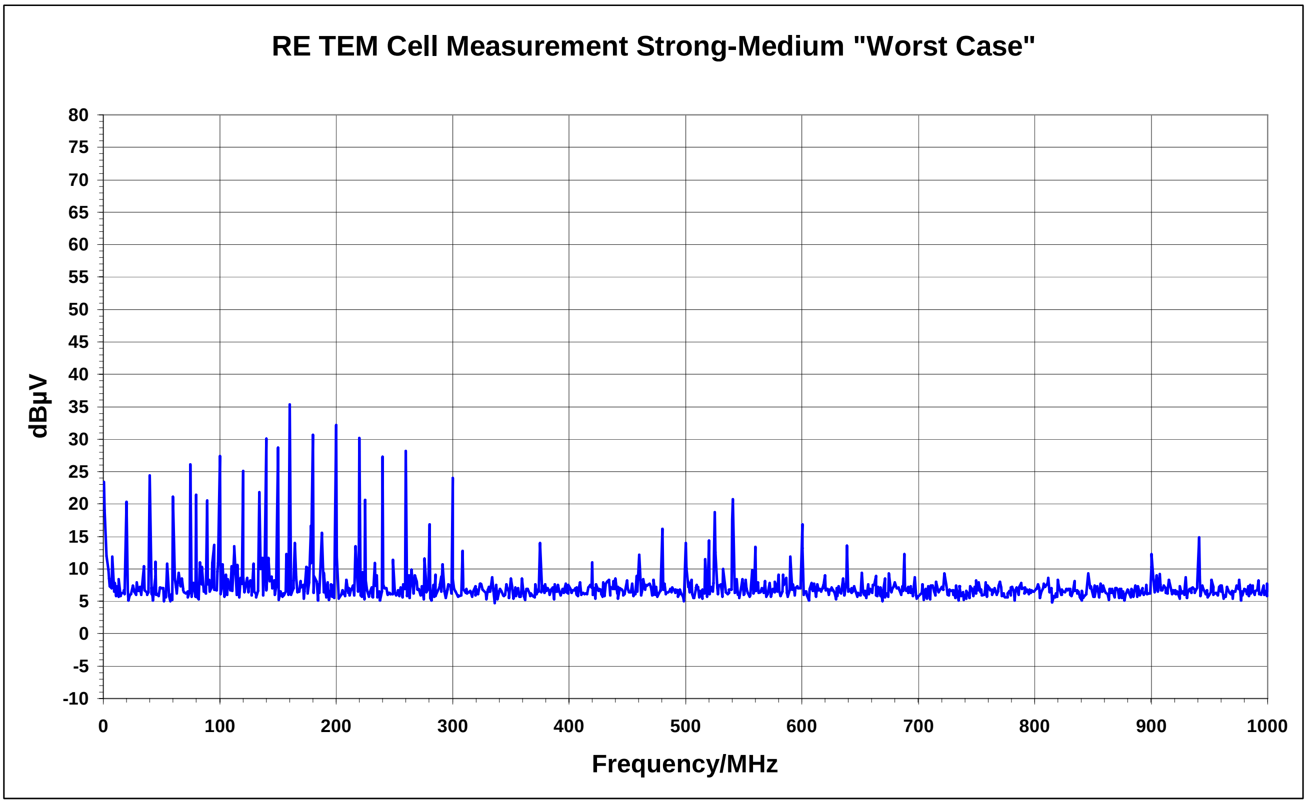


Figure 168: Class A2 "Strong-Medium" driver at 0pF load – radiated emission

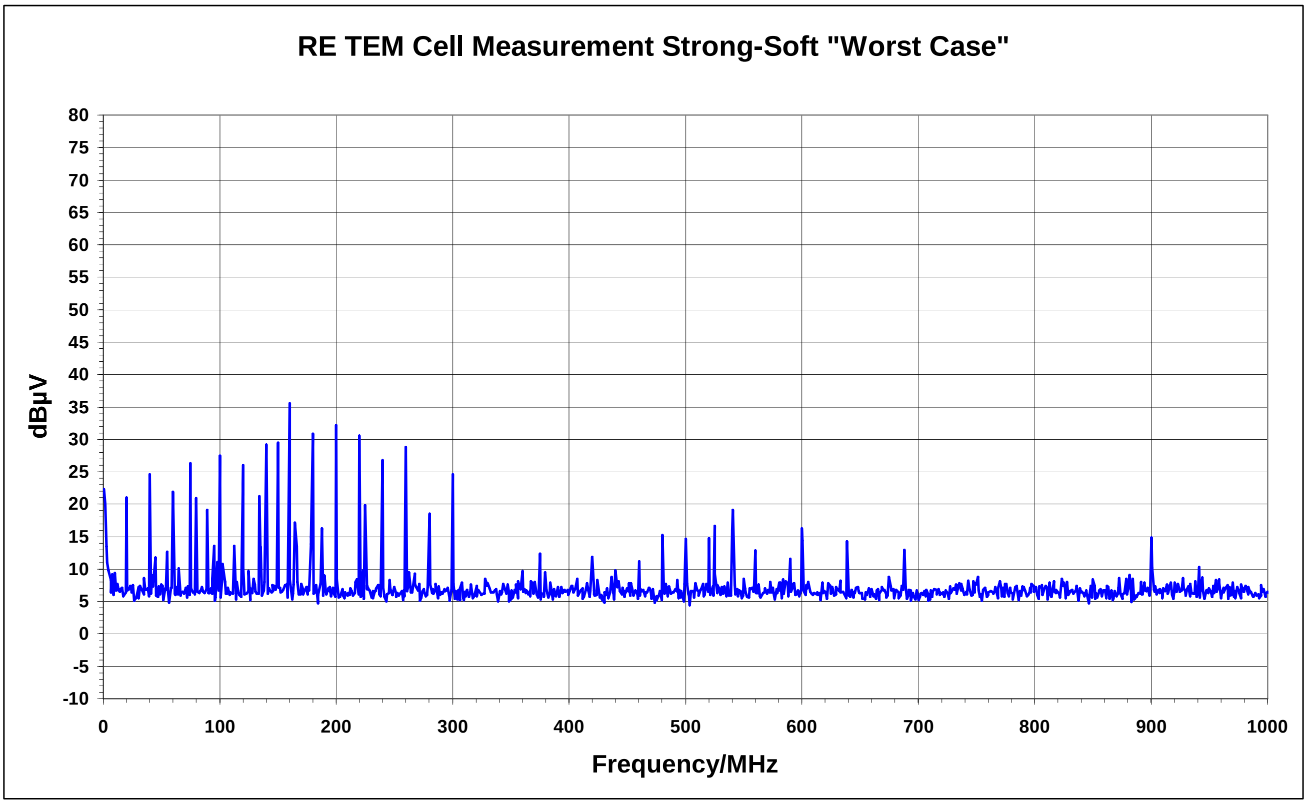


Figure 169: Class A2 "Strong-Soft" driver at 0pF load – radiated emission

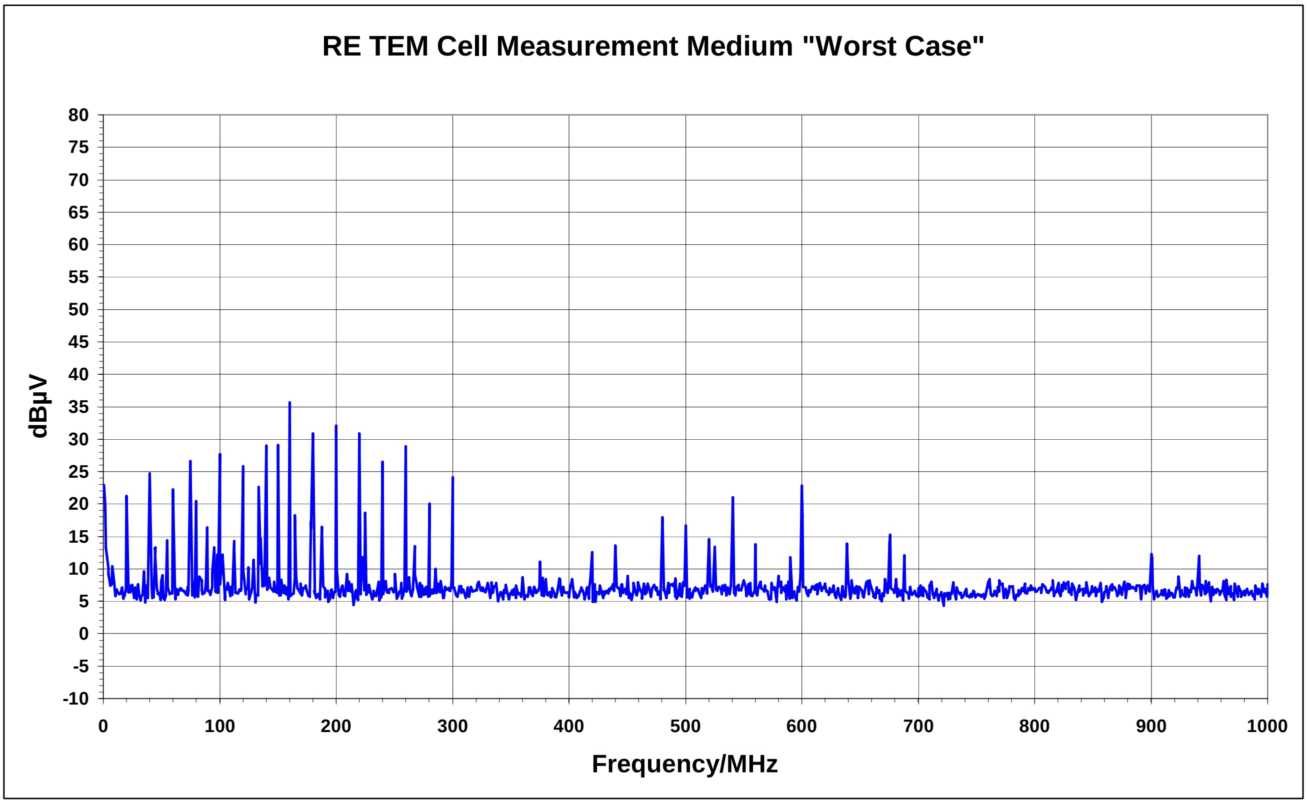


Figure 170: Class A2 "Medium" driver at 0pF load – radiated emission

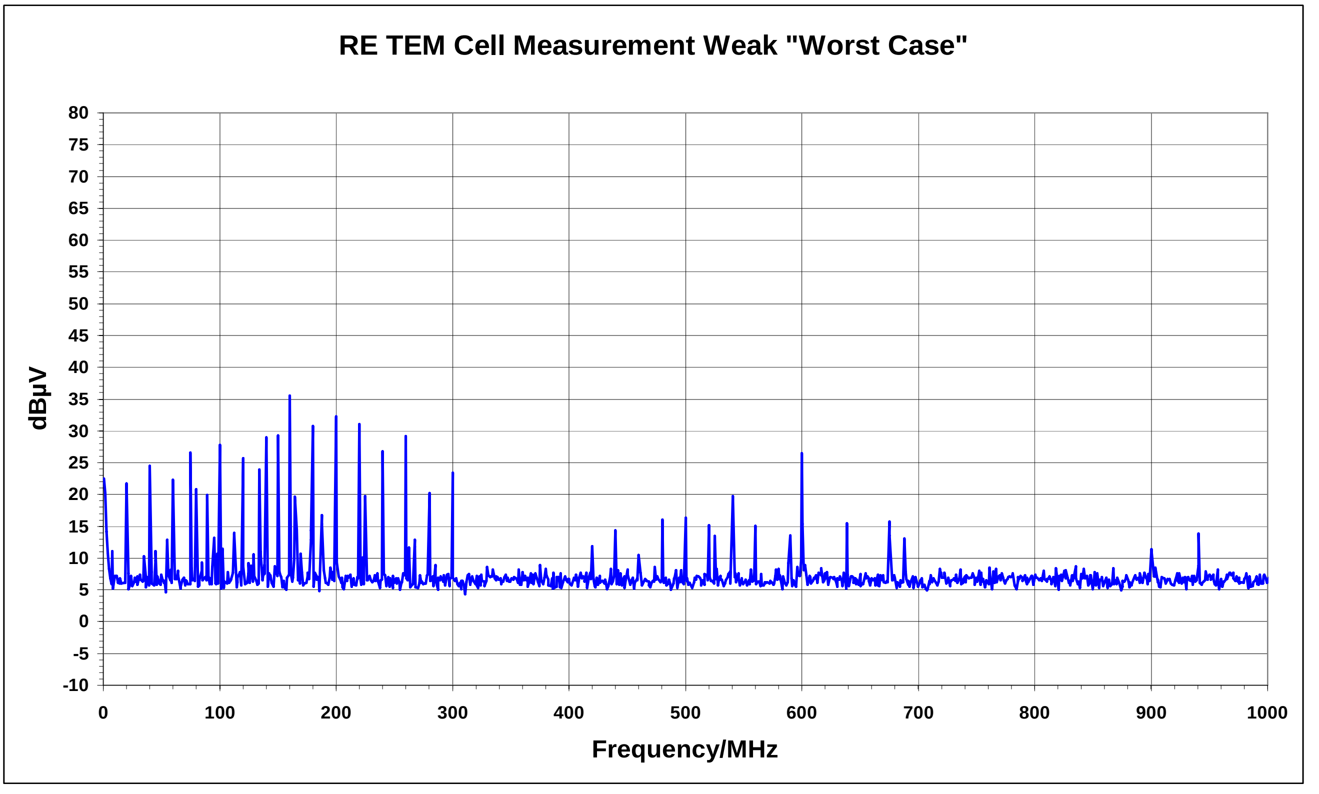


Figure 171: Class A2 “Weak” driver at 0pF load – radiated emission

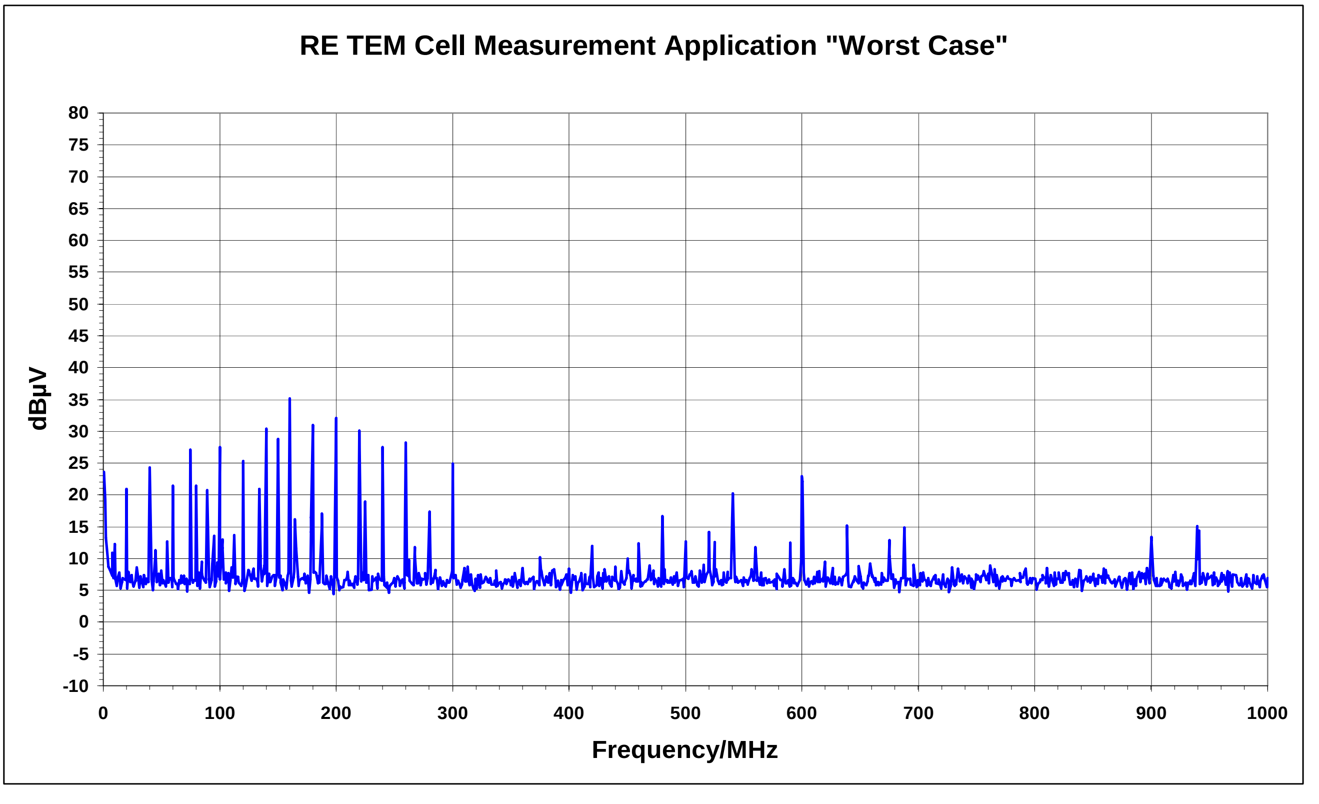


Figure 172: Class A2 “Application”at 0pF load – radiated emission

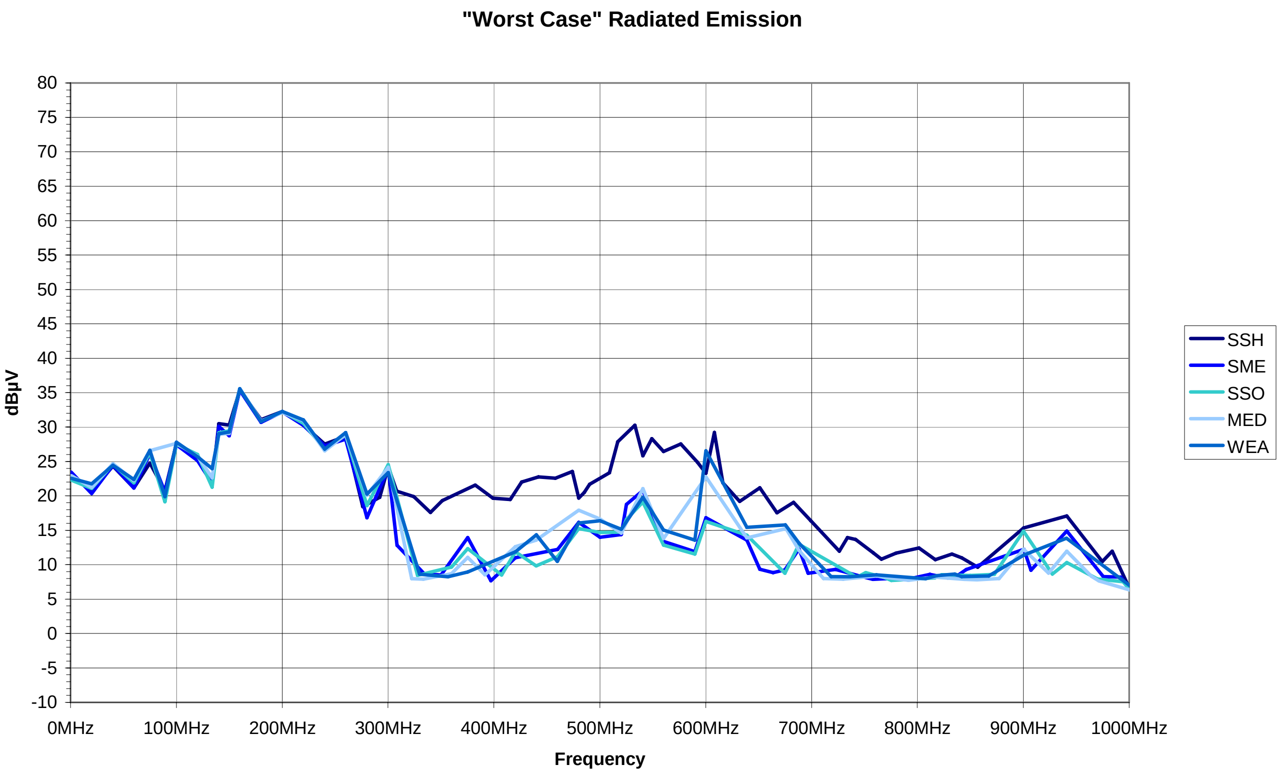


Figure 173a: Class A2; various driver settings at no load –radiated emission

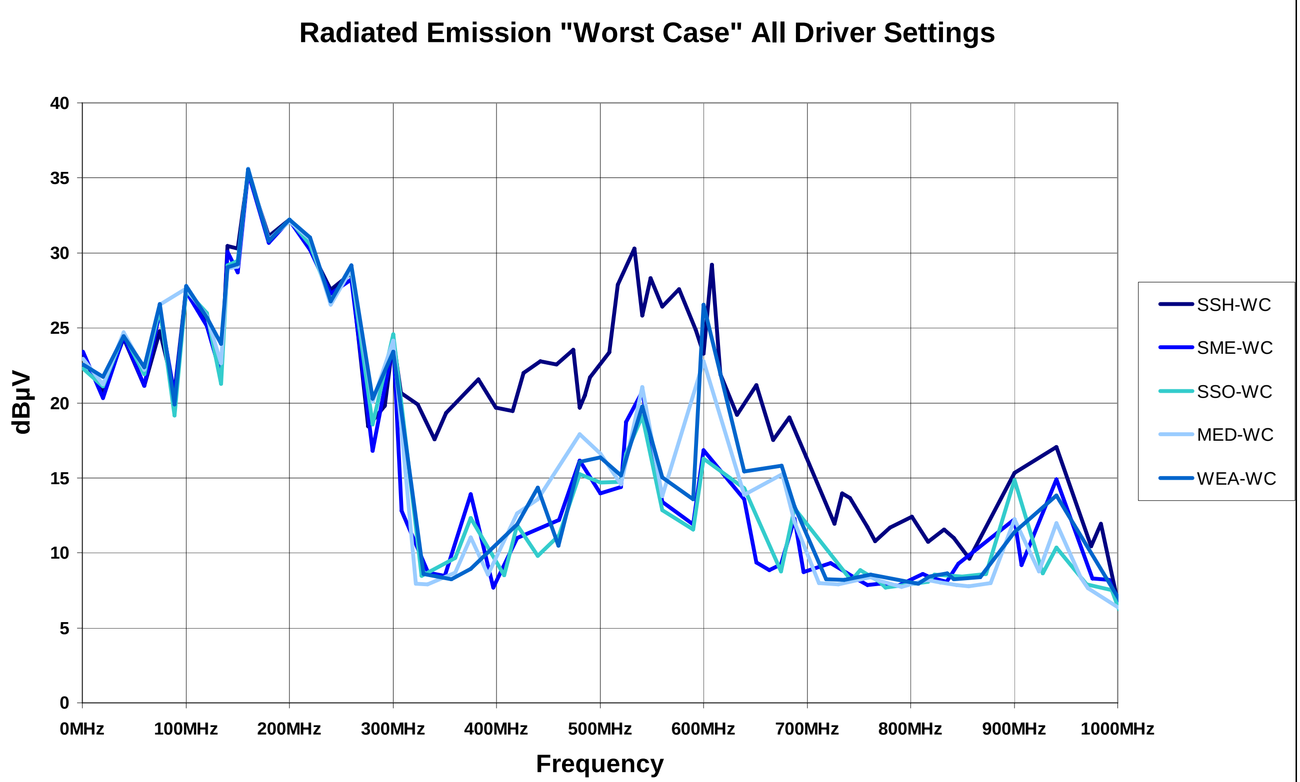


Figure 173b: Class A2; various driver settings at no load –radiated emission (zoomed)

6 Simulated Electromagnetic Emission

Since the various trace layout structures were not available for measurements, the emission diagrams in Fig. 174-189 have been calculated by Fast Fourier Transformation algorithms (FFT) from the simulated timings. Please note that the FFT calculation was done for active ports. One diagram contains the FFTs of several driver settings. As indicated by the timing waveform in chapter 4.1.3, different driver settings allow different data rates. The FFTs were calculated using these realistic data rates. This fact of different base frequencies explains why the knee-points on the envelope curves appear at different (harmonic) frequencies.

For this overview, only “point-to-point” and “bus” structures have been considered because there is no significant difference for “star” and “tree” structures.

Furthermore, the FFT calculation was restricted to room temperature which is the standard condition for emission measurements.

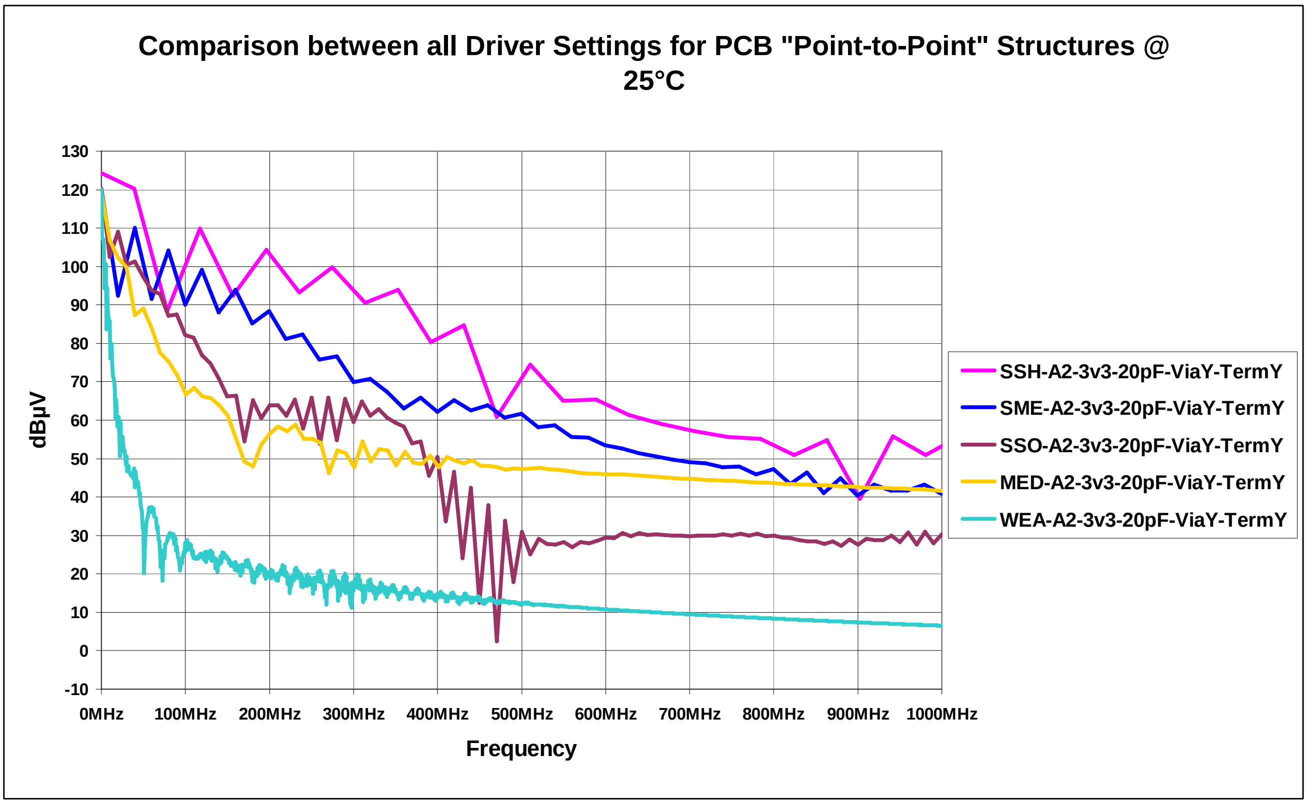


Figure 174: Class A2; various driver settings at 20pF load for "P2P" layout w/ Vias w/ Term

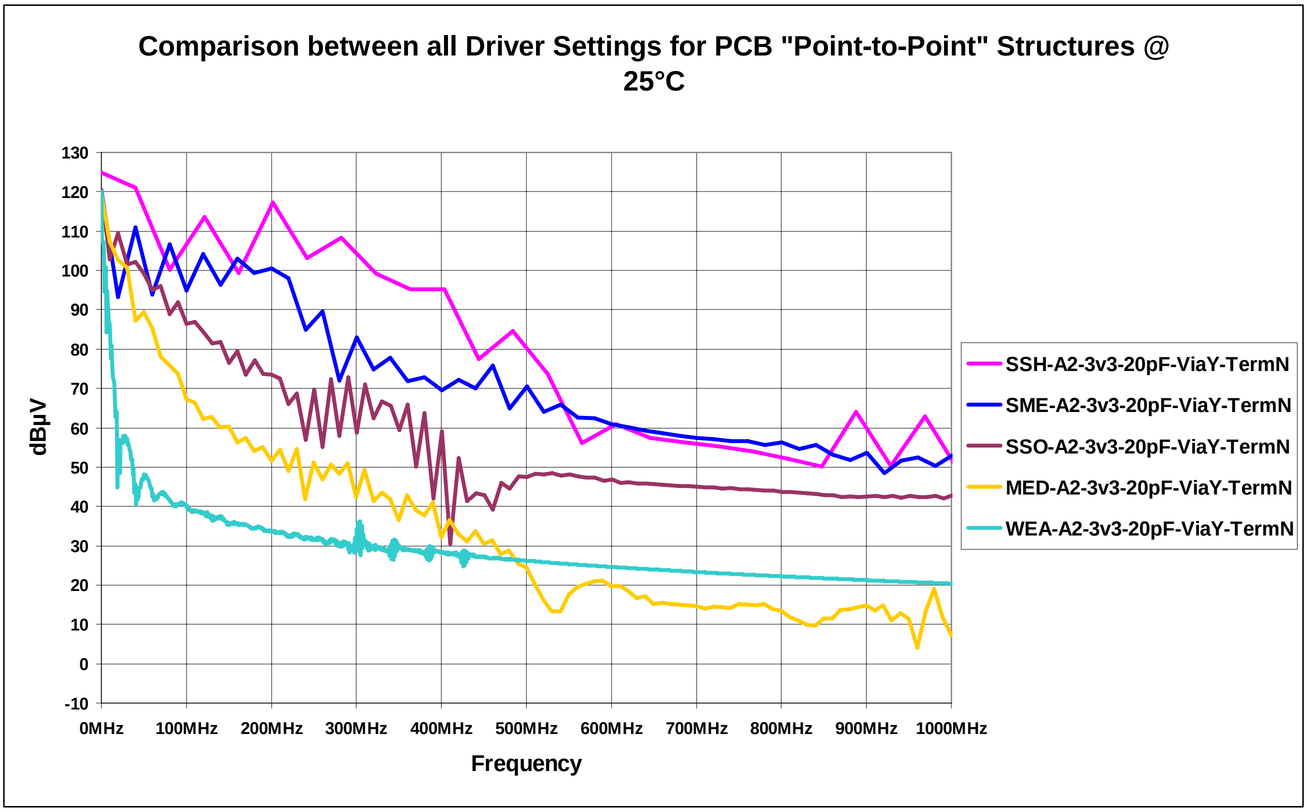


Figure 175: Class A2; various driver settings at 20pF load for "P2P" layout w/ Vias w/o Term

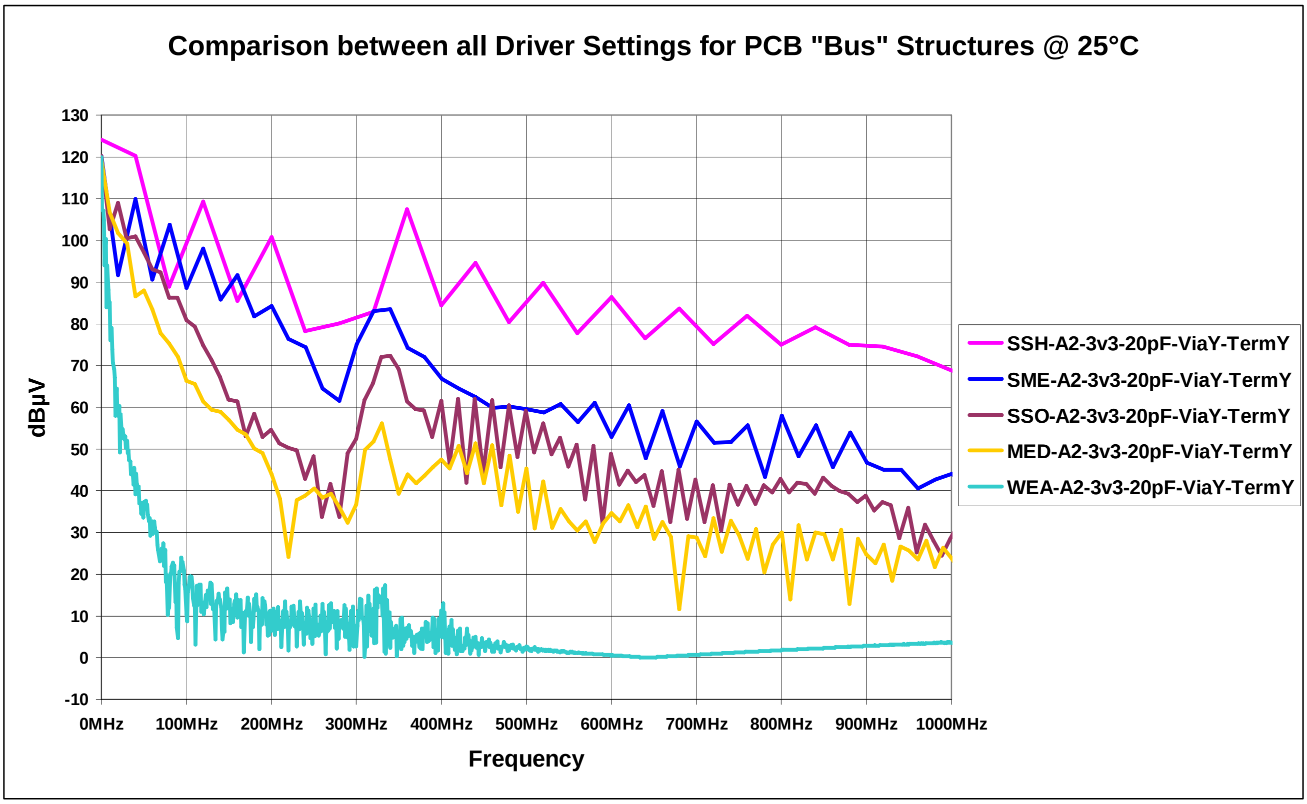


Figure 176: Class A2; various driver settings at 20pF load for “Bus” layout w/ Vias w/ Term

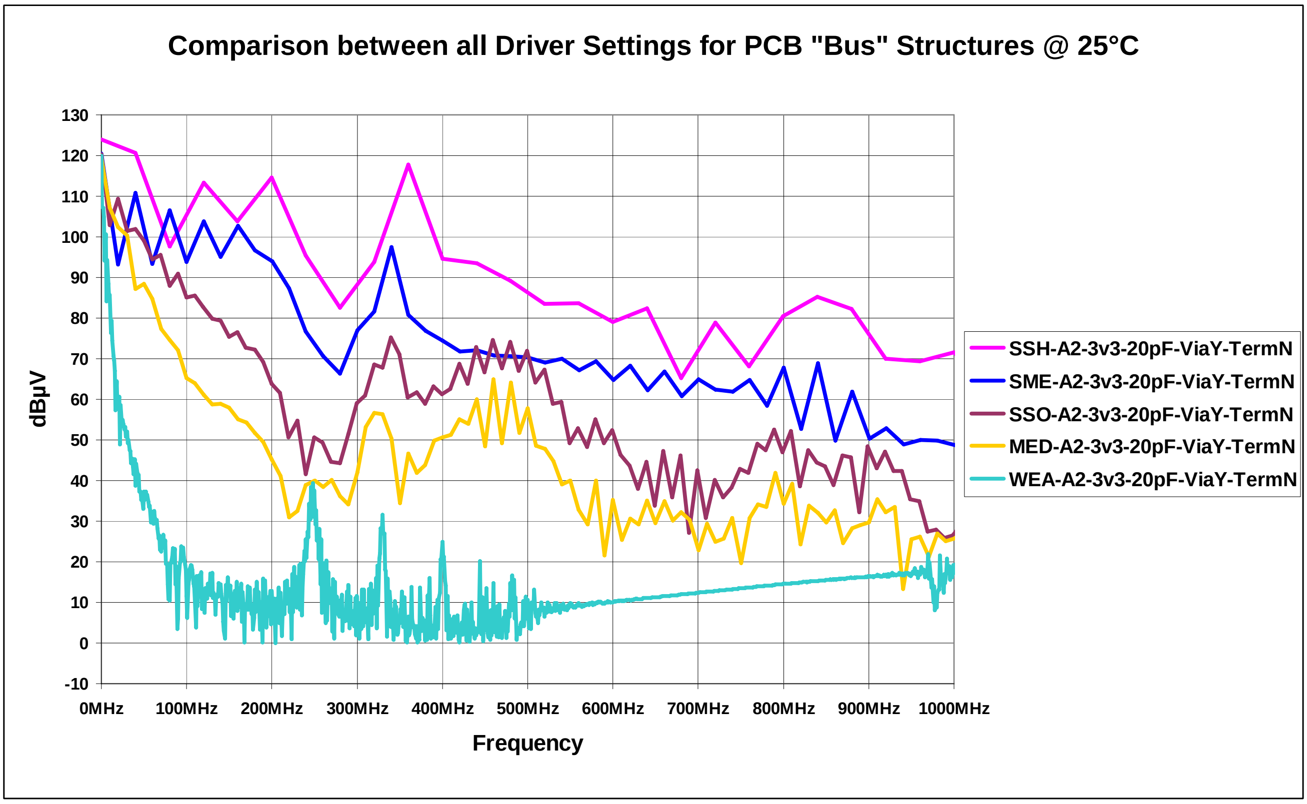


Figure 177: Class A2; various driver settings at 20pF load for “Bus” layout w/ Vias w/o Term

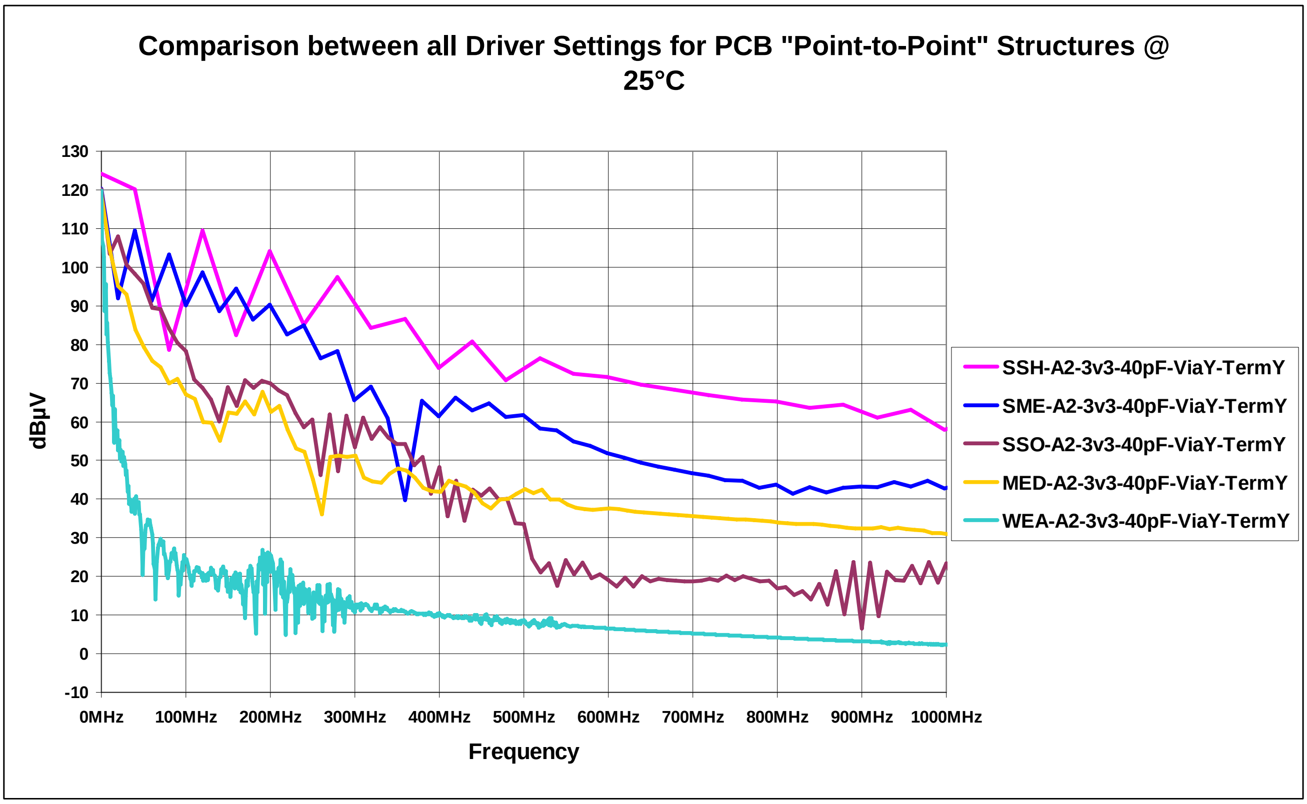


Figure 178: Class A2; various driver settings at 40pF load for “P2P” layout w/ Vias w/ Term

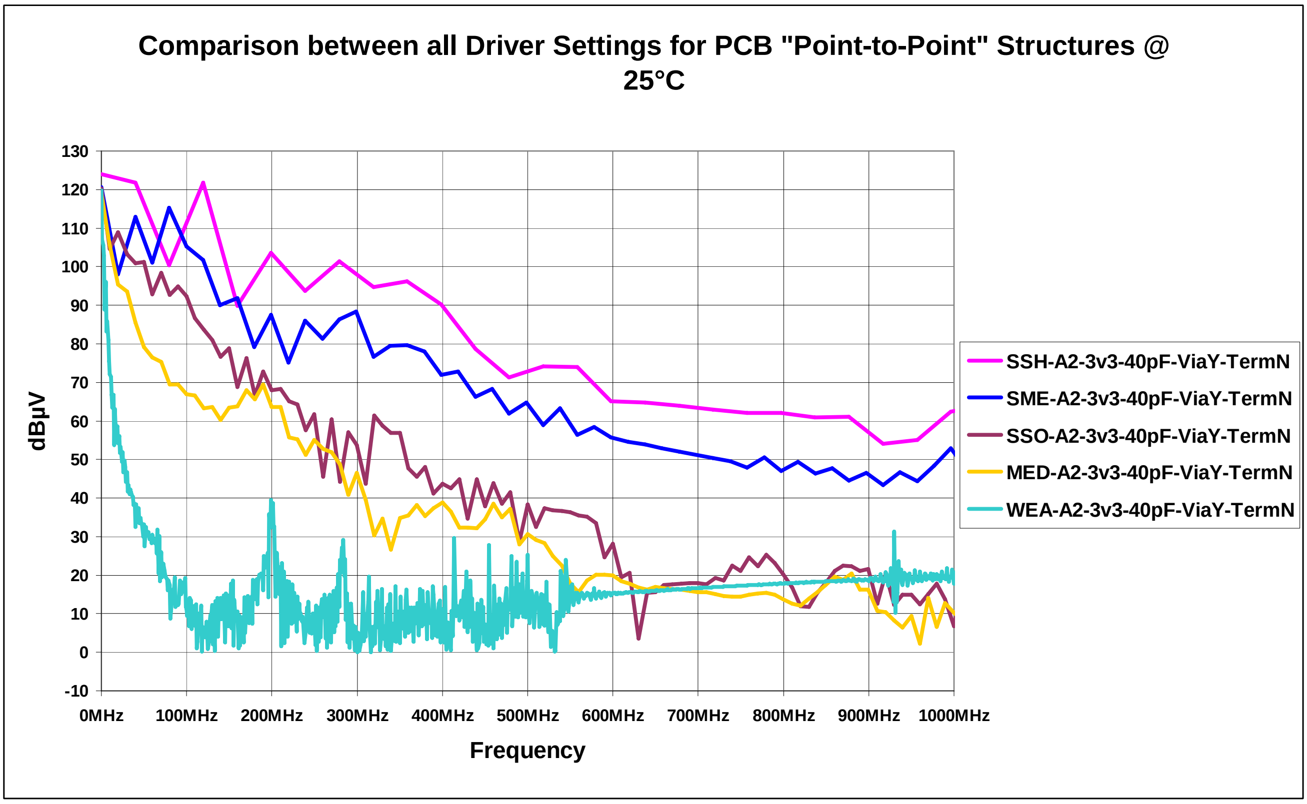


Figure 179: Class A2; various driver settings at 40pF load for “P2P” layout w/ Vias w/o Term

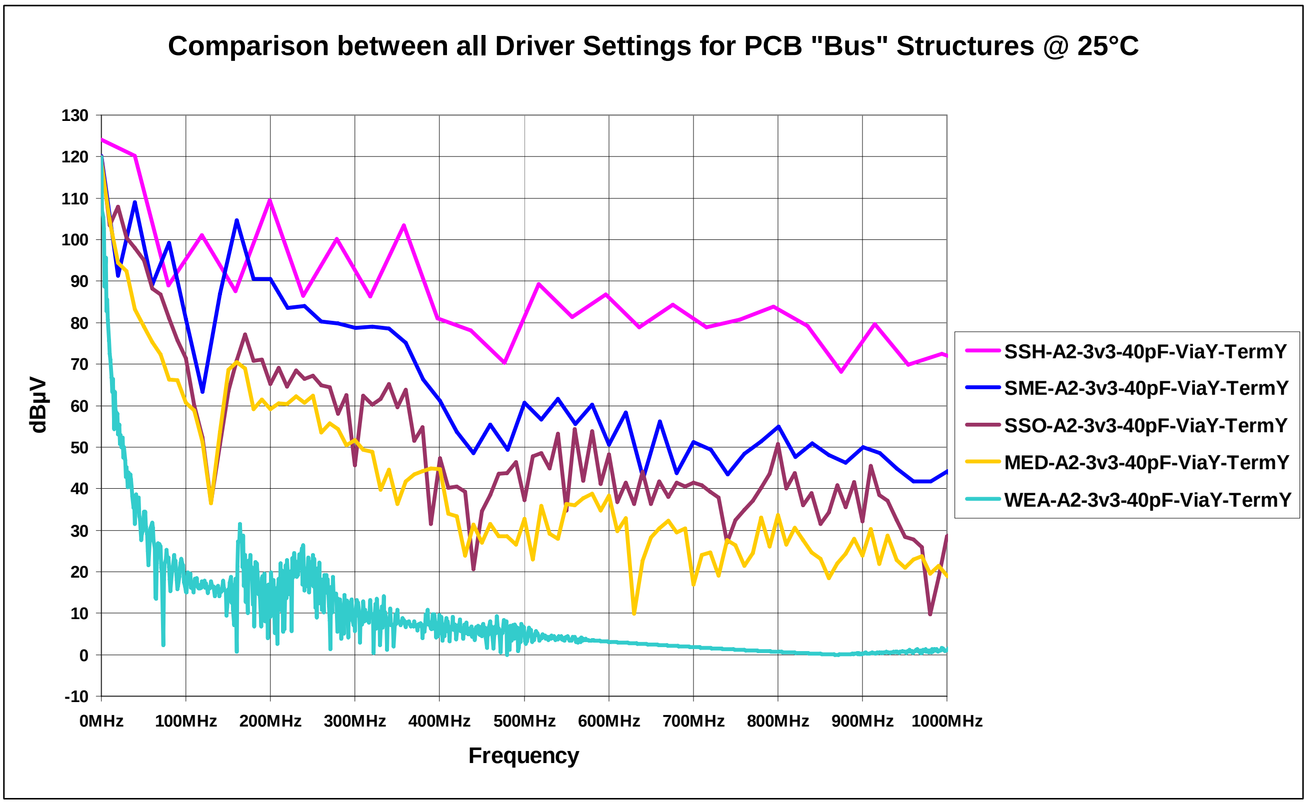


Figure 180: Class A2; various driver settings at 40pF load for “Bus” layout w/ Vias w/ Term

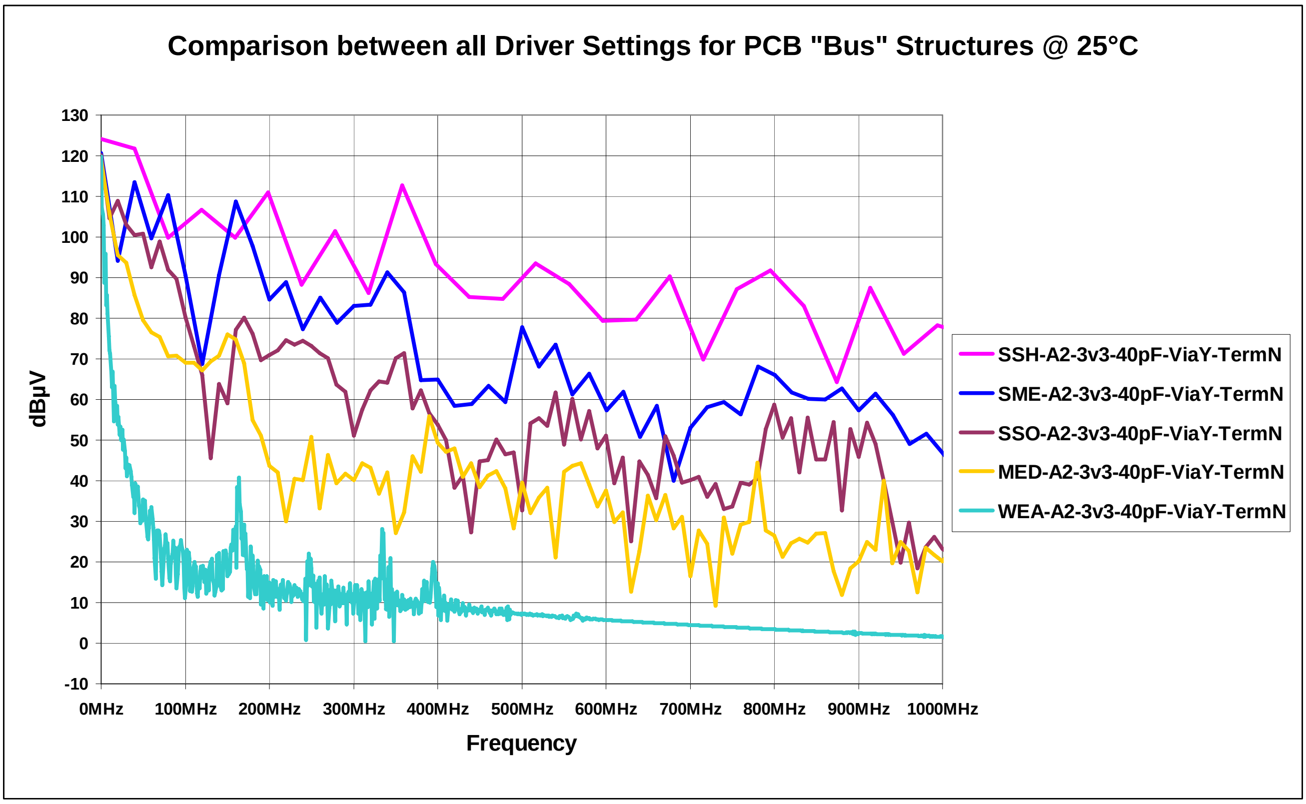


Figure 181: Class A2; various driver settings at 40pF load for “Bus” layout w/ Vias w/o Term

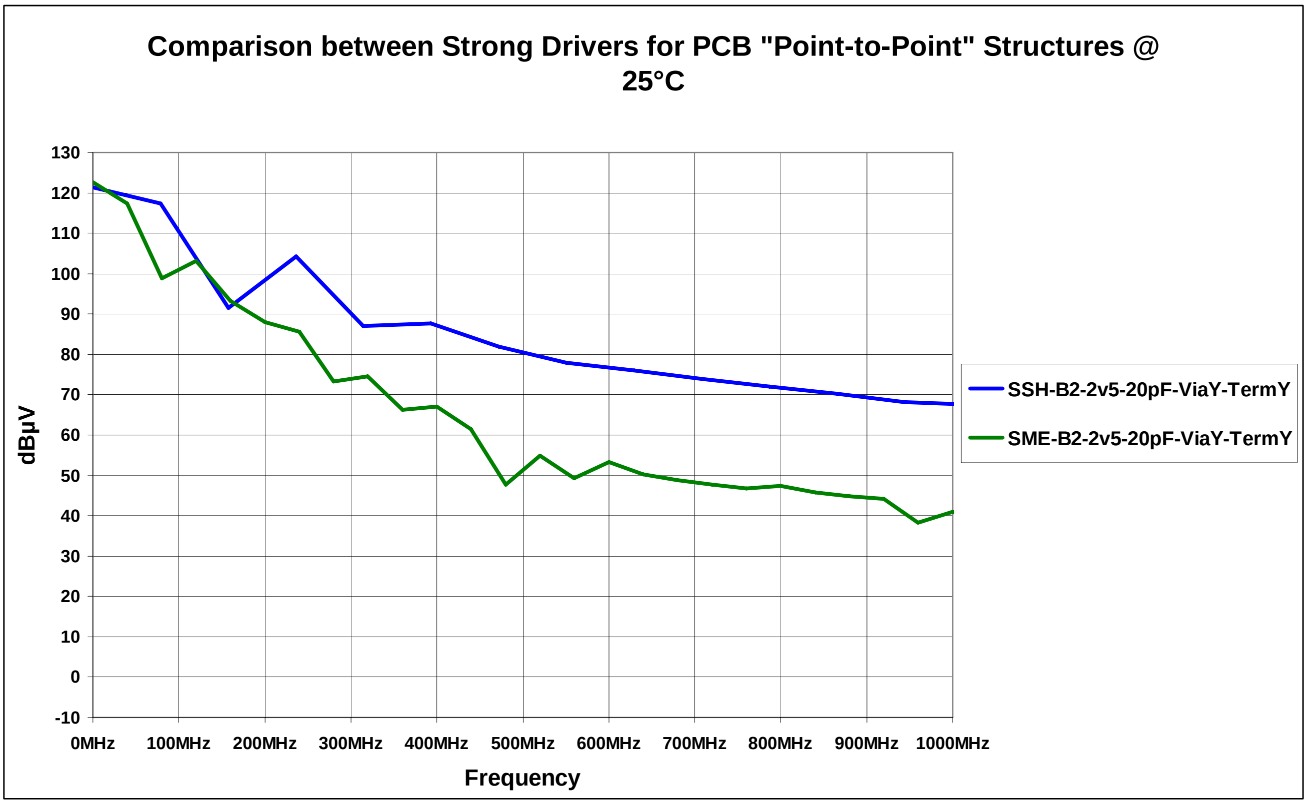


Figure 182: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 20pF load for "P2P" layout w/ Vias w/ Term

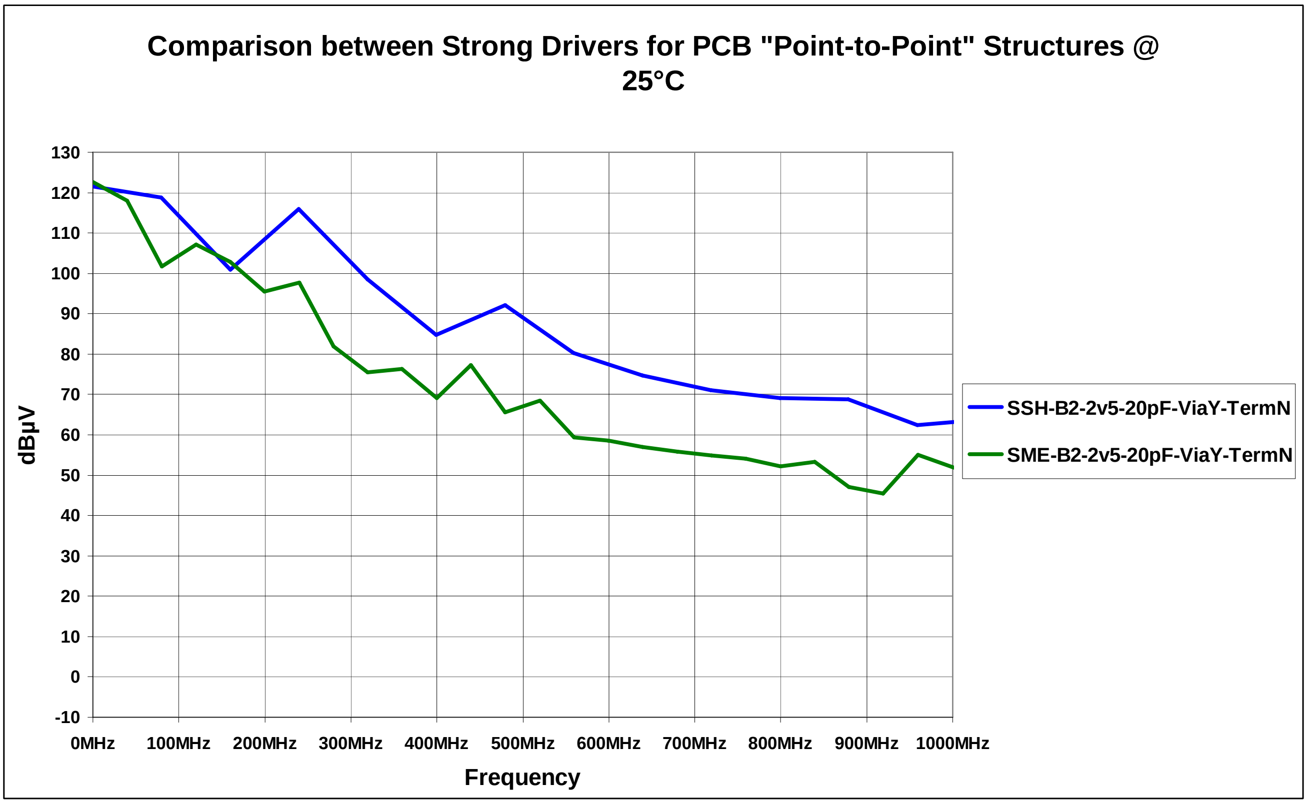


Figure 183: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 20pF load for "P2P" layout w/ Vias w/o Term

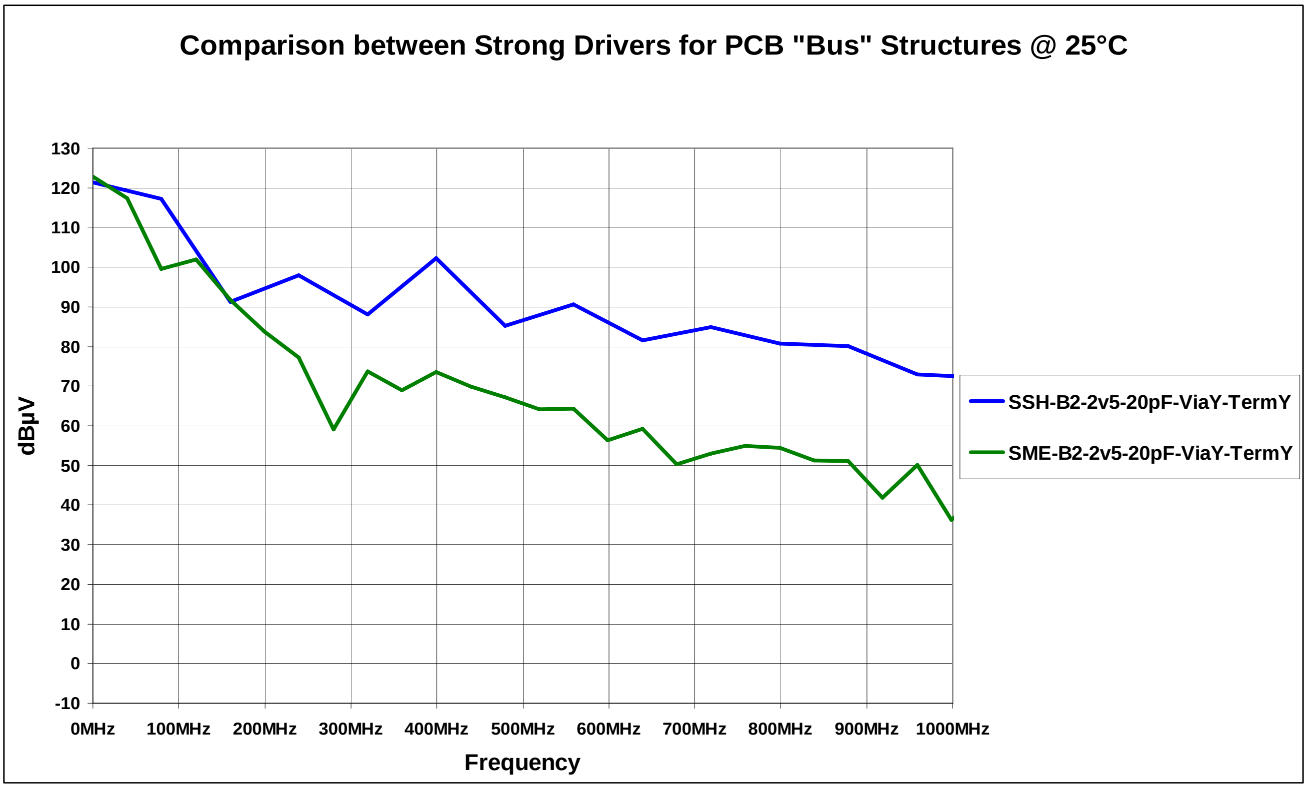


Figure 184: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 20pF load for "Bus" layout w/ Vias w/ Term

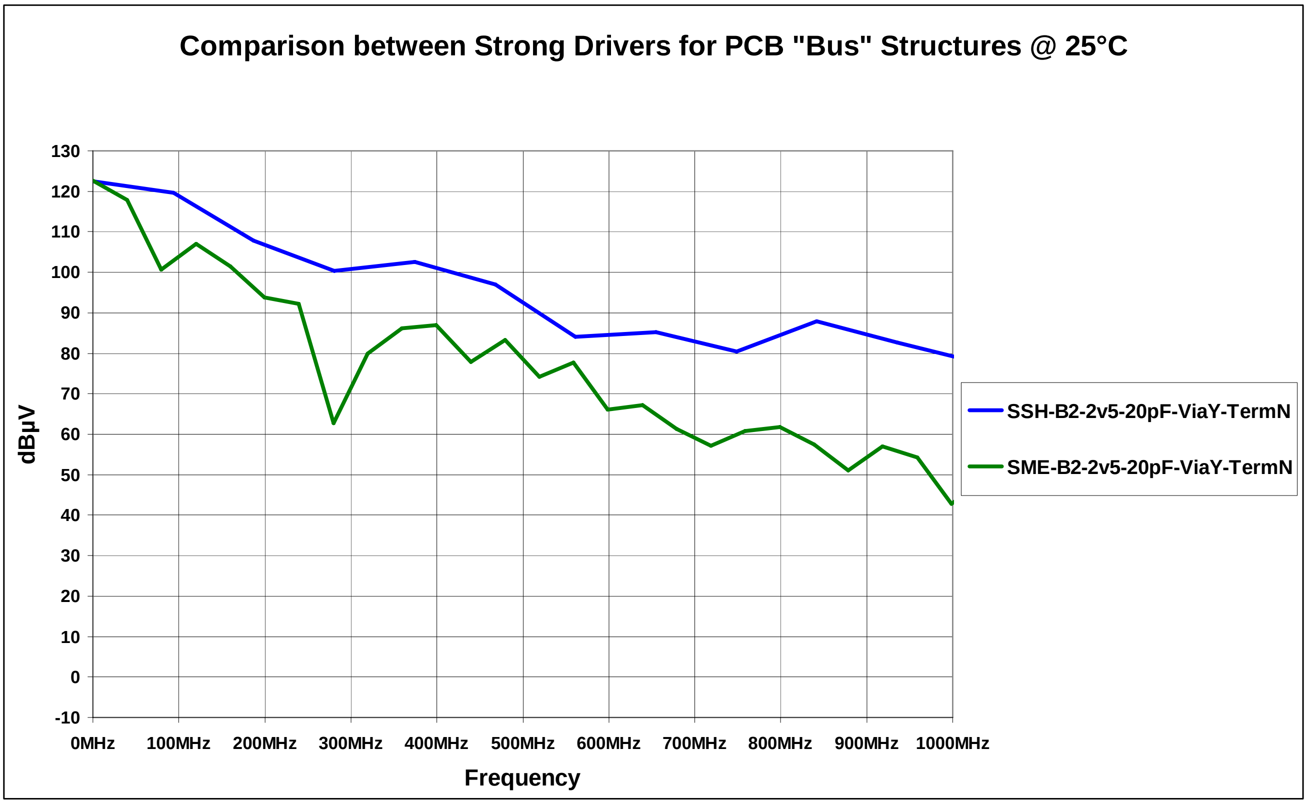


Figure 185: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 20pF load for "Bus" layout w/ Vias w/o Term

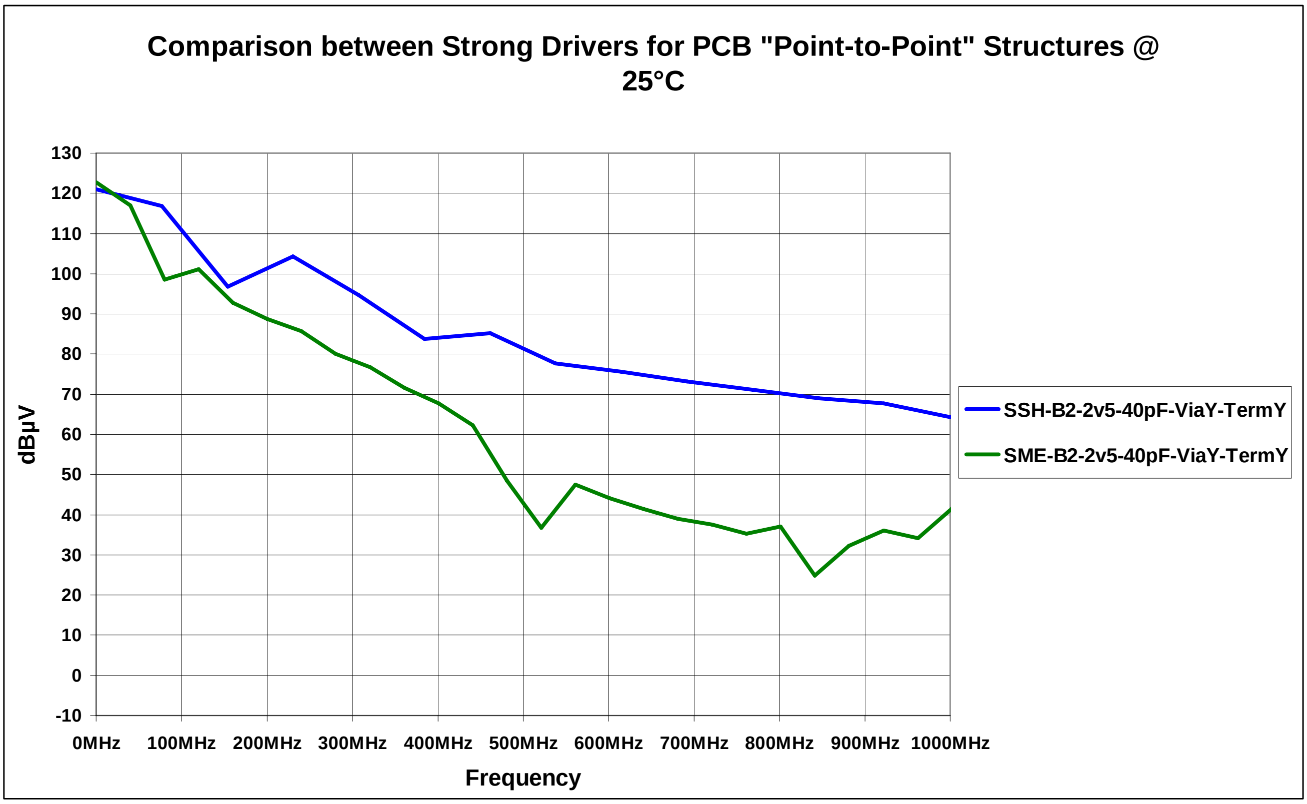


Figure 186: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 40pF load for "P2P" layout w/ Vias w/ Term

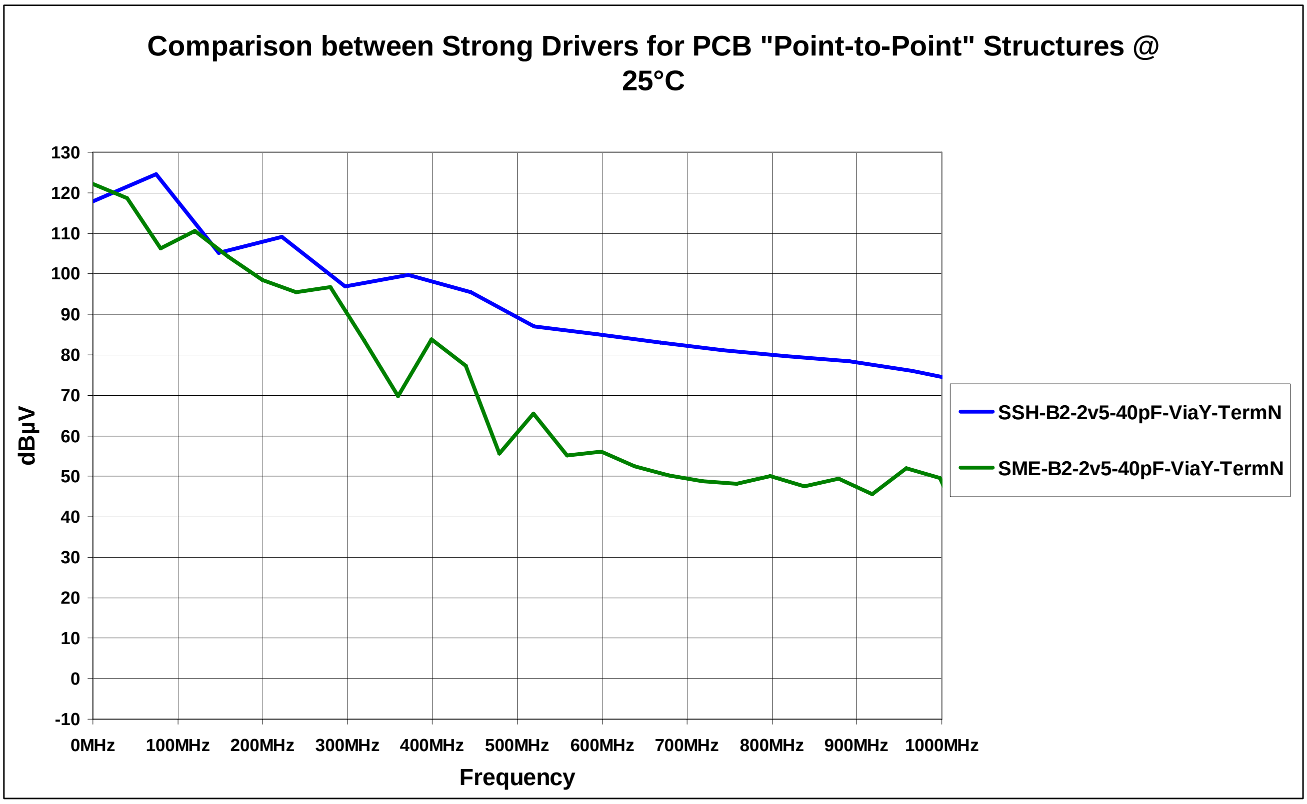


Figure 187: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 40pF load for "P2P" layout w/ Vias w/o Term

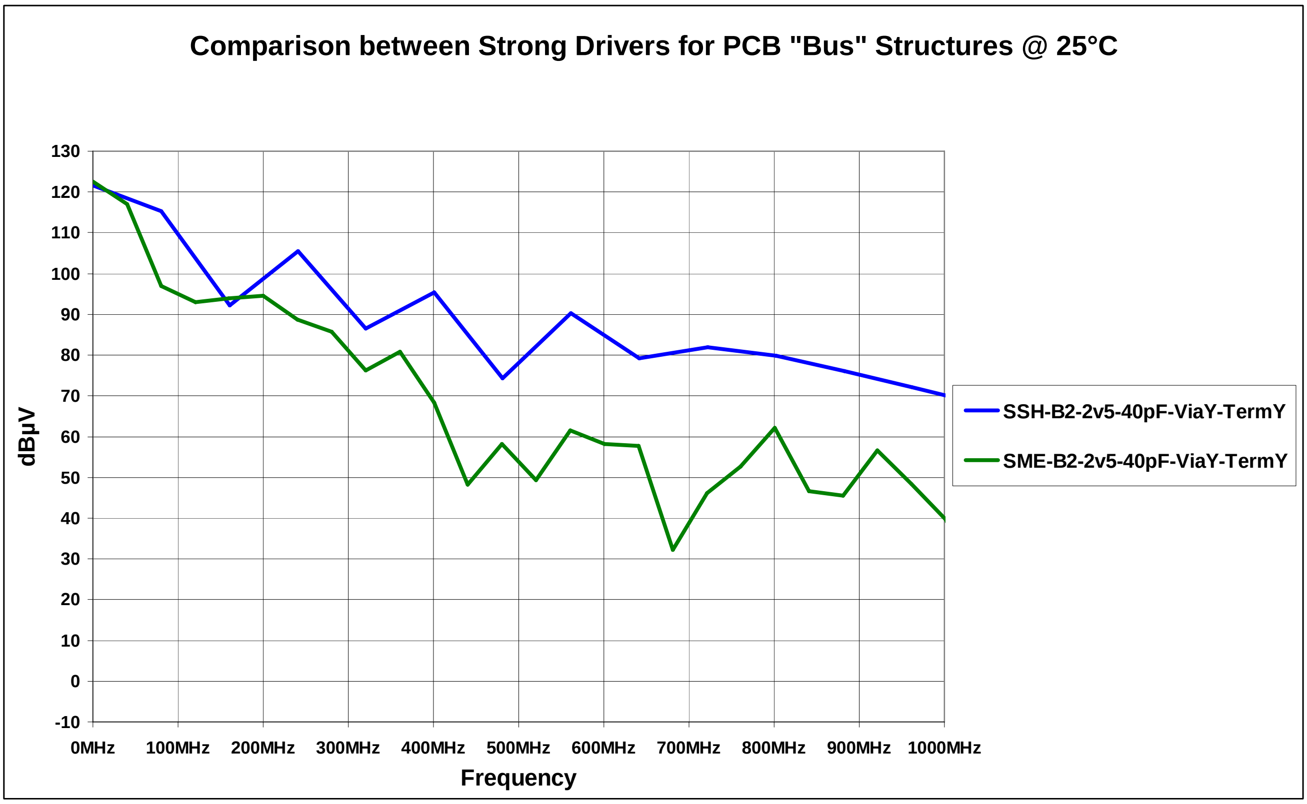


Figure 188: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 40pF load for "Bus" layout w/ Vias w/ Term

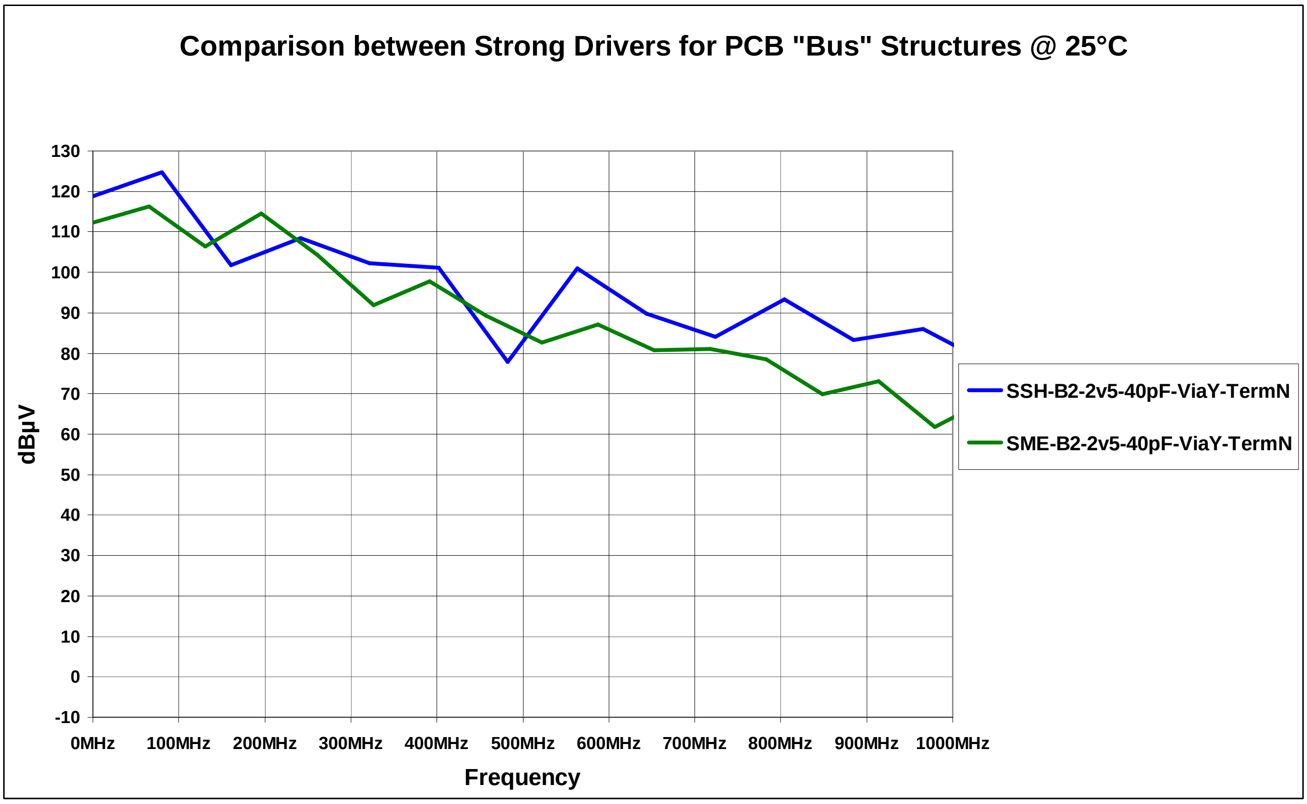


Figure 189: Class B2; "Strong-Sharp" & "Strong-Medium" drivers at 40pF load for "Bus" layout w/ Vias w/o Term

7 Recommended settings for signal categories

7.1 General

In the previous chapters, many detailed results were provided for the impact of driver settings and load capacitance on resulting rise and fall times as well as on conducted and radiated emission.

Generally the required signal integrity determines the selection of driver strength and slew rate for a given toggle rate and capacitive load. However, due to the simultaneous impact on electromagnetic emission, the weakest possible driver setting which still meets the signal integrity should be chosen.

To decide for the proper pad driver settings for a signal, its electrical characteristics should be considered. This leads to the definition of signal categories by means of clock or data transfer (AC view) or current driving capability (DC view). According these views, any signal can be characterized as shown in Table 5.

Signal category	Clock rate	Capacitive load	DC driving capability
EBU clock	40..80MHz	10..50pF	n/a
System clock	20..40MHz	10..50pF	n/a
High-speed data line	5..20MHz	10..50pF	n/a
Low-speed data line	0.5..5MHz	10..50pF	n/a
Low-speed control line	<1MHz	<20pF	n/a
High-current control line	n/a	n/a	10..30mA
Medium-current control line	n/a	n/a	1..10mA
Low-current control line	n/a	n/a	<1mA

Table 5: Signal categories

The following settings for pad output drivers are available, see also Table 6:

- strong driver / sharp edge (setting 1)
- strong driver / medium edge (setting 2)
- strong driver / soft edge (setting 3)
- medium driver / no edge configuration available (setting 4)
- weak driver / no edge configuration available (setting 5)

Setting	Driver configuration	Edge configuration	Signal category	Capacitive Load	DC Current 1)
1	STRONG	SHARP	System clock	High	2.0/-2.0/-1.4 mA
2	STRONG	MEDIUM	System clock High-speed data lines	Low High	
3	STRONG	SOFT	High-speed data lines High-current control lines	Low All	
4	MEDIUM	none	Low-speed data lines Medium-current control lines	All All	1.8/-1.8/-1.0 mA
5	WEAK	none	Very low-speed control lines Low-current control line	All All	0.37/-0.37/-0.28mA

Table 6: Recommended output driver settings

Note [1]: Three values are given for the DC current of Class A2 pins in the format "$I_{OL}/I_{OH1}/I_{OH2}$". I_{OL} is the maximum output current for $V_{OL} \leq 0.4V$. I_{OH1} is the maximum output current for $V_{OH} \geq 2.4V$. I_{OH2} is the maximum output current for $V_{OH} \geq VDDP-0.4V$.

The following parameters determine the final selection of driver settings:

- signal performance category (AC and DC)
- maximum temperature
- maximum acceptable electromagnetic emission

7.2 Decision Tables and Graphs

Following the recommendations given above, the driver setting selection should be based on (1) proper signal integrity and (2) minimal electromagnetic emission. Since electromagnetic emission increases with stronger driver settings, the weakest driver and slew rate settings should be selected which are able to force the rise/fall times required for the desired signal integrity.

This chapter offers decision numbers in table and graphical format for proper driver settings at maximum clock or data rates expected to be driven. The rise/fall times occupy 1/6 of the clock period each, see Fig. 190 on top. Alternatively, the rise/fall times occupy 1/4 of the clock period each, see Fig. 190 on bottom.

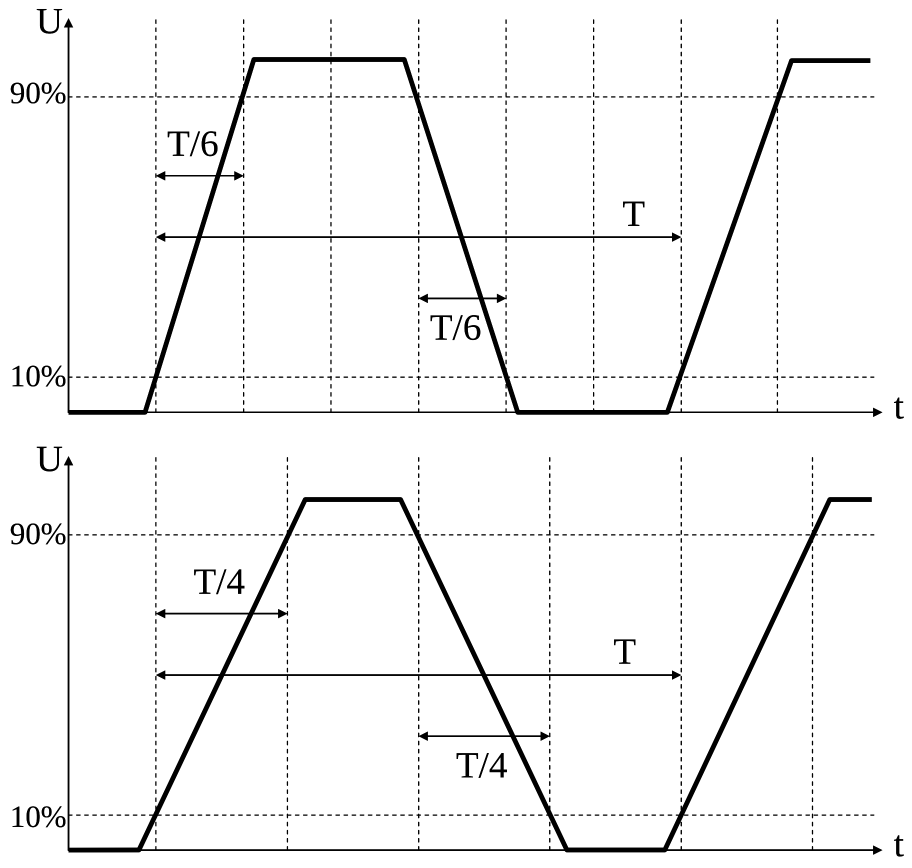


Figure 190: Assumed rise/fall timing conditions related to signal period

Please note that all values given in this chapter are proposals for system application designers using Infineon Audo-NG and Audo-Future microcontrollers in 0.13µm CMOS technology. They are based on timing measurements of Class A2 drivers operating at 3.3V supply voltage, performed on center lot devices. Thus all values are subject to ca. 10% offset depending on fabrication process variation. Additionally, pad supply voltages different from nominal conditions, impact the resulting timings. The finally selected driver setting should include this ca. 10% offset. It has to be added to all numbers given in the tables and graphs.

Fig. 191 shows an example of a decision graph.

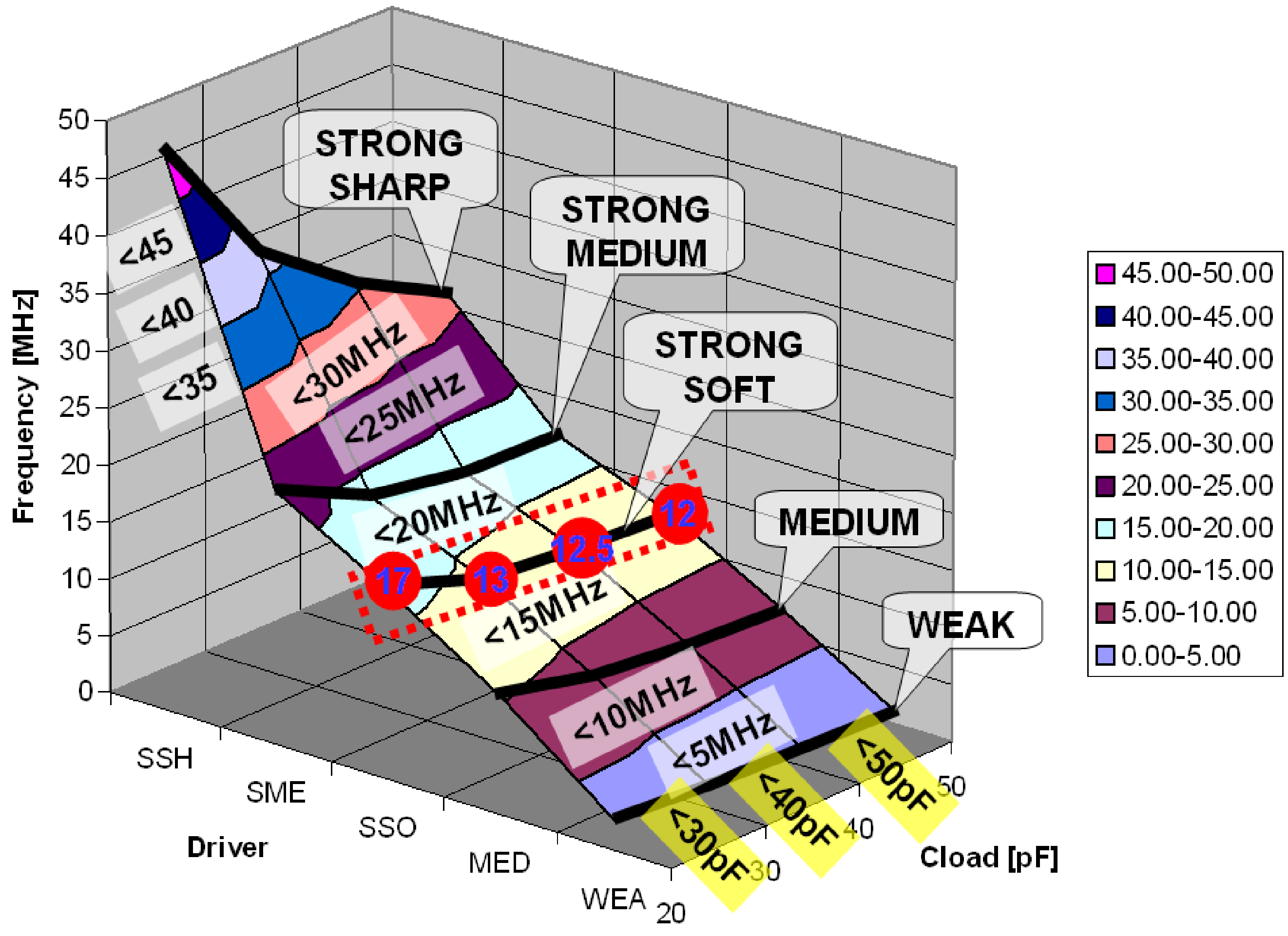


Figure 188: Assumed rise/fall timing conditions related to signal period

The clock/data rate is given in MHz for capacitive loads of 20, 30, 40 and 50pF and driver selections of weak, medium, strong soft/medium/sharp for Class A2 drivers. Class B2 drivers are only used in the external bus interface, operating at high data rates. Thus Class B2 drivers are only represented by strong-sharp and strong-medium driver settings. However, operations at 2.5V and 3.3V supply voltage are considered.

In the example given in Fig. 164, the resulting maximum data rates are marked with red circles as 17MHz at 20pF load, 13MHz at 30pF load, 12.5MHz at 40pF load and 12MHz at 50pF load. If a pin is intended to toggle a 35pF load at 15MHz, the strong-soft setting is not sufficient. Instead strong-medium must be selected. Strong-sharp is of course also capable of driving 35pF load at 15MHz, but should be avoided due to unnecessary high electromagnetic emission.

The rise/fall times occupy 1/6 of the clock period each, see Fig. 163 on top. This relation should be acceptable for most interface signals and protocols.

Tables 8 and 9 give an overview of the maximal toggle rates in [MHz] for all Class A2 driver settings (WEA=weak, MED=medium, SSO=strong-soft, SME=strong-medium, SSH=strong-sharp) connected to capacitive loads of 20, 30, 40 and 50pF. Each ambient temperature is marked by its own color. According the microcontroller specification or marking, one of the following maximal temperatures should apply: 125°C, 110°C, 85°C. The other temperatures 30°C, 0°C and -40°C are given for reference only.

In Table 8, the rise/fall times are assumed to occupy 1/6 of the clock period. In Table 9, the rise/fall times are assumed to occupy 1/4 of the clock period.

Fig. 189-200 show the values of Tables 8 and 9 in the graphical representation explained in Fig. 188, separated by ambient temperatures. In the respective titles, “16% Edges” stands for rise/fall times

occupying 1/6 of the clock period; “25% Edges” stands for rise/fall times occupying 1/4 of the clock period.

Decision graphs are provided in 4 sections:

7.2.1: Measured values for Class A2 drivers operated at 3.3V supply, for different ambient temperatures from -40°C up to 125°C.

7.2.2: Simulated values for Class A2 drivers operated at 3.3V supply, using point-to-point connection between driver and receiver, consisting of a signal trace without termination, but with vias (according Fig. 46 a), for different ambient temperatures from 30°C up to 125°C.

7.2.3: Simulated values for Class B2 drivers operated at 3.3V supply, using point-to-point connection between driver and receiver, consisting of a signal trace without termination, but with vias (according Fig. 46 a), for different ambient temperatures from 30°C up to 125°C.

7.2.4: Simulated values for Class B2 drivers operated at 2.5V supply, using point-to-point connection between driver and receiver, consisting of a signal trace without termination, but with vias (according Fig. 46 a), for different ambient temperatures from 30°C up to 125°C.

Note that the simulated values for temperatures other than 30°C and 125°C have been interpolated from the 30°C and 125°C numbers. The measured values have been recorded for all given temperatures.

7.2.1 Measured values for Class A2 drivers operated at 3.3V supply

125°C		20	30	40	50
	SSH	182.55	129.60	81.66	61.96
	SME	56.69	45.98	32.20	27.23
	SSO	16.38	14.63	10.06	10.02
	MED	9.53	7.46	3.70	2.65
	WEA	1.70	1.38	0.85	0.64

110°C		20	30	40	50
	SSH	184.77	132.27	81.78	57.07
	SME	58.79	47.17	33.93	28.39
	SSO	16.68	14.84	11.07	8.43
	MED	9.34	7.68	3.64	2.79
	WEA	1.74	1.41	0.89	0.76

85°C		20	30	40	50
	SSH	183.55	135.40	89.32	65.10
	SME	60.23	49.50	35.71	29.65
	SSO	17.11	15.35	9.32	8.52
	MED	9.45	7.98	3.88	2.99
	WEA	1.82	1.49	0.96	0.82

30°C		20	30	40	50
	SSH	198.89	133.87	96.17	72.46
	SME	76.91	58.83	43.63	35.29
	SSO	21.67	18.92	13.43	12.01
	MED	12.60	9.33	4.97	3.38
	WEA	2.37	1.81	1.13	0.76

0°C		20	30	40	50
	SSH	221.93	145.18	100.40	82.63
	SME	93.79	71.38	49.25	38.47
	SSO	24.69	21.87	16.76	14.96
	MED	14.16	10.09	5.04	4.16
	WEA	2.59	2.02	1.16	0.86

-40°C		20	30	40	50
	SSH	233.43	156.94	102.50	88.14
	SME	108.01	84.05	54.06	43.67
	SSO	28.93	23.71	16.94	14.99
	MED	15.26	10.30	5.95	4.20
	WEA	3.07	2.26	1.27	0.93

Table 7: Maximal toggle rates [MHz] for all driver settings at loads 20..50pF; 16% edges

125°C		20	30	40	50
	SSH	273.82	194.40	122.49	92.94
	SME	85.03	68.96	48.30	40.85
	SSO	24.58	21.95	15.09	15.03
	MED	14.30	11.18	5.54	3.99
	WEA	2.56	2.07	1.28	0.96

110°C		20	30	40	50
	SSH	277.16	198.41	122.67	85.62
	SME	88.18	70.76	50.89	42.59
	SSO	20.02	22.26	16.61	12.64
	MED	14.01	11.51	5.46	4.19
	WEA	2.61	2.11	1.33	1.14

85°C		20	30	40	50
	SSH	275.33	203.09	133.98	97.66
	SME	90.35	74.25	53.57	44.48
	SSO	25.67	23.02	13.98	12.79
	MED	14.17	11.97	5.82	4.48
	WEA	2.74	2.24	1.44	1.23

30°C		20	30	40	50
	SSH	298.33	200.80	144.26	108.70
	SME	115.37	88.25	65.45	52.93
	SSO	32.51	28.38	20.15	18.01
	MED	18.90	13.99	7.45	5.06
	WEA	3.56	2.72	1.69	1.14

0°C		20	30	40	50
	SSH	332.89	217.77	150.60	123.95
	SME	140.69	107.06	73.88	57.71
	SSO	37.04	32.81	25.15	22.44
	MED	21.24	15.14	7.56	6.25
	WEA	3.89	3.04	1.74	1.29

-40°C		20	30	40	50
	SSH	350.14	235.40	153.75	132.20
	SME	162.02	126.07	81.09	65.51
	SSO	43.40	35.56	25.40	22.48
	MED	22.89	15.45	8.92	6.29
	WEA	4.60	3.39	1.91	1.40

Table 8: Maximal toggle rates [MHz] for all driver settings at loads 20..50pF; 25% edges

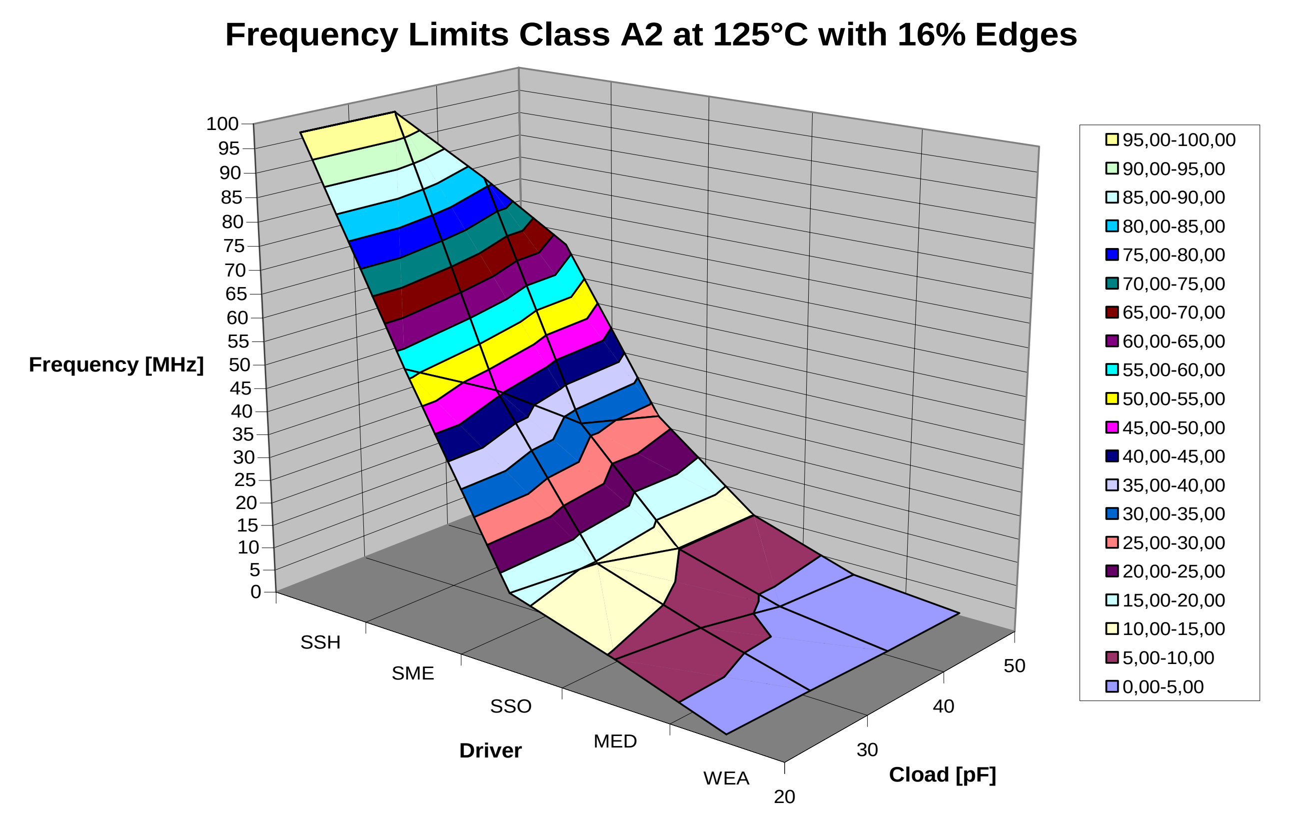


Figure 192: Driver selection decision graph for Class A drivers at T_A=125°C; edges occupy 1/6 period

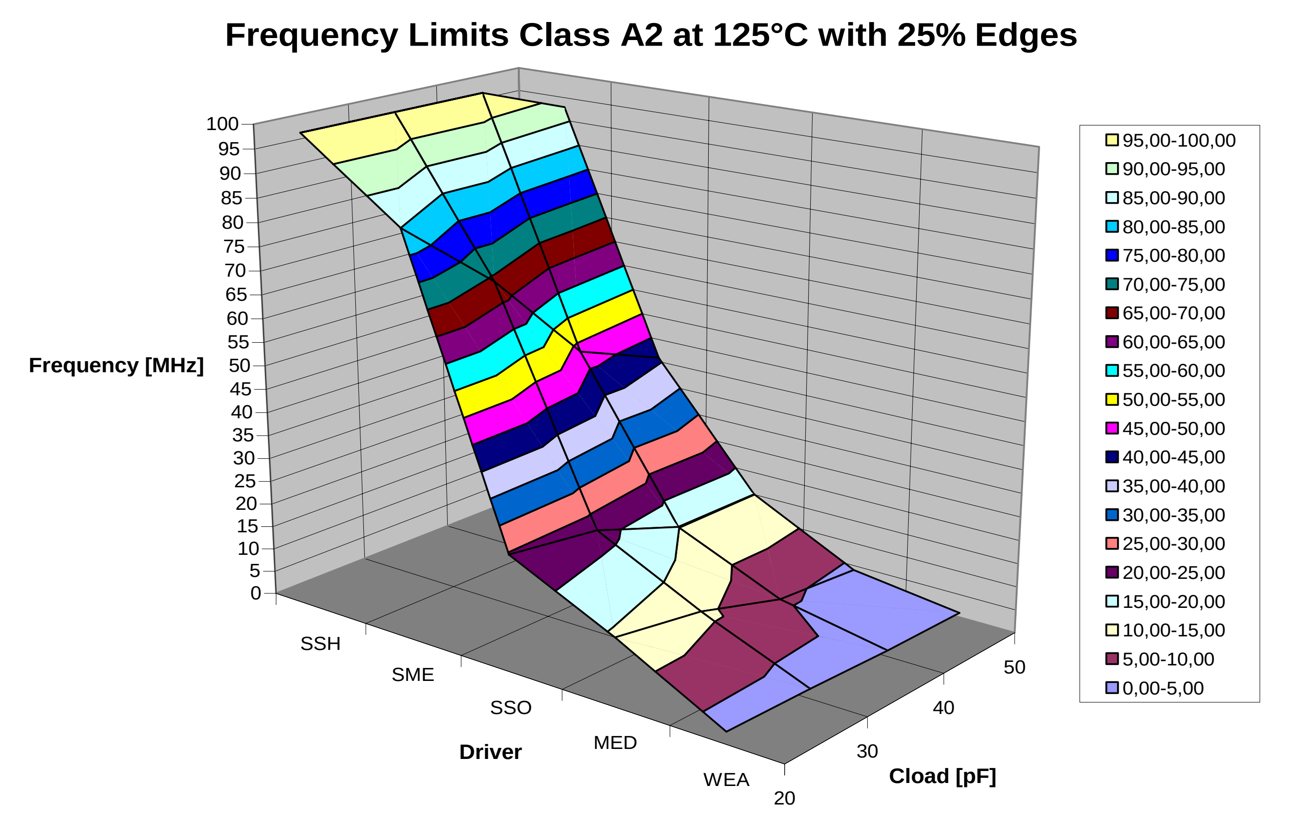


Figure 193: Driver selection decision graph for Class A drivers at T_A=125°C; edges occupy 1/4 period

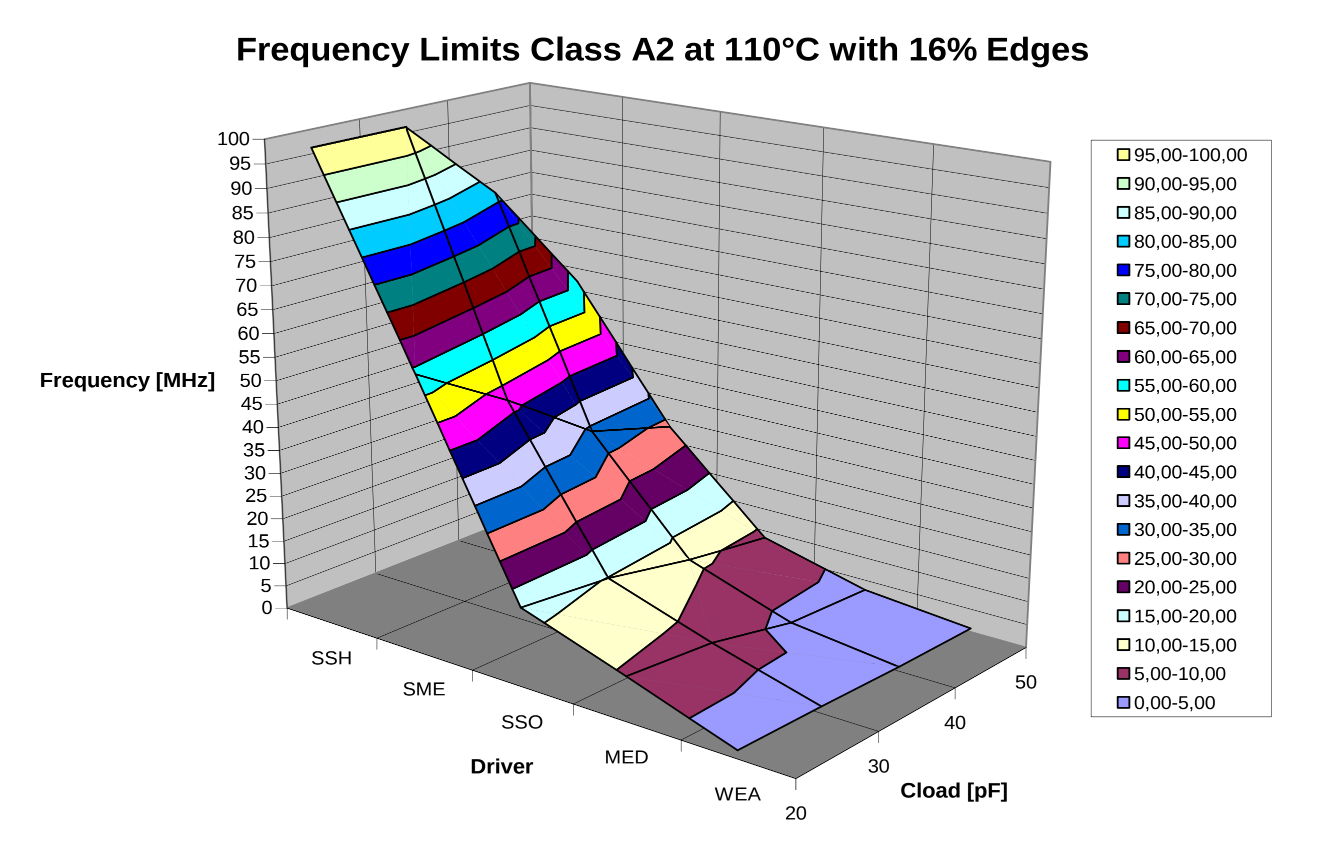


Figure 194: Driver selection decision graph for Class A drivers at T_A=110°C; edges occupy 1/6 period

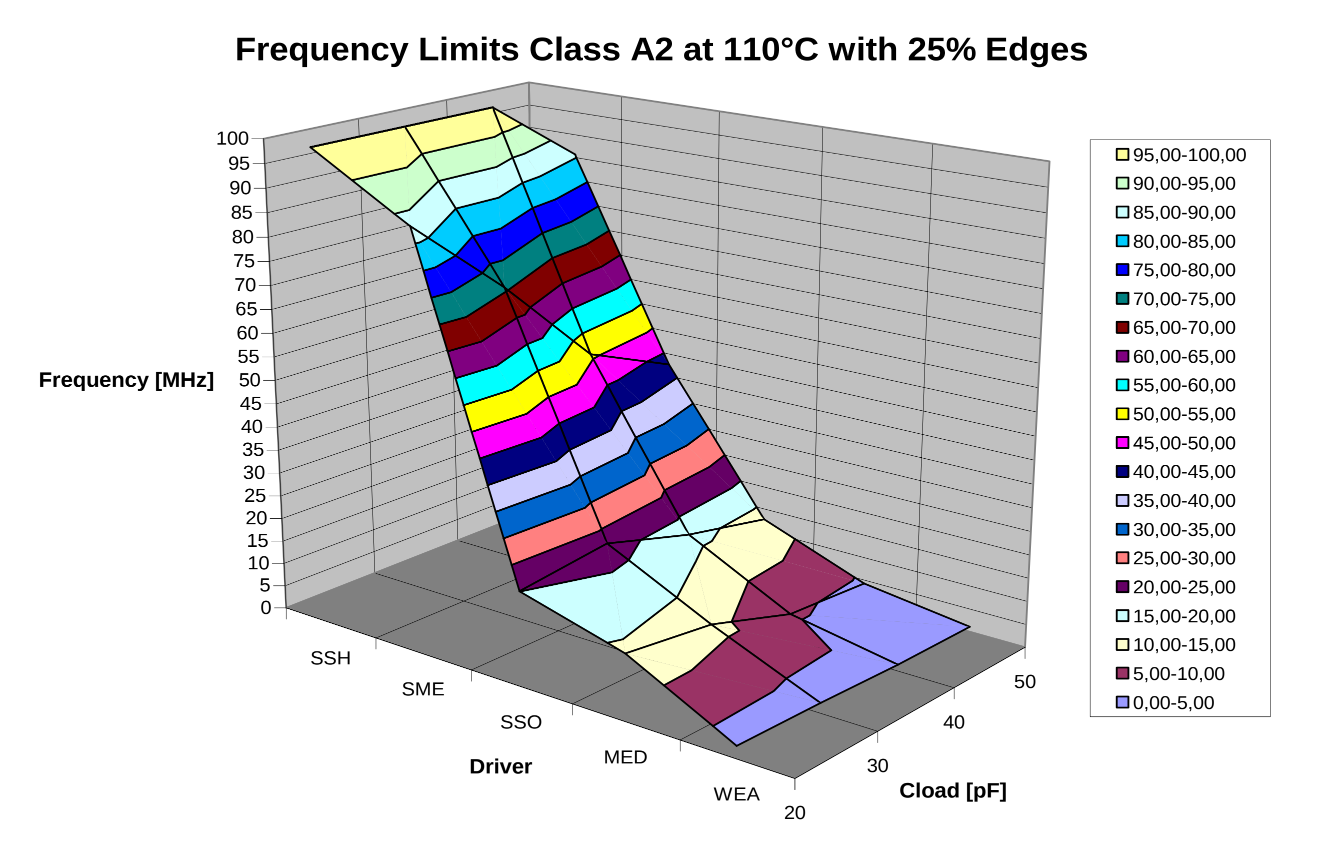


Figure 195: Driver selection decision graph for Class A drivers at T_A=110°C; edges occupy 1/4 period

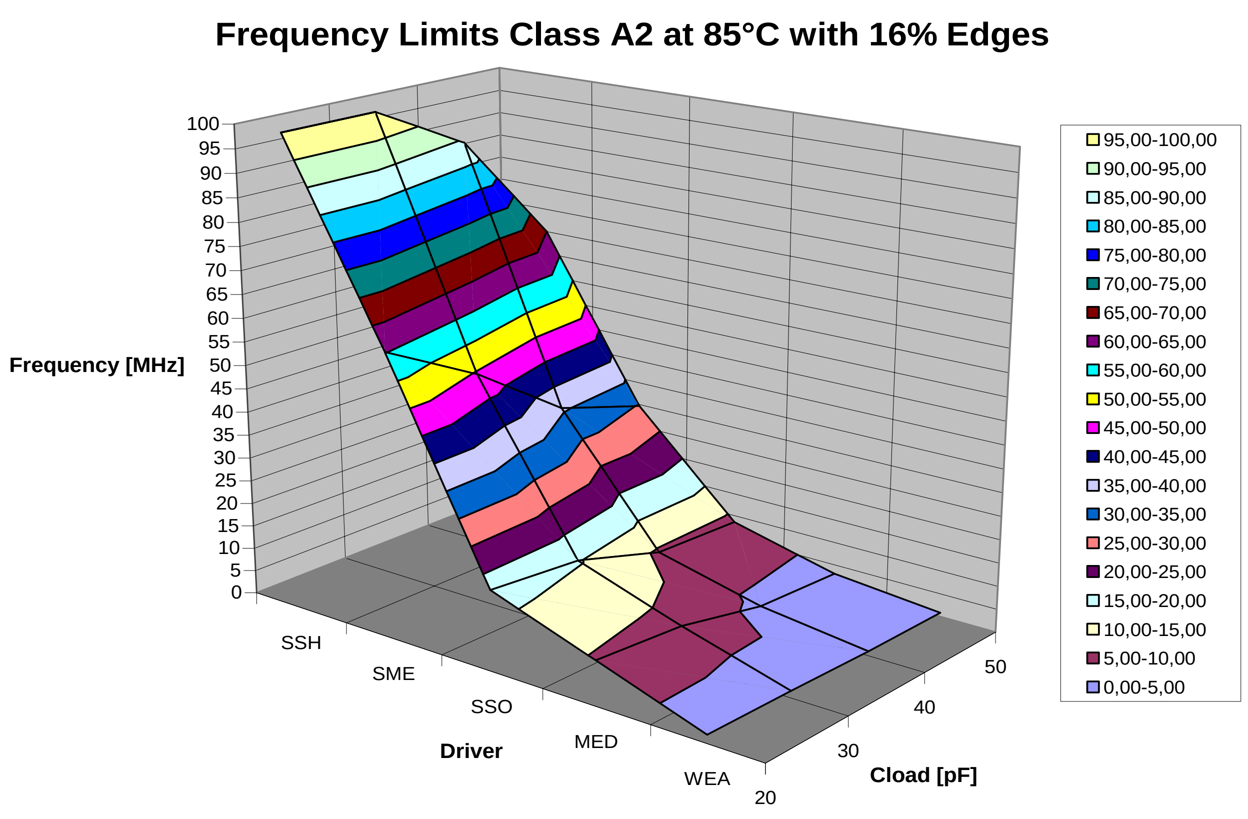


Figure 196: Driver selection decision graph for Class A drivers at T_A=85°C; edges occupy 1/6 period

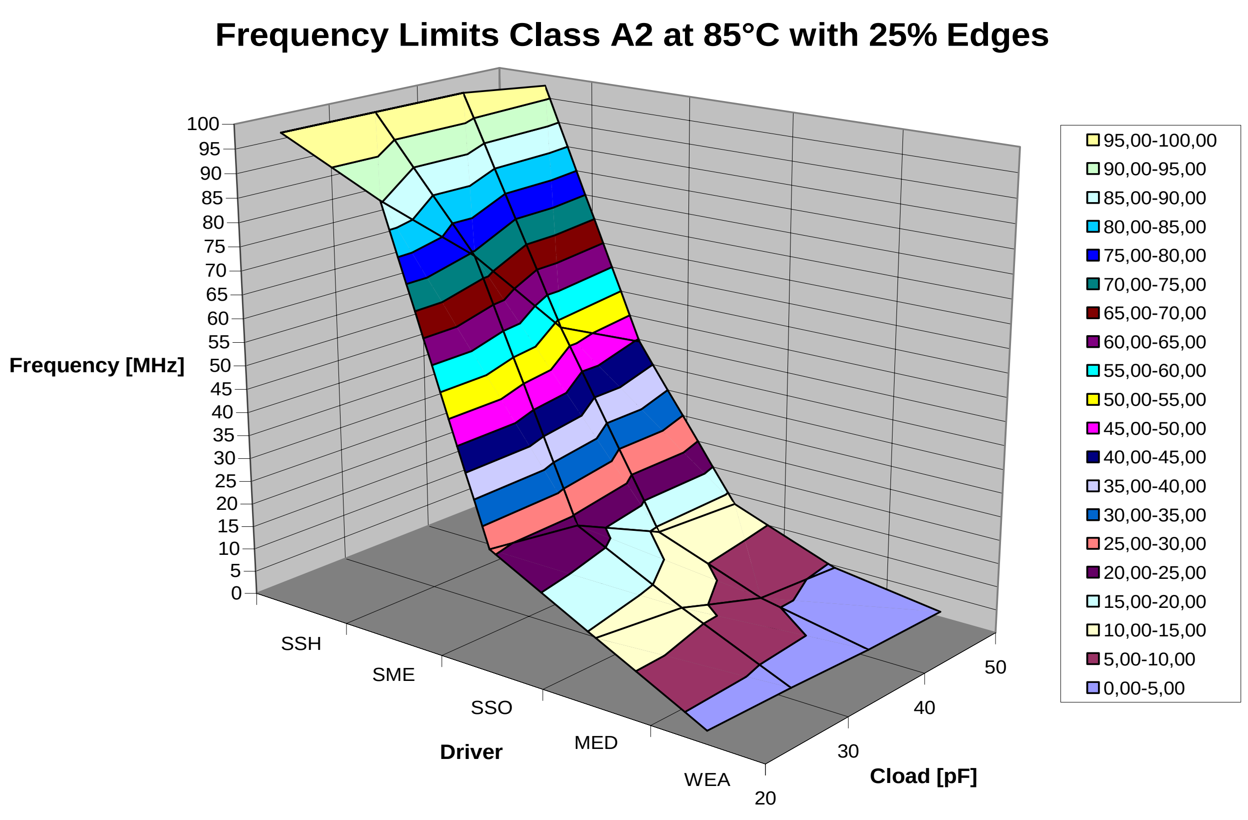


Figure 197: Driver selection decision graph for Class A drivers at T_A=85°C; edges occupy 1/4 period

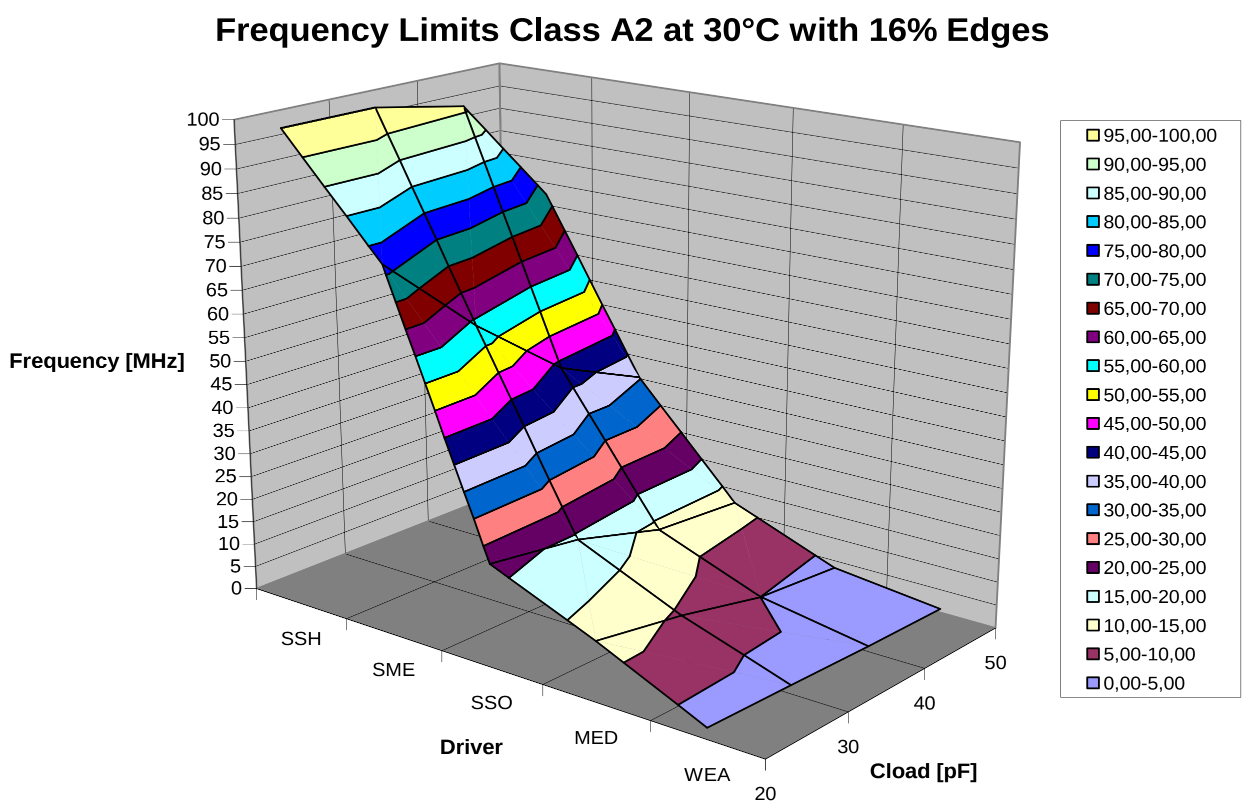


Figure 198: Driver selection decision graph for Class A drivers at T_A=30°C; edges occupy 1/6 period

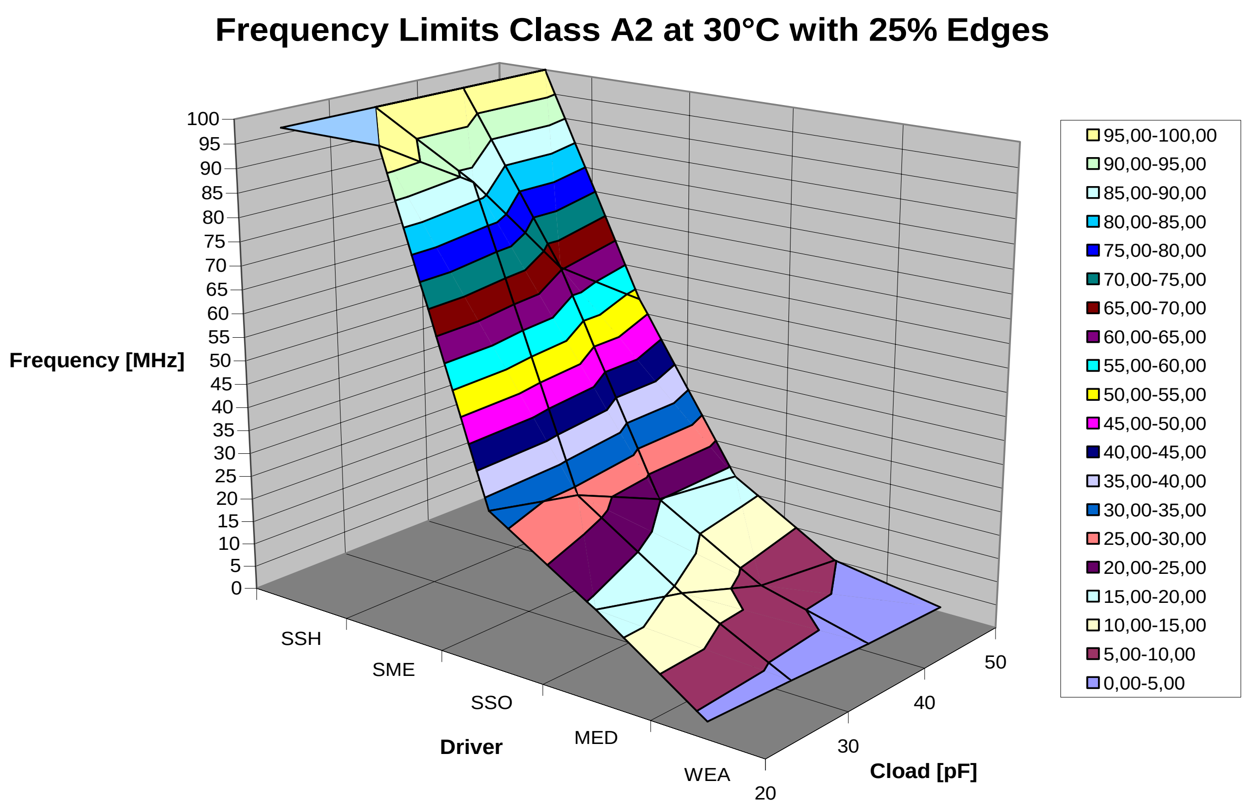


Figure 199: Driver selection decision graph for Class A drivers at T_A=30°C; edges occupy 1/4 period

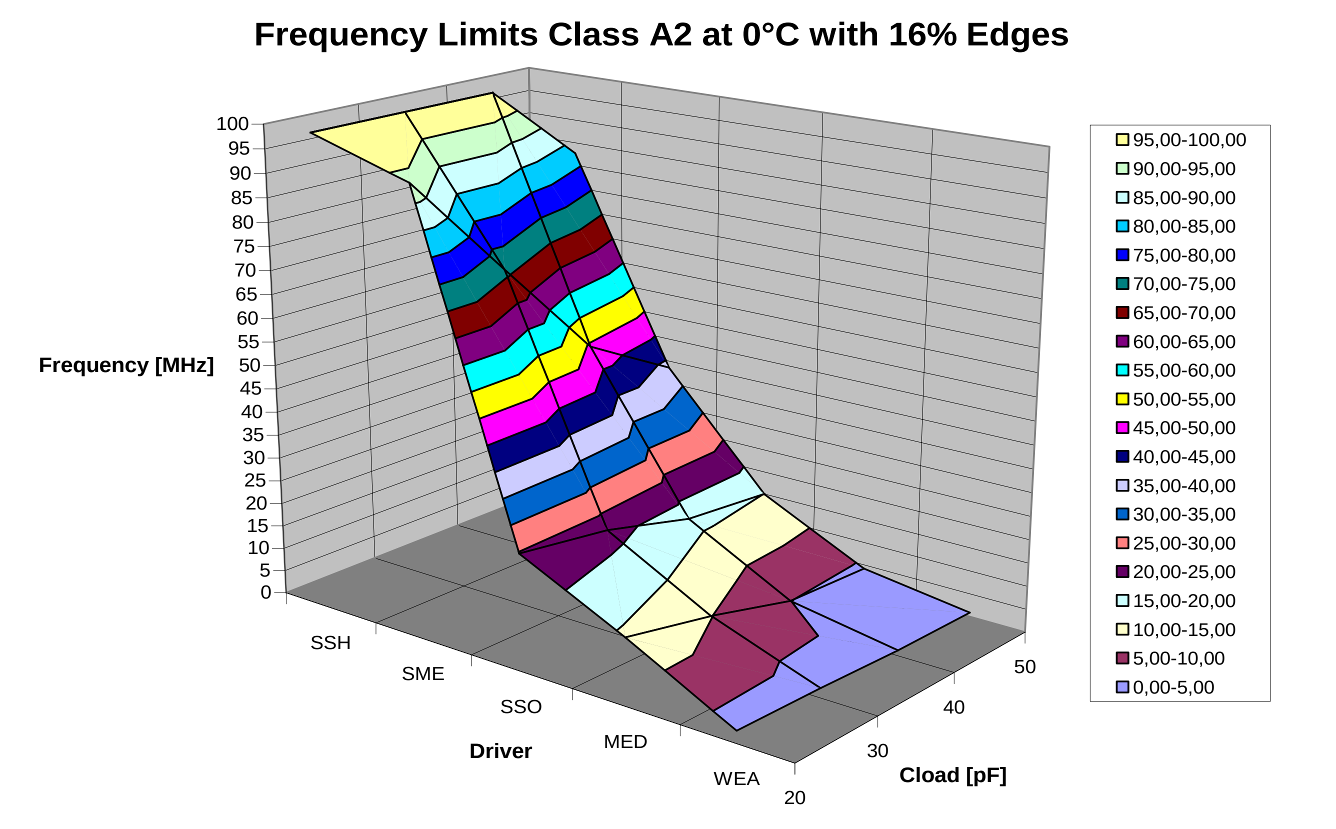


Figure 200: Driver selection decision graph for Class A drivers at T_A=0°C; edges occupy 1/6 period

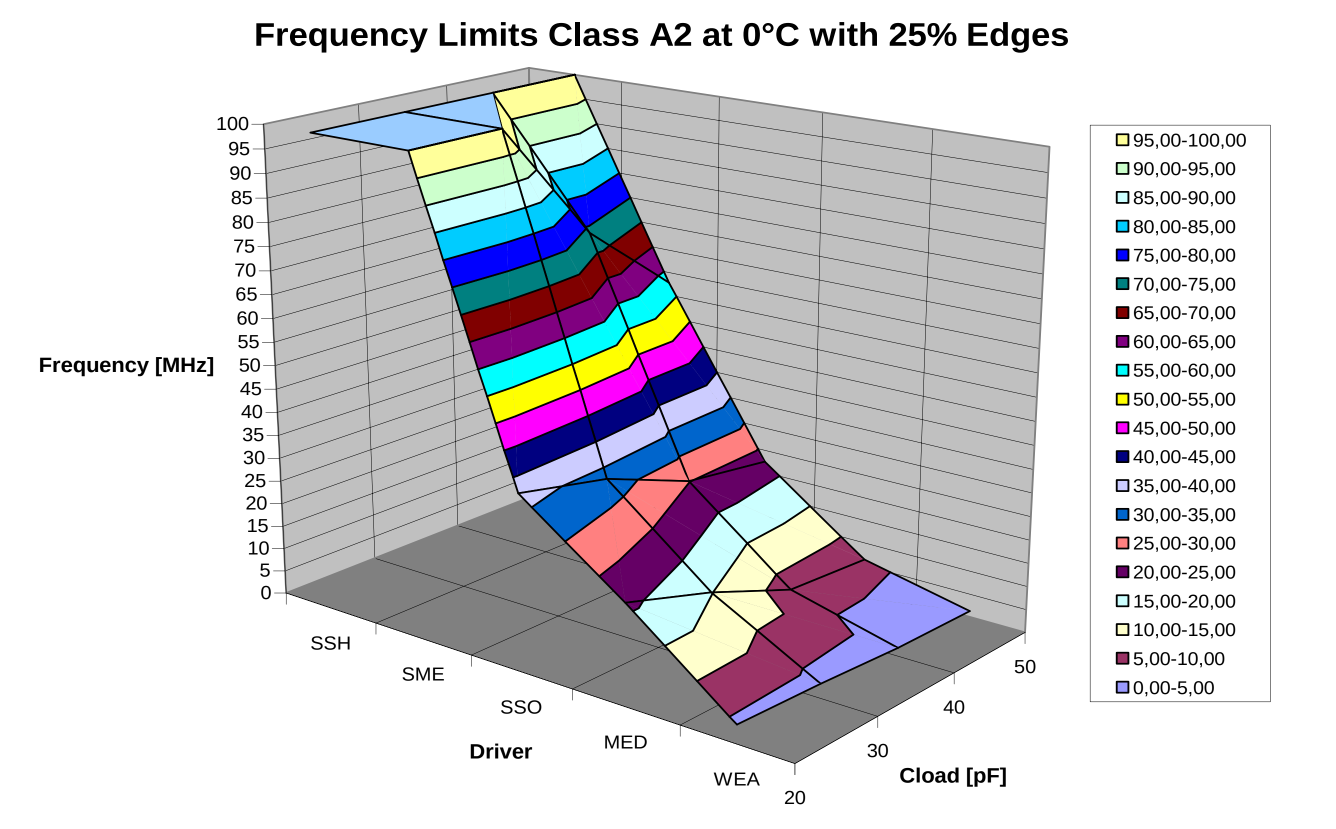


Figure 201: Driver selection decision graph for Class A drivers at T_A=0°C; edges occupy 1/4 period

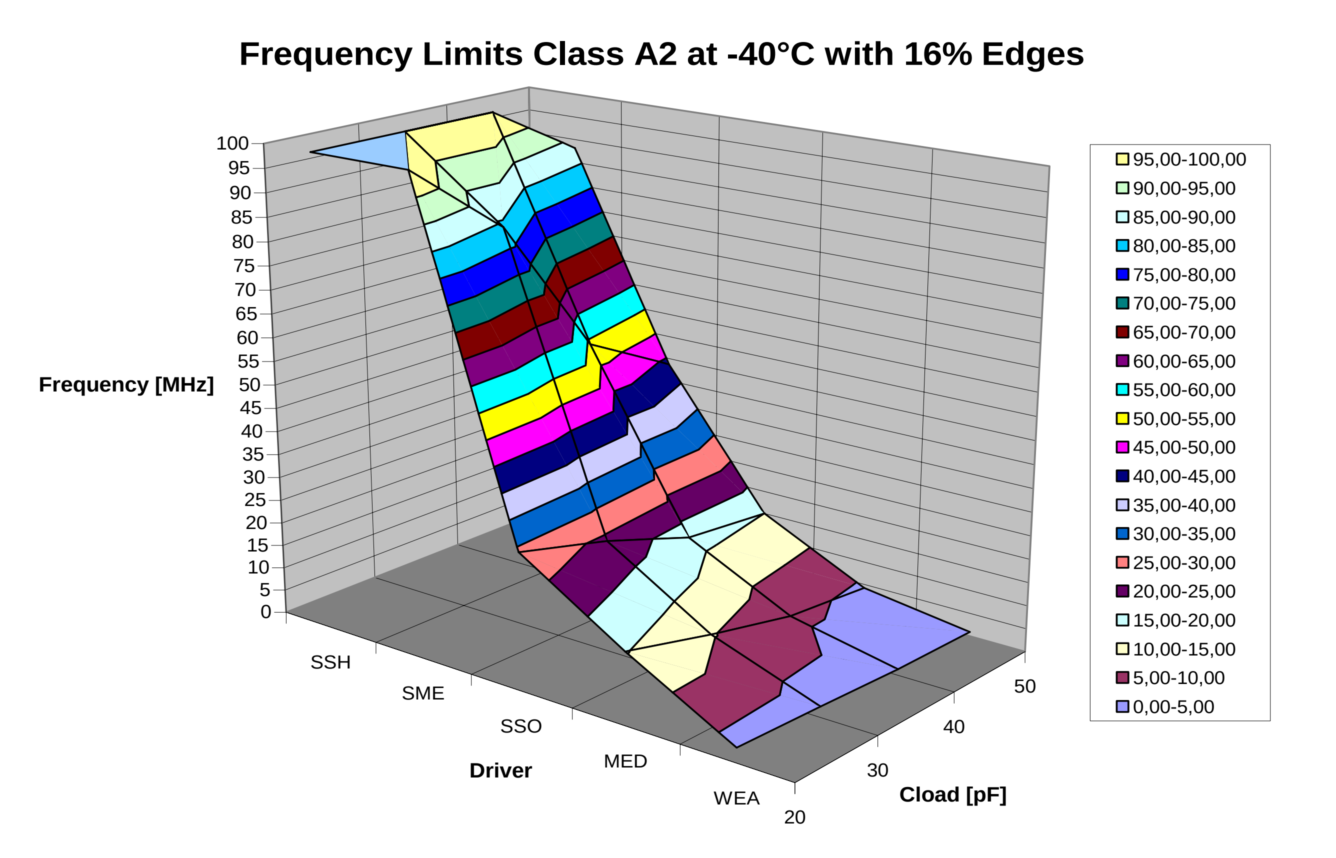


Figure 202: Driver selection decision graph for Class A drivers at T_A=-40°C; edges occupy 1/6 period

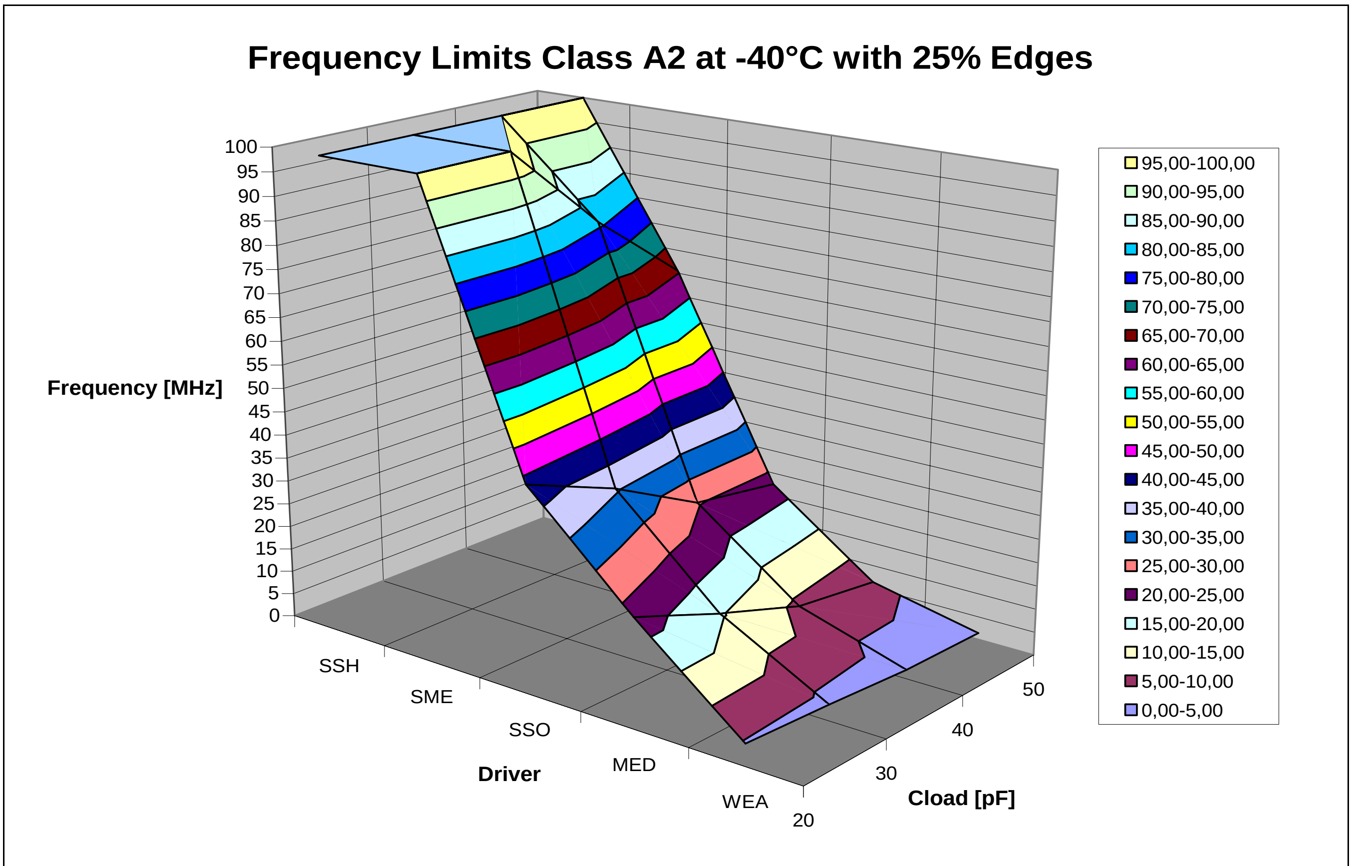


Figure 203: Driver selection decision graph for Class A drivers at T_A=-40°C; edges occupy 1/4 period

7.2.2 Simulated values for Class A2 drivers operated at 3.3V supply

Whereas the diagrams given in chapter 7.2.1 resulted from measurements on a board with simple trace structures, and the load capacitance was formed by a capacitor, the simulation results given in this chapter are derived from simulations of a point-to-point trace as shown in Fig. 204. The load capacitance is formed by an adequate trace length according Table 9.

The simulation results are more conservative than the measurement results, i.e. longer traces with vias delay the signals up to ca. 20% compared to a short trace without vias.

To stay on the safe side, the values from simulation should be taken for driver strength decisions.

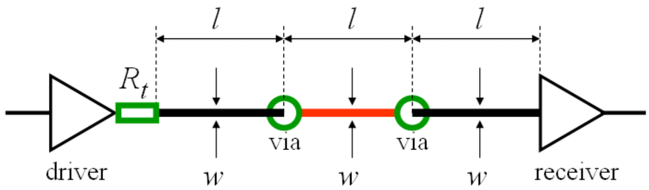


Figure 204: Point-to-point trace used for timing simulations

Structure	Load	Length "*l*"	Width "*w*"
Point-to-Point	20 pF	5.1 cm	300 µm
	30 pF	8.5 cm	300 µm
	40pF	11.9 cm	300 µm
	50 pF	15.3 cm	300 µm

Table 9: Point-to-point trace dimensions

125°C		20	30	40	50
	SSH	152,59	141,98	70,99	44,00
	SME	36,58	31,71	22,04	17,12
	SSO	14,15	12,40	10,47	9,07
	MED	5,46	4,81	3,81	3,45
	WEA	0,84	0,73	0,66	0,60

110°C		20	30	40	50
	SSH	160,42	146,92	74,86	47,57
	SME	39,42	33,10	23,25	18,08
	SSO	15,03	13,31	11,27	9,81
	MED	5,92	5,19	4,15	3,76
	WEA	0,93	0,80	0,72	0,66

85°C		20	30	40	50
	SSH	175,42	153,82	82,34	54,99
	SME	45,28	35,69	25,58	19,93
	SSO	16,75	15,15	12,93	11,36
	MED	6,88	5,98	4,89	4,40
	WEA	1,14	0,98	0,87	0,79

30°C		20	30	40	50
	SSH	212,40	167,80	105,56	83,75
	SME	67,29	43,11	32,83	25,73
	SSO	22,41	21,78	19,09	17,38
	MED	10,71	8,97	7,35	6,23
	WEA	2,30	1,85	1,57	1,38

Table 10: Simulated maximal toggle rates [MHz] for all Class A2 driver settings operated at 3.3V with capacitive loads of 20..50pF; 16% edges

125°C		20	30	40	50
	SSH	228,89	212,97	106,48	66,00
	SME	54,87	47,57	33,06	25,68
	SSO	21,23	18,61	15,70	13,60
	MED	8,20	7,22	5,71	5,18
	WEA	1,26	1,09	0,99	0,90

110°C		20	30	40	50
	SSH	240,63	220,38	112,29	71,35
	SME	59,13	49,64	34,87	27,12
	SSO	22,54	19,96	16,91	14,72
	MED	8,88	7,79	6,23	5,63
	WEA	1,40	1,21	1,09	0,99

85°C		20	30	40	50
	SSH	263,14	230,73	123,52	82,49
	SME	67,92	53,53	38,37	29,90
	SSO	25,13	22,72	19,39	17,03
	MED	10,33	8,97	7,34	6,59
	WEA	1,72	1,46	1,31	1,19

30°C		20	30	40	50
	SSH	318,60	251,70	158,34	125,63
	SME	100,93	64,67	49,24	38,60
	SSO	33,62	32,66	28,64	26,07
	MED	16,07	13,46	11,03	9,35
	WEA	3,45	2,77	2,35	2,07

Table 11: Simulated maximal toggle rates [MHz] for all Class A2 driver settings operated at 3.3V with capacitive loads of 20..50pF; 25% edges

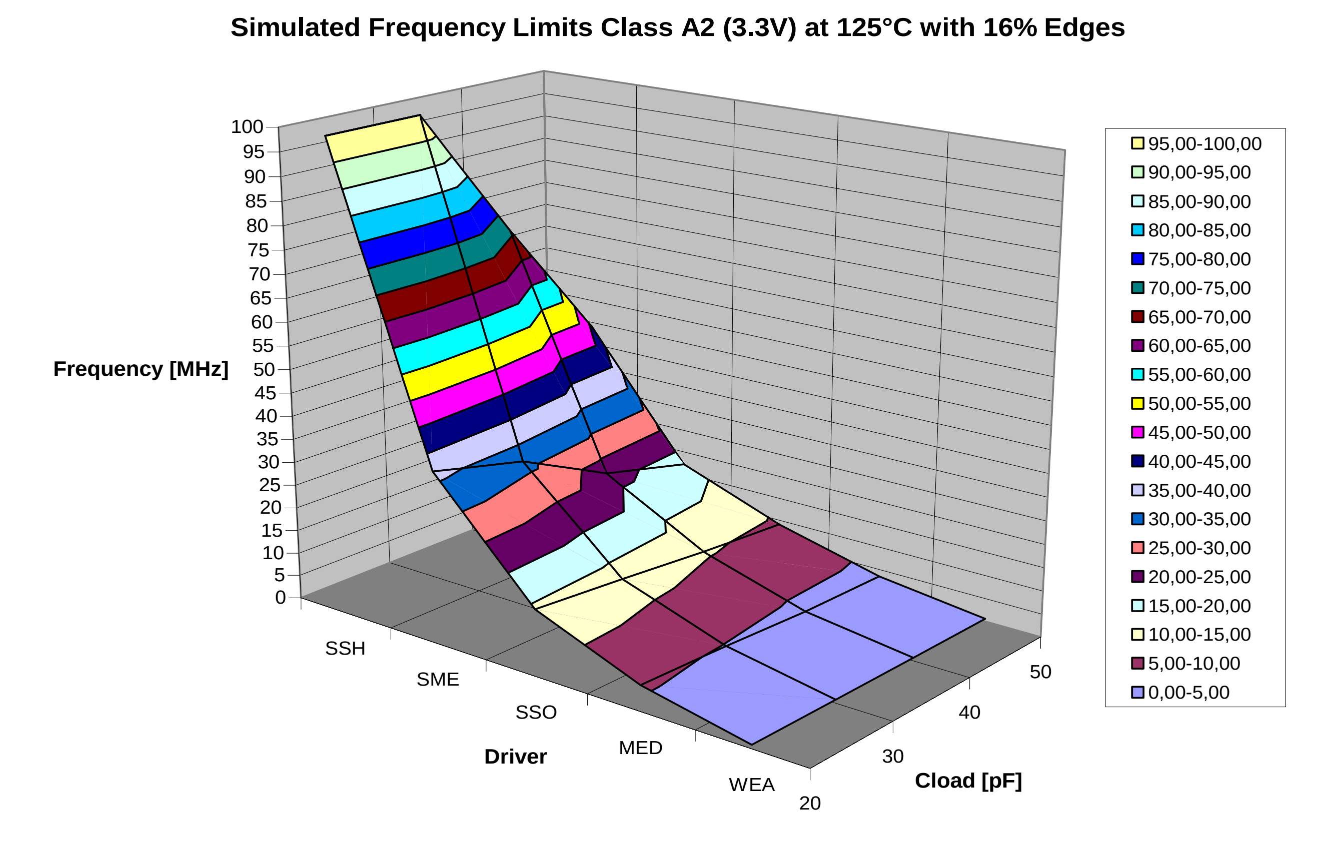


Figure 205: Driver selection decision graph for Class A drivers at T_A=125°C; edges occupy 1/6 period

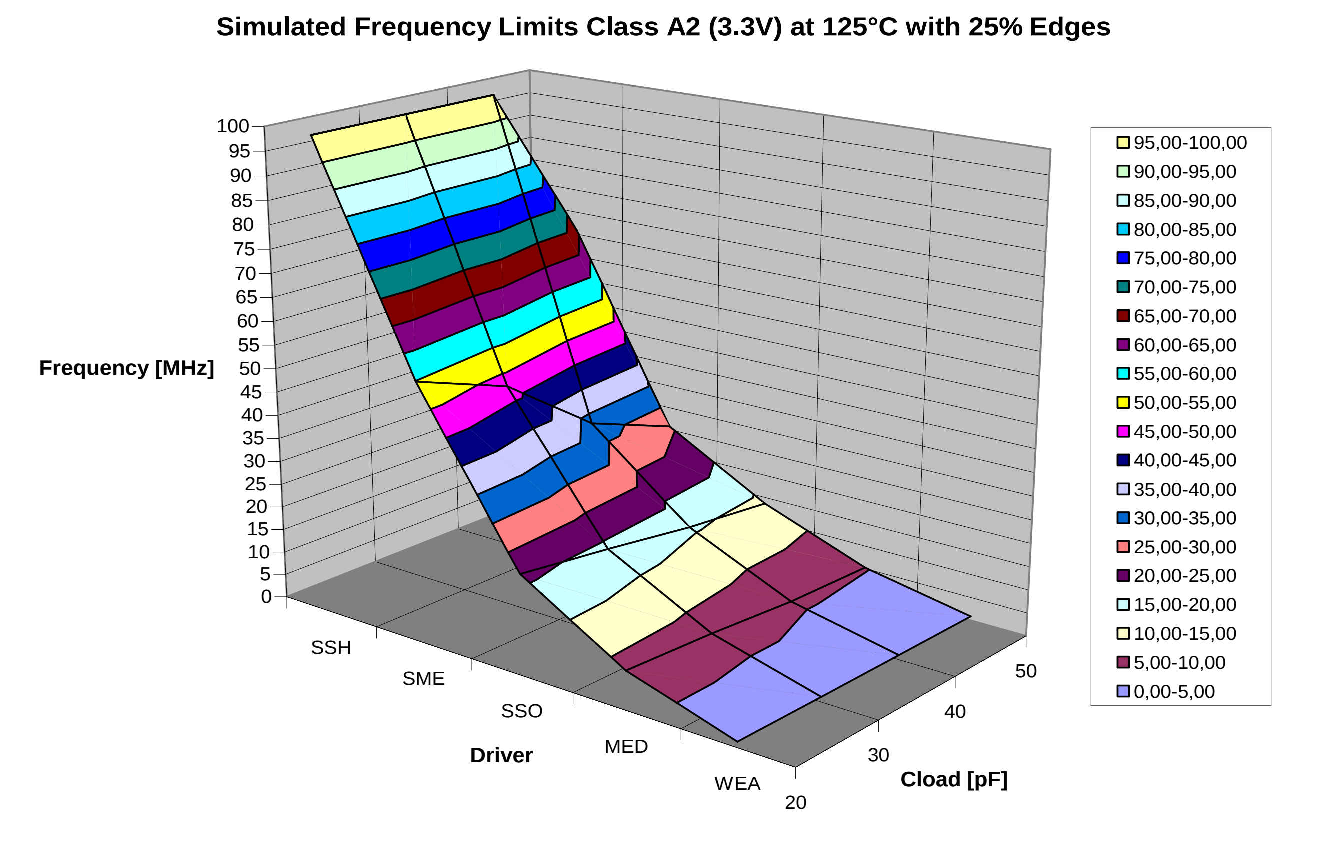


Figure 206: Driver selection decision graph for Class A drivers at T_A=125°C; edges occupy 1/4 period

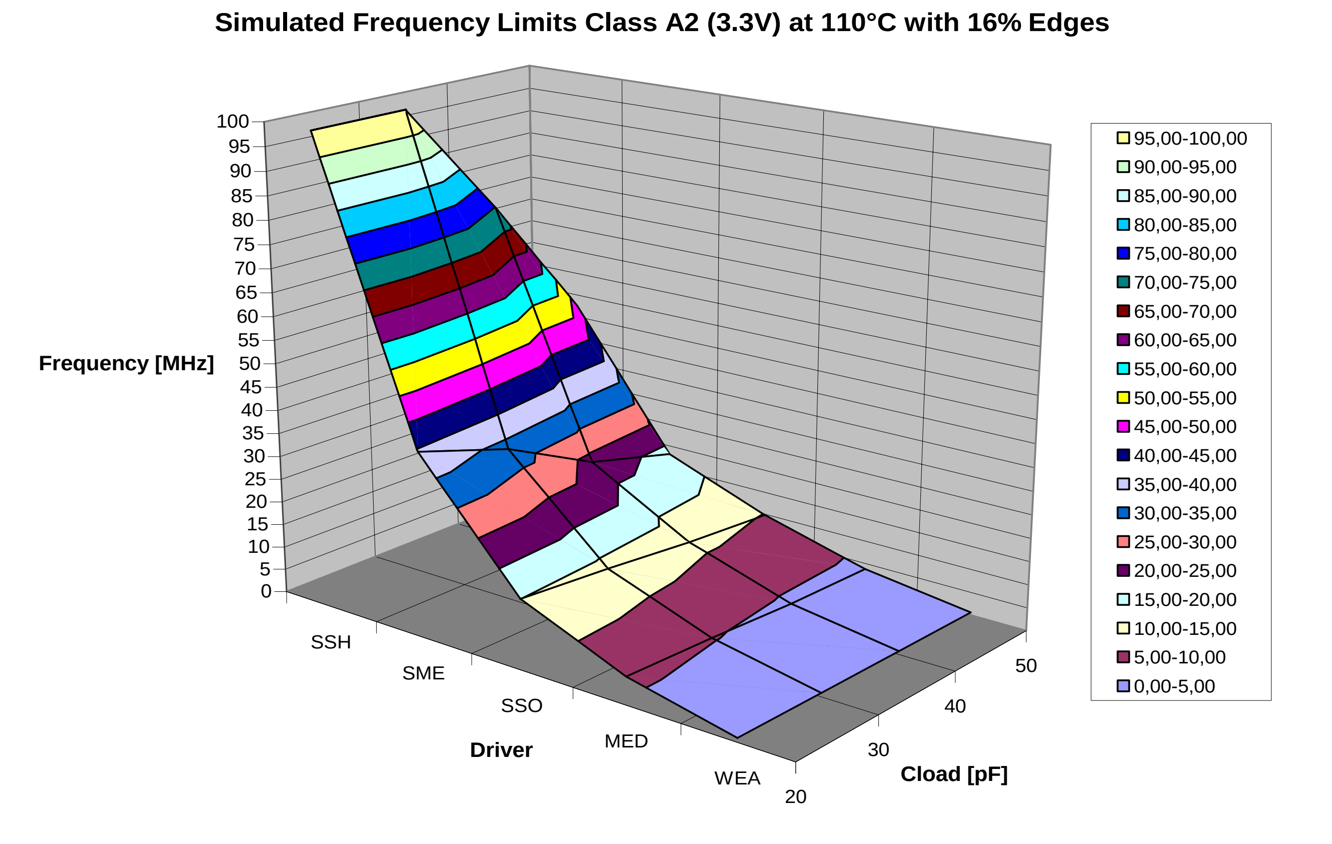


Figure 207: Driver selection decision graph for Class A drivers at T_A=110°C; edges occupy 1/6 period

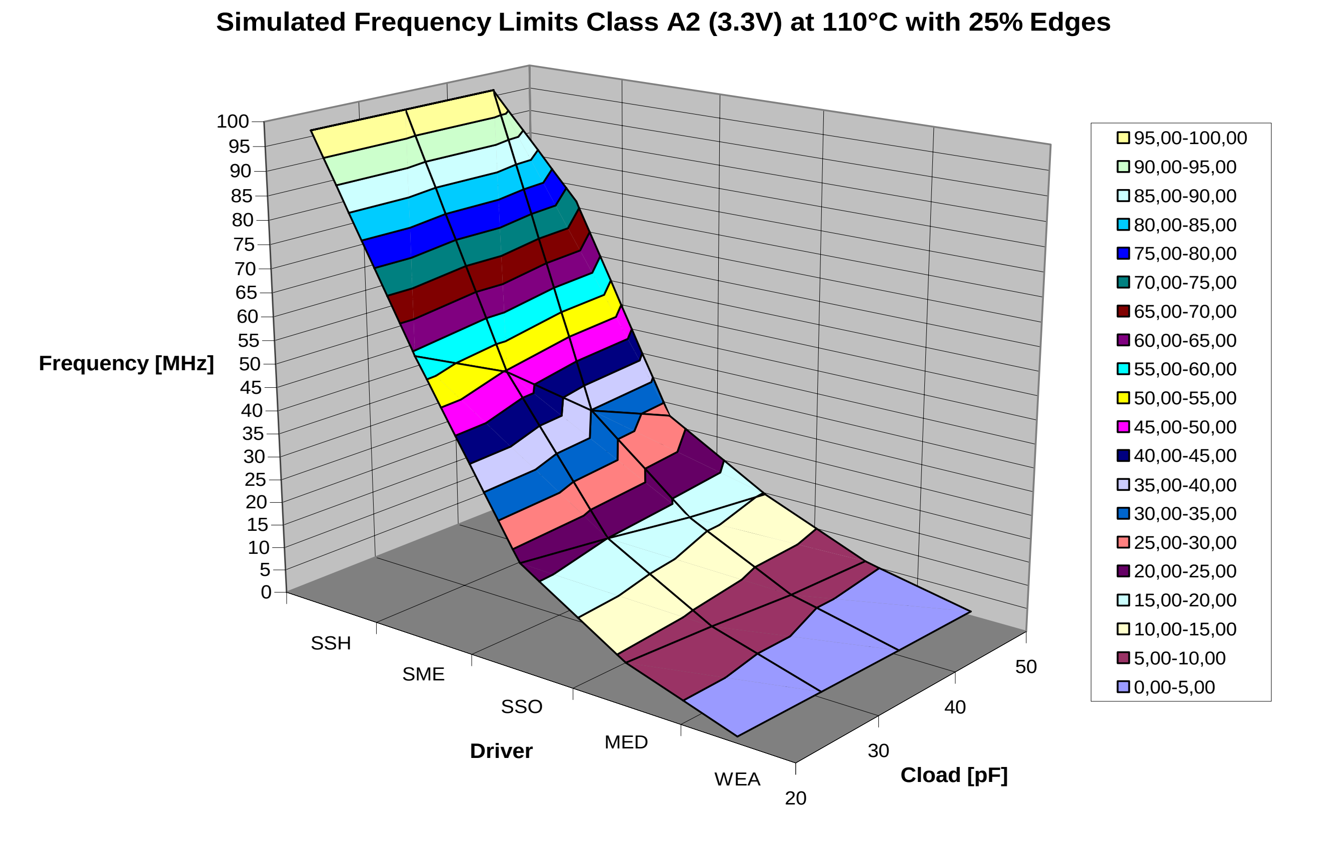


Figure 208: Driver selection decision graph for Class A drivers at T_A=110°C; edges occupy 1/4 period

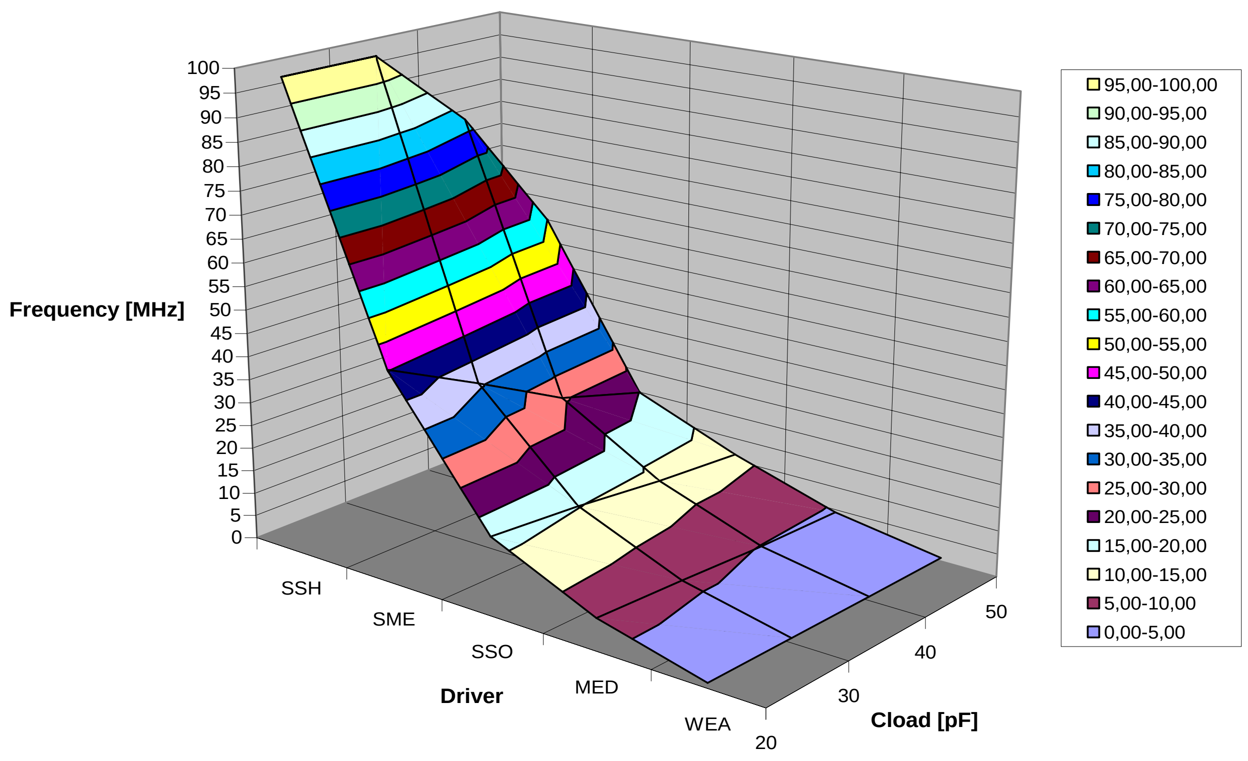


Figure 209: Driver selection decision graph for Class A drivers at T_A=85°C; edges occupy 1/6 period

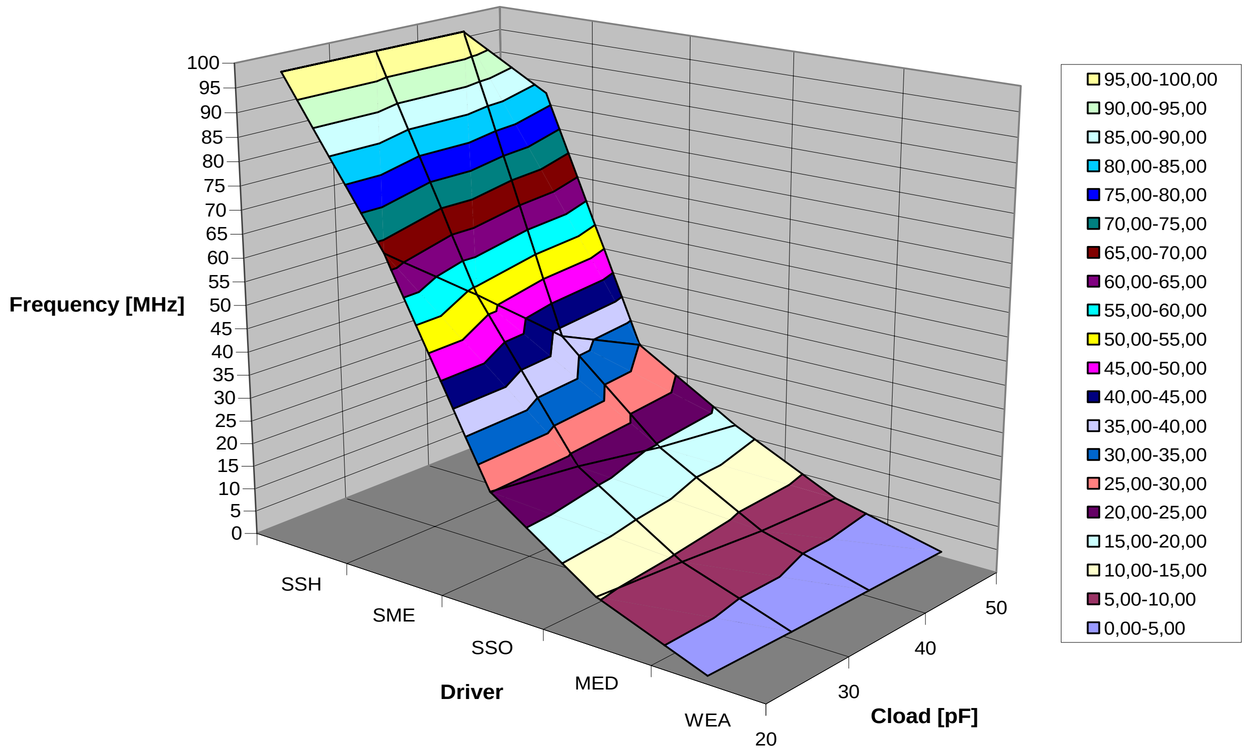


Figure 210: Driver selection decision graph for Class A drivers at T_A=85°C; edges occupy 1/4 period

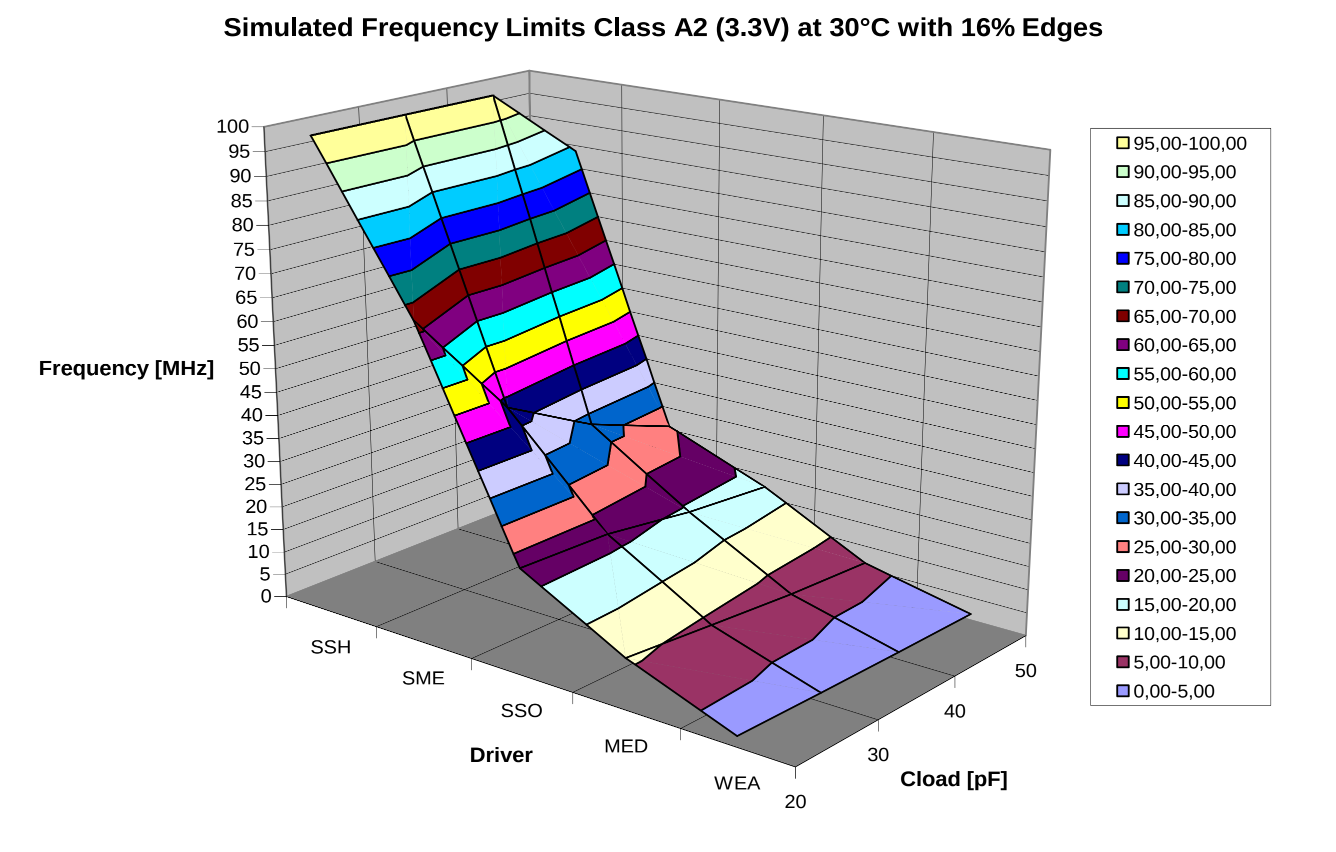


Figure 211: Driver selection decision graph for Class A drivers at T_A=30°C; edges occupy 1/6 period

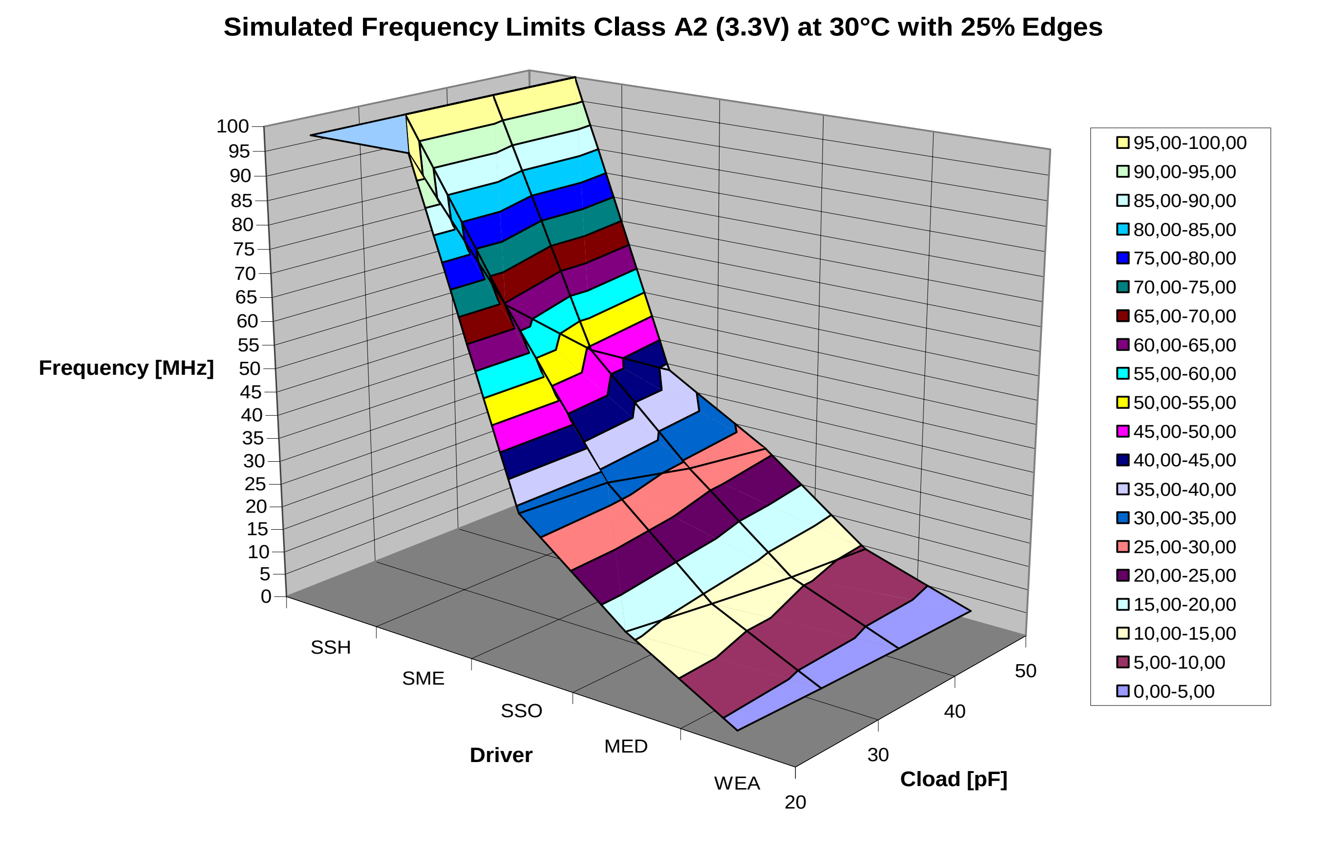


Figure 212: Driver selection decision graph for Class A drivers at T_A=30°C; edges occupy 1/4 period

7.2.3 Simulated values for Class B2 drivers operated at 3.3V supply

The simulation results given in this chapters are derived from simulations of a point-to-point trace as shown in Fig. 213. The load capacitance is formed by an adequate trace length according Table 12.

The simulation results are more conservative than the measurement results, i.e. longer traces with vias delay the signals up to ca. 20% compared to a short trace without vias.

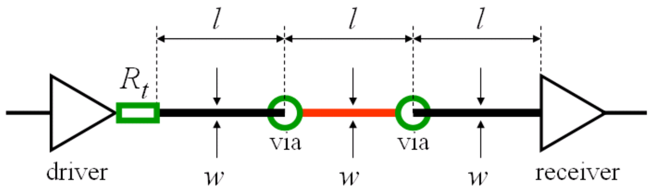


Figure 213: Point-to-point trace used for timing simulations

The Class B2 drivers used in the TC1796 EBU do not offer a software controlled driver scaling, thus the decision diagrams given in Fig. 214-221 identify only the frequency range which is covered by the default strong-sharp driver setting.

Structure	Load	Length "*l*"	Width "*w*"
Point-to-Point	20 pF	5.1 cm	300 µm
	30 pF	8.5 cm	300 µm
	40pF	11.9 cm	300 µm
	50 pF	15.3 cm	300 µm

Table 12: Point-to-point trace dimensions

125°C		20	30	40	50
	SSH	115,33	95,87	71,03	60,72
	SME	30,90	22,81	22,48	17,97

110°C		20	30	40	50
	SSH	126,81	104,04	77,81	66,75
	SME	33,87	25,39	24,87	19,89

85°C		20	30	40	50
	SSH	152,05	120,92	92,53	79,99
	SME	40,34	31,28	30,22	24,20

30°C		20	30	40	50
	SSH	210,97	188,04	158,47	141,38
	SME	69,54	63,87	57,41	46,25

Table 13: Simulated maximal toggle rates [MHz] for all Class B2 driver settings operated at 3.3V with capacitive loads of 20..50pF; 16% edges

125°C		20	30	40	50
	SSH	172,99	143,81	106,55	91,08
	SME	46,35	34,22	33,72	26,96

110°C		20	30	40	50
	SSH	190,22	156,05	116,72	100,13
	SME	50,81	38,08	37,30	29,84

85°C		20	30	40	50
	SSH	228,07	181,37	138,79	119,99
	SME	60,51	46,92	45,33	36,31

30°C		20	30	40	50
	SSH	316,46	282,06	237,71	212,07
	SME	104,30	95,81	86,12	69,38

Table 14: Simulated maximal toggle rates [MHz] for all Class B2 driver settings operated at 3.3V with capacitive loads of 20..50pF; 25% edges

Note: The values in rows “SME” of the Tables 13 and 14 give the maximum data rate for the strong-medium driver. Since this is not selectable in Class B2 drivers, also lower data rates must be driven by strong-sharp drivers. However, the values in rows “SSH” identify the maximum data rate which can be achieved by the Class B2 drivers under the respective temperature and load conditions.

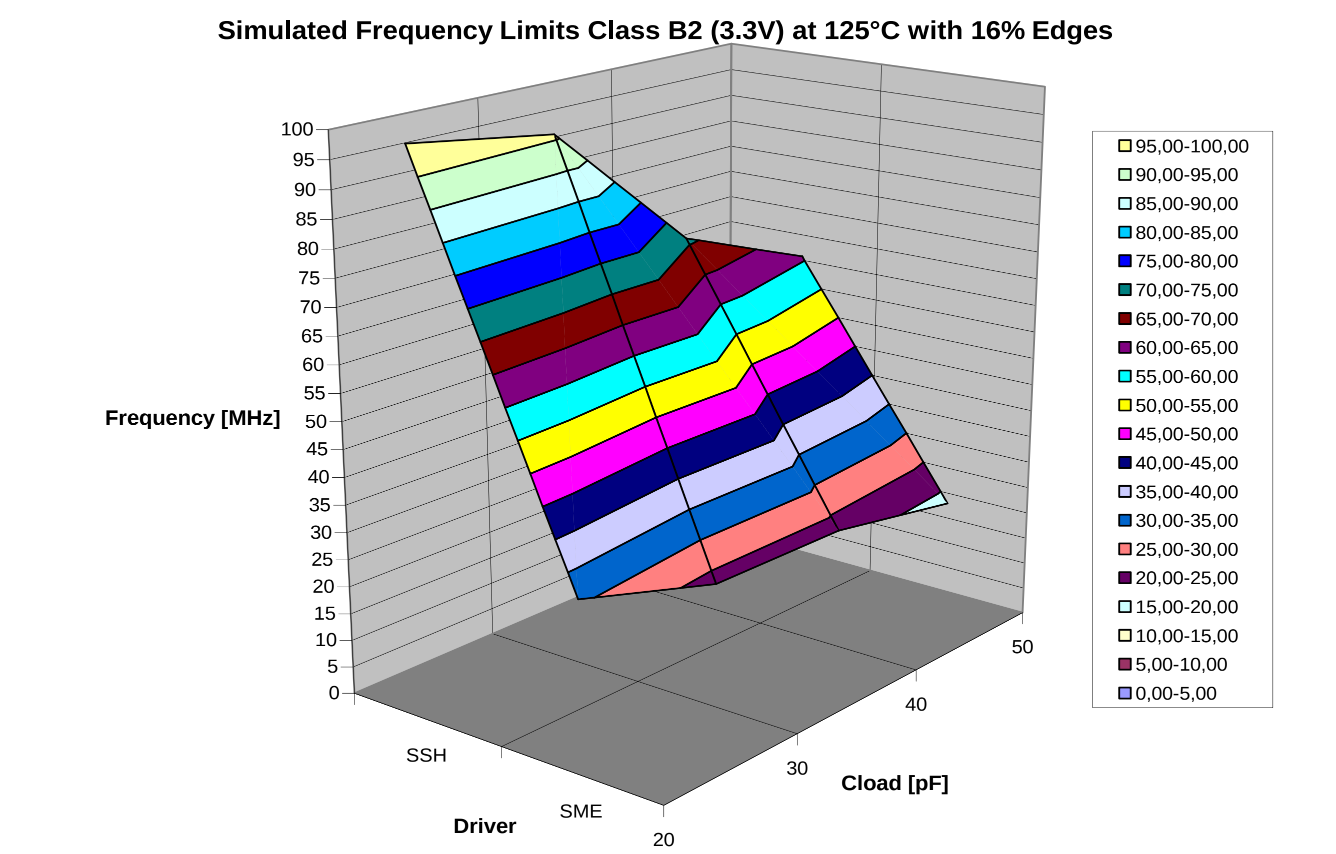


Figure 214: Strong-sharp driver graph for Class B2 drivers at T_A=125°C; edges occupy 1/6 period

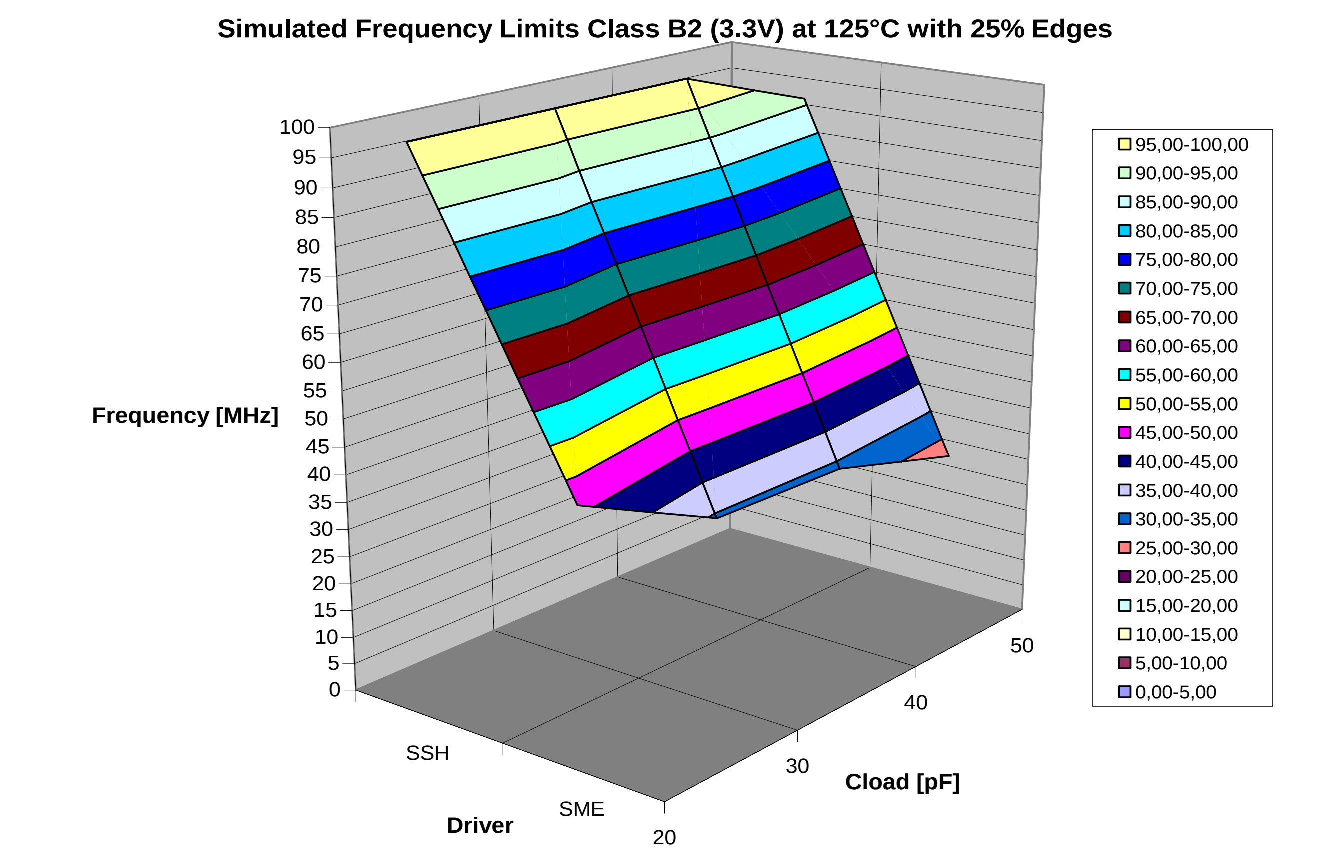


Figure 215: Strong-sharp driver graph for Class B2 drivers at T_A=125°C; edges occupy 1/4 period

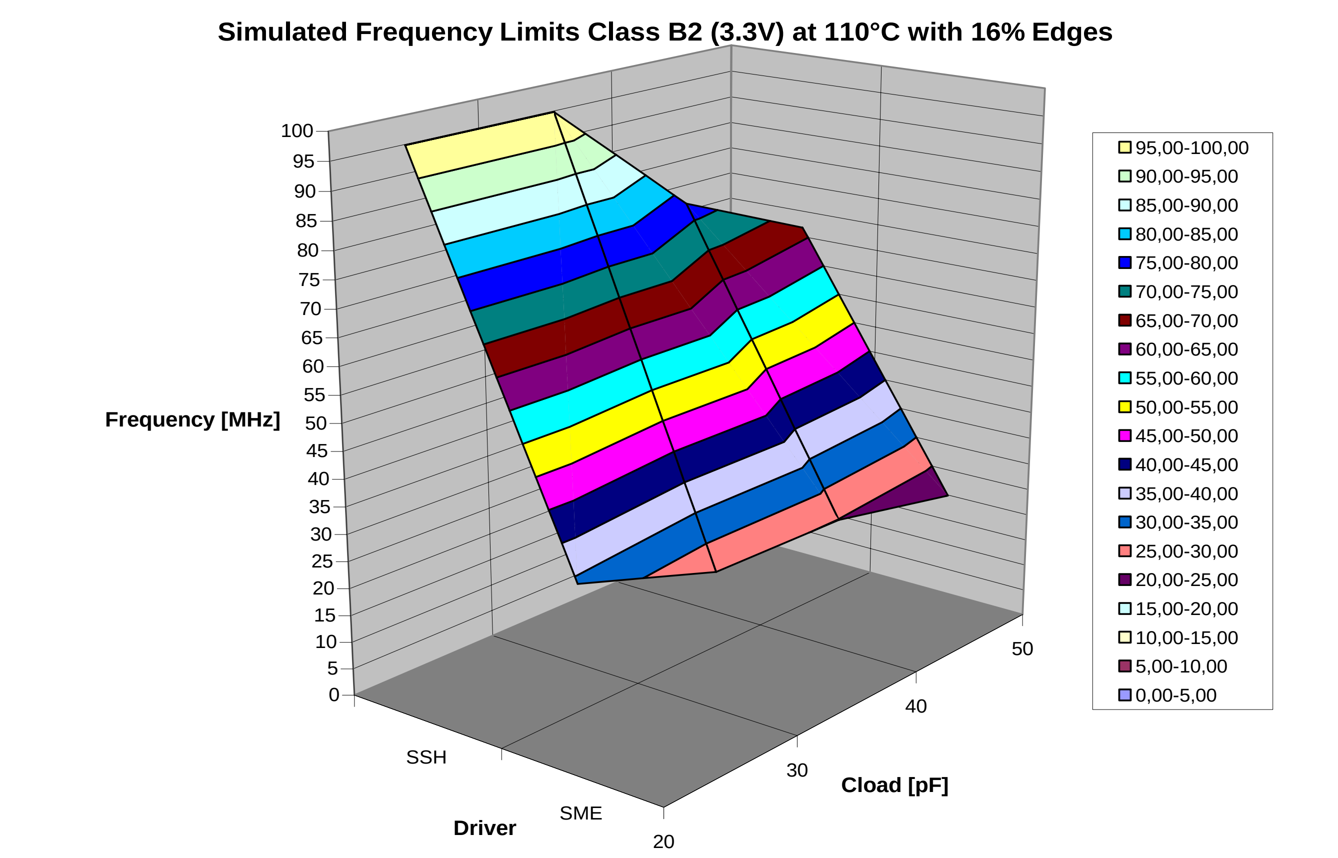


Figure 216: Strong-sharp driver graph for Class B2 drivers at T_A=110°C; edges occupy 1/6 period

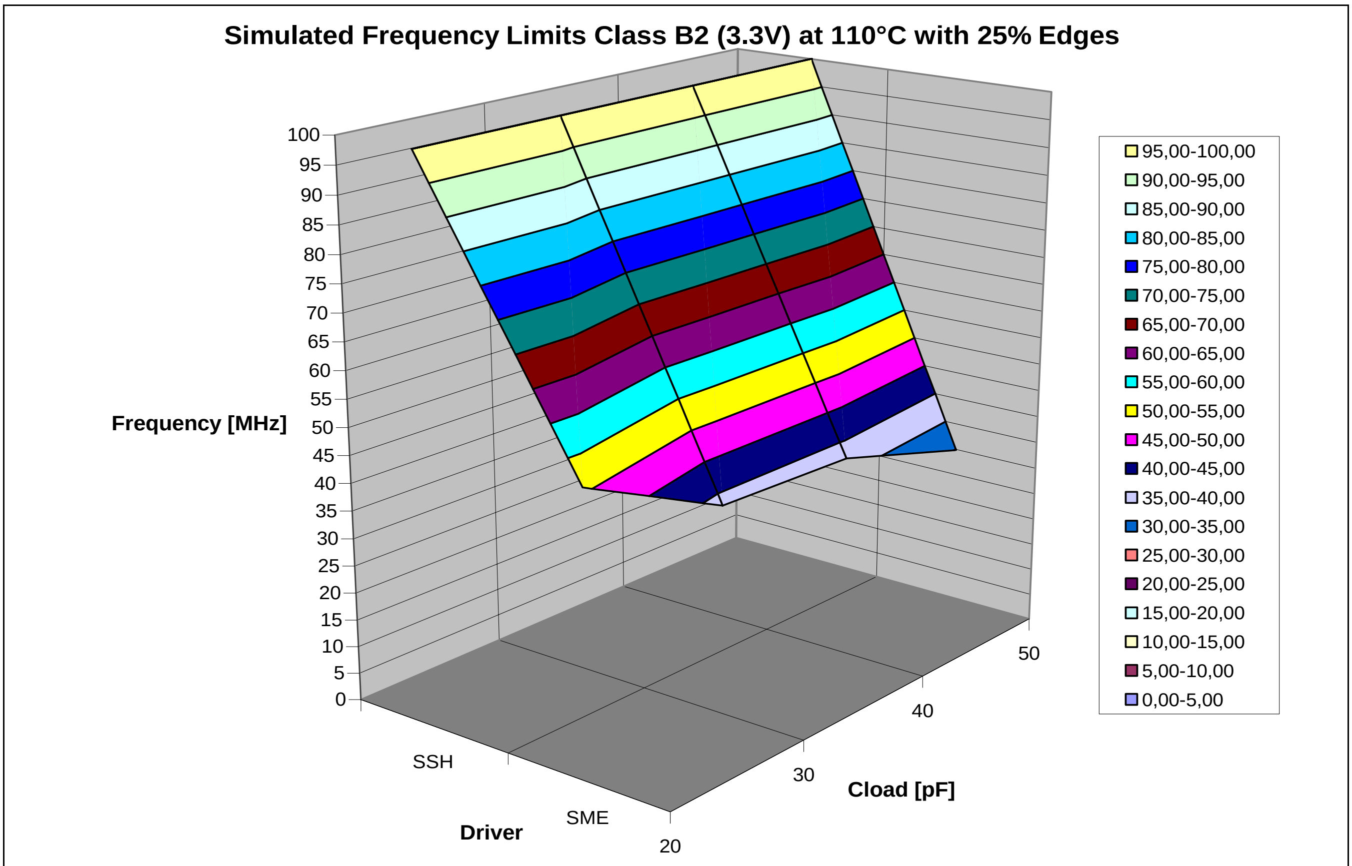


Figure 217: Strong-sharp driver graph for Class B2 drivers at T_A=110°C; edges occupy 1/4 period

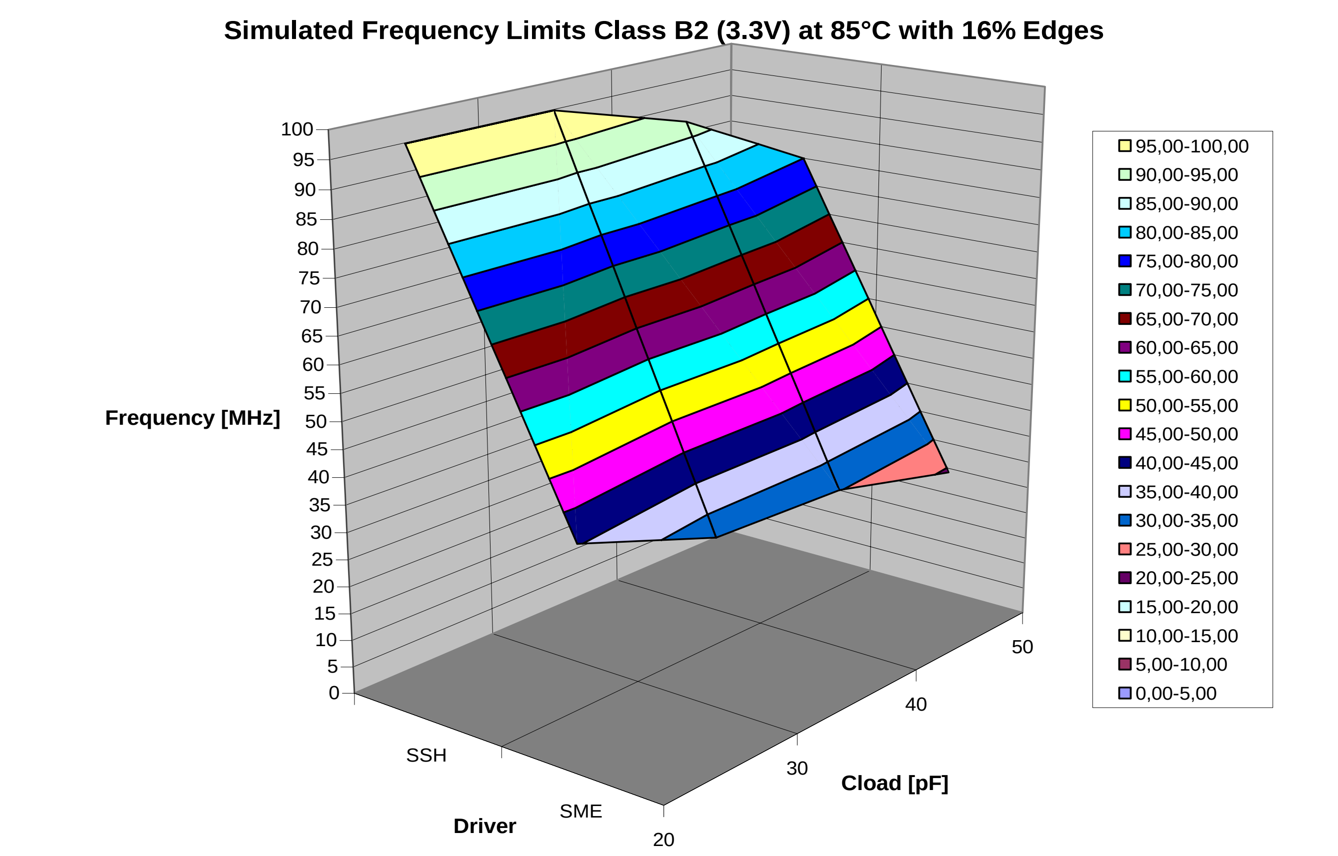


Figure 218: Strong-sharp driver graph for Class B2 drivers at T_A=85°C; edges occupy 1/6 period

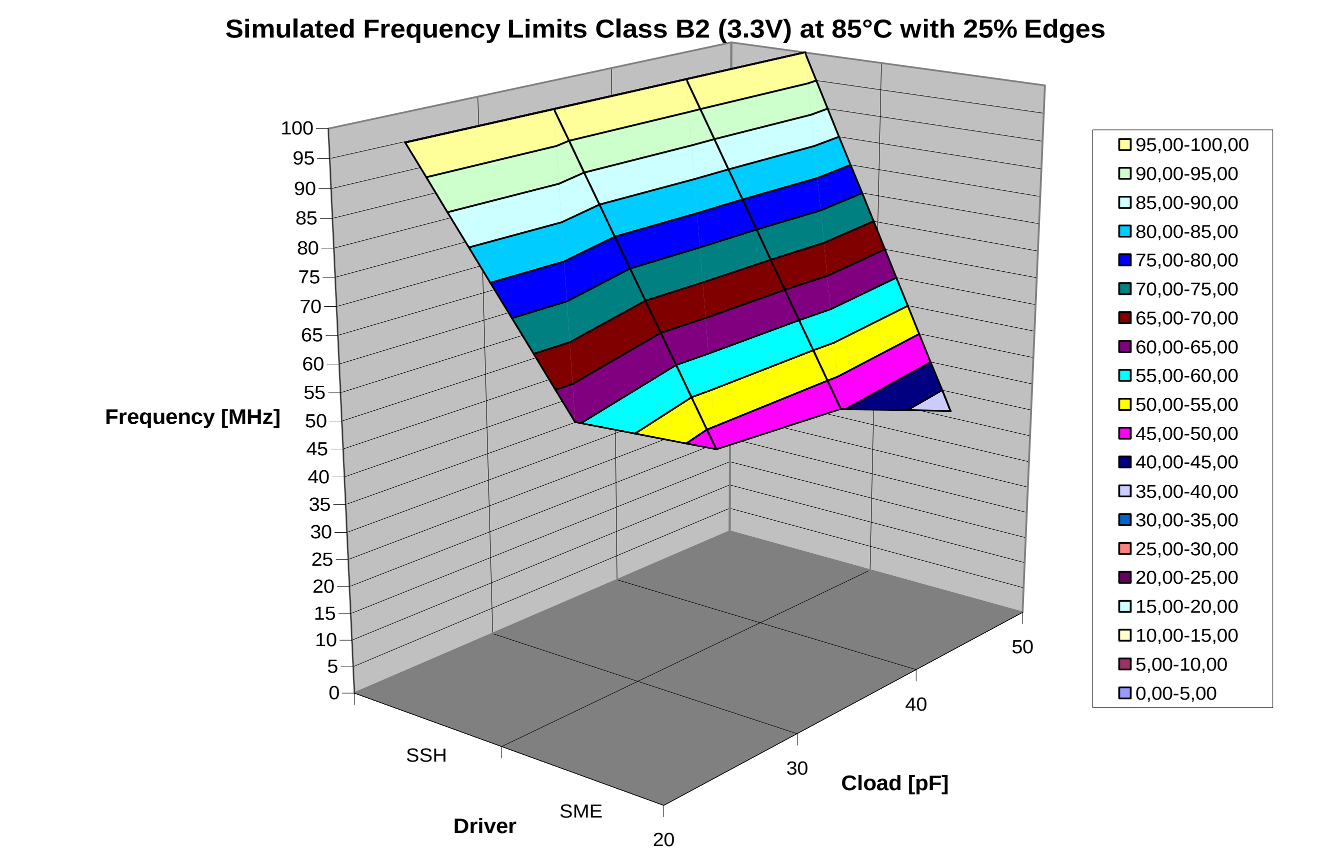


Figure 219: Strong-sharp driver graph for Class B2 drivers at T_A=85°C; edges occupy 1/4 period

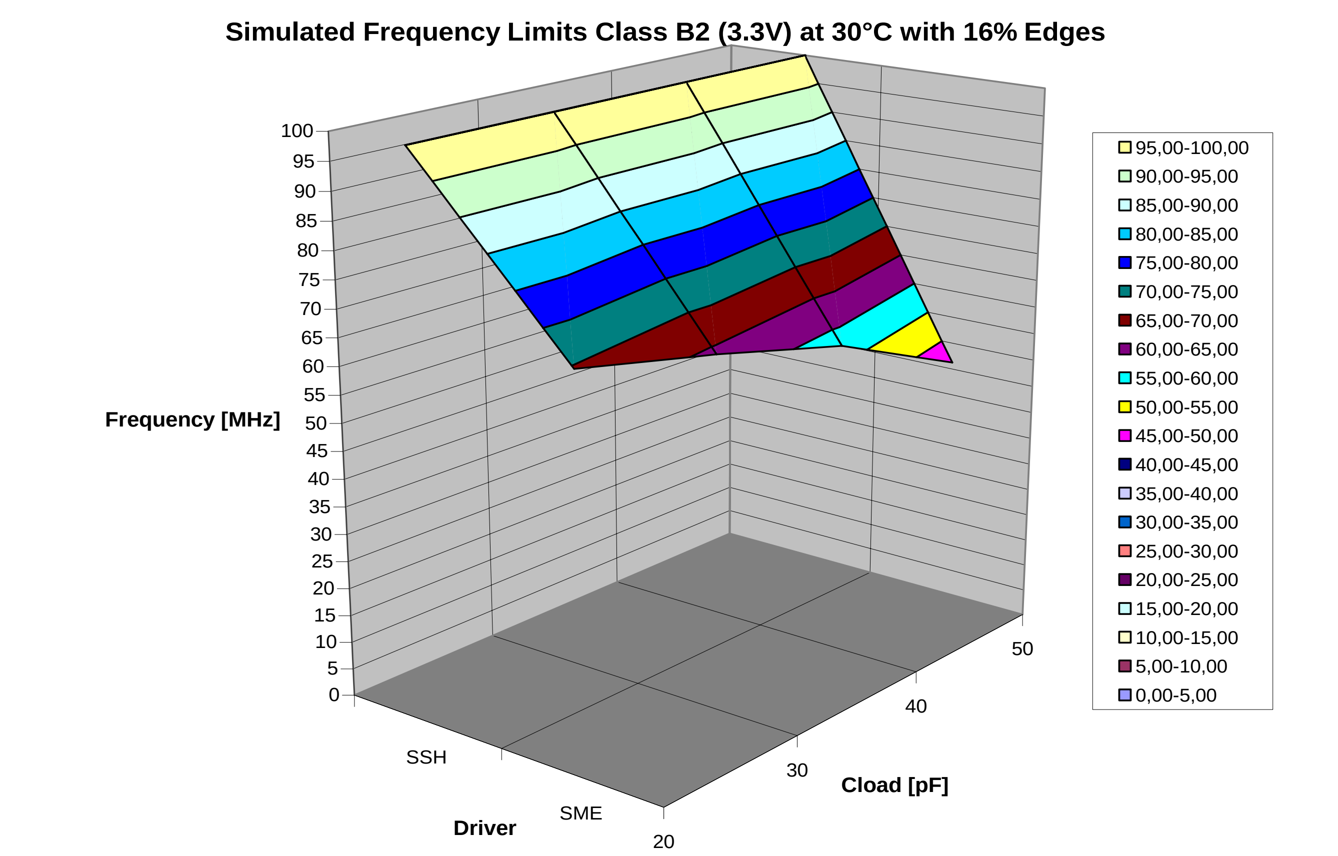


Figure 220: Strong-sharp driver graph for Class B2 drivers at T_A=30°C; edges occupy 1/6 period

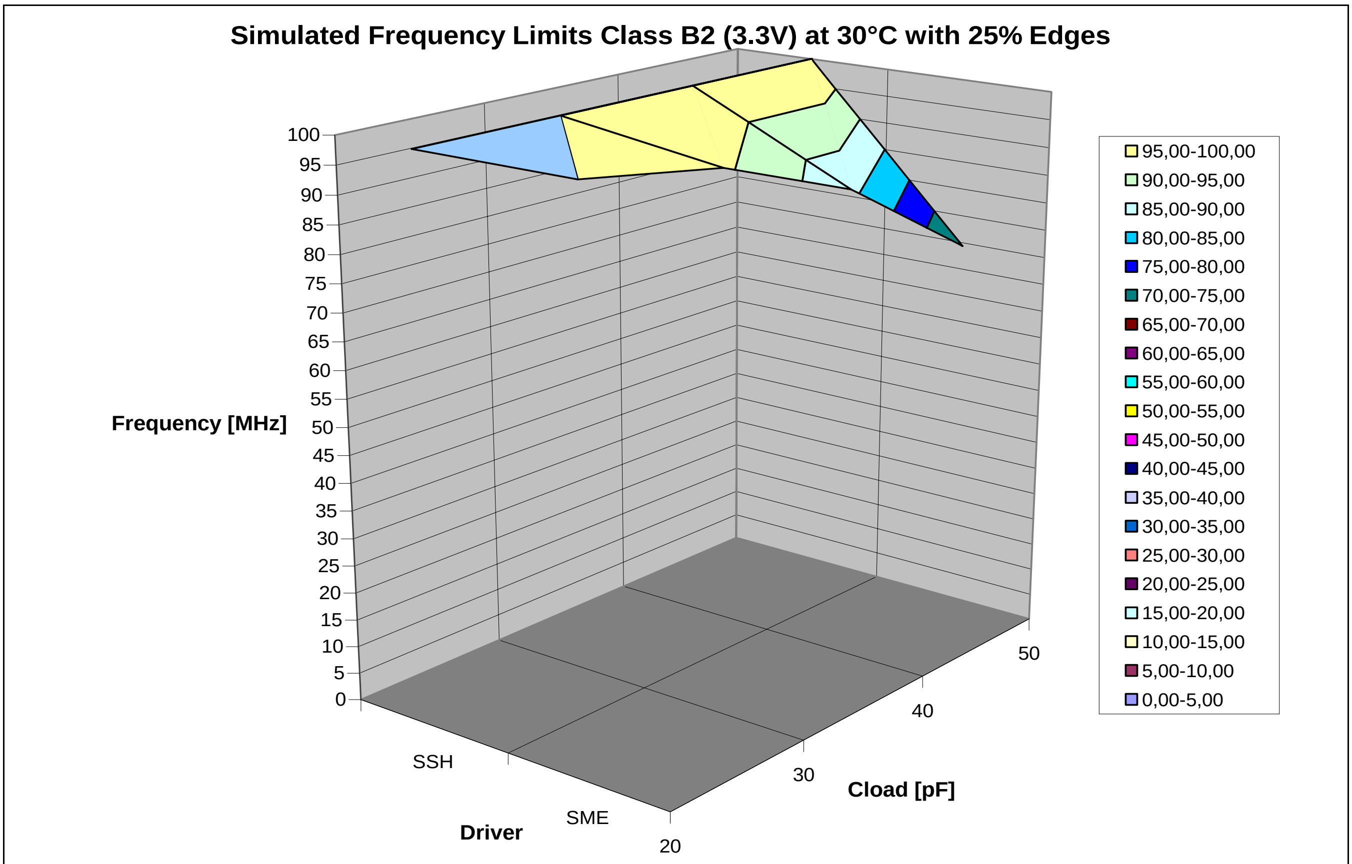


Figure 221: Strong-sharp driver graph for Class B2 drivers at T_A=30°C; edges occupy 1/4period

7.2.4 Simulated values for Class B2 drivers operated at 2.5V supply

The simulation results given in this chapters are derived from simulations of a point-to-point trace as shown in Fig. 222. The load capacitance is formed by an adequate trace length according Table 15.

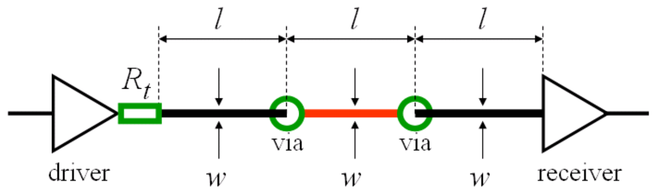


Figure 222: Point-to-point trace used for timing simulations

The simulation results are more conservative than the measurement results, i.e. longer traces with vias delay the signals up to ca. 20% compared to a short trace without vias.

The Class B2 drivers used in the TC1796 EBU do not offer a software controlled driver scaling, thus the decision diagrams given in Fig. 223-230 identify only the frequency range which is covered by the default strong-sharp driver setting.

Structure	Load	Length "*l*"	Width "*w*"
Point-to-Point	20 pF	5.1 cm	300 µm
	30 pF	8.5 cm	300 µm
	40pF	11.9 cm	300 µm
	50 pF	15.3 cm	300 µm

Table 15: Point-to-point trace dimensions

125°C		20	30	40	50
	SSH	115,78	64,57	58,53	49,56
	SME	30,34	23,07	20,27	19,04

110°C		20	30	40	50
	SSH	126,33	71,07	64,28	53,82
	SME	33,81	25,68	22,71	21,30

85°C		20	30	40	50
	SSH	148,93	85,39	76,85	62,81
	SME	41,77	31,62	28,44	26,55

30°C		20	30	40	50
	SSH	210,32	153,42	134,91	99,30
	SME	68,89	64,38	63,90	57,98

Table 16: Simulated maximal toggle rates [MHz] for all Class B2 driver settings operated at 2.5V with capacitive loads of 20..50pF; 16% edges

125°C		20	30	40	50
	SSH	173,68	96,86	87,80	74,34
	SME	45,51	34,61	30,40	28,56

110°C		20	30	40	50
	SSH	189,49	106,60	96,42	80,73
	SME	50,72	38,51	34,07	31,94

85°C		20	30	40	50
	SSH	223,39	128,09	115,28	94,21
	SME	62,66	47,42	42,66	39,82

30°C		20	30	40	50
	SSH	315,48	230,13	202,37	148,95
	SME	103,33	96,57	95,84	86,97

Table 17: Simulated maximal toggle rates [MHz] for all Class B2 driver settings operated at 2.5V with capacitive loads of 20..50pF; 25% edges

Note: The values in rows “SME” of the Tables 17 and 18 give the maximum data rate for the strong-medium driver. Since this is not selectable in Class B2 drivers, also lower data rates must be driven by strong-sharp drivers. However, the values in rows “SSH” identify the maximum data rate which can be achieved by the Class B2 drivers under the respective temperature and load conditions.

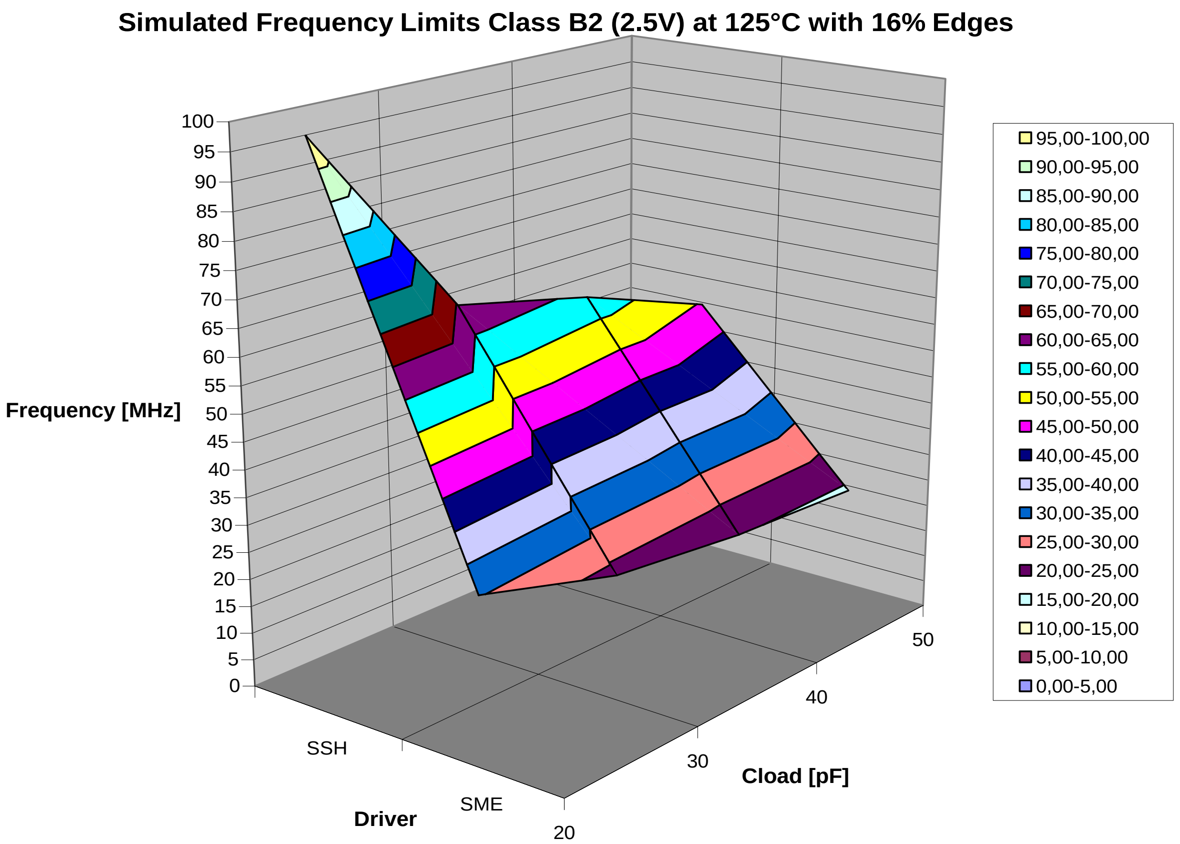


Figure 223: Strong-sharp driver graph for Class B2 drivers at T_A=125°C; edges occupy 1/6 period

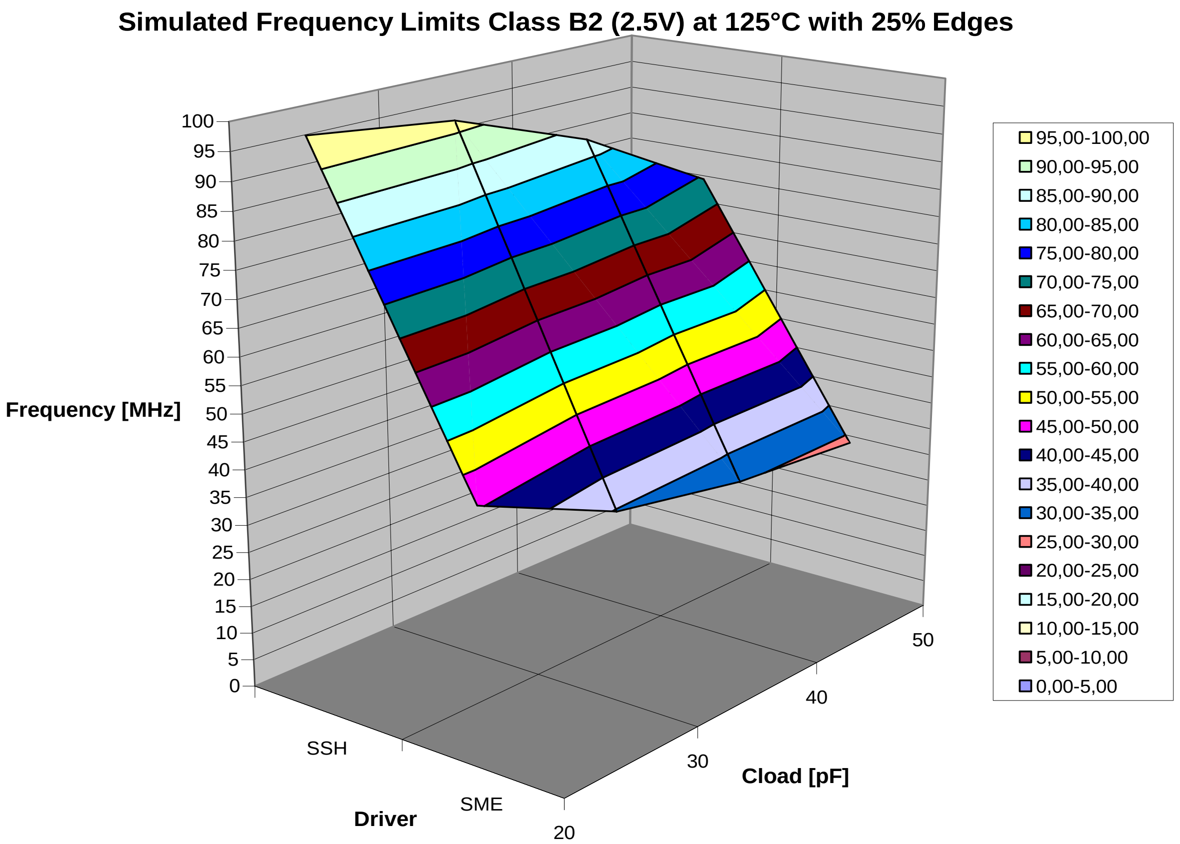


Figure 224: Strong-sharp driver graph for Class B2 drivers at T_A=125°C; edges occupy 1/4 period

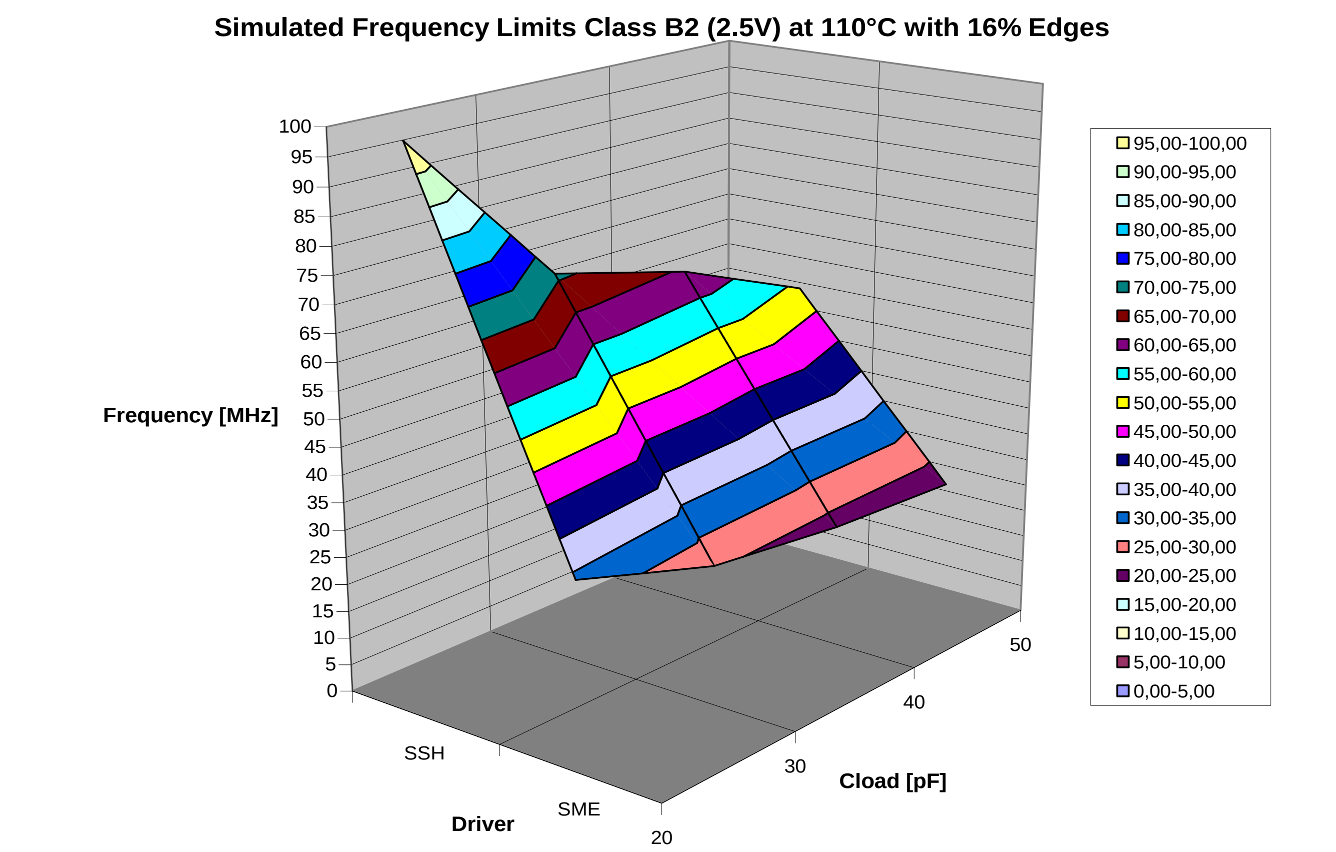


Figure 225: Strong-sharp driver graph for Class B2 drivers at T_A=110°C; edges occupy 1/6 period

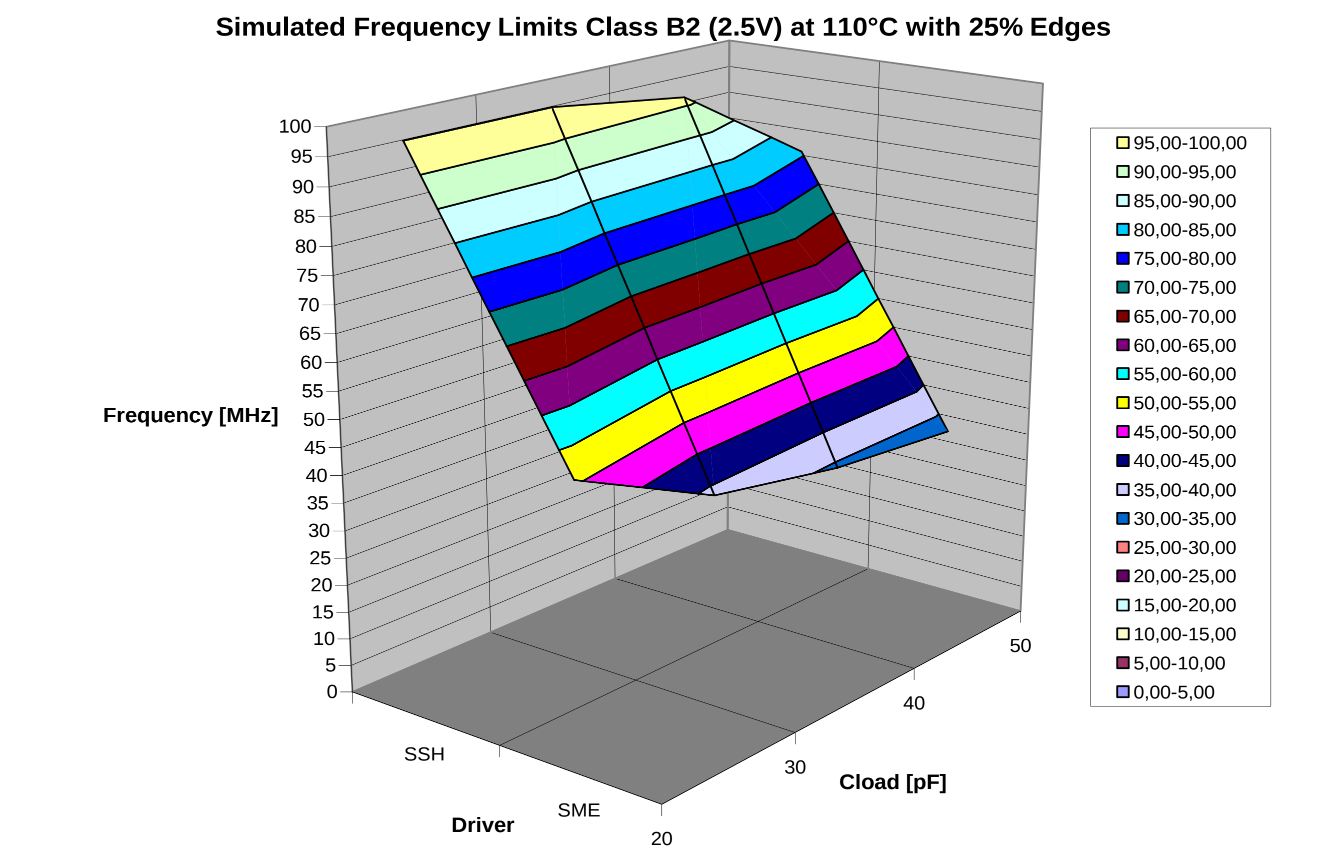


Figure 226: Strong-sharp driver graph for Class B2 drivers at T_A=110°C; edges occupy 1/4 period

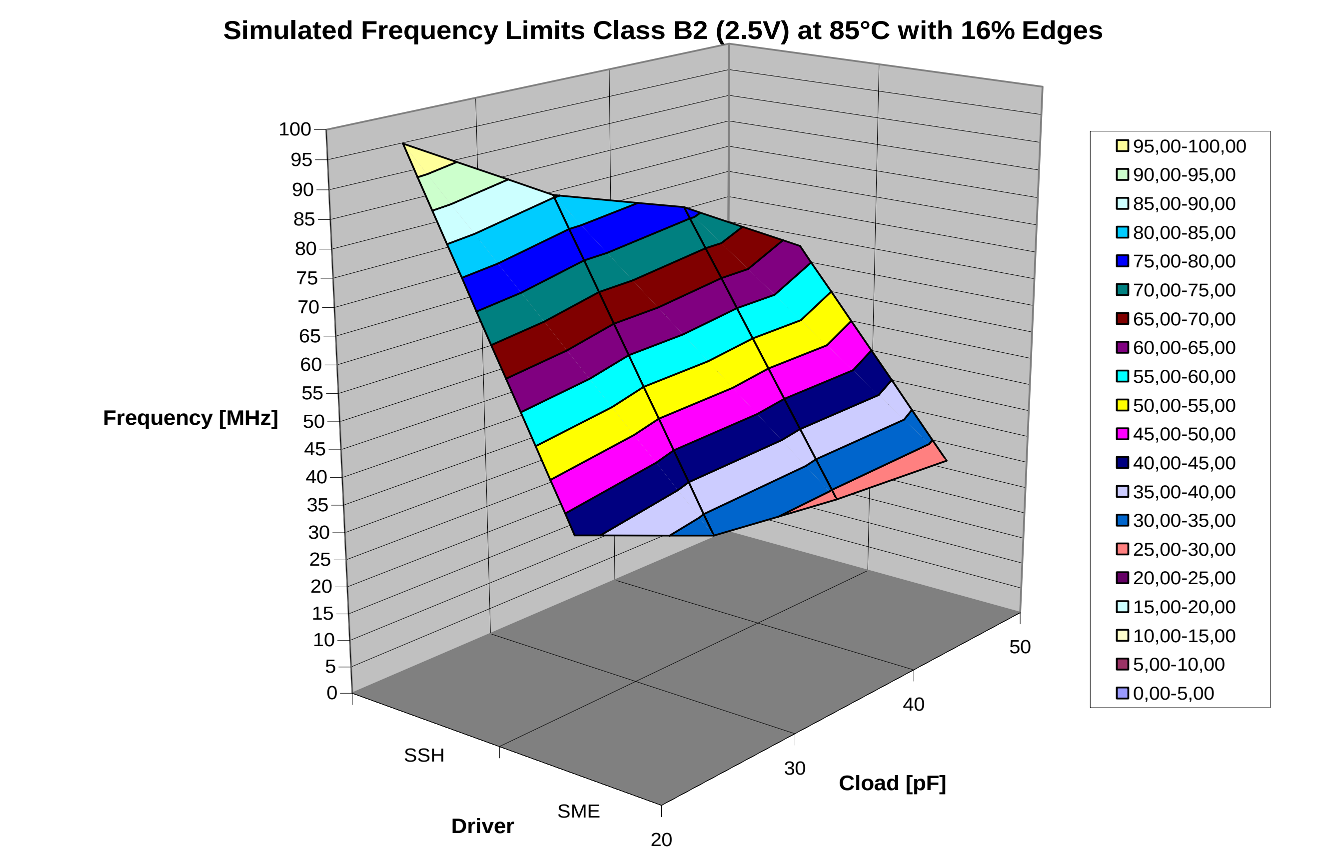


Figure 227: Strong-sharp driver graph for Class B2 drivers at T_A=85°C; edges occupy 1/6 period

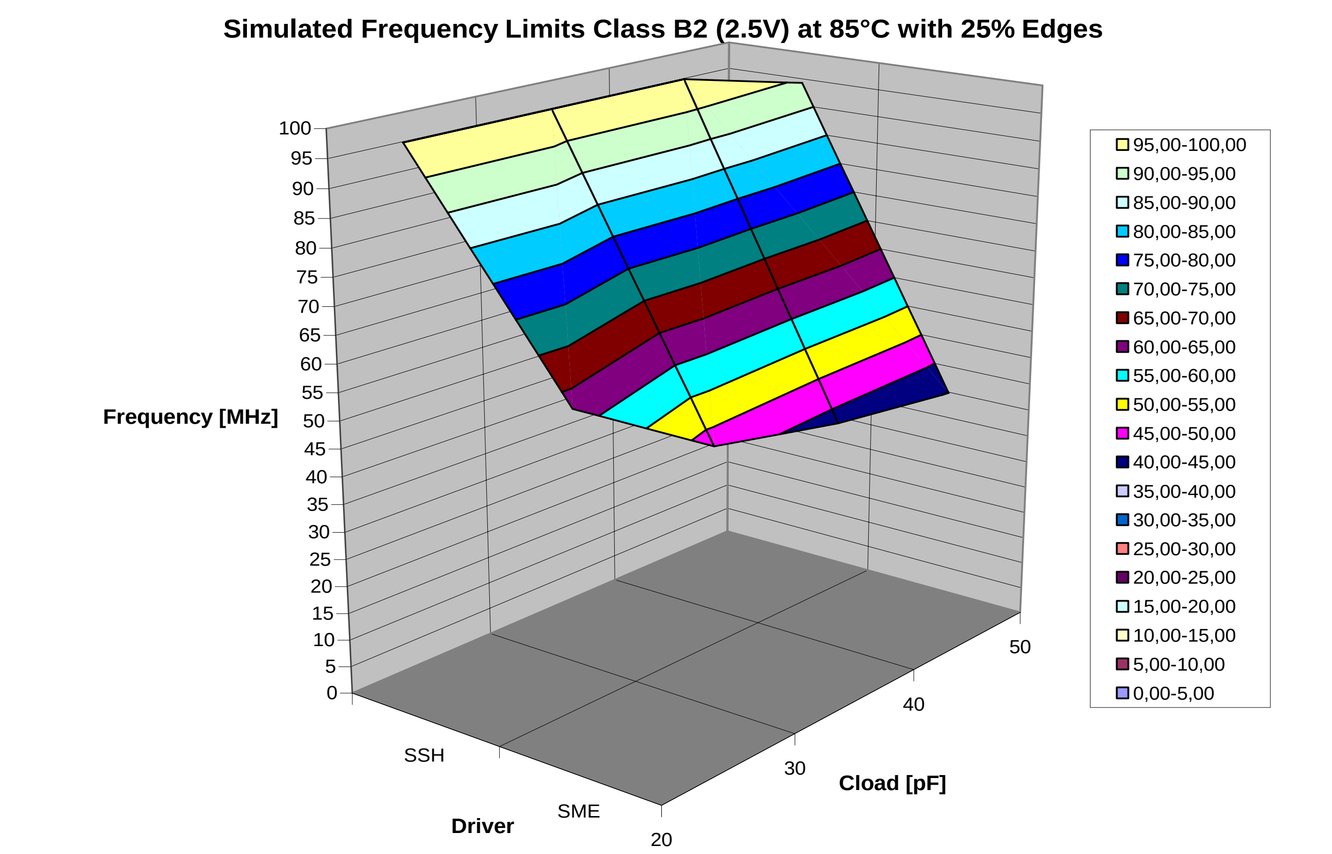


Figure 228: Strong-sharp driver graph for Class B2 drivers at T_A=85°C; edges occupy 1/4 period

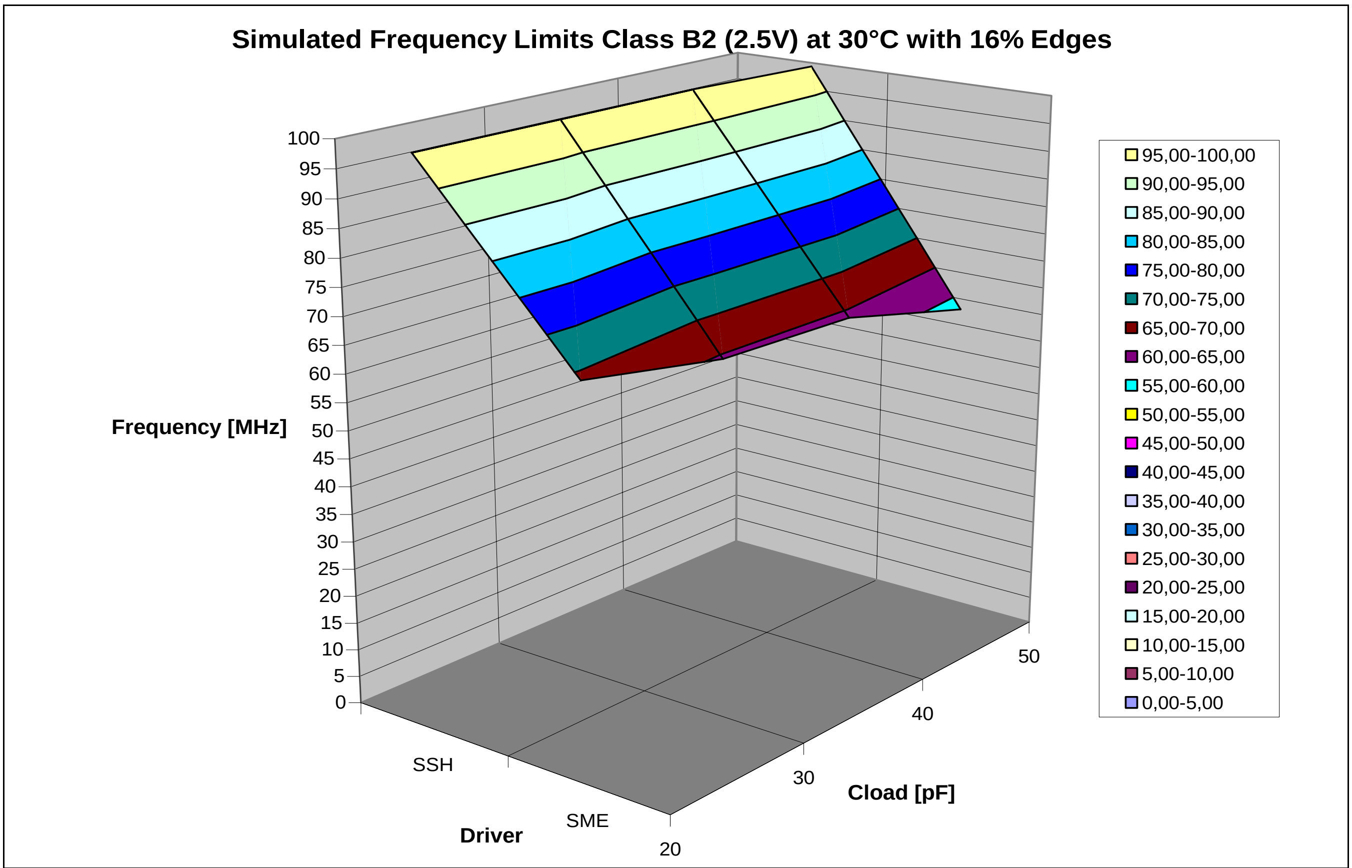


Figure 229: Strong-sharp driver graph for Class B2 drivers at T_A=30°C; edges occupy 1/6 period

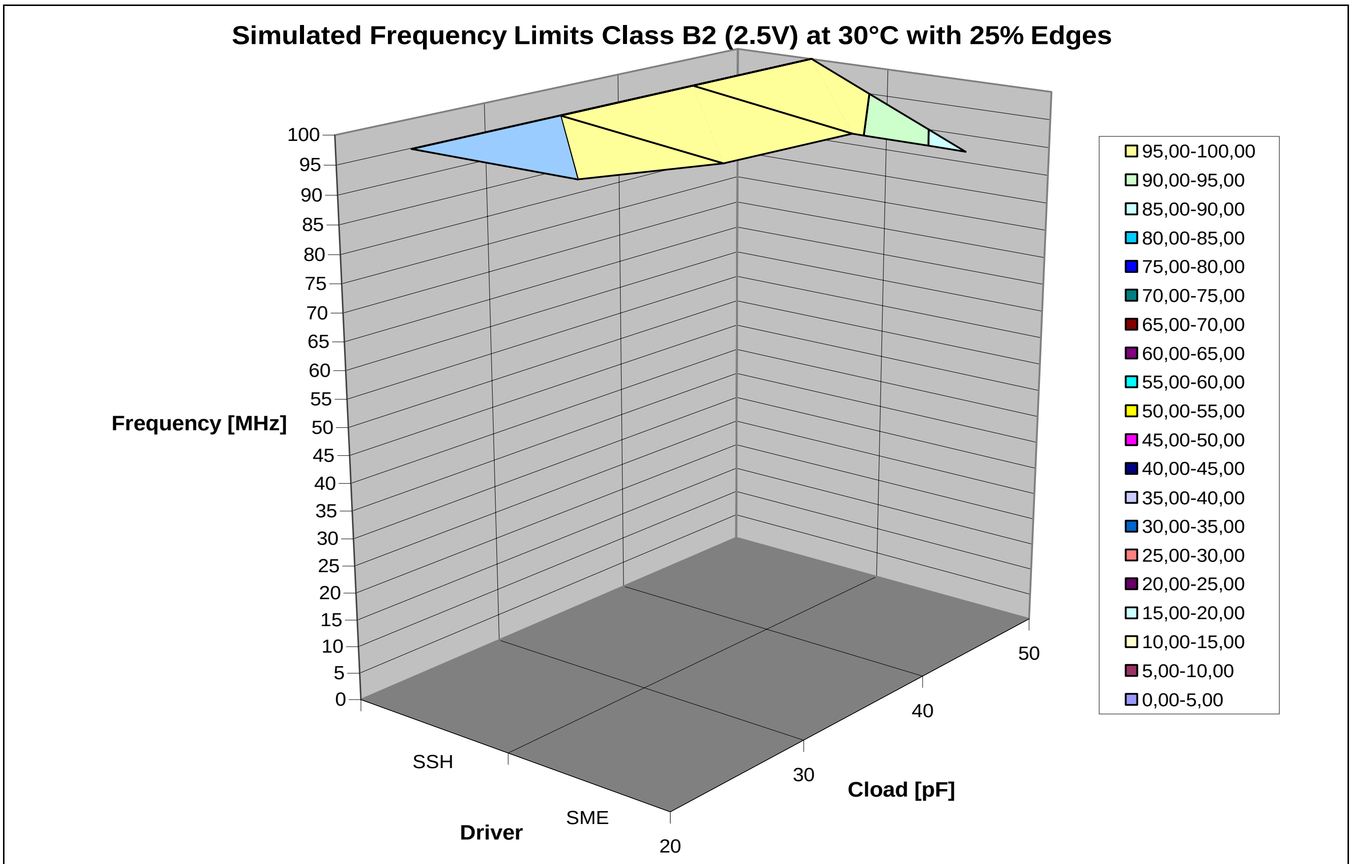


Figure 230: Strong-sharp driver graph for Class B2 drivers at T_A=30°C; edges occupy 1/4period

8 Glossary

BISS	Bosch/Infineon/SiemensVDO Specification	An addendum to the IEC 61967 IC emission test standard. Available on request.
CLKOUT	System Clock Output	Strong output driver for the system clock.
C_{load}	Load Capacitor	Ideal capacitive load connected to an output driver.
di/dt		Dynamic current over time
EMC	Electromagnetic Compatibility	The ability of an electrical device to function satisfactorily in its electromagnetic environment (“Immunity”) without having an impermissible effect on its environment (“Emission”).
EME	Electromagnetic Emission	→ EMC
GND	Ground	Ground reference of the power supply.
GPIO	General Purpose Input/Output	Standard output driver with no special electric specification.
PI	Power Integrity	Good PI means clean power supply system which is not polluted by switching noise.
SI	Signal Integrity	Good SI means proper signal waveform to fulfill the required data communication.
T_A	Ambient Temperature	Temperature in the direct environment of the IC.
VDD		Power supply voltage in general.
VDDC		Core supply voltage = 2.5V nominal.
VDDP		Pad supply voltage = 5.0V nominal.
VSS		→ GND

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