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AP32091

TC1766

Design Guideline for TC1766 Microcontroller Board Layout

Microcontrollers

Never stop thinking.

Edition

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Page	Subjects (major changes since last revision)	
7,10	Figure 2 changed, Capacitor values changed	

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1 Overview

The TC1766 is a 32-Bit microcontroller in a LQFP 176-pin package, which requires a PCB carefully designed for electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for TC1766 are discussed here.

1.1 General Informations:

The microcontroller has two supply domains (1.5V Core / 3.3V I/O Pad), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1766

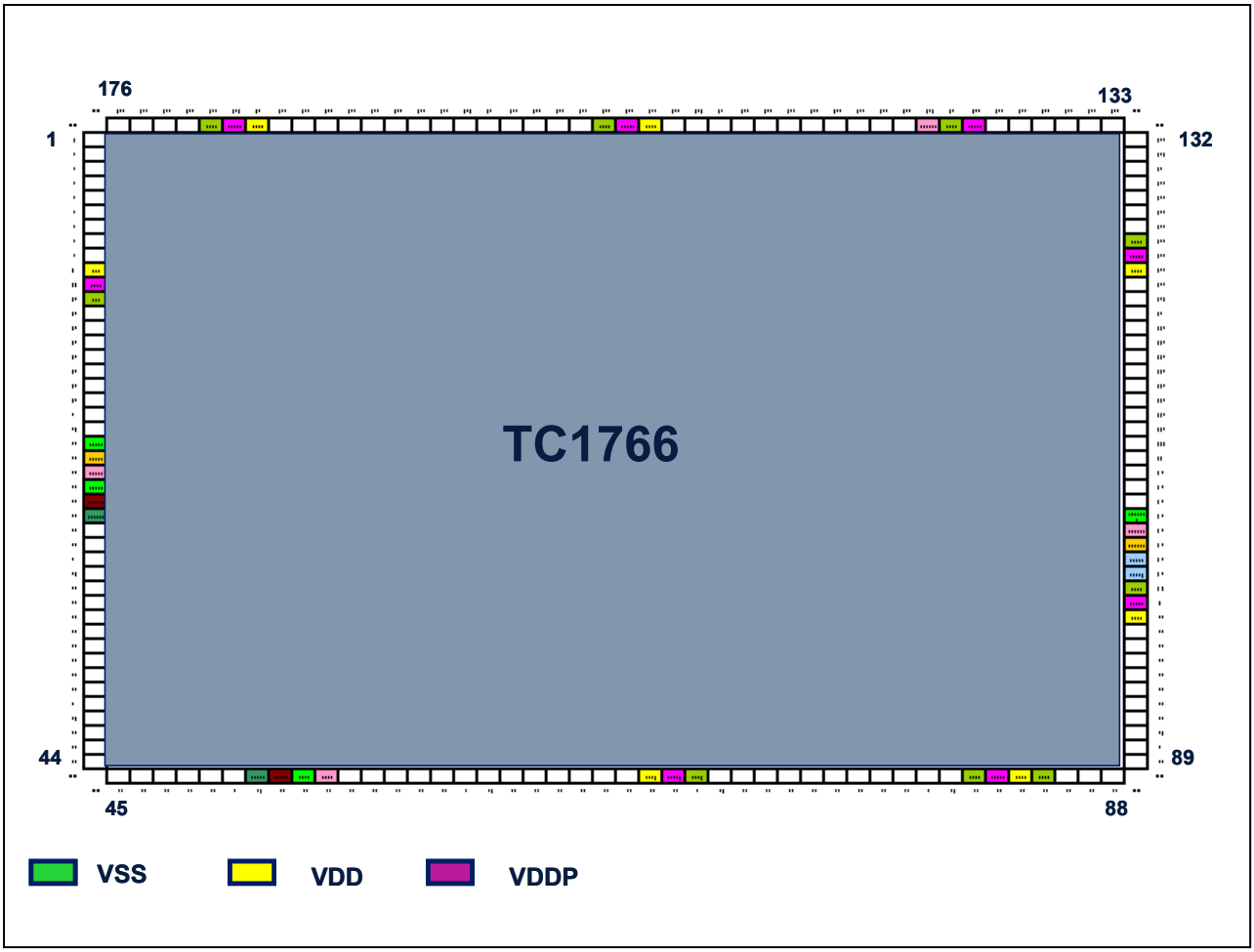

Figure 1 Pinout of TC1766 (Supply pins colored to show the position):

1.3 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
  - TCLKO and SYSCLK: Transmit channel clock output/ System clock output
  - LVDS Pins
  - MLI Pins
  - Supply pins

  Route these signals with adjacent ground reference and use as less as possible vias (no reference layer change!).

  Route them as short as possible. Routing ground on each side can help to reduce coupling to the other signals.

- For unused **"Output, Supply, Input and I/O "** pins following points must be considered:

1. Supply Pins (Modules)	• See the User´s Manual.
2. I/O-Pins	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Confuguration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins including LVDS	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4.Input Pins without internal pull device	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device	• For pins with alternate function see product specification to define the necessary logic level. • Should be configured as pull-down and should be activated static low (exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering).

- The ground system must be designed as follows:

  - Separate analog and digital grounds.

  - The analog ground must be separated into three groups:

    1. Ground for OSC (104),
    2. Ground for ADC0/1 (53),
    3. Ground for FADC (22,25)

- To reduce the radiation / coupling from oscillator circuit, a separated ground island (see Figure 5) on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections of the load capacitors and VSSOSC should also be connected to this island. Traces for load capacitors and Xtal should be as short as possible.

- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads).
- A target inductance value of <2nH (VDDC), <1nH (VDDP) for the connection of decoupling capacitors to the supply pins is required.
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3 (see Figure 2). Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dBµV on the related supply net.
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32111).
- Use lowest possible frequency for SYSCLK .
- Avoid to cut the GND plane by via groups. A solid GND plane must be designed.

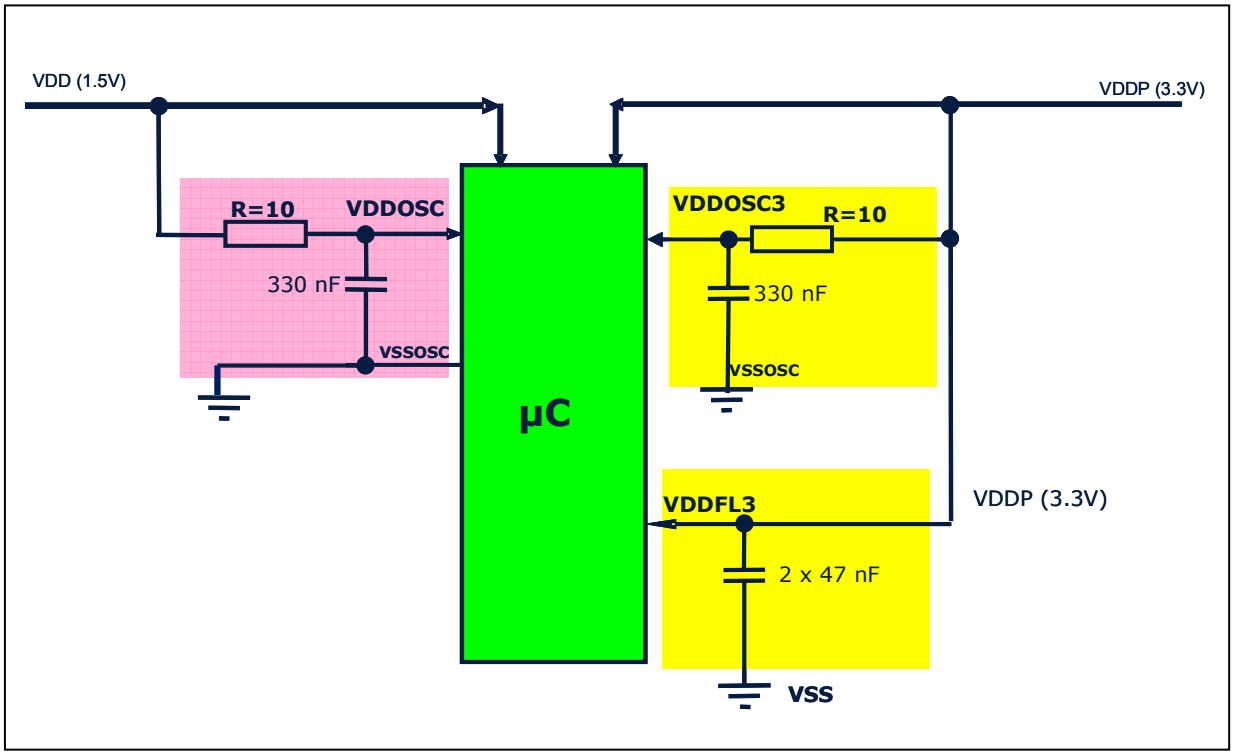

Figure 2 Filtering of VDDOSC, VDDOSC3 and VDDFL3 supply pins

1.4 Decoupling

- All two supply domains of TC1766 should be decoupled separately (see decoupling layout example)
- Type of capacitors:
  - Values: 10 nF, 47nF, 100 nF, 330 nF
  - X7R Ceramic Multilayer (Low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND layer (see layout example on next figure).
- The decoupling capacitors should be placed directly under the IC or if neccesary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias can be used at capacitors to get a low impedance connection between capacitors and power/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

A power-plane/grounding concept example for a 32-bit microcontroller like TC1766 with LQFP package can be seen in figure 3. This layout example shows two supply domains (1.5V, 3.3V), where 1.5V is core supply and 3.3V is pad supply voltage. In Figure 3 shown examples are based on device power supply concept and implementation. Alternative implementations are also acceptable and must be evaluated within application by customer.

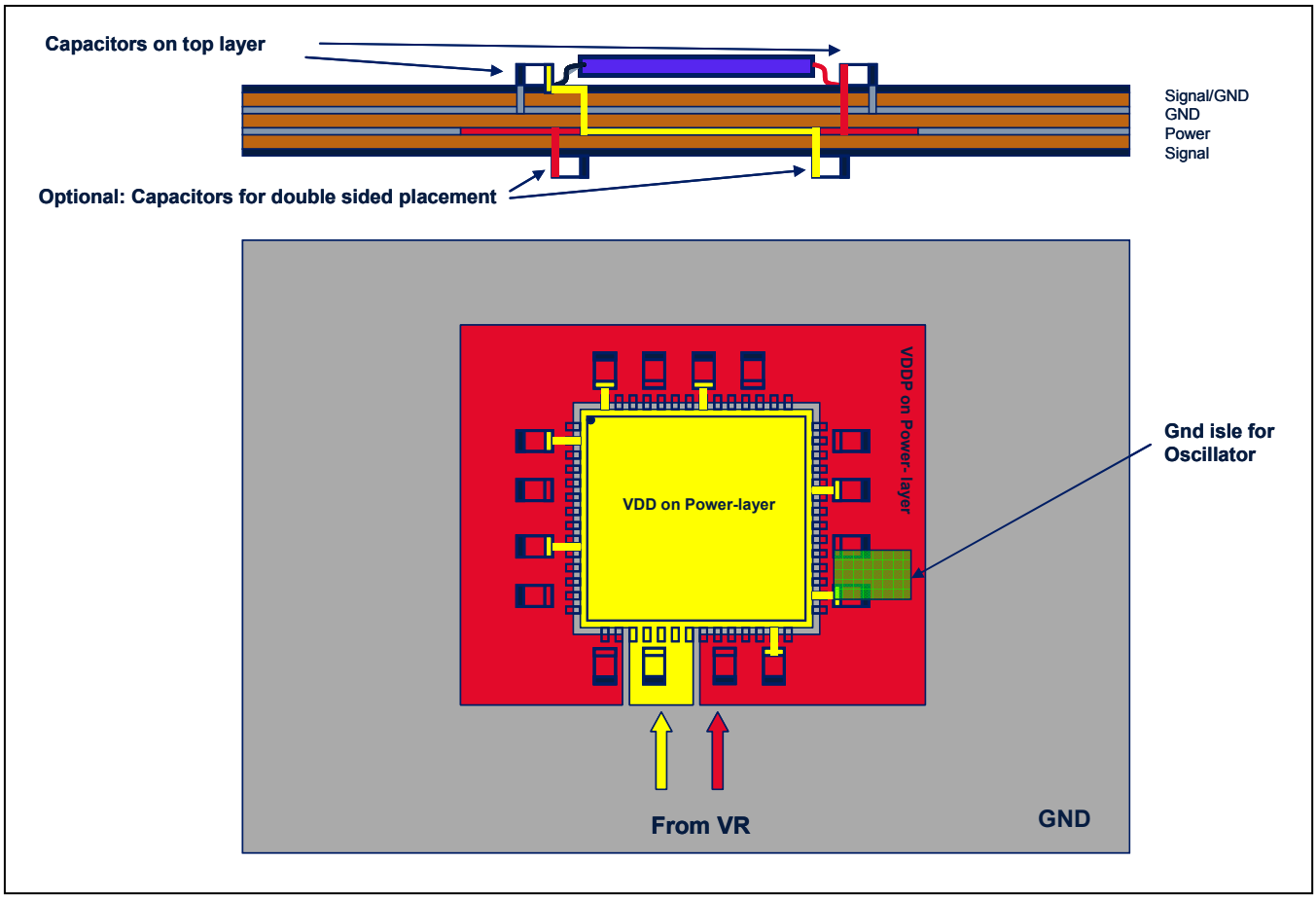

Figure 3 Layout example for decoupling of TC1766

The general way is to connect the VDD and GND first to the capacitors and then connect to the pins of the IC. The GND and VDD supply planes are on the second and third layer (inner layers).

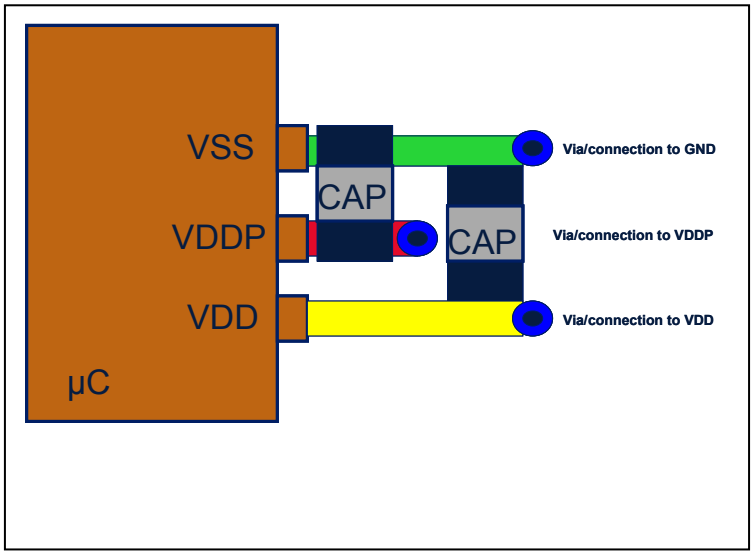

Figure 4 Connection example for decoupling capacitors (Placement on same layer)

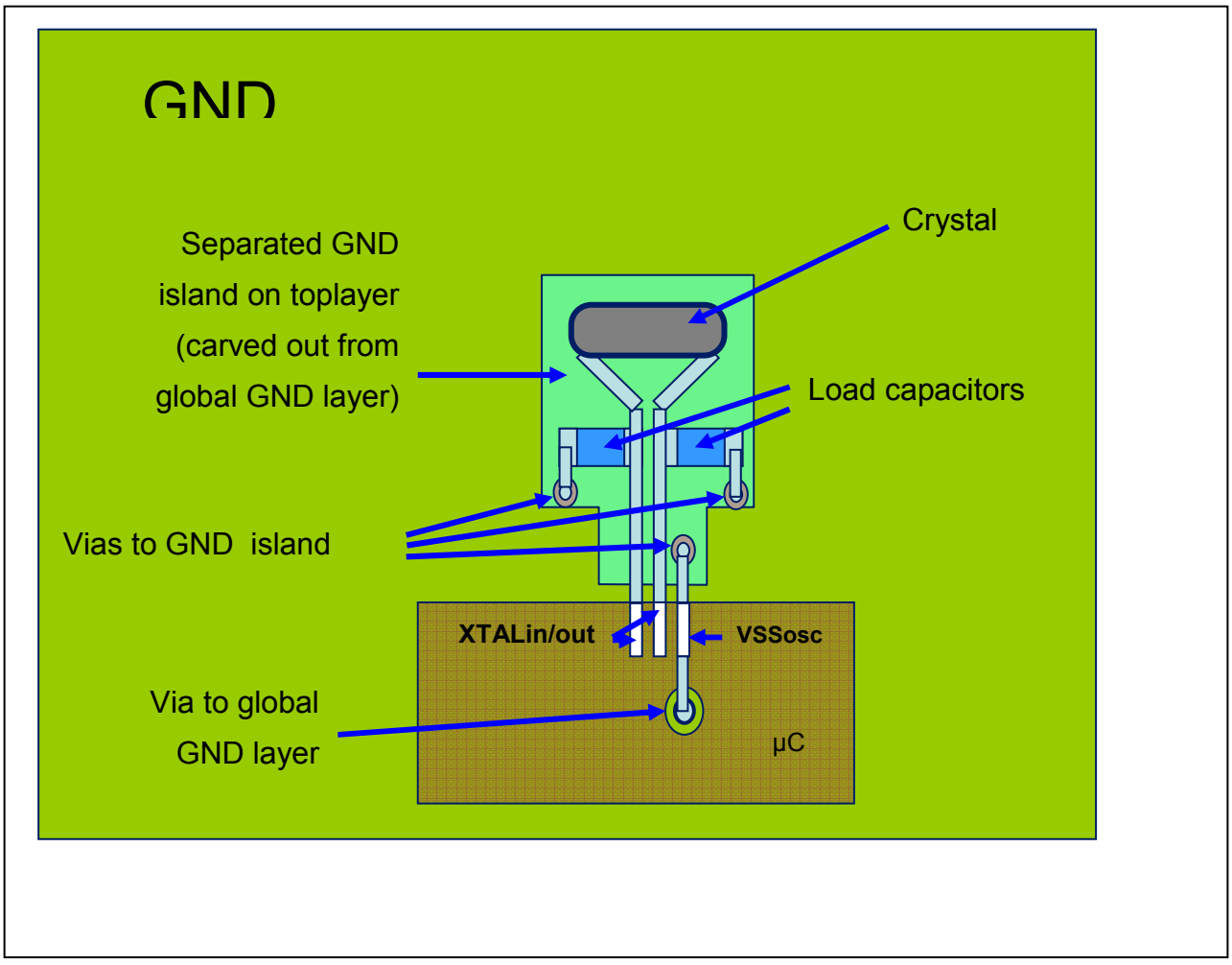

Figure 5 Layout Proposal Oscillator Circuit

Decoupling Capacitor List:

Capacitor	Type	Supply	Pins
100nF	X7R	VDD	68
100nF	X7R	VDD	84
100nF	X7R	VDD	99
100nF	X7R	VDD	99
100nF	X7R	VDD	153
100nF	X7R	VDD	10
47nF	X7R	VDD	68
47nF	X7R	VDD	84
47nF	X7R	VDD	99
47nF	X7R	VDD	123
47nF	X7R	VDD	153
47nF	X7R	VDD	170
10nF	X7R	VDDP	83
10nF	X7R	VDDP	124
10nF	X7R	VDDP	139
10nF	X7R	VDDP	154
10nF	X7R	VDDP	171
10nF	X7R	VDDP	11
47nF	X7R	VDDP	69
47nF	X7R	VDDP	100
47nF	X7R	VDDAF	23
47nF	X7R	VDDM	54
47nF	X7R	VDDMF	24
330nF	X7R	VDDOSC	105
330nF	X7R	VDDOSC3	106
47nF	X7R	VDDFL3	141
47nF	X7R	VDDFL3	141

Total= 6 x 100nF, 13 x 47nF, 6 x 10nF, 2 x 330nF

Note: This application note contains design recommendations from Infineon Technologies point of view. Customer, based on dedicated implementation choices, must validate effectiveness and performance of the final application implementation.

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