Application Note, V2.2.1, July 2003

AP24001

OCDS Level 1 JTAG Connector

16-Bit & 32-Bit Microcontrollers

AI Microcontrollers

Never stop thinking.

OCDS Level 1 JTAG Connector

Revision History: 2003-07 V2.2.1

Previous Version:V2.2.0

Page	Subjects (major changes since last revision)
	Changes and corrections to the technical content and document layout and design.
	Adapted to reflect current signal naming conventions.
	Table footnotes added.
	V2.1 was an intermediate version.
pg3/5	Added Connector manufacturer example (section 2.2) and confirmed which signals are Pull-up (section 3.1)

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1 Introduction

This document describes the Infineon Technologies JTAG Connector for the C166CBC, C166S V1, C166S V2 and TriCore cores. Since there is no standard connector defined in the JTAG standard (IEEE1149.1) specification, nor an established industry standard, we are defining, for debug purposes, our own standard.

2 The Connector Layout

2.1 Slow and Fast Signals, Shielding

Since the connector will be used together with a flat ribbon cable, the pins on the left and right side of the connector will alter within the flat ribbon cable. Slow signals and GND are on the right side and fast signals are on the left side. This gives some shielding. The key pin should be forced down by the debugger side to GND.

2.2 Mechanical

The connector (Pin Header) is a standard 2.54 mm (0.1 inch) centres and 10mm pins. An example manufacturer is Molex (www.molex.com) C-Grid III, 8w Dual Row (Molex part number 90131-0764. These can also be ordered from RS).

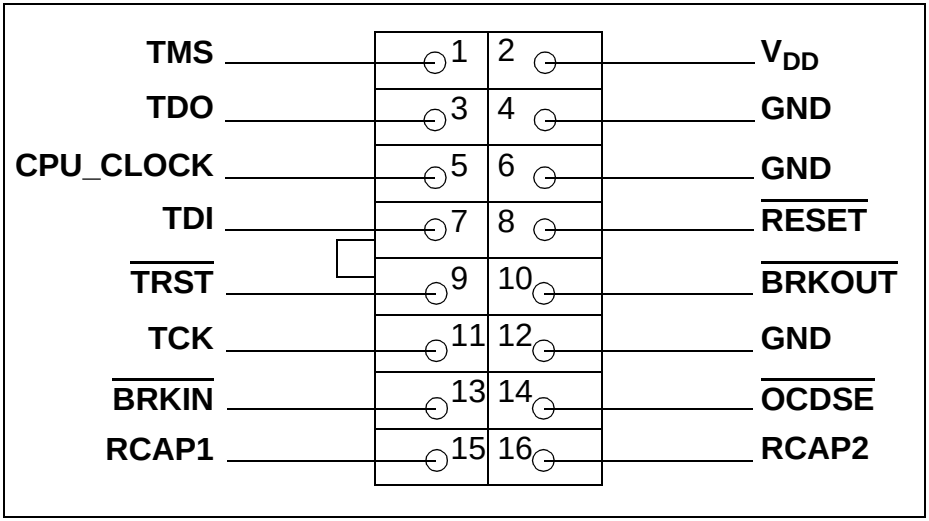

Figure 1 Connector Layout

2.3 Signal Description

The following are the Infineon JTAG connector signals.

Note that directions are indicated as follows:

- O = output from the CPU processor board to the debugger.
- I = input to the CPU processor board from the debugger.

Table 1 Signal Descriptions

Signal Name	Direction	Pin	Comment
TDO	O	3	IEEE 1149.1
TDI	I	7	IEEE 1149.1
TMS	I	1	IEEE 1149.1
TCK	I	11	IEEE 1149.1
$\overline{\text{TRST}}$	I	9	IEEE 1149.1
$\overline{\text{BRKIN}}$	I	13	Break Input & OCDS configuration
$\overline{\text{BRKOUT}}$	O	10	
$\overline{\text{RESET}}$	I	8	Open drain, TriCore: $\overline{\text{PORST}}$ (Power On Reset)
CPU_CLOCK	O	5	Optional
RCAP1		15	Reserved for customer application purposes
$\overline{\text{OCDSE}}$[1)]	I	14	TriCore, OCDS configuration
GND		4,6,12	
V_{DD}		2	I/O ring voltage of CPU
RCAP2		16	Reserved for customer application purposes

1) This signal is not available on each Microcontroller implementation. This signal must be forced to a low level from the Trace Hardware (Emulator). If the Microcontroller derivative has no corresponding signal, it should be left unconnected in the target hardware.

2.4 Voltage

All Signals have the voltage of the I/O ring. Current Microcontroller implementations have 5 V, 3.3 V or 2.5 V V_{DD} on I/O ring.

The V_{DD} I/O ring should be provided from the target based board to the active buffers at the cable level (if present).

3 Implementation Considerations

3.1 Pull-Ups

On the CPU board the following signals should each be connected to pull-ups of 10 kΩ respectively.

- $\overline{\text{OCDS}}$
- TMS
- TCK
- TDI
- $\overline{\text{TRST}}$
- $\overline{\text{RESET}}$
- $\overline{\text{BRKIN}}$

3.2 Clock Pin

The clock is optional since not every CPU has a Clock-out pin available. Since the clock pin could be a very good antenna it should be connected via any sort of Jumper. If not implemented it should be GND so that it can be sensed if there is clock or not.

3.3 RCAP1 and RCAP2 Pins

These pins are reserved for customer application purposes.

3.4 $\overline{\text{OCDSE}}$ and $\overline{\text{BRKIN}}$ Pins

These pins are used during power on reset (POR reset pin) to setup the OCDS system (TriCore only)

4 Low Cost EVA Board Connector

The Infineon StarterKit boards are equipped with a low cost DB25 printer port connector. The JTAG Signals are mapped to the following Printer-Port signals. It is not recommended to use a DB25 connector in customer applications since the onboard-wiggler would eat up additional board space & power.

Table 2 Connector Signals

LPT Pin	LPT Signal	Type	JTAG/Board Signals	16-pin JTAG Connector	Comment
1	Strobe	O			
14	$\overline{\text{Auto feed}}$	O	VPP User		Optional: 12 V for external User. FLASH programming
2	D0	O	TDI	7	
15	$\overline{\text{Error}}$	I	10 kΩ pull-up to 5 Volt		
3	D1	O	TMS	1	
16	$\overline{\text{Init}}$	O			
4	D2	O	TCK	11	
17	$\overline{\text{Select}}$	O	VPP Mon		Optional: 12 V for external Mon. FLASH programming.
5	D3	O	TRST	9	
18	GND	SH	GND	4,6,12	
6	D4	O	$\overline{\text{BRKIN}}$	13	
19	GND	SH	GND	4,6,12	
7	D5	O	$\overline{\text{RESET}}$	8	TriCore: $\overline{\text{PORST}}$ (Power On Reset)
20	GND	SH	GND	4,6,12	
8	D6	O	$\overline{\text{OCDSE}}$[1)]	14	
21	GND	SH	GND	4,6,12	
9	D7	O	$\overline{\text{NMI}}$		Optional
22	GND	SH	GND	4,6,12	
10	$\overline{\text{Ack}}$	I	$\overline{\text{BRKOUT}}$	10	
23	GND	SH	GND	4,6,12	

Table 2 Connector Signals

LPT Pin	LPT Signal	Type	JTAG/Board Signals	16-pin JTAG Connector	Comment
11	Busy	I	10 kΩ pull-down to GND		
24	GND	SH	GND	4,6,12	
12	Paper empty	I	TDO	3	
25	GND	SH	GND	4,6,12	
13	Select	O	IRQ pending		Optional

[1] This signal is not available on each Microcontroller implementation. This signal must be forced to a low level from the Trace Hardware (Emulator). If the Microcontroller derivative has no corresponding signal, it should be left unconnected in the target hardware.

5 Onboard Wiggler

The Infineon Technologies StarterKit boards are equipped with Onboard Wigglers. The Onboard Wiggler protects the microcontroller from voltage peaks and operates as a level shifter if needed.

Please note that the above Wiggler describes a stand-alone version. On the StarterKit board the right side of the Wiggler would be connected with the chip.

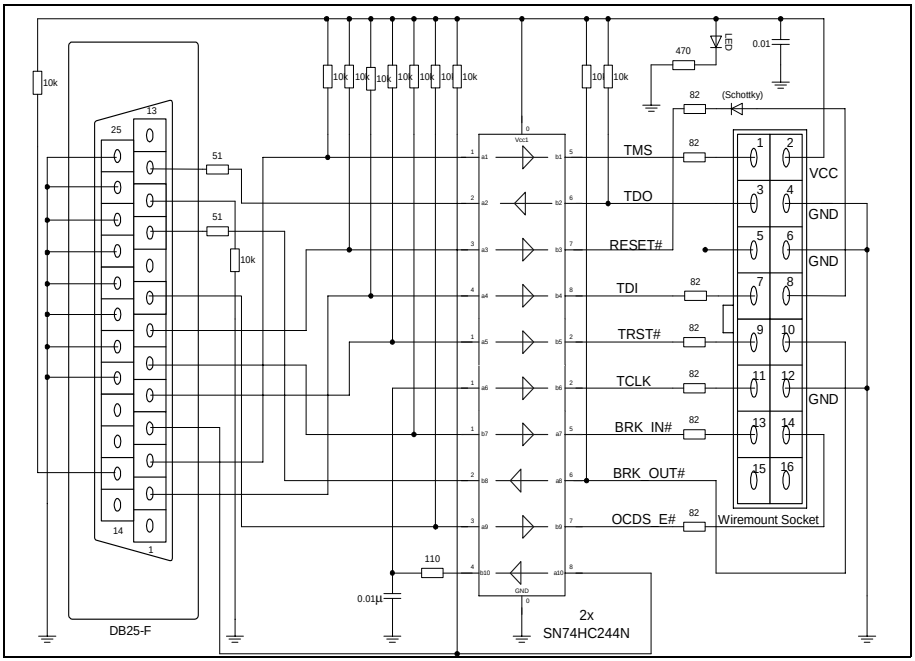

Figure 2 Wiggler Circuit Diagram

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Dr. Ulrich Schumacher

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